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(54) **STACKED MEMORY CELL UTILIZING NEGATIVE DIFFERENTIAL RESISTANCE DEVICES**

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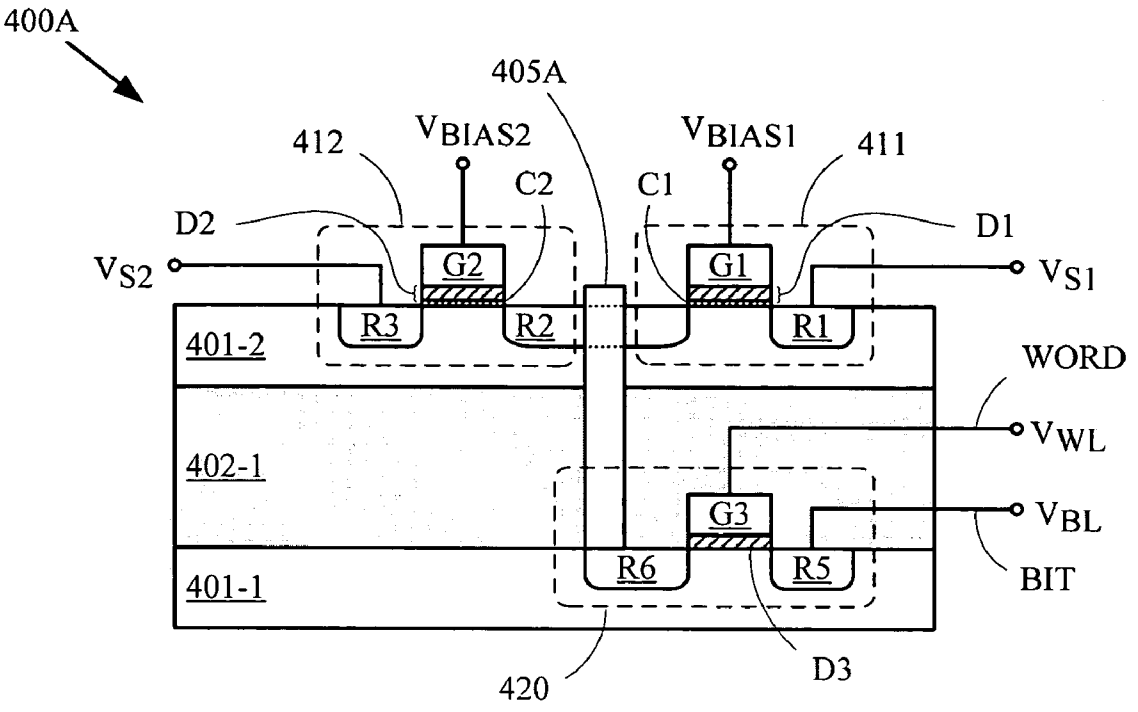
(57) **ABSTRACT**

A memory cell includes two negative differential resistance (NDR) field effect transistors (FETs) forming a bistable latch, and an access transistor for allowing data to be passed to and from the storage node formed by the bistable latch. By stacking the NDR-FETs and the access transistor in two or more layers, area requirements for the memory cell can be reduced, thereby enabling increased circuit density in an integrated circuit (IC) incorporating the memory cell.



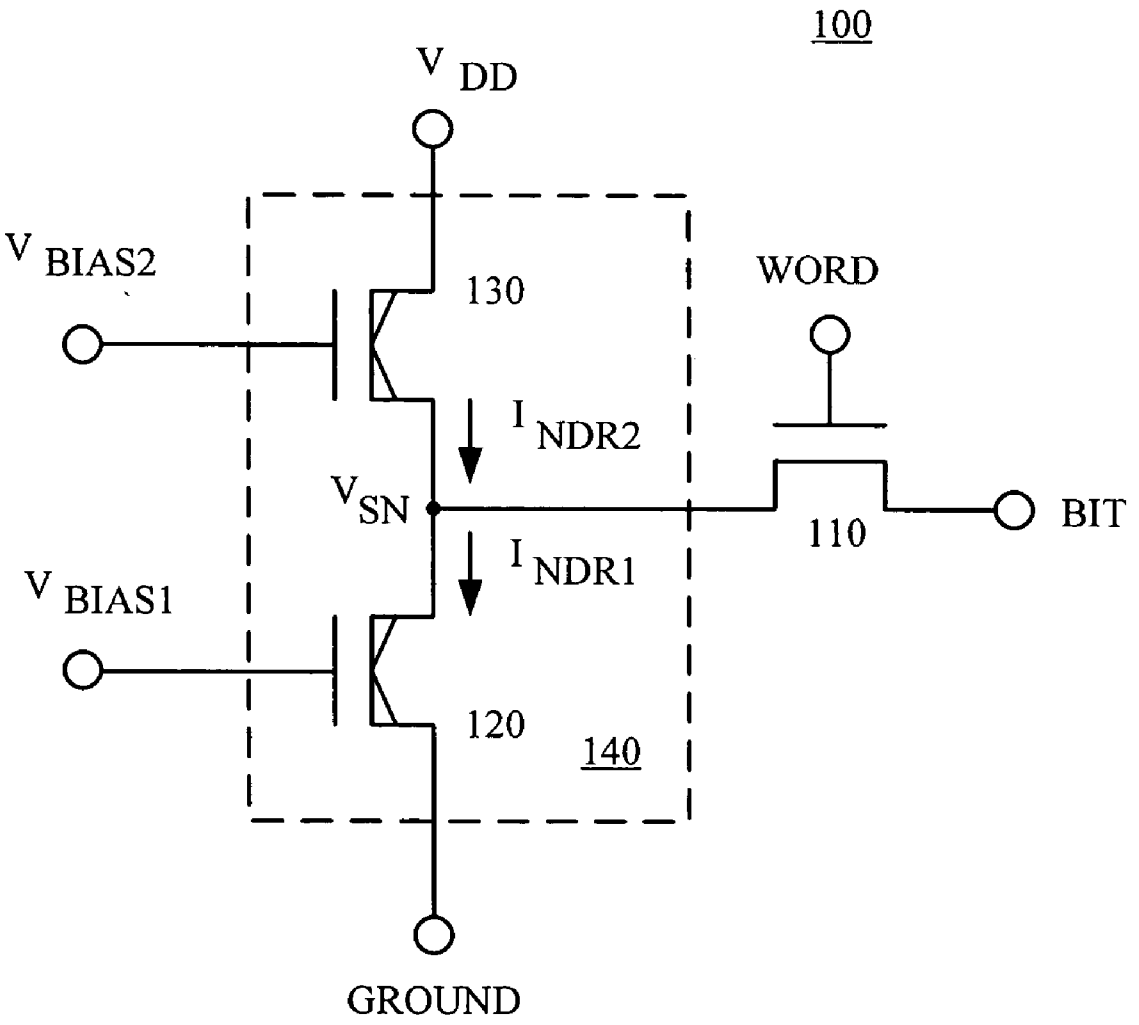
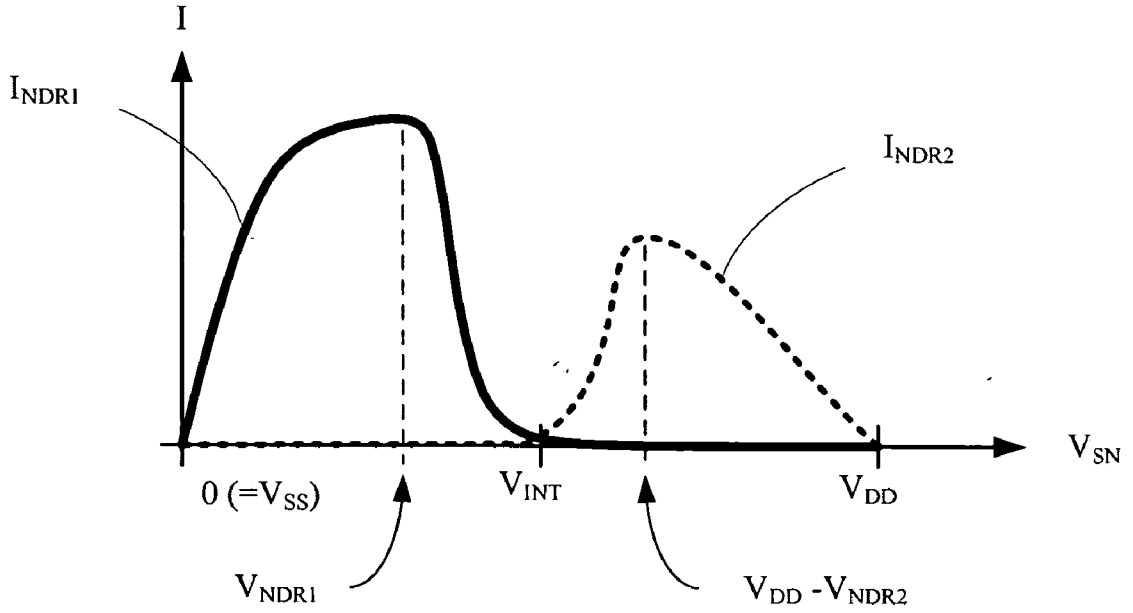

100
V DD
V BIAS2
130
WORD
I NDR2
V SN
110
BIT
I NDR1
V BIAS1
120
140
GROUND

Figure 1

Figure 2



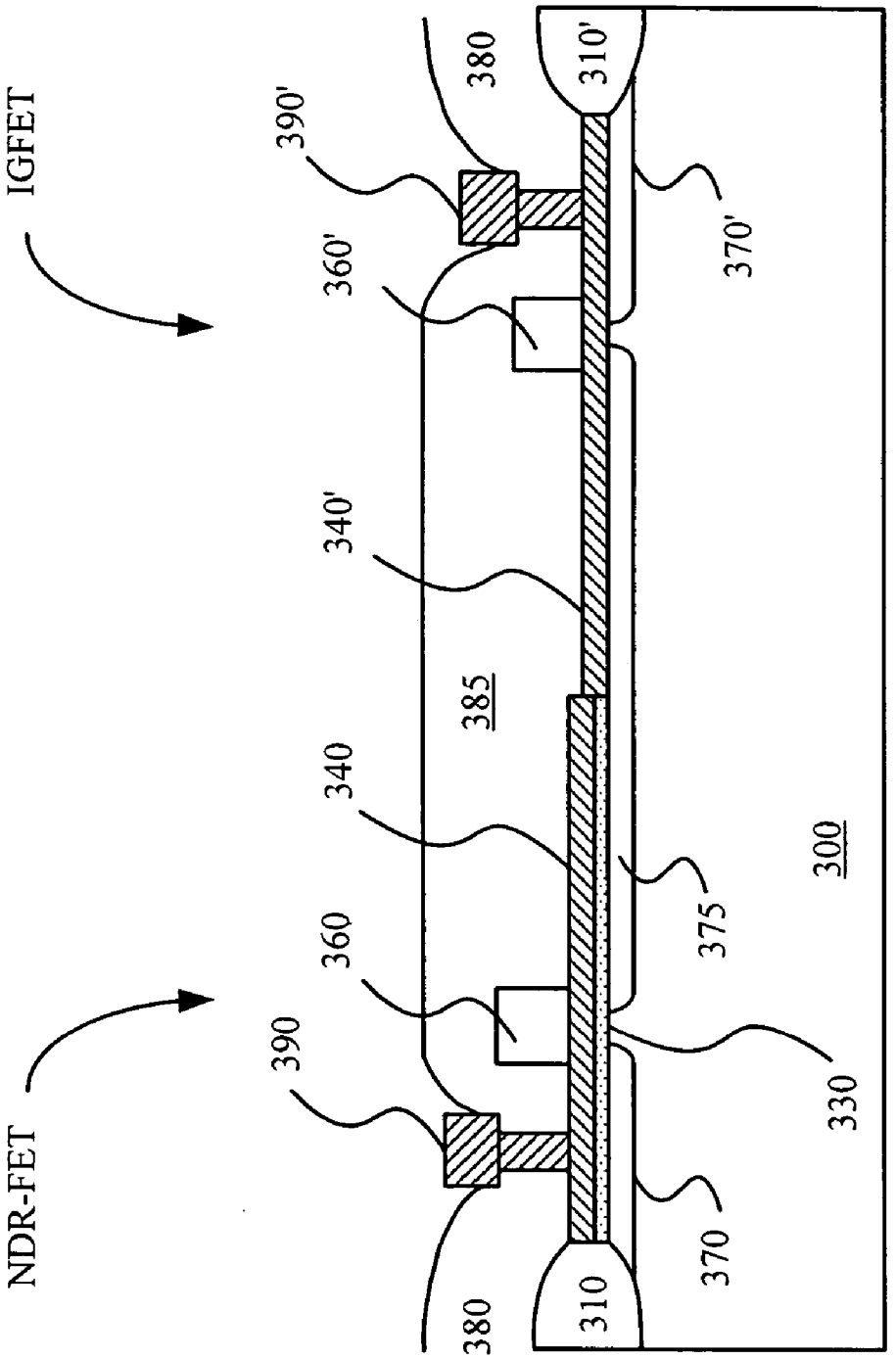

IGFET
NDR-FET
390'
380
310'
360'
370'
340'
385
340
360
375
300
390
330
370
380
310

Figure 3

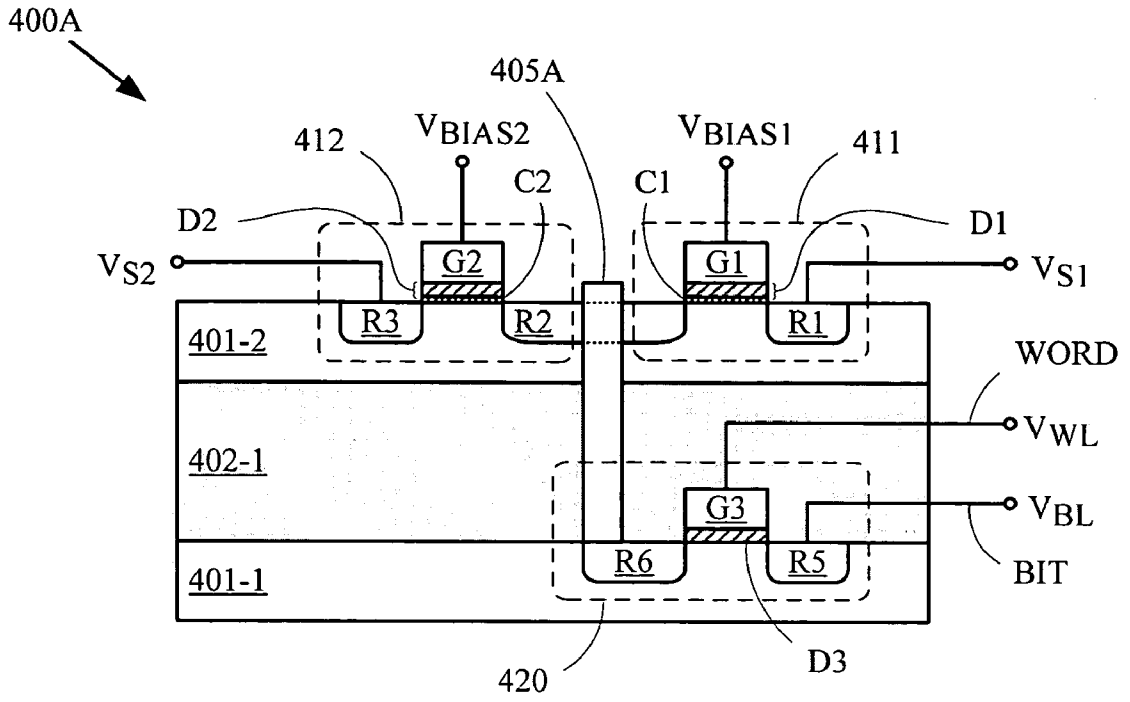


Figure 4A

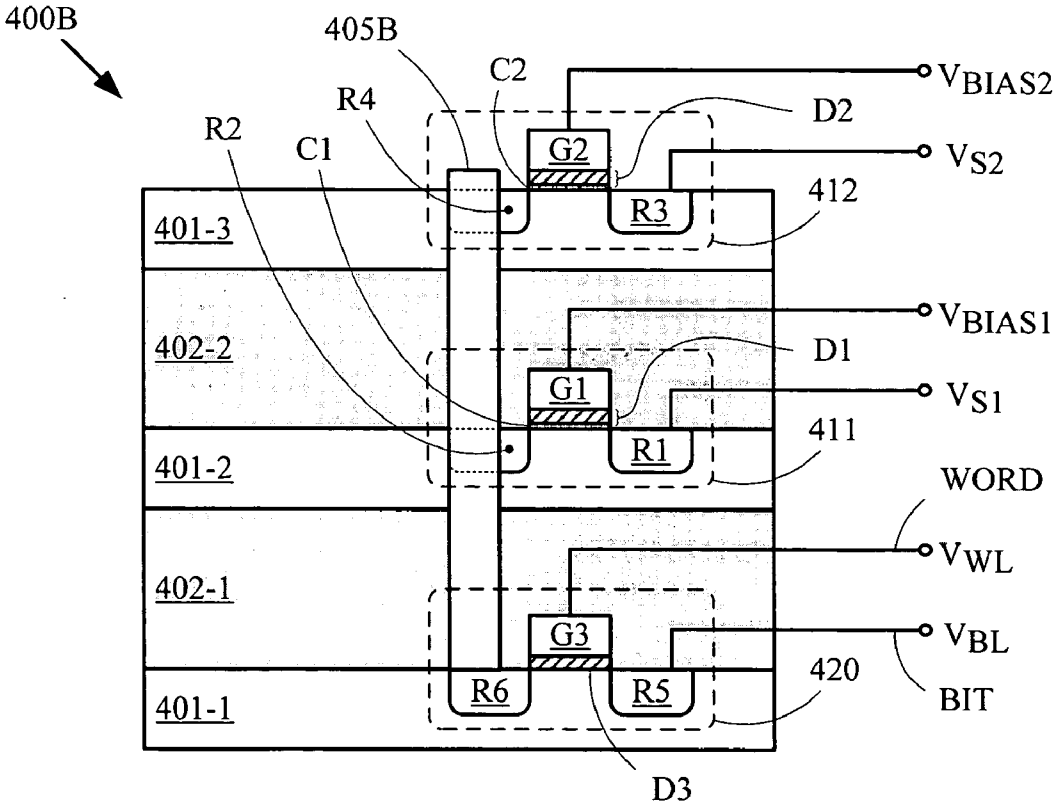


Figure 4B

STACKED MEMORY CELL UTILIZING NEGATIVE DIFFERENTIAL RESISTANCE DEVICES

CROSS REFERENCE TO RELATED APPLICATIONS

Related Applications

[0001] The present application is a continuation-in-part of U.S. patent application Ser. No. 10/827,787, entitled "Method Of Making Memory Cell Utilizing Negative Differential Resistance Devices" filed Apr. 19, 2004 which is a divisional of U.S. patent application Ser. No. 10/029,077, entitled "Memory Cell Using Negative Differential Resistance Field Effect Transistors" filed Dec. 21, 2001, now U.S. Pat. No. 6,724,655.

[0002] The present application is also related to the following applications, all of which are filed simultaneously with parent application Ser. No. 10/029,077, and which are hereby incorporated by reference as if fully set forth herein:

[0003] An application Ser. No. 10/028,084 entitled "INSULATED-GATE FIELD-EFFECT TRANSISTOR INTEGRATED WITH NEGATIVE DIFFERENTIAL RESISTANCE (NDR) FET"; Attorney Docket No. PROG 2001-1; and

[0004] An application Ser. No. 10/028,394 entitled "DUAL MODE FET & LOGIC CIRCUIT HAVING NEGATIVE DIFFERENTIAL RESISTANCE MODE"; Attorney Docket No. PROG 2001-3, now U.S. Pat. No. 6,518,589;

[0005] An application Ser. No. 10/028,089 entitled "CHARGE PUMP FOR NEGATIVE DIFFERENTIAL RESISTANCE TRANSISTOR" Attorney Docket No. PROG 2001-4, now U.S. Pat. No. 6,594,193;

[0006] An application Ser. No. 10/028,085 entitled "IMPROVED NEGATIVE DIFFERENTIAL RESISTANCE FIELD EFFECT TRANSISTOR (NDR-FET) & CIRCUITS USING THE SAME"; Attorney Docket No. PROG 2001-5; now U.S. Pat. No. 6,559,470.

FIELD OF THE INVENTION

[0007] This invention generally relates to semiconductor memory devices and technology, and in particular to static random access memory (SRAM) devices.

BACKGROUND OF THE INVENTION

[0008] The rapid growth of the semiconductor industry over the past four decades has largely been enabled by continual advancements in manufacturing technology which have allowed the size of the transistor, the basic building block in integrated circuits (ICs), to be steadily reduced with each new generation of technology. As the transistor size is scaled down, the chip area required for a given circuit is reduced, so that more chips can be manufactured on a single silicon wafer substrate, resulting in lower manufacturing cost per chip; circuit operation speed also improves, because of reduced capacitance and higher transistor current density. State-of-the-art fabrication facilities presently manufacture ICs with minimum transistor feature size smaller than 100 nm, so that microprocessor products with transistor counts approaching 1 billion transistors per chip can be manufactured cost-effectively. High-density semiconductor memory devices have already reached the gigabit scale, led by dynamic random access memory (DRAM) technology. The DRAM memory cell consists of a single pass transistor and a capacitor (1T/1C), wherein information is stored in the form of charge on the capacitor. Although the DRAM cell provides the most compact layout (with area ranging between $4F^2$ and $8F^2$, where F is the minimum feature half-pitch defined by lithography), it requires frequent refreshing (typically on the order of once per millisecond) because the charge on the capacitor leaks away at a rate of approximately 10^{-15} Amperes per cell. This problem is exacerbated by technology scaling, because the transistor leakage current increases with decreasing channel length, and also because a reduction in cell capacitance results in a smaller number of stored charge carriers, so that more frequent refreshing is necessary. Thus, scaling of DRAM technology to much higher densities presents significant technological challenges.

[0009] Static RAM (SRAM) does not require refreshing and is generally faster than DRAM (approaching 1 ns access times as compared to tens of ns for DRAM). However, the SRAM cell is more complex, requiring either four n-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) and two p-channel MOSFETs, or four n-channel MOSFETs and two polycrystalline-silicon (poly-Si) load resistors, resulting in significantly larger cell size (typically greater than $>80\ F^2$). Innovations which provide significant reductions in SRAM cell size while allowing the SRAM cell to retain its favorable operating characteristics are therefore highly desirable.

[0010] Negative differential resistance (NDR) devices have previously been proposed for compact static memory applications. E. Goto in *IRE Trans. Electronic Computers,* March 1960, p. 25 disclosed an SRAM cell consisting of two resonant tunneling diodes (RTDs) and a pass transistor. For a variety of NDR devices including RTDs, the current first increases with increasing applied voltage, reaching a peak value, then decreases with increasing applied voltage over a range of applied voltages, exhibiting negative differential resistance over this range of applied voltages and reaching a minimum ("valley") value. At yet higher applied voltages, the current again increases with increasing applied voltage. Thus, the current-vs.-voltage characteristic is shaped like the letter "N". A key figure of merit for NDR devices is the ratio of the peak current to the valley current (PVCR). The higher the value of the PVCR, the more useful the NDR device is for variety of circuit applications. The PVCR of RTDs is generally not high enough to make it practical for low-power SRAM application, because in order for the RTDs in a Goto cell to have sufficient current drive, the valley current is too large, causing large static power dissipation. In addition, RTDs require specialized fabrication process sequences so that the complexity of an integrated RTD/MOSFET SRAM process would be substantially higher than that of a conventional complementary MOS (CMOS) SRAM process, resulting in higher manufacturing cost.

[0011] Accordingly, there exists a significant need for NDR devices with very high ($>10^6$) PVCR which can be easily integrated into a conventional CMOS technology, for compact, low-power, low-cost SRAM.

SUMMARY OF THE INVENTION

[0012] An object of the present invention is to provide a static random access memory (SRAM) cell of significantly smaller size as compared to a conventional six-transistor SRAM cell, while retaining the desirable operating characteristics of the conventional SRAM cell without significant increase in manufacturing cost.

[0013] For achieving the object, the invention provides a semiconductor device comprising an n-channel insulated-gate field-effect transistor (IGFET) including a gate and source/drain electrodes, and two (preferably n-channel) NDR-FETs each including gate and source/drain electrodes, wherein the IGFET and NDR-FET elements are formed on a common substrate, with one of the source/drain electrodes of the IGFET semiconductor element connected to the drain electrode of a first NDR-FET and also to the source electrode of a second NDR-FET, the gate electrode of the IGFET connected to a first control terminal, the other one of the source/drain electrodes of the IGFET connected to a second control terminal, the drain electrode of the first NDR-FET connected to a power-supply terminal, the source electrode of the second NDR-FET connected to a grounded or negatively-biased terminal, and the gate electrodes of the NDR-FETs each biased at a constant voltage. The point of connection between the drain electrode of the first NDR-FET and the source electrode of the second NDR-FET is the data storage node. This semiconductor device can function as a bistable memory cell, with access to the data storage node provided via the IGFET.

[0014] In various embodiments, the first NDR-FET, the second NDR-FET, and the IGFET access transistor that make up the SRAM cell can be formed in two or more semiconductor layers in a stacked configuration, thereby reducing the layout area requirements of the SRAM cell. In one embodiment, the first NDR-FET, the second NDR-FET, and the IGFET access transistor can be formed in two different semiconductor layers, such that one of the first and second NDR-FETs and the IGFET access transistor overlies another of the first and second NDR-FETs and the IGFET access transistor. In another embodiment, the first and second NDR-FETs and the IGFET access transistor can each be formed in a different semiconductor layer, such that the three transistors are arranged one above another (e.g., the first NDR-FET overlies the IGFET access transistor, and the second NDR-FET overlies the first NDR-FET).

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] **FIG. 1** is a circuit diagram of a static random access memory (SRAM) cell consisting of the combination of two NDR-FET elements which form a bistable latch and one n-channel enhancement-mode IGFET access element;

[0016] **FIG. 2** is a plot of the current vs. storage node voltage characteristic of the bistable latch formed by the combination of two NDR-FETs as shown in **FIG. 1**;

[0017] **FIG. 3** is a schematic cross-sectional view of an NDR-FET element connected to an IGFET, showing the various layers shared by the two elements which are co-fabricated using a single process flow.

[0018] **FIGS. 4A and 4B** are cross-sectional views of SRAM cells consisting of the combination of two NDR-FET elements and one n-channel enhancement-mode IGFET access element formed in multiple stacked semiconductor layers.

DETAILED DESCRIPTION OF THE INVENTION

[0019] A semiconductor device according a preferred embodiment of the invention will now be described with reference to **FIGS. 1 and 2**. **FIG. 1** is a circuit diagram of a preferred embodiment of a static memory (SRAM) cell **100** consisting of two NDR-FET elements **120**, **130** which form a bistable latch **140** and one enhancement-mode IGFET access element **110**. **FIG. 2** is a current vs. storage node voltage plot illustrating the operational characteristics of the static memory cell of **FIG. 1**. The NDR-FET element of the present invention is preferably of the type disclosed in the following King et al. applications: Ser. No. 09/603,101 entitled "A CMOS-PROCESS COMPATIBLE, TUNABLE NDR (NEGATIVE DIFFERENTIAL RESISTANCE) DEVICE AND METHOD OF OPERATING SAME" now U.S. Pat. No. 6,512,274; and Ser. No. 09/603,102 entitled "CHARGE TRAPPING DEVICE AND METHOD FOR IMPLEMENTING A TRANSISTOR HAVING A NEGATIVE DIFFERENTIAL RESISTANCE MODE" now U.S. Pat. No. 6,479,862; and Ser. No. 09/602,658 entitled "CMOS COMPATIBLE PROCESS FOR MAKING A TUNABLE NEGATIVE DIFFERENTIAL RESISTANCE (NDR) DEVICE" now U.S. Pat. No. 6,596,617 all of which were filed Jun. 22, 2000 and which are hereby incorporated by reference as if fully set forth herein.

[0020] As is shown in **FIG. 1**, IGFET **110** is configured as a transfer gate, allowing a BIT line to be connected to a storage node under the control of a WORD line. One of the source/drain electrodes of IGFET **110** is connected to the storage node at potential V_{SN}, the other source/drain electrode of IGFET **110** is connected to the BIT line, and the gate electrode of IGFET **110** is connected to the WORD line.

[0021] The source electrode of first NDR-FET **120** is connected to a ground terminal, the gate electrode of first NDR-FET **120** is supplied with first bias voltage V_{BIAS1}, the drain electrode of the NDR-FET **120** is connected together with the source electrode of a second NDR-FET **130** to the storage node, the gate electrode of second NDR-FET **130** is supplied with a second bias voltage V_{BIAS2} and the drain electrode of second NDR-FET **130** is supplied with a positive voltage V_{DD}. The current flowing in the first NDR-FET, I_{NDR1}, is dependent on the difference between its drain electrode potential and its source electrode potential, V_{SN}, at first increasing rapidly as V_{SN} increases, reaching a peak value when V_{SN} is equal to a critical voltage V_{NDR1}, and rapidly decreasing to nearly zero as V_{SN} increases beyond the critical voltage V_{NDR1}. The bias voltage V_{BIAS1} is sufficiently high so as to ensure that first NDR-FET **120** is turned on for values of V_{SN} ranging from 0 V (ground potential) to V_{NDR1}. The current flowing in the second NDR-FET, I_{NDR2} is dependent on the difference between its drain electrode potential and its source electrode potential, $V_{DD}-V_{SN}$, at first increasing rapidly as $V_{DD}-V_{SN}$ increases, reaching a peak value when $V_{DD}-V_{SN}$ is equal to a critical voltage V_{NDR2}, and rapidly decreasing to nearly zero as $V_{DD}-V_{SN}$ increases beyond the critical voltage V_{NDR2}. The bias voltage V_{BIAS2} is ideally sufficiently high so as to ensure that second NDR-FET **130** is turned on for values of $V_{DD}-V_{SN}$ ranging from 0 V (ground potential) to V_{NDR2}.

[0022] Next the preferred operation of bistable latch **140** in SRAM cell **100** of **FIG. 1** will be described. **FIG. 2** shows the current I_{NDR1} vs. storage node voltage V_{SN} characteristic curve of first NDR-FET **120** obtained by changing the storage node voltage V_{SN} in a range between **0** and V_{DD}, superimposed with the current I_{NDR2} VS. storage node voltage V_{SN} characteristic curve of second NDR-FET **130**. A stable operating point of circuit **140** is a point where the I_{NDR1} vs. V_{SN} characteristic curve of the first NDR-FET crosses the the I_{NDR2} vs. V_{SN} characteristic curve of the second NDR-FET and additionally the characteristic curves I_{NDR1} and I_{NDR2} have the same gradient sign (positive or negative). (The crossing point where the characteristic curves I_{NDR1} and I_{NDR2} have opposite gradient is not a stable operating point.)

[0023] Therefore it is understood that circuit **140** is stable when the potential V_{SN} at the storage node is one of two values 0 and V_{DD} as shown in **FIG. 2**. Accordingly, the circuit can be used as a bistable memory cell by applying a potential of one of the two values 0 and V_{DD} to the BIT line as a write voltage. If the value of V_{SN} increases slightly above that of the low (0 V) stable operating point, current I_{NDRI} flowing in first NDR-FET **120** becomes higher than the current I_{NDR2} flowing in second NDR-FET **130**, causing the value of V_{SN} to be decreased toward 0 V (ground potential), to restore it to that of the stable operating point. Thus first NDR-FET **120** serves as a "pull-down" device. If the value of V_{SN} falls slightly below that of the high (V_{DD}) stable operating point, the current I_{NDR2} flowing in second NDR-FET **130** becomes higher than the current I_{NDR1} flowing in first NDR-FET **120**, causing the value of V_{SN} to be increased toward V_{DD}, to restore it to that of the stable operating point. Thus second NDR-FET **130** serves as a "pull-up" device.

[0024] IGFET **110** is controlled by the WORD line as follows: when the WORD line potential is sufficiently high, IGFET **110** is turned on, connecting the BIT line to the storage node to allow data transfer (reading data from the storage node, or writing data to the storage node); when the WORD line potential is low, IGFET **110** is turned off, so that the storage node is electrically isolated from the BIT line. In this manner, a bistable latch **140** is realized with two series-connected NDR-FET elements, and a compact static memory cell is obtained by integrating latch **140** with a IGFET pass transistor **110**.

[0025] It should be noted that in order to achieve low standby current in the SRAM cell, the valley currents of the NDR-FETs (i.e. I_{NDR1} at $V_{SN}=V_{DD}$ and I_{NDR2} at $V_{SN}=0V$) are preferably minimized, while in order to achieve a fast read access time, the peak currents of the NDR-FETs are preferably maximized. Since the NDR-FET peak current and valley current are controlled by the gate bias voltage applied to the NDR-FET, it is possible to achieve a very low valley current by using a lower gate bias voltage when the SRAM cell is in storage mode to achieve low static power dissipation, and to achieve a very high peak current by using a higher gate bias voltage when the SRAM cell is in read mode to achieve fast read access time. In this aspect, the NDR-FET PVCR can effectively be enhanced by several orders of magnitude.

[0026] As previously stated, the bias voltage V_{BIAS2} should ideally be sufficiently high so as to ensure that second (pull-up) NDR-FET **130** is turned on for values of $V_{DD}-V_{SN}$ ranging from 0 V (ground potential) to V_{NDR2}. Accordingly, V_{BIAS2} should ideally be greater than or equal to $V_{DD}+V_T$, where V_T. is the threshold voltage of second NDR-FET **130**. If second NDR-FET **130** is substantially an enhancement-mode device (i.e. $V_T>0$ V), then V_{BIAS2} should be greater than V_{DD}. Thus, a separate power supply voltage or a boosted supply (such as that provided by a charge pump circuit) would be needed. It should be noted that the charge pump circuit would not consume much power, as it would only supply a high voltage, with negligible current.

[0027] As previously stated, the bias voltage V_{BIAS1} should be sufficiently high so as to ensure that first (pull-down) NDR-FET **120** is turned on for values of V_{SN} ranging from 0 V (ground potential) to V_{NDR1}. Therefore, V_{BIAS1} can be tied or coupled to V_{DD} if desired to reduce constraints on the aforementioned charge pump circuit. Alternatively, V_{BIAS1} can be tied to V_{BIAS2} to simplify the cell architecture and layout.

[0028] **FIG. 3** is a schematic cross-sectional view of an NDR-FET element connected to an IGFET, such as would exist in the preferred embodiment. The NDR-FET and IGFET are formed to include and share many common layers, including at least a portion of the gate insulating film, gate film, interlayer insulator and metal, and hence can be readily fabricated together on a single substrate using a single process flow. For example, a common substrate **300**, a common isolation area **310** and common interlayer insulation layers **380** (**380'**) are used by NDR-FETs and IGFETs respectively. Furthermore, a single gate electrode layer is used for gates **360**, **360'** and a single metal/contact layer **390**, **390'**. Source/drain regions **370**, **370'** are formed at the same time, and a common source/drain region **375'** is shared by the NDR-FET and IGFET. This latter region can serve as a storage node for example in the above embodiments. An NDR charge trapping layer **330** is included only within an NDR-FET region, for the reasons set forth in the aforementioned referenced applications. Finally, both devices can also share a gate insulation film **340**, **340'** in some implementations.

[0029] **FIG. 4A** is a schematic cross-sectional view of an SRAM cell **400**A consisting of two NDR-FET elements **411** and **412**, which form a bistable latch, and one enhancement-mode IGFET access element ("transfer element") **420**. The circuit implemented by SRAM cell **400**A is described above with respect to SRAM cell **100** in **FIG. 1**. SRAM cell **400**A depicts an exemplary implementation of SRAM cell **100** in which the devices forming SRAM cell **400**A are formed in a stacked configuration to reduce layout area consumed by SRAM cell **400**A in an actual integrated circuit (IC). Specifically, IGFET access element **420** is formed in a first semiconductor layer **401-1**, and NDR-FET elements **411** and **412** are formed in a second semiconductor layer **401-2** (separated from first semiconductor layer **401-1** by an insulating layer **402-1** (e.g., oxide layer)), such that NDR-FET element **411** overlies IGFET access element **420**.

[0030] IGFET access element **420** includes source/drain regions R**5** and R**6** that are formed in first semiconductor layer **401-1**, with a dielectric layer D**3** formed on first semiconductor layer **401-1** between source/drain regions R**5** and R**6**, and with a gate G**3** formed on dielectric layer D**3**. Note that IGFET access element **420** is considered to be formed "in" first semiconductor layer **401-1** because source/

drain regions R5 and R6 are formed in first semiconductor layer **401-1** (even through dielectric layer D3 and gate G3 are actually formed "on" first semiconductor layer **401-1**). NDR-FET element **411** includes a source/drain region R1 and a source/drain region R2 that is shared with NDR-FET element **412**. NDR-FET element **411** further includes a dielectric layer D1 formed on second semiconductor layer **401-2** between source/drain regions R1 and R2, and a gate G1 formed on dielectric layer D1. Similarly, NDR-FET element **412** includes source/drain regions R2 and R3, a dielectric layer D2 formed on second semiconductor layer **401-2** between source/drain regions R2 and R3, and a gate G2 formed on dielectric layer D2. Dielectric layers D1 and D2 include charge trapping layers C1 and C2, respectively, that provide the NDR characteristics for NDR-FET elements **411** and **412** described above. Finally, a vertical interconnect (plug) **405**A connects source/drain region R6 of IGFET access element **420** with source/drain region R2 of NDR-FET elements **411** and **412** and forms a storage node for SRAM cell **400**A.

[0031] As described above with respect to **FIG. 1**, supply voltages V_{S1} and V_{S2} (e.g., ground potential and V_{DD}, respectively) are connected across the series-connected NDR-FET elements **411** and **412**, and appropriate bias voltages V_{BIAS1} and V_{BIAS2} are supplied to gates G1 and G2, respectively, to cause NDR-FET elements **411** and **412** to exhibit the desired bi-stable latch behavior. As further described above with respect to **FIG. 1**, gate G3 and source/drain region R5 of IGFET access element **420** are coupled to word (read/write) line WORD and a bit (data) line BIT, respectively, to control access and data communications with SRAM cell **400**A.

[0032] In this manner, SRAM cell **400**A provides a compact implementation of an SRAM cell. Because NDR-FET element **411** overlies (i.e., is positioned above) IGFET access element **420**, the chip area (i.e., plan view area looking down at the chip) consumed by SRAM cell **400**A is essentially equivalent to a 2T (two transistor) cell. Note that although both NDR-FET elements **411** and **412** are depicted as being formed in the same semiconductor layer **401-2** for exemplary purposes (and to simplify manufacturing), any distribution of devices between semiconductor layers **401-1** and **401-2** can be used to achieve the benefit of the stacked configuration. For example, IGFET access element **420** could be formed in second semiconductor layer **401-2** and both NDR-FET elements **411** and **412** could be formed in first semiconductor layer **401-1**. Alternatively, IGFET access element **420** could be formed with one of NDR-FET elements **411** and **412** in one of semiconductor layers **401-1** and **401-2**, with the other NDR-FET element being formed by itself in the other semiconductor layer. Various other configurations will be readily apparent.

[0033] Note further that additional area reduction for a 3T SRAM cell can be achived via stacking of all three devices in the cell (i.e., arranging the three transistors one above another). **FIG. 4B** is a schematic cross-sectional view of an SRAM cell **400**B consisting of the two NDR-FET elements **411** and **412** and the one enhancement-mode IGFET access element **420** described with respect to SRAM cell **400**A in **FIG. 4A**. However, unlike SRAM cell **400**A, which is formed in two semiconductor layers, SRAM cell **400**B is formed in three semiconductor layers **401-1**, **401-2**, and **401-3** (which are separated by insulating layers **402-1** and **402-2**). Therefore, IGFET access element **420** and NDR-FET elements **411** and **412** can be formed over one another so that SRAM cell **400**A effectively occupies the area of a 1T (one transistor) cell.

[0034] For exemplary purposes, IGFET access element **420** (which includes source/drain regions R5 and R6, dielectric layer D3, and gate G3) is formed in first semiconductor layer **401-1**, NDR-FET element **411** (which includes source/drain regions R1 and R2, dielectric layer D1 (including charge trapping layer C1), and gate GI) is formed in second semiconductor layer **401-2**, and NDR-FET element **412** (which includes source/drain regions R3 and R4, dielectric layer D2 (including charge trapping layer C2), and gate G2) is formed in third semiconductor layer **401-3**. Note, however, that in various other embodiments, SRAM cell **400**B can include any distribution of NDR-FET elements **411** and **412** and IGFET access element **420** among semiconductor layers **401-1**, **401-2**, and **401-3**. A vertical interconnect **405**B connects the source/drain regions R2, R4, and R6 of NDR-FET element **412**, NDR-FET element **411**, and IGFET access element **420**, respectively, and forms storage node for SRAM cell **400**B. Because NDR-FET elements **411** and **412** and IGFET access element **420** all overlie one another (i.e., are formed one over the other in a single stack), SRAM cell **400**B implements the circuit of **FIG. 1** in an extremely space-efficient manner.

[0035] While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. It will be clearly understood by those skilled in the art that foregoing description is merely by way of example and is not a limitation on the scope of the invention, which may be utilized in many types of integrated circuits made with conventional processing technologies. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. Such modifications and combinations, of course, may use other features that are already known in lieu of or in addition to what is disclosed herein. It is therefore intended that the appended claims encompass any such modifications or embodiments. While such claims have been formulated based on the particular embodiments described herein, it should be apparent the scope of the disclosure herein also applies to any novel and non-obvious feature (or combination thereof) disclosed explicitly or implicitly to one of skill in the art, regardless of whether such relates to the claims as provided below, and whether or not it solves and/or mitigates all of the same technical problems described above. Finally, the applicants further reserve the right to pursue new and/or additional claims directed to any such novel and non-obvious features during the prosecution of the present application (and/or any related applications).

1. A memory cell comprising:

a first negative differential resistance field effect transistor (NDR-FET);

a second NDR-FET connected in series with the first NDR-FET; and

an access transistor connected between a data line and a junction between the first NDR-FET and the second NDR-FET,

wherein at least one of the first NDR-FET, the second NDR-FET, and the access transistor overlies at least another of the first NDR-FET, the second NDR-FET, and the access transistor.

2. The memory cell of claim 1, wherein the access transistor is formed in a first semiconductor layer,

wherein the first NDR-FET and the second NDR-FET are formed in a second semiconductor layer, the second semiconductor layer overlying the first semiconductor layer, and

wherein one of the first NDR-FET and the second NDR-FET overlies the access transistor.

3. The memory cell of claim 2, wherein the first NDR-FET and the second NDR-FET share a common source/drain region.

4. The memory cell of claim 1, wherein the first NDR-FET and the second NDR-FET are formed in a first semiconductor layer,

wherein the access transistor is formed in a second semiconductor layer, the second semiconductor layer overlying the first semiconductor layer, and

wherein the access transistor overlies one of the first NDR-FET and the second NDR-FET.

5. The memory cell of claim 4, wherein the first NDR-FET and the second NDR-FET share a common source/drain region.

6. The memory cell of claim 1, wherein the first NDR-FET and the access transistor are formed in a first semiconductor layer,

wherein the second NDR-FET is formed in a second semiconductor layer, the second semiconductor layer overlying the first semiconductor layer, and

wherein the second NDR-FET overlies one of the first NDR-FET and the access transistor.

7. The memory cell of claim 1, wherein the first NDR-FET is formed in a first semiconductor layer,

wherein the second NDR-FET and the access transistor are formed in a second semiconductor layer, the second semiconductor layer overlying the first semiconductor layer, and

wherein one of the second NDR-FET and the access transistor overlies the first NDR-FET.

8. The memory cell of claim 1, wherein the first NDR-FET, the second NDR-FET, and the access transistor are arranged one above another.

9. The memory cell of claim 8, wherein the first NDR-FET is formed in a first semiconductor layer,

wherein the second NDR-FET is formed in a second semiconductor layer,

wherein the access transistor is formed in a third semiconductor layer,

wherein the first semiconductor layer overlies the second semiconductor layer, and

wherein the second semiconductor layer overlies the third semiconductor layer.

10. The memory cell of claim 8, wherein the first NDR-FET is formed in a first semiconductor layer,

wherein the second NDR-FET is formed in a second semiconductor layer,

wherein the access transistor is formed in a third semiconductor layer, and

wherein the third semiconductor layer overlies the first semiconductor layer and the second semiconductor layer overlies the third semiconductor layer.

11. The memory cell of claim 8, wherein the first NDR-FET is formed in a first semiconductor layer,

wherein the second NDR-FET is formed in a second semiconductor layer,

wherein the access transistor is formed in a third semiconductor layer, and

wherein the third semiconductor layer overlies the first semiconductor layer and the second semiconductor layer.

12. A method for making a memory cell, the method comprising:

forming a first negative differential resistance (NDR) field effect transistor (FET) in series with a second NDR-FET;

forming an access transistor for connecting a data line to a junction between the first NDR-FET and the second NDR-FET,

wherein at least one of the first NDR-FET, the second NDR-FET, and the access transistor overlies at least another of the first NDR-FET, the second NDR-FET, and the access transistor.

13. The method of claim 12, wherein forming the access transistor comprises forming the access transistor in a first semiconductor layer, the method further comprising:

forming an insulating layer over the access transistor;

forming a second semiconductor layer over the insulating layer, wherein forming the first NDR-FET in series with the second NDR-FET comprises forming the first NDR-FET and the second NDR-FET in the second semiconductor layer such that one of the first NDR-FET and the second NDR-FET overlies the access transistor; and

forming a vertical interconnect between a source/drain region of the access transistor and the junction between the first NDR-FET and the second NDR-FET.

14. The method of claim 13, wherein the junction between the first NDR-FET and the second NDR-FET comprises a shared source/drain region.

15. The method of claim 12, wherein forming the forming the first NDR-FET in series with the second NDR-FET comprises forming the first NDR-FET and the second NDR-FET in a first semiconductor layer, the method further comprising:

creating an insulating layer over the first NDR-FET and the second NDR-FET;

creating a second semiconductor layer over the insulating layer, wherein forming the access transistor comprises forming the access transistor in the second semiconductor layer such that the access transistor overlies one of the first NDR-FET and the second NDR-FET; and

forming a vertical interconnect between a source/drain region of the access transistor and the junction between the first NDR-FET and the second NDR-FET.

16. The method of claim 15, wherein the junction between the first NDR-FET and the second NDR-FET comprises a shared source/drain region.

17. The method of claim 12, wherein forming the access transistor comprises forming the access transistor in a first semiconductor layer, and

wherein forming the first NDR-FET in series with the second NDR-FET comprises:

forming the first NDR-FET in the first semiconductor layer;

creating an insulating layer over the access transistor and the first NDR-FET;

creating a second semiconductor layer over the insulating layer; and

forming the second NDR-FET in the second semiconductor layer,

wherein the second NDR-FET overlies one of the first NDR-FET and the access transistor.

18. The method of claim 12, wherein forming the access transistor comprises forming the access transistor in a first semiconductor layer, and

wherein forming the first NDR-FET in series with the second NDR-FET comprises:

creating a first insulating layer over the access transistor;

creating a second semiconductor layer over the first insulating layer;

forming the first NDR-FET in the second semiconductor layer such that the first NDR-FET overlies the access transistor;

creating a second insulating layer over the first NDR-FET;

creating a third semiconductor layer over the second insulating layer;

forming the second NDR-FET in the third semiconductor layer such that the second NDR-FET overlies the first NDR-FET; and

forming a vertical interconnect connecting a source/drain region of the second NDR-FET, a source/drain region of the first NDR-FET, and a source/drain region of the access transistor.

19. The method of claim 12, wherein forming the first NDR-FET in series with the second NDR-FET comprises:

forming the first NDR-FET in a first semiconductor layer;

creating a first insulating layer over the first NDR-FET;

creating a second semiconductor layer over the first insulating layer;

forming the second NDR-FET in the second semiconductor layer such that the second NDR-FET overlies the first NDR-FET;

creating a second insulating layer over the second NDR-FET;

creating a third semiconductor layer over the second insulating layer, wherein forming the access transistor comprises forming the access transistor in the third semiconductor layer such that the access transistor overlies the second NDR-FET; and

forming a vertical interconnect connecting a source/drain region of the access transistor, a source/drain region of the second NDR-FET, and a source/drain region of the first NDR-FET.

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