OPEN TUBE DIFFUSION IN III-V COMPOUNDS

Filed May 1, 1972 8 Sheets-Sheet 1

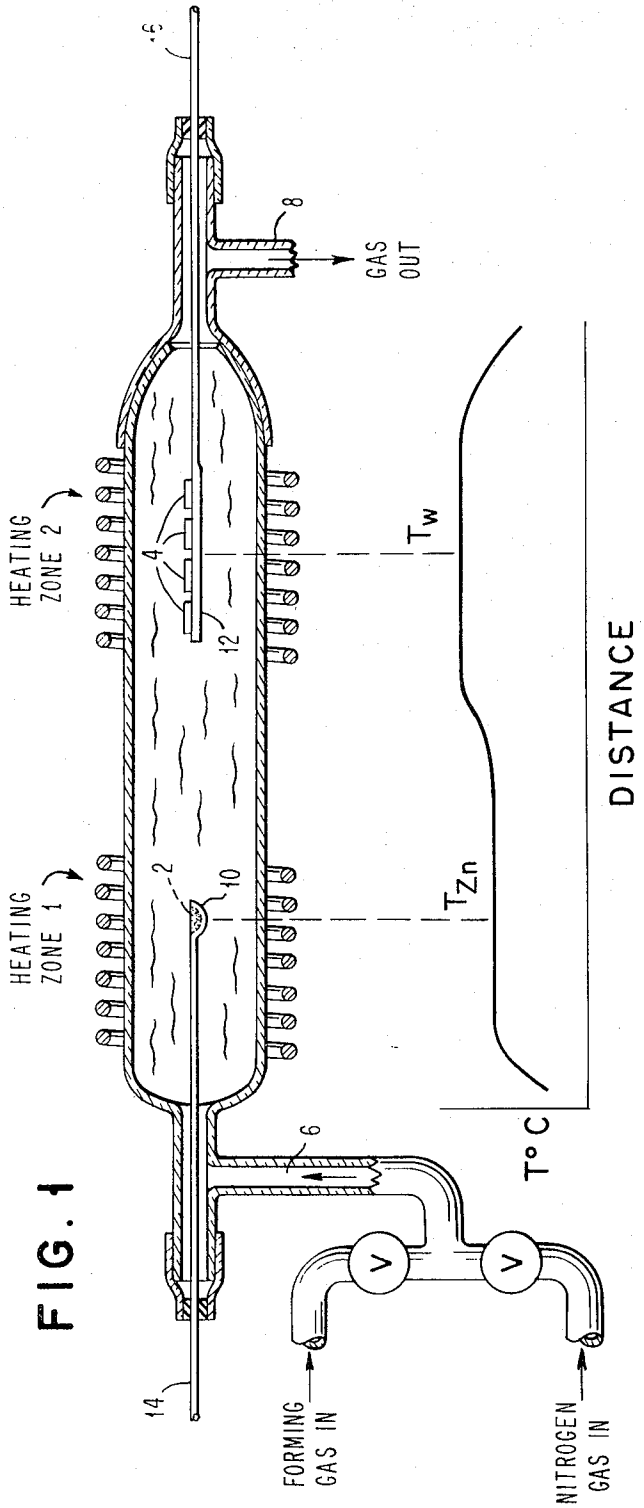


FIG. 1

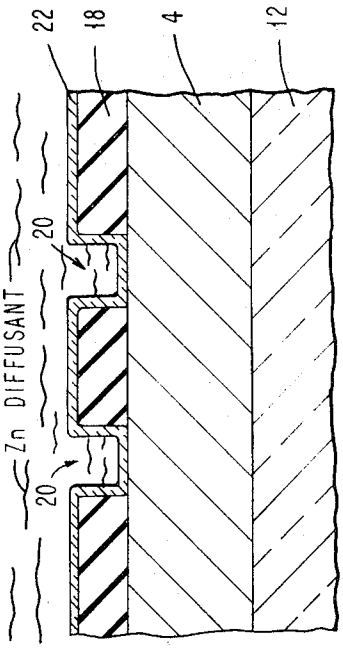


FIG. 2

FIG. 4

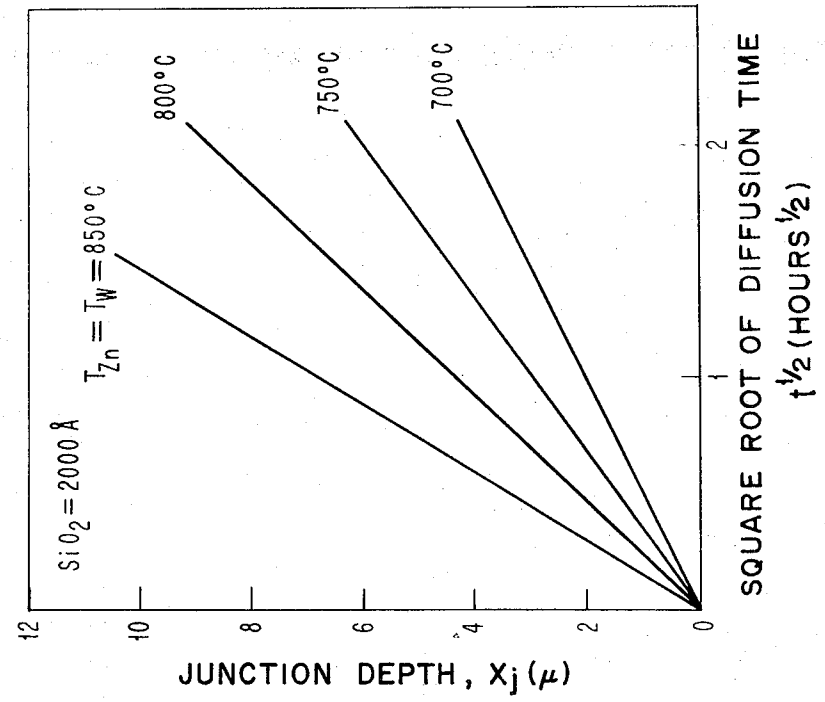

$SiO_2 = 2000$ Å
$T_{Zn} = T_W = 850°C$
800°C
750°C
700°C
JUNCTION DEPTH, X_j (μ)
SQUARE ROOT OF DIFFUSION TIME
$t^{1/2}$ (HOURS$^{1/2}$)

FIG. 3

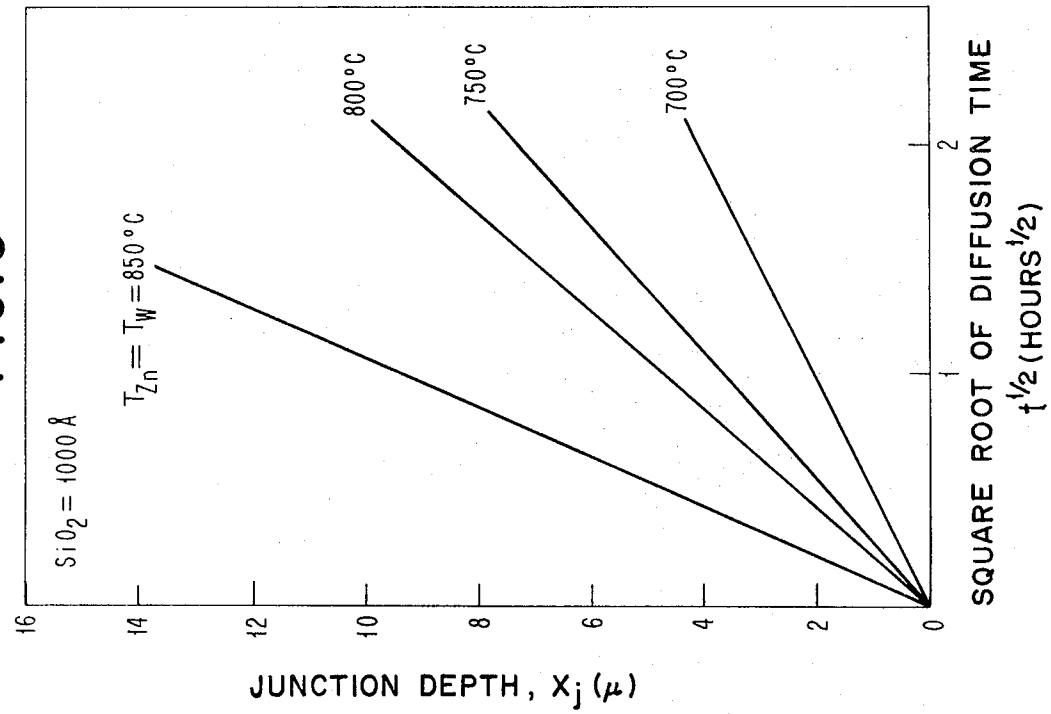

$SiO_2 = 1000$ Å
$T_{Zn} = T_W = 850°C$
800°C
750°C
700°C
JUNCTION DEPTH, X_j (μ)
SQUARE ROOT OF DIFFUSION TIME
$t^{1/2}$ (HOURS$^{1/2}$)

FIG. 5

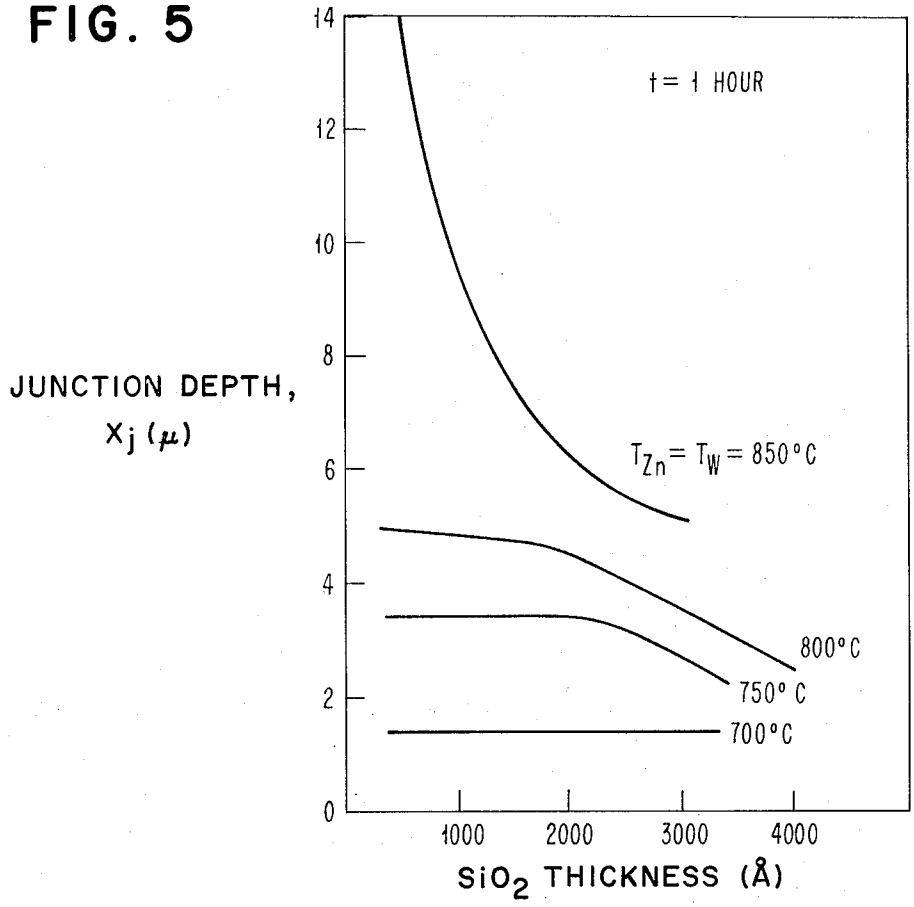

JUNCTION DEPTH, X_j (μ)
14
12
10
8
6
4
2
0
t = 1 HOUR
$T_{Zn} = T_W = 850°C$
800°C
750°C
700°C
1000
2000
3000
4000
SiO_2 THICKNESS (Å)

FIG. 6

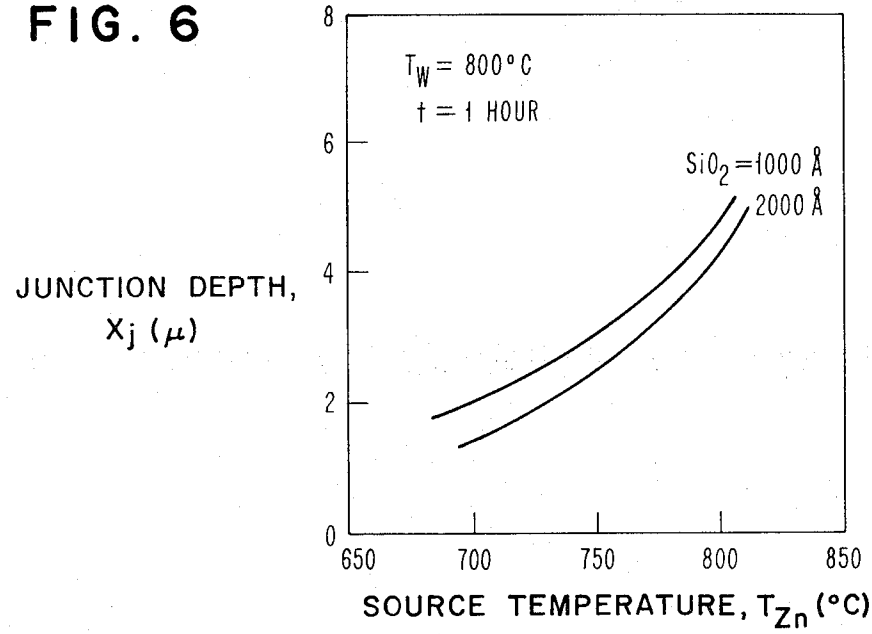

JUNCTION DEPTH, X_j (μ)
8
6
4
2
0
$T_W = 800°C$
t = 1 HOUR
SiO_2 = 1000 Å
2000 Å
650
700
750
800
850
SOURCE TEMPERATURE, T_{Zn} (°C)

FIG. 7

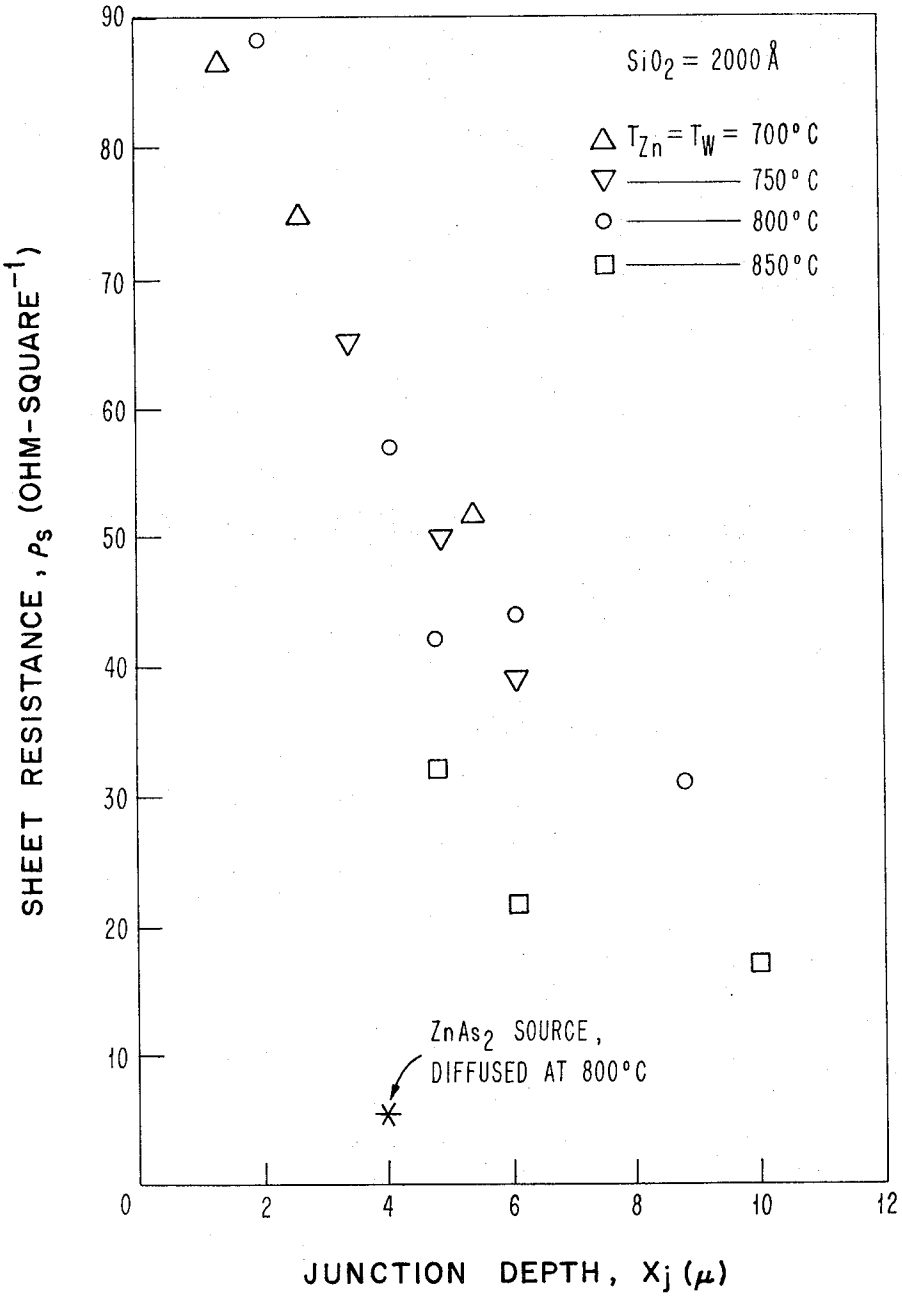

SiO_2 = 2000 Å
$T_{Zn} = T_W$ = 700° C
750° C
800° C
850° C
$ZnAs_2$ SOURCE, DIFFUSED AT 800°C
SHEET RESISTANCE, ρ_s (OHM-SQUARE^{-1})
JUNCTION DEPTH, X_j (μ)
90
80
70
60
50
40
30
20
10
0
2
4
6
8
10
12

FIG. 8

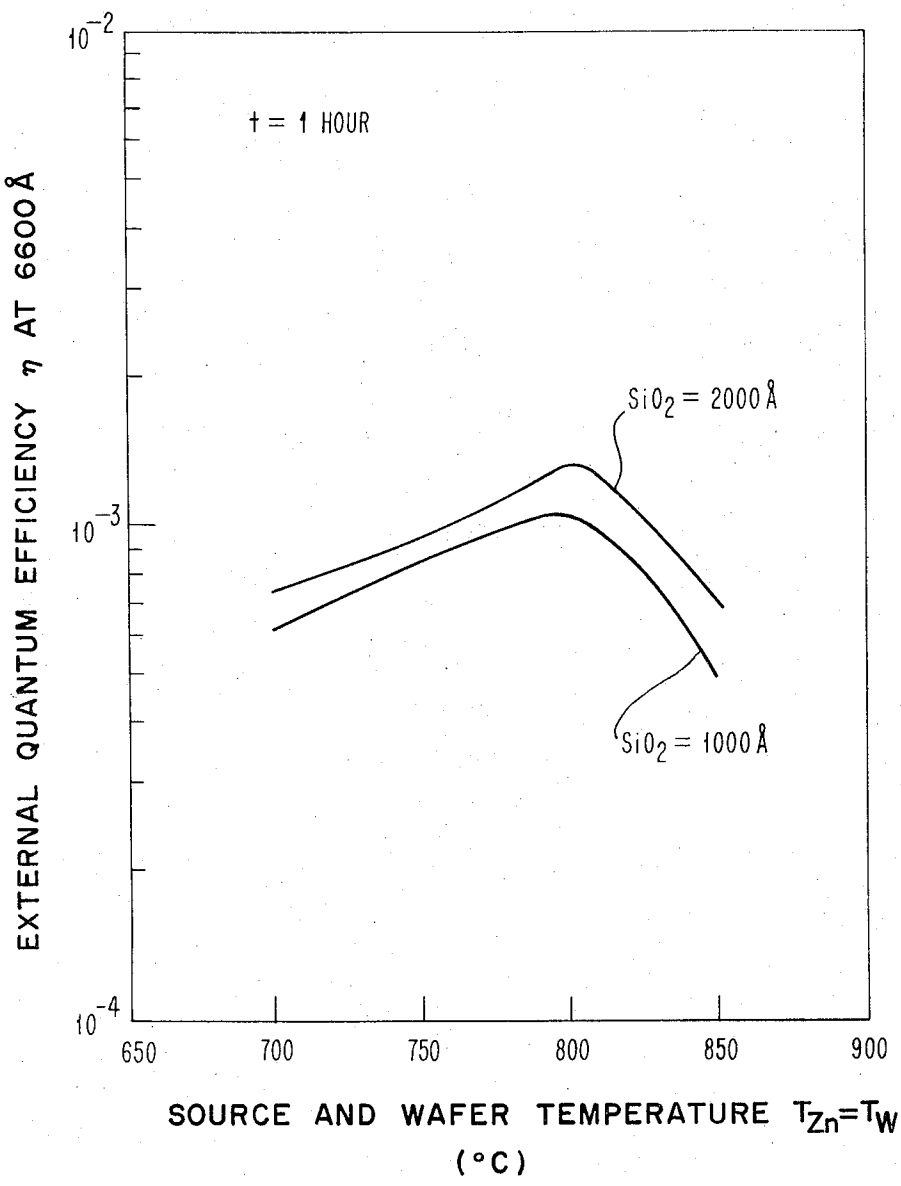
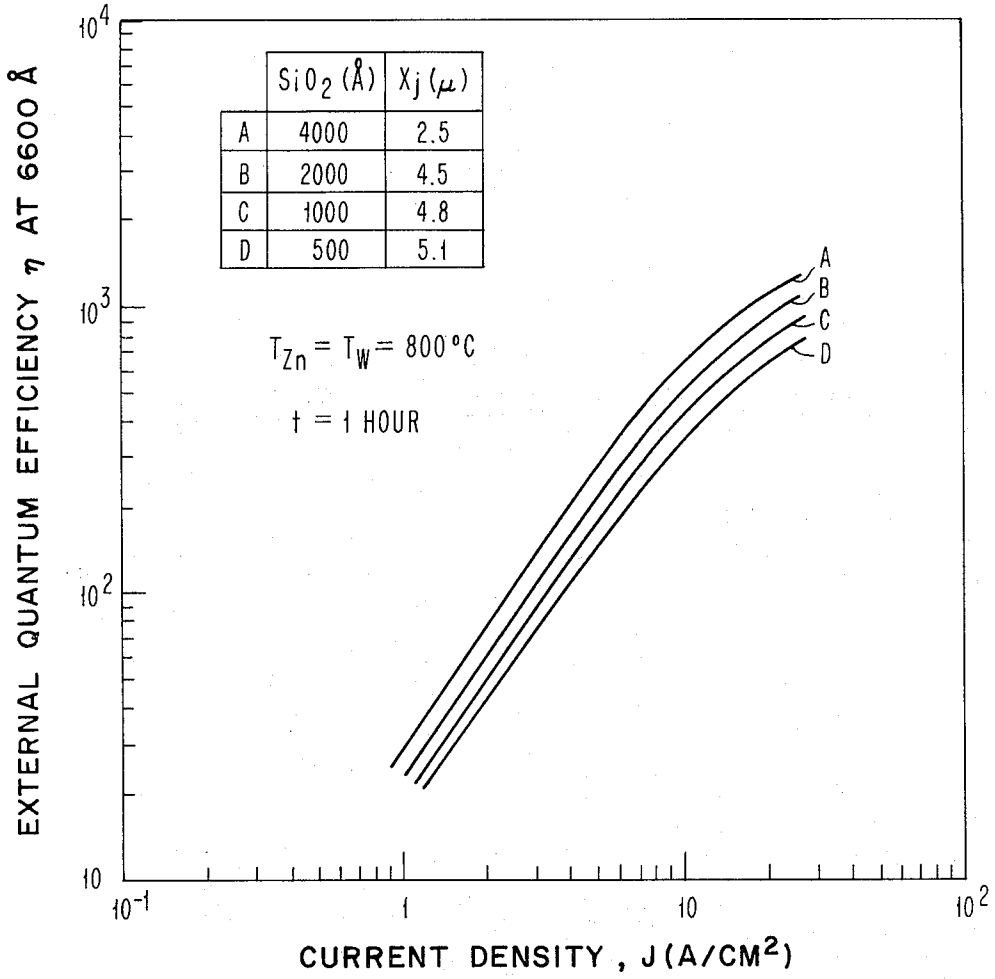

10^{-2}
10^{-3}
10^{-4}
t = 1 HOUR
SiO_2 = 2000 Å
SiO_2 = 1000 Å
650
700
750
800
850
900
EXTERNAL QUANTUM EFFICIENCY η AT 6600 Å
SOURCE AND WAFER TEMPERATURE $T_{Zn}=T_W$
(°C)

FIG. 9



	SiO_2 (Å)	X_j (μ)
A	4000	2.5
B	2000	4.5
C	1000	4.8
D	500	5.1

FIG. 10

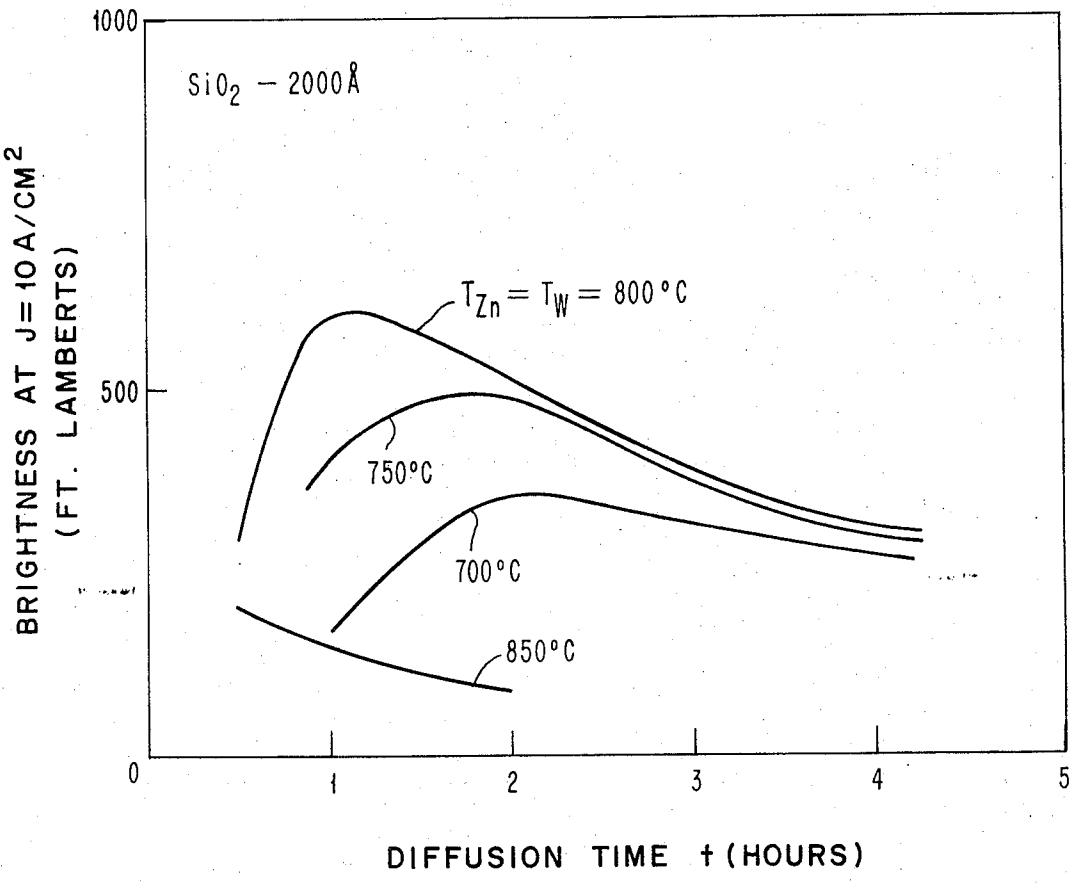

1000
500
0
SiO_2 – 2000Å
$T_{Zn} = T_W = 800°C$
750°C
700°C
850°C
1
2
3
4
5
BRIGHTNESS AT J = 10 A/CM²
(FT. LAMBERTS)
DIFFUSION TIME t (HOURS)

FIG. 11

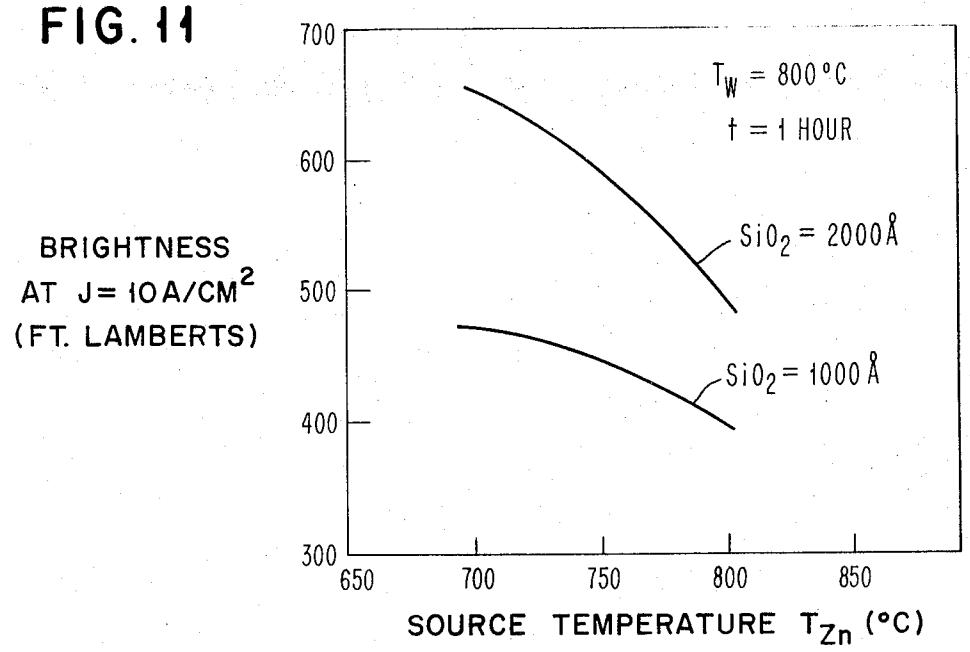
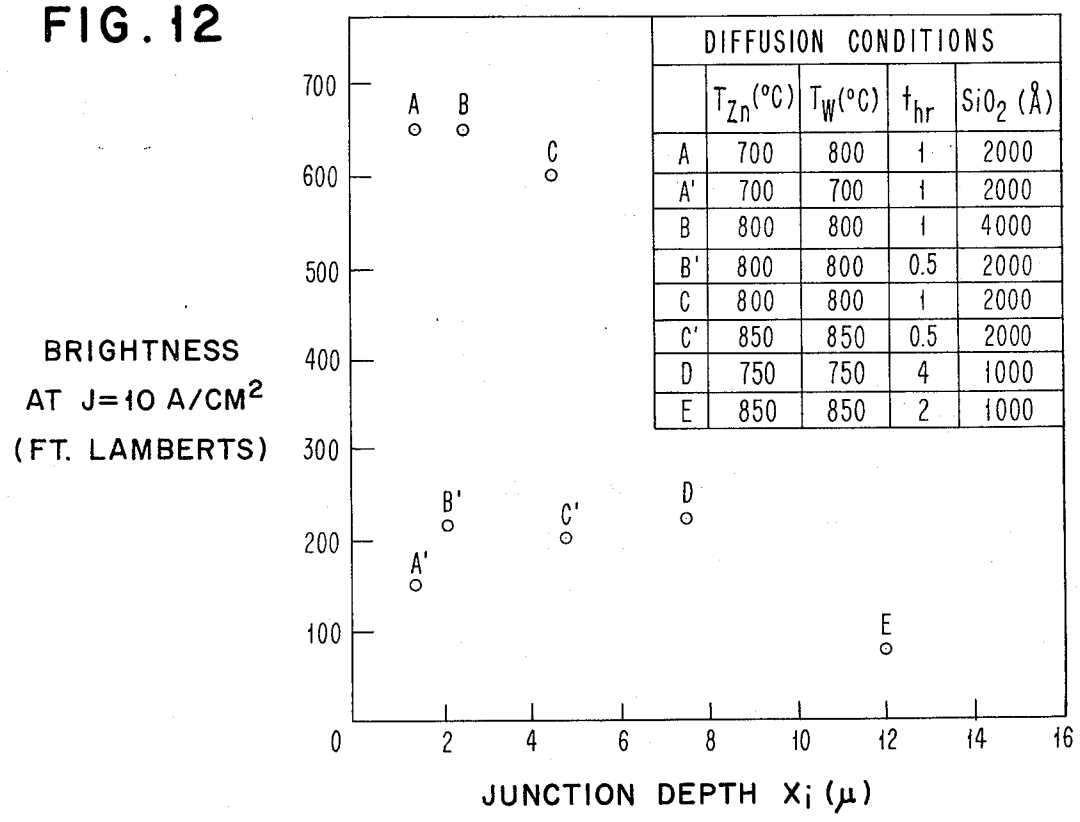


FIG. 12



DIFFUSION CONDITIONS				
	T_{Zn}(°C)	T_W(°C)	t_{hr}	SiO_2 (Å)
A	700	800	1	2000
A'	700	700	1	2000
B	800	800	1	4000
B'	800	800	0.5	2000
C	800	800	1	2000
C'	850	850	0.5	2000
D	750	750	4	1000
E	850	850	2	1000

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3,764,414

OPEN TUBE DIFFUSION IN III–V COMPOUNDS

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Int. Cl. H01l 7/44
U.S. Cl. 148—189 8 Claims

ABSTRACT OF THE DISCLOSURE

An open tube process is used for Zn diffusion in III–V compounds coated with SiO_2 films to form p-n junctions. Electroluminescent diodes made by this method have high brightness with no etching of the p-n junction surface required.

BACKGROUND OF THE INVENTION

Zn diffusion into III–V compounds such as GaAs, $GaAs_{1-x}P_x$, GaP, etc. has commonly been carried out in sealed quartz ampoules or tubes. The vacuum and arsenic pressure in such a closed system are critical factors in the control of (a) junction depth and (b) surface concentration of the zinc dopant. Failure to control either vacuum or arsenic pressure within very close tolerances makes it difficult to attain reproducibility of uniformly diffused compounds. Additionally, zinc and arsenic vapors, when an oxide mask is used in conjunction with a wafer undergoing diffusion, attack the window openings of such mask, further complicating the probability of achieving reproducibility in that subsequent processing of the wafer is made difficult by such attack.

Workers in the field of dealing with Zn diffused GaAs, as exemplified by an article by S. R. Shorts et al., appearing on pages 300+ in the 1964 issue of Transactions of the Metallurgical Society AIME 230 and an article by M. Beeke et al. which appeared on pages 307+ of the same publication, in order to reduce the surface Zn concentration for making transistors, employed a thin layer of SiO_2 on the surface of their GaAs wafer. The thin layer of SiO_2 also served as a film protecting GaAs from erosion due to the dissociation of GaAs. However, what was not appreciated by such prior workers in the field was that the use of a SiO_2 erosion-preventing layer now removed the need for employing a closed tube diffusion process with its attendant ills, i.e., cumbersome, time-consuming, expensive, etc. Besides, this process can be applied to other III–V compounds such as $GaAs_{1-x}P_x$ which yields high efficient, bright, light-emitting diodes with no surface etching required.

The process of fabricating planar monolithic II–V light emitting diodes and arrays is greatly simplified by sputtering an Al_2O_3 film as a mask against zinc on a III–V compound crystal wafer. Diffusion patterns are delineated in the Al_2O_3. Before diffusion of zinc is begun, a film of SiO_2 is deposited over the wafer to prevent surface erosion during diffusion. The diffusions are done in an open tube furnace with forming gas, i.e., a gas mixture of 90% nitrogen and 10% hydrogen, flowing in the furnace at a temperature of about 800° C. for a time varying from 30 minutes to an hour to give a diffusion depth of about 3–6μ.

Consequently, it is an object to diffuse dopants into III–V crystal wafers using open tube apparatus.

It is yet another object that pure Zn can be used as a source in an open tube at high temperature.

It is yet another object to achieve planar monolithic doped III–V compounds using an open tube apparatus.

It is yet another object to use an open tube apparatus for doping III–V compounds coated with SiO_2 films without eroding the surface of such compounds.

It is a further object to obtain high bright efficient $GaAs_{1-x}P_x$ light emitting diodes with no surface etching required.

The foregoing and other objects, features, and advantages of the invention will be apparent from the following more particular description of the preferred embodiments of the invention as illustrated in the accompanying drawings.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is an open tube furnace employed in the diffusing of a dopant into a III–V compound with an accompanying graph plotting temperature as a function of distance into the furnace.

FIG. 2 is a showing of an Al_2O_3 mask, having an SiO_2 layer in the windows of the mask, employed with a wafer of a III–V compound in an open tube diffusion apparatus.

FIGS. 3–12 are graphs depicting various characteristics of a Zn diffused $GaAs_{1-x}P_x$ by an open tube method as functions of SiO_2 thickness, temperature of the furnace, time of diffusion, etc.

DESCRIPTION OF THE INVENTION

The open tube diffusion system is applicable to many III–V materials, such as, but not limited to $GaAs_{1-x}P_x$, $Al_xGa_{1-x}As$, GaAs or GaP. For purposes of demonstrating the invention, extensive tests were made only on the compound GaAs $_{1-x}P_x$, where x varied between 0.38–0.4. The latter choice of x was made so that the doped $GaAs_{1-x}P_x$ would, when made into a diode, emit in the visible region of the electromagnetic spectrum. The carrier concentration n was between 1 to 3×10^{17} cm.$^{-3}$. Additionally, the GaAsP wafer had a total thickness of vapor grown epitaxial layer of 76.9μ with ~35.9μ of it graded in composition and the remaining layer having constant composition.

The diffusion apparatus shown in FIG. 1 consists of a two-zone furnace, zone **1** housing a souce **2** of dopant, which was chosen to be zinc, and a second zone, zone **2**, that houses the wafers **4** of GaAsP. A constant flow of N_2 is maintained throughout the diffusion process, entering the furnace through inlet **6** and leaving through exit port **8**. Zn pellets **2** of high purity are loaded in a boat **10** and the wafers **4** of GaAsP are loaded on a flat plate **12** in zone **2** of the furnace. N_2 gas is turned off and forming gas is then turned on to flow at a rate of about 400 cc./min. for a half-hour to flush the furnace. After flushing, the Zn-containing boat **10** is pushed into zone **1** and, after ten minutes, the wafers **4** are pushed into zone **2**, rods **14** and **16** being relied upon for locating Zn and wafers, respectively, in the furnace.

Prior to inserting a GaAsP wafer **4** into the furnace, a mask **18** (see FIG. 2) of Al_2O_3 is deposited over the wafer **4** and the windows **20** of the mask, as well as the mask, are covered with a thin layer **22**, of the order of 1000 A.–2000 A. thick, of SiO_2. The SiO_2 layers are deposited by a pyrolytic decomposition process wherein SiO_2 is deposited as a result of the decomposition of tetraethylorthosilicate (TEOS) in an oxygen atmosphere. SiO_2 thicknesses of 500 A. to 4000 A. have been grown with a deposition rate of 60 A./min., with a thickness of 1000 A.–2000 A. being preferred.

Diffusions of Zn, in the open tube furnace of FIG. 1, have taken place where the temperature of the wafer **4** was the same as that of the source **2** and the temperatures were chosen to be 700° C., 750° C., 800° C. and 850° C. and the times of diffusion varied from one half-hour to 4 hours in intervals of a half-hour. Results were obtained, and will be discussed hereinafter, using a fixed wafer **4** temperature of 800° C., but different Zn temperature of 700° C., 750° C. and 800° C., and a diffusion time of one hour.

After diffusion, the forming gas is turned of and N_2 is turned on prior to removal of the wafers **4** from the furnace. SiO_2 films **22** are removed by etching from the wafers **4** and the junction depth of a GaAsP wafer can be measured by developing a junction interface with a

$$1\ HF:1H_2O_2:3H_2O$$

etch in a cleavage plane normal to the junction. Diodes are made by electroplating Au–Sn films or spots onto the substrate side of a wafer **4** after that substrate has been thinned to reduce series resistance. Small cleaved sections, having an area of about 10^{-3} cm.^{2}, are mounted on a header and aluminum wire is ultrasonically bonded to the p-surface of the cut wafer. Plots shown in FIGS. 3–12 are measurements of wavelength, λ, external quantum efficiency, η, and brightness β, of such diodes that were manufactured from a doped GaAsP wafer that was treated with SiO_2 prior to being placed in a diffusion furnace.

Films of SiO_2 with thicknesses of 500 A., 1000 A., 2000 A. and 4000 A. were deposited on the surfaces of the wafers to study the effect of SiO_2 thickness on other parameters. However, for SiO_2 films around 4000 A. thick, the oxide sometimes cracked to give an erratic junction depth. On the other hand, if the oxide thickness was less than 500 A., a non-uniform junction depth often occurred. Hence, most of the data are from wafers deposited with 1000 A. and 2000 A. thick SiO_2 films.

The junction depth X_j for various Zn diffusions with the same source and wafer temperatures between 700° C. and 850° C. verus the square root of time are plotted inn FIGS. 3 and 4 for 1000 A. and 2000 A. thick SiO_2 films, respectively. An approximately linear relationship is observed which means that Fick's law is obeyed. This information is helpful for predicting the junction depths at other diffusion temperatures and times. Results of diffused junction depth X_j versus the SiO_2 thickness when Zn temperature (T_{Zn}) equals wafer temperature (T_w) for a one hour of Zn diffusion are shown in FIG. 5. This figure indicates that at the lowest temperature (700° C.) the junction depth is almost independent of oxide thickness; while at higher temperatures (850° C.), the junction depth decreases drastically with increasing oxide thickness.

FIG. 6 shows the diffused junction depth as a function of source temperature for a one hour diffusion while the wafer temperature is kept constant at 800° C. The junction depth decreases when the source temperature decreases which implies that different junction depths can be also obtained by varying the source temperature.

The sheet resistance ρ_s of the diffused layers of some of the wafers have been measured by the four point probe method. In FIG. 7, the sheet resistance versus junction depth for zinc diffused layers formed at different temperatures are plotted. The sheet resistance of the Zn diffused layers in $GaAs_{1-x}P_x$ using $ZnAs_2$ as a source diffused at 800° C. in a closed tube has been measured as denoted by a star in FIG. 7. One significant result is that at a given junction depth, the sheet resistance of the layers diffused in the open tube system is much higher than that using $ZnAs_2$ source in a closed tube system. Hence the Zn concentration in the oxide coated

$$GaAs_{1-x}P_x$$

layers diffused by the open tube method must be lower than that in layers diffused by conventional $ZnAs_2$ source closed tube method. The surface concentration C_0 of some wafers were measured using plasma resonance method. For the wafers diffused at $T_{Zn}=T_w=800°$ C. with a 2000 A. thick SiO_2 film on the surface, C_0 is approximately equal to 3.5×10^{19} cm.$^{-3}$. The lowest C_0 measured is about 1.4×10^{19} cm.$^{-3}$ when $T_{Zn}=T_w=700°$ C. with a 1000 A. thick SiO_2 film on the surface during diffusion. C_0 is approximately equal to 1.1×10^{20} cm.$^{-3}$ if $ZnAs_2$ source is used in a closed ampoule diffused at 800° C. This result is consistent with the sheet resistance measurement.

The external quantum efficiency and wavelength of the diffused $GaAs_{1-x}P_x$ diodes have been measured. It was found that the efficiency did not vary very much in our diffusion studies even though the temperatures of the source and wafers was changed between 700° C. to 850° C. The average efficiency was about 10^{-3} at 6600 A. for uncoated diodes. The highest value obtained was about 2.4×10^{-3} at 6650 A. for uncoated diodes. Values of the external quantum efficiencies of diodes made from wafers diffused for one hour at various temperatures and with $T_{Zn}=T_w$ are shown in FIG. 8. The results show that the efficiencies of diodes made with an SiO_2 thickness of 2000 A. are better than those with a thickness of 1000 A.

The brightness was measured with a Spectra Brightness Spot Meter Model UB viewing an 8 mil diameter area. The area of most of the diodes varied between $.8\times10^{-3}$ cm.^{2} and 1.2×10^{-3} cm.^{2}. So far, the highest brightness we have measured was about 1000 ft. Lamberts at a current density of 10 a./cm.^{2} and at 6650 A., without etching the surface of the diodes.

Typical curves of brightness versus current density of diodes made from wafers diffused at $T_{Zn}=T_w=800°$ C. for one hour with different oxide thicknesses are shown in FIG. 9. These results are to be expected. When the oxide thickness increases, the junction depth decreases and the brightness increases. FIG. 10 demonstrates the effects of diffusion time on brightness when the wafer 4 temperature and source temperature of Zn source 2 are equal. The brightness at current density 10 a./cm.^{2} is plotted for comparison. When the temperature increases from 700° C. to 800° C., the brightness also increases. A maximum value is obtained at 800° C. for a one hour diffusion. When the temperature increases further to 850° C., an adverse result is obtained which may either be caused by high free carrier absorption due to higher zinc solubility at that temperature or a detrimental heat treatment effect above 800° C. such as an increase of dislocations. In FIG. 11, the luminance is plotted versus source temperature (T_{Zn}) for two different oxide thicknessess while the wafers were diffused for one hour at 800° C. It is apparent that some improvement in brightness can be obtained at a lower source temperature because the junction depth decreases with decreasing source temperature and results in less light absorption at the surface.

FIG. 12 demonstrates the effect of junction depth on the brightness of the diodes. At about the same shallow junction depth of about 1 to 2 μm. deep (points A, A' and B, B' in FIG. 12), the brightness of the diodes can differ by a factor of 3 to 4 depending on the diffusion conditions. When the junction depth is about 4 to 5 μm. deep, the difference in brightness can still be great depending on diffusion conditions. By comparing these diffusion conditions, it seems that some kind of heat treatment effect is involved so that a different wafer temperature and diffusion time could give a different result in brightness at the same junction depth. From FIG. 7 it was found that the sheet resistance of the wafers diffused in the open tube process with SiO_2 film on the surface is higher than that using the $ZnAs_2$ source Higher sheet resistance implies lower Zn concentration or lower p-type free carrier concentration in the diffused layer. Hence, the free carrier absorption in the layer is also reduced. When the junction depth is greater than 7 μm. as shown by points D and E in FIG. 12, the brightness dropped very fast.

Point B in FIG. 12 corresponds to one hour diffusion at $T_{Zn}=T_w=800°$ C. with a 4000 A. SiO_2 deposited on the surface, and point A in FIG. 12 corresponds to a one hour diffusion at $T_{Zn}=700°$ C. and $T_w=800°$ C. with a 2000 A. SiO_2 deposited on the surface. Both diffusions give the same brightness with a shallow junction depth of about 2μm. Since a 4000 A. SiO_2 film usually cracks during the diffusion process, the diffusion condition cor-

responding to point A is preferred. The shallow junction may cause high contact resistance which is not desirable for some applications. In case lower contact resistance is required, diffusion condition corresponding to point C in FIG. 12 which has a deeper junction depth (~4.8 μm.) and higher surface Zn concentration can be used. The diffusion conditions for both points A and C are the same except the source temperature.

In conclusion, it has been shown that SiO_2 films on the surface during diffusion offers surface protection allowing the retention of smooth surfaces. With this protection, open tube diffusions can be used. The surface zinc concentration is lowered by the SiO_2 film so that the free carrier absorption is reduced. Therefore, high brightness results are achieved in these diodes with no etching of the surface required. This in fact is thus a truly planar process. In addition, the open tube approach enables many diffusions to be carried out in quick succession, avoiding the complications associated with encapsulation under vacuum which is necessary in the closed tube system. While only data on $GaAs_{1-x}P_x$ has been given herein, the process has been successfully applied to other III–V semiconductor materials such as: $Al_xGa_{1-x}As$, GaP, and GaAs.

What is claimed is:

1. In a method for forming a p-n- junction in an n-type Group III–V compound comprising the steps of:
   (a) placing a zinc diffusant in one zone of a two zone open tube furnace and a Group III–V compound in the other zone of said furnace, said Group III–V compound having a zinc diffusion mask on its surface to be exposed to the diffusant,
   (b) depositing a layer of pyrolytic SiO_2 on said mask, said layer being of the range between 500–4000 A. thick,
   (c) flushing said open tube contents with forming gas at a rate of about 400 cc./min. for about ½ hour, and
   (d) maintaining said zinc zone at a temperature range of about 700° C. to 850° C. and the Group III–V compound at a temperature range equal to or greater than the zinc zone temperature whereby the efficiency of subsequent light emitting diodes made with such p-n junction is substantially increased.

2. The method of claim 1 wherein said zinc diffusant source is pure zinc.

3. The method of claim 1 wherein the Group III–V compound is $GaAs_{1-x}P_x$.

4. The method of claim 3 wherein x varies from 0.38 to 0.4.

5. The method of claim 1 wherein the Group III–V compound is $Al_xGa_{1-x}As$.

6. The method of claim 1 wherein the Group III–V compound is GaAs.

7. The method of claim 1 wherein the Group III–V compound is GaP.

8. In a method for forming a p-n junction in an n-type Group III–V compound comprising the steps of:
   (a) placing a zinc diffusant in one zone of a two zone open tube furnace and a Group III–V compound in the other zone of said furnace,
   (b) depositing a layer of pyrolytic SiO_2 on said Group III–V compound, said layer being of the range between 500–4000 A. thick,
   (c) flushing said open tube tube contents with forming gas at a rate of about 400 cc./min. for about ½ hour, and
   (d) maintaining said zinc zone at a temperature range of about 700° C. to 850° C. and the Group III–V compound at a temperature range equal to or greater than the zinc zone temperature whereby the efficiency of subsequent light emitting diodes made with such p-n junction is substantially increased.

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GEORGE T. OZAKI, Primary Examiner

U.S. Cl. X.R.

148—186, 187; 252—62.3 G A