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(54) **Title:** AUTOMATIC, HIGHLY RELIABLE, FULLY REDUNDANT ELECTRONIC CIRCUIT BREAKER THAT IN - CLUDES MEANS FOR PREVENTING SHORT-CIRCUIT OVERCURRENT
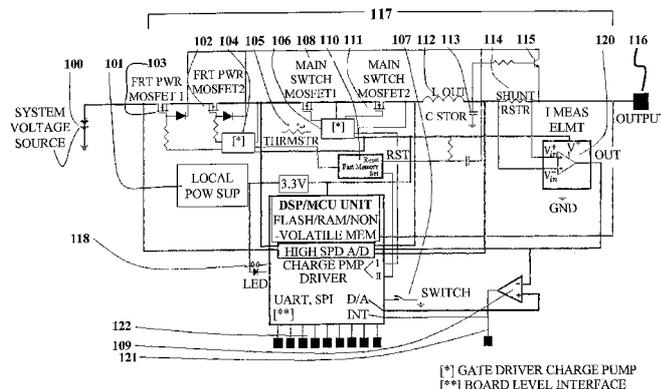
FIG. 1

(57) **Abstract:** A programmable power (PPSE) switching element. In preferred embodiments, the PPSE comprises a front power transistor, a main switching transistor, and optionally at least one reverse current blocking transistors (preferably MOSFETs) in series, the gate of each of which is connected to a gate driver; an inductor and shunt resistor connected in series with the transistors; a charge storage capacitor connected between ground and a junction located between the inductor and the shunt resistor; a high-speed NPN transistor, the collector of which is connected to the front power transistor and the emitter of which is connected to an output of the main switching transistor via the shunt resistor; a current measurement element in parallel to the shunt resistor; a voltage amplifier; and a high-speed MCU.

AUTOMATIC, HIGHLY RELIABLE, FULLY REDUNDANT ELECTRONIC CIRCUIT
BREAKER THAT INCLUDES MEANS FOR PREVENTING SHORT-CIRCUIT
OVERCURRENT

REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from Israel Pat. Appl. No. 237775, filed 16 March 2015, which is incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] This invention relates in general to electronic fuses. In particular, it relates to programmable electronic fuses that prevent high current flow under short circuit conditions, eliminate power source current surges, prevents switching element destruction and increase total fuse reliability.

BACKGROUND OF THE INVENTION

[0003] Programmable Power Switching Systems (PPSS) and Programmable Power Switching Elements (PPSE) and methods are well known in the art for both AC and DC current applications. Such systems are variously known as "smart power switches," "protection systems," "electronic fuses," etc. Most of the systems currently known in the art are directed to detection of short circuits or open loads and to the subsequent execution of steps to protect and isolate the energy source and the load branch. These systems fail to provide any protection or redundancy within the relevant switch if the MOSFET malfunctions, however. Moreover, if there is a delay between the detection of the short circuit and the disconnection of the load branch from the energy source, the MOSFET, the shorted load, and the power source are exposed to the overcurrent, which may reduce the entire system voltage or even melt the MOSFET.

[0004] The systems currently on the market mainly comprise mechanical, thermal, and magnetic fuses. More recently, electronic fuses based on MOSFETs, SiC MOSFETs IGBTs, power transistors or SCR/Triac have been developed. These systems can detect a short circuit and then disconnect the load from the voltage source, but until the disconnection has been completed, the voltage source and the MOSFET(s) will absorb a high current. The relatively high internal resistance of batteries and fuel cells puts constraints on the system reliability, however, because these types of fuses cannot act quickly enough to prevent the

battery from experiencing a high current surge from which they will almost certainly be damaged.

[0005] For example, if the energy source is a 24 V battery with an internal resistance of $0.5\,\Omega$, a short circuit of 50A for even 1 mSec will cause a short to the battery, causing all loads in the electric switching system to lose energy. Due to the high short circuit current, connecting capacitors near the battery will not provide a practical solution to the problem.

[0006] Similarly, if the energy source is for example a 24 V vehicle battery with an internal resistance of lmQ connected to a MOSFET having an internal resistance of 5mQ, a short circuit will conduct a current of 24 V/0.006 Ω = 4000 A. Thus, a delay prior to detection of the short circuit of even 1 ms will cause a short to the battery, causing all loads in the electric switching system to lose energy. Due to the high short circuit current, the MOSFET will be melted.

[0007] In cases in which the power source has a high impedance, power switching systems known in the art generally introduce significant undesired surge current into the circuit. On the other hand, in cases in which the power source is a very low impedance battery or power supply, a short circuit will inevitably produce a high current, at least transiently. A typical circuit that includes a MOSFET cannot handle such a transient high current (on the order of thousands of amperes) even for $1\mu s$. Such an event would melt the transistor and permanently short the load.

[0008] A PPSS/PPSE that rapidly isolates the energy source from the load branch under either short circuit or open load conditions, thereby protecting the energy source and the switching elements from transient high currents produced under such conditions; that insures the reliability and isolation of the MOSFET; and that will fit into a standard fuse holder, remains a long-felt, yet unmet, need.

SUMMARY OF THE INVENTION

[0009] It is an object of the invention herein disclosed to provide such a PPSS and PPSE, in the case of the present invention, in the form of an improved electronic fuse.

[0010] It is therefore an object of the present invention to disclose a programmable power switching element (PPSE), wherein said PPSE comprises: a first terminal (110); a front power transistor (103) comprising a drain connected in series to said first terminal, a source, and a gate; a first gate driver (104) connected to said gate of said front power transistor; a main switching transistor (108) connected in series with said front power transistor, said main

switching transistor comprising a drain, said drain connected to said source of said front power transistor; a first reverse current blocking transistor (102), comprising a drain, a source, and a gate, said first reverse current blocking transistor connected in series with and located between said front power transistor and said main switching transistor, the gate of said first reverse current blocking transistor connected to the first gate driver; a second gate driver (106) connected to said gate of said main switching transistor; second reverse current blocking transistor (111), comprising a drain, a source, and a gate, said second reverse current blocking transistor connected in series with and located between said main switching transistor and a shunt resistor (114), the gate of said second reverse current blocking transistor connected to the second gate driver (106); an inductor (112) connected in series with said second reverse current blocking transistor and located between said second reverse current blocking transistor and said shunt resistor; a charge storage capacitor (113) connected between ground and a junction located between said inductor and said shunt resistor; a first NPN transistor (115) comprising a collector and an emitter, said collector connected to said gate of said front power transistor and said emitter connected to an output (116) of said at least one main switching transistor via said shunt resistor (114) and said inductor; a current measurement element (120) comprising a bidirectional shunt voltage amplifier, said current measurement element connected in parallel with said shunt resistor; a second terminal (116) connected in series with said shunt resistor; and, a high-speed MCU (118) comprising a high-speed A/D converter connected to said transistors and charge storage capacitor and to said voltage amplifier.

[0011] In some preferred embodiments of the invention, the PPSE additionally comprises a high speed memory device (110) configured to identify a short circuit condition and to electrically disconnect said transistors (108, 111) from a source of electrical current. In some particularly preferred embodiments of the invention, said high speed memory device is configured to disconnect said transistors within 200 ns of an occurrence of a short circuit condition.

[0012] It is a further object of this invention to disclose a programmable power switching element (PPSE), wherein said PPSE comprises: a first terminal (110); a first main switching transistor (141) comprising a drain connected in series with said first terminal, a source, and a gate; a gate driver (144) connected to said gate of first main switching transistors; a second main switching transistor (145) connected in series with said first main switching transistor, and comprising a drain, said drain connected to said source of said first main switching

transistor and act as a reverse current blocking transistor connected in series; an inductor **(147)** connected in series with said second main switching transistor; a shunt resistor **(149)** connected in series with said inductor; a charge storage capacitor **(148)** connected between ground and a junction located between said inductor and said shunt resistor; a second terminal **(116)** connected in series with said shunt resistor; an NPN transistor **(150)** comprising a collector and an emitter, said collector connected to said gates of said front power transistors and said emitter connected to said second terminal via said shunt resistor and said inductor; a current measurement element comprising a bidirectional voltage amplifier **(151),** said current measurement element connected in parallel with said shunt resistor; and a high-speed MCU **(146),** comprising a programmable delay unit and a high-speed A/D converter connected to said transistors, to said charge storage capacitor, and to said voltage amplifier.

[0013] It is a further object of this invention a PPSE to disclose a PPSE as defined in any of the above, wherein at least one of said transistors is a MOSFET.

[0014] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said PPSE comprises said first terminal is connectable to a voltage source and said second terminal is connectable to a load.

[0015] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said gate of said first reverse current blocking transistor is connected to said first gate driver **(104).**

[0016] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said gate of said second reverse current blocking transistor is connected to said second gate driver **(106).**

[0017] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said inductor has an inductance of between 10 and 500 nH.

[0018] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said charge capacitor has a capacitance of between 1 and 50 µE.

[0019] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said NPN transistor **(115)** is characterized by an FT of at least 200 MHz. In some preferred embodiments of the invention, said NPN transistor **(115)** is characterized by an FT of about 300 MHz.

[0020] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said MCU is programmed to read a voltage drop across said charge storage capacitor; read a voltage rise on said current measurement element; store predetermined current limits for said system; detect a value and a waveform of current flowing through said system; and to send a signal to said front power transistors to direct said front power transistors to open or close.

[0021] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said MCU is programmed to measure a current waveform and to correlate said current waveform with a system status. In some preferred embodiments of the invention, said system status is selected from the group consisting of normal operation; short circuit; and motor stall.

[0022] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said MCU comprises: flash memory; RAM; non-volatile memory; at least one charge pump driver; UART; SPI; an analog to digital converter; and, a board level interface.

[0023] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said electronic fuse comprises exactly one main switching transistor.

[0024] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said electronic fuse comprises two main switching transistors connected in series source to source.

[0025] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said electronic fuse is characterized by standard fuse dimensions.

[0026] It is a further object of this invention to disclose a PPSE as defined in any of the above, wherein said electronic fuse is configured to fit in a housing selected from the group consisting of a standard fuse holder and a PCB-mountable housing.

[0027] It is a further object of this invention to disclose a Programmable Power Switching System (PPSS) comprising: an energy source (200); a plurality of PPSEs as defined in any of the above connected to said energy source; and, an MCU (204) configured to transmit to and receive from signals from said MCUs of said plurality of PPSEs. In some preferred embodiments of the PPSS, said energy source is a battery.

[0028] It is a further object of this invention to disclose a method for determining a location of a short circuit in a system comprising a voltage source and at least one branch current load, comprising: obtaining a PPSE as defined in any of the above; inserting said electronic fuse into said system between said voltage source and said at least one branch current load; determining an initial voltage v_b across said charge storage capacitor; determining an electrical resistance of said system R_{34} as a function of distance from said electronic fuse; determining a capacitance C of said system; using said electronic fuse to open said circuit upon occurrence of said short circuit; determining a voltage across said charge storage capacitor at at least one point in time t following said step of using said electronic fuse to open said circuit; determining a resistance R according to $V_t = V_0 e^{-t/RC}$, where V_t is the voltage across said charge storage capacitor at time t; and, determining said location by calculating $R/R^\wedge$.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The invention will now be described with reference to the drawings, wherein:

[0030] FIG. 1 presents a schematic circuit diagram of one embodiment of the PPSE of the present invention;

[0031] FIG. 2 presents diagrammatic illustrations of the turn-on and turn-off processes of one embodiment of the invention herein disclosed;

[0032] FIG. 3 presents a schematic circuit diagram of a portion of an embodiment of the PPSE of the present invention in which it is configured for short circuit detection in an AC system;

[0033] FIG. 4 presents a schematic circuit diagram of a second embodiment of the PPSE of the invention herein disclosed;

[0034] FIGs. 5A and 5B present schematic diagrams of a complete electric switching system that incorporates the invention herein disclosed;

[0035] FIGs. 6A and 6B present side and rear views (not to scale) of one embodiment of a housing for the PPSE of the invention herein disclosed;

[0036] FIGs. 7A and 7B illustrate the voltage as a function of time at the power source and output, respectively, as an unstable power source connected to the PPSE of the invention herein disclosed ramps up to its final voltage;

[0037] FIG. **8A** presents a circuit diagram of a model that was used in simulations of the behavior of the PPSE of the invention herein disclosed; and,

[0038] FIGs. **8B - 8D** present graphs of load current, capacitor voltage, and voltage waveform as a function of time for various short circuit conditions as simulated using the circuit shown in FIG. **8A.**

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0039] In the following description, various aspects of the invention will be described. For the purposes of explanation, specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent to one skilled in the art that there are other embodiments of the invention that differ in details without affecting the essential nature thereof. Therefore the proper scope of the invention is to be understood as indicated in the accompanying claims, with the proper scope determined only by the broadest interpretation of said claims.

[0040] As used herein, with regard to numerical quantities, the term "about" refers to a value within ± 25% of the nominal value.

[0041] The electronic fuse (Programmable Power Switching Element or PPSE) disclosed herein enables measurement, management, control, protection, and isolation of branch loads from the energy source along with high surge current limits of the current that passes through the circuit and transistors. A plurality of transistors in series protects and isolates the energy source from any short circuit that may occur as well as from any overcurrent that might occur on one the branch circuits. In some preferred embodiments, the PPSE comprises a pair of transistors in series. In some other preferred embodiments, the PPSE comprises four transistors in series. As described in detail below, the PPSE disclosed herein is fully usable in both DC and AC systems, and enables sensing of current flow in any direction through the circuit, any voltage polarity, and both positive and negative disconnection.

[0042] Reference is now made to FIG. **1,** which presents a schematic circuit diagram of one embodiment of the PPSE disclosed herein. The PPSE is connected to a voltage source **100** that is characterized by an internal resistance R_{source} and which delivers energy to at least one branch circuit **117.** In preferred embodiments, the PPSE comprises four transistors connected in series: front power transistor **103,** first reverse current blocking transistor **102,** main switching transistor **108,** and second reverse current blocking transistor **111.** The PPSE also comprises at least one gate driver; in preferred embodiments, the PPSE comprises a first gate

driver **104** and a second gate driver **106.** In preferred embodiments of the invention, each gate driver is combined with a charge pump. In some preferred embodiments of the invention, the gate drivers are galvanically isolated.

[0043] Front power transistor **103** is connected to the voltage source. The source of front first reverse current blocking power transistor **102** is connected to the source of front power transistor **103,** while the drain of first reverse current blocking power transistor **102** is connected to the drain of main switching transistor **108.** The source of main switching transistor **108** is connected to the source of the second reverse current blocking transistor **111.** The drain of the second reverse blocking transistor is connected to a low-inductance inductor **112** which in typical embodiments has an inductance of 10 - 500 nH.

[0044] The gates of the transistors are connected to the gate drivers. In preferred embodiments, the gates of the front power transistor and the first reverse blocking transistor are connected to first gate driver **104,** while the gates of the main switching transistor and the second reverse blocking transistor are connected to second gate driver **106.** The gate drivers may operate either in an autonomous mode or under control of MCU **118.** Because of the stringent timing requirements of the system, in particular, the timing of on/off signals as described in detail below, a high-speed MCU with a high-speed A/D converter is required for operation of the PPSE disclosed herein. Inductor **112** is connected to the load via a shunt resistor **114,** thereby being charged to the load voltage. The PPSE also comprises a low ESR charge storage capacitor **113** having capacitance $C_{st0^{re}}$ (in typical embodiments of the invention, $C_{st0^{re}}$ is in the range of 1 - 50 μE) that is connected between ground and a junction located between inductor **112** and resistor **114.**

[0045] In preferred embodiments of the invention, the PPSE also includes a high speed memory device **110** that is configured to identify a short circuit condition and to electrically disconnect said transistors **(108, 111)** from the source of electrical current, as described in detail below. In some particularly preferred embodiments of the invention, said high speed memory device is configured to disconnect said transistors within 200 ns of an occurrence of a short circuit condition.

[0046] The transistors used in the PPSE can be any kind of semiconductor switching element such as transistors, FETs, MOSFETs, IGBTs, SIC transistors, SCR/triacs, etc. In preferred embodiments of the invention, transistors **102, 103, 108,** and **111** are MOSFETs.

[0047] When the PPSE connects the voltage source to the load, MCU **118** opens front power transistor **103** and first reverse current blocking transistor **102** to main switching transistor **108** and second reverse current blocking transistor **111.**

[0048] The gate driver / charge pump **104** is turned on at this stage and the front power transistors start to conduct (with no current drain). After a short period of time (typically $1-3\mu8$), the MCU **118** opens main switching transistor **108** and second reverse current blocking transistor **111** and connects the source to PPSE output **116,** transferring power to the load. Since the front power transistor and first reverse current blocking transistor are already open, the switching energy loss appears only on the main switching transistor and the first reverse blocking transistor. The MCU reads the voltage drop across shunt resistor **114** and current flows normally.

[0049] Under normal operating conditions, current flow through the power transistors is measured by the shunt resistor and a bidirectional current measurement element **120** and the MCU **118.** For system level power management, the PPSS can interrogate by serial or other communication means each of the PPSEs. When a moderate current rise short circuit occurs, the PPSE shuts the transistors and informs the PPSS (e.g. by sending an interrupt signal). The system continues to operate in this mode unless a rapid current rise short circuit occurs that requires a rapid response from the PPSE to prevent damage to the voltage source and the transistors.

[0050] When an abrupt or rapid current rise short circuit occurs, the PPSE output is shorted to ground, and the current rises through the shunt resistor **114.** This current is measured by current measurement element **120.** The current rise on the current measurement element is converted to voltage and amplified by a high speed, high common mode bidirectional current to voltage amplifier, the output of which is connected to the high speed A/D converter of the MCU. This process is very effective for slow rise time short circuit conditions, such as, for example, a short at a remote point, but even with a very fast shunt amplifier and A/D converter or comparator, it will be too slow to be of practical use. In the case of a nearby short circuit, however, the low resistance path from the power source to the short location would carry a transient current of thousands of amperes, melting the fuse and burning or melting the transistors, as discussed above. In order to protect the transistors, in the PPSE of the present invention, an inductor and capacitor are added to the high current path. The current is supplied to the load by transistors which feed inductor **112** and charge storage capacitor **113.**

[0051] Due to the rapid current rise, inductor **112** experiences high impedance Z (Z = jωL). For example, for an inductance of 100 nH and a short circuit that occurs over a time of 1 μs, the impedance Z will be 0.628 Ω [= (1)(2 π X 10^6)(100 X 10^{-9})]. An impedance of this magnitude will limit the short circuit current in a 24VDC power source to 24/0.628 = 38.2 A. The rapid rise of the current yields a high impedance element that isolates the transistors from the load, so the transistors therefore do not experience the short circuit current. During this rapid current rise the short circuit current flows from storage capacitor **113** through the shunt resistor **114** to the short.

[0052] The rapid current flow on the shunt resistor **114** is supplied from storage capacitor **113,** creating a voltage on the base emitter of NPN transistor **115** which in turn shuts the gate voltage of front power transistors **103** and **102** and resets the gate driver fast memory **110** (i.e. performs a high speed flip-flop), disconnecting transistors **108** and **111** from the source of current. In preferred embodiments, NPN transistor **115** is high speed (in preferred embodiments, FT > 200 MHz; in more preferred embodiments, FT is about 300 MHz) in order to enable front power transistors **103** and **102** to shut down in less than 100 ns. This process is sufficiently fast that inductor **112** remains in a high impedance state to protect the supply voltage source and transistors **102, 103, 108,** and **111** from the high short circuit current.

[0053] The PPSE obtains the power needed for its operation from the drain of the front power transistor and regulates the internal power supply on board **101.** Low-mass thermistors **105** (typically one or two) measure the temperature of the power transistors to allow a rapid response when the transistor temperature is near or above the maximum allowed temperature.

[0054] Reference is now made to FIG. **2,** which shows schematically the turn-on and turn-off processes (**300** and **350,** respectively) of the PPSE of the present invention. During the turn-on process, transistors **108** and **111** absorb the switching losses in the turn-on process while transistors **103** and **102** absorb the turn-off switching losses. This configuration insures redundancy and enhances the overall reliability of the PPSE.

[0055] The novel design of the PPSE disclosed herein prevents any damage to the transistors and increases the total PPSE reliability sufficiently to make semiconductor systems practical for use as fuses in real-life applications. The PPSE can thus act as a fuse that disconnects the power source from the load completely. This functionality is achieved with the AC / reverse current block (transistors **102** and **111).** If the PPSE is disconnected, the reverse current

transistor block acts to block return current and the PPSE behaves like a normal fuse. In many DC applications, e.g. motor control, the PPSE can conduct a reverse current back to the power source. Embodiments intended for such applications do not comprise transistors **102** and **111** reverse current block; if the PPSE originally supplied was of an embodiment containing these elements, they can be removed or bypassed (e.g. by use of a short wire) for these types of DC applications.

[0056] In order to achieve the maximum cost effectiveness and reliability possible, each of the PPSE branch circuit fuses can operate in autonomous mode by operating under stored parameters inside the MCU **118**. In this mode, the output of current measurement element **120** voltage amplifiers can be fed into analog comparator **109** and compared with a predetermined fixed value set by the local MCU **118** or by a fixed potentiometer, or it can be digitally controlled by using a non-volatile potentiometer and interrupt the PPSE MCU and (PPSS) via signals passed via connector **122**. The previously described process by which high speed front power transistors **102** and **103** are disconnected and reconnected procedure is retained. The same interrupt can generate a PPSS interrupt **121** for complete system control.

[0057] The PPSE unit **117** obtains operating parameters from the PPSS and generates return data for complete system control via a serial bus and flags **122.**

[0058] In preferred embodiments of the invention, the PPSE has a self-learning phase in which the load behavior of each branch is determined under short circuit conditions. In the self-learning phase, the MCU copies the waveforms and the time dependence of the current rise into the MCU memory. Optionally, the operator can deliberately produce conditions such as a motor stall or a short circuit so that the current waveforms in these conditions can be measured and stored as well. After the learning phase is completed, the MCU algorithm is capable of recognizing the expected current patterns and to act according to those patterns when an overcurrent situation occurs.

[0059] In some preferred embodiments of the invention, the local PPSE MCU is programmed to notify the PPSS processor of a short circuit or overcurrent situation.

[0060] In some preferred embodiments of the invention, the MCU is programmed to implement an automatic recovery algorithm. As a non-limiting example of the operation of an automatic recovery algorithm, if the current waveform indicates that a motor has stalled, the MCU increases the current before a short circuit occurs. In many cases, this procedure will cause the system to recover from the stall and return to normal. As another non-limiting

example, if the system is used in an unmanned aerial vehicle (UAV), the MCU can be programmed to tighten the constraints on the definition of a short circuit condition in circumstances when the battery has nearly completely discharged.

[0061] Some preferred embodiments of the invention disclosed herein provide means for determining the location of a short circuit. During the learning phase, the transistors in series are put through connection/disconnection sequence with inductor **112** and charge capacitor **113** in order to determine the capacitor voltage, output voltage, charge, and current. The MCU can then compare the actual voltage and current values at time *t* with the values initially determined during the connection/disconnection sequence according to equations (1) and (2), where V_t and I_t are the charge and current on the charge storage capacitor at time *t,* V_0 is the initial voltage on the charge storage capacitor, *R* is the resistance of the wires in the system, and $\mathbf{C_{st0re}}$ is the capacitance of the charge storage capacitor.

$$V_t = V_0 e^{\sim t/RCstore} \tag{1}$$

$$I_t = \frac{V_0}{R} e^{-t/RC_{store}} \tag{2}$$

[0062] Since *Vo* and $\mathbf{C_{st0re}}$ are known (the parasitic parallel capacitance and resistance can be measured at the time of installation of the electronic fuse or ignored as will in general be small relative to C), equation (1) can be solved for *R* by using the measured values of V_t. Comparing *R* under short-circuit conditions with *R* measured at the time of installation of the electronic fuse or calculated from the known resistance of the wires provides sufficient information to determine the location of the short circuit.

[0063] In some embodiments of the invention, determination of the location of a short circuit is performed by the use of a variable voltage generated at the output by use of a pulse-width modulated (PWM) signal. In these embodiments, due to the *RLC* architecture of the PPSE, the PPSE generates a variable voltage at the output that varies as a function of the PWM duty cycle. As non-limiting examples, if the input voltage is 24 V with a 10% duty cycle (i.e. the transistors conduct 10% of the time), the voltage at output **116** will be 5 V, while if the duty cycle is 90%, the voltage at output **116** will be 18 V. Thus, it is possible to produce a low voltage that will lower the short-circuit current, and to measure the short-circuit current even if the short circuit reduces the overall resistance by only a few milliohms.

[0064] In this configuration, in the event of a short circuit, a known low current produced by a PWM signal of known duty cycle is injected into the circuit. Since the total resistance

between the voltage source and the short circuit is given by the ratio of the output voltage to the short-circuit current and the resistance pre unit length of the wire is known, calculation of the location of the short circuit can readily be performed by measuring the current produced by the PWM signal, and calculating the total resistance from Ohm's Law and the distance to the short circuit from the resistance of the wire per unit length.

[0065] Reference is now made to FIG. **3,** which provides a schematic diagram of a portion of one embodiment of the PPSE in which the PPSE is configured to detect a short circuit in an AC electrical system. In these embodiments, current measurement device **120** is configured to measure AC current, and NPN transistor **115** is a phototransistor that is optically coupled to a light source **302,** thereby constituting a bidirectional input optocoupler. In preferred embodiments, the light source comprises two LEDs connected in parallel in opposite directions, as shown in the figure. When a short circuit occurs, whether on the positive portion or on the negative portion of the current waveform, a voltage drop occurs across the current sense resistor. When the voltage drop is greater than a preset level, the optocoupler starts to conduct, thereby causing the fast memory device to reset and to disconnect the switching transistors **(108, 111)** from the current source.

[0066] Reference is now made to FIG. **4,** which provides a schematic diagram of an additional embodiment of the electronic fuse disclosed herein. The embodiment comprises two transistors rather than four. In the embodiment illustrated in FIG. **4,** the PPSE comprises two main power transistors (switching transistors **141** and **145).** The second transistor **145** acts as the reverse current blocking transistor. In the event of a rapid rise time current surge caused by a short circuit, main switching power transistors **141** and **145** are disconnected by the overcurrent circuit via high-speed NPN transistor **150,** which is located near shunt resistor **149.** When this occurs, the internal memory is reset, and the main switching power transistors **(141, 145)** and gate driver **144** are shut down by a signal passed via programmable delay unit within MCU **146.** Surge current protection in this reduced cost embodiment of the invention is provided by inductor **147** and storage capacitor **148,** which protect the switching transistors **141, 145** from high current. This embodiment does not achieve the redundancy level of the four-transistor embodiment described previously, but nonetheless, the arrangement fully protects the switching transistor from high surge current.

[0067] As with the embodiments shown in FIG. **1,** the embodiment of the PPSE shown in FIG. **4** will perform on-off switching within $100 \, ns$ (in preferred embodiments, within $50 \, ns$). In contrast to those known in the art, however, the load current that supplies the PPSE will

not have to supply surge current in the event of a short circuit due to the inductor L and the storage capacitor. Short circuit current is supplied via the storage capacitor until shutoff of the main switching transistors. During a "normal" rise time short circuit event, the current measurement element **151** will send the value of the current to comparator **155,** which will trigger a programmable delay to shut down the main switching power transistors **141** and **145** to restart the connection after a predetermined period of time. The digital or analog potentiometers **156** and potentiometer POT2 of the programmable delay unit can adjust the circuit to various values of short circuit current level and reconnection delay time. In preferred embodiments of the invention, thermistor **157** is in connection with the trip current voltage to allow changes of the trip current if the transistor temperature varies, significantly increasing the overall reliability of the PPSE.

[0068] The embodiment shown in FIG. **4** can be used in an AC current system in a manner analogous to the embodiment shown in FIG. **1.** Analogously to the embodiment shown in FIG. **1,** current measurement element **151** is configured to measure AC current, and NPN transistor **150** is a phototransistor optically coupled to a light source (e.g. LED) **302** to form an optocoupler.

[0069] Data from the PPSE is made available to the PPSS via a connector **158** that conveys at least the following signals: current analog level; trip point threshold; signals to program the optional digital potentiometers; and signal ground in this standalone PPSE digital potentiometers data can be carried by a RF or contact less communication system **159.**

[0070] Reference is now made to FIG. **5,** which provides a schematic diagram of one embodiment of a complete electric switching system PPSS that incorporates the electronic fuse disclosed herein. In the embodiment shown, energy source **200** is a battery, but any energy source known in the art may be used. The energy source is connected to a plurality of electronic fuses. In the embodiment illustrated (FIG. **5A),** three electronic fuses **201, 202,** and **203** are shown, but any number may be connected to the energy source. The embodiment illustrated comprises a single-level switching matrix. In other embodiments, the fuses can be implemented as a group or in a hierarchical fashion. The signals for control and reading are routed to the MCU FPGA or to a plurality of MCUs **204** (FIG. **5B).**

[0071] Another advantage of the electronic fuse disclosed herein is its small size. In preferred embodiments, the entire electronic fuse is of standard fuse dimensions and hence will fit into any standard fuse holder that has an internal volume of at least 0.75 cm^3.

Reference is now made to FIG. **6,** which shows schematic views of a non-limiting exemplary embodiment of a housing **600** for the PPSE herein disclosed. FIG. **6A** shows a side view of the housing (not to scale). The front of the housing comprises on/off switch **605** and an indicator light **610** that is lit when the PPSE is in use. FIG. **6B** shows a rear view of the housing, showing power in tab **615,** power out tab **620,** ground tab **625,** and an optional communication and network connector **630** (tabs **615** and **620** can also be seen in FIG. **6A).** A non-limiting example of a pin arrangement in the embodiment of the electronic fuse illustrated schematically in FIG. **6** is presented in Table 1.

Table 1

Pin Number	Pin Name	Description
1	Current IN	Current flow input signal, connected to power source side
2	Current OUT	Current flow output signal, connected to load side
3	GND	Ground signal
4	Serial CLK/SCL	10 MHz SPI clock signal
5	Serial IN/SDA	Data in signal. SPI MOSI signal
6	Serial OUT/NC	Data out signal. SPI MISO signal
7	Fuse/POT select	Fuse or POT select active low signal
8	Status	LED driving signal duty cycle proportional to load current
9	DP	Short circuit carry signal, enables double protection scheme

[0072] In preferred embodiments of the invention, the PPSE is characterized by dimensions that are standard for use in electrical panels; the exact dimensions of a particular PPSE are in general adapted to a specific application and will depend on the current carried by the application for which the PPSE is to be used. The PPSE of the present invention can thus be adapted to fit in any standard fuse holder for use in any circuit that can be protected by any type of fuse or circuit breaker currently known in the art.

[0073] In a similar fashion to the above discussion of the use of PWM input signals in the determination of the location of a short circuit, in some embodiments of the invention, a PWM input signal is used in the case of unstable power on/off situations. In these embodiments, a voltage is produced at the output from a PWM input signal; as described above, the output voltage will vary depending on the PWM duty cycle, as will its rise time. In these embodiments, the fuse will produce the correct voltage ramp-up at the output even if the input ramp-up is unstable. Reference is now made to FIG. **7,** which shows graphs of the

voltage at the power source (FIG. **7A)** and the output (FIG. **7B)** as a function of time following the activation of an unstable power source. As shown in the graphs, even if the power source does not provide a smooth ramp-up during the -10 ms it takes to reach its final voltage, the output will experience a smooth rise to its final voltage.

[0074] Reference is now made to FIG. **7,** which presents results of simulations of the operation of the PPSE disclosed herein. The simulations were performed using the commercially available SPICE (Simulation Program with Integrated Circuit Emphasis) program. The simulations were performed on the simplified circuit shown in FIG. **7A.**

[0075] FIGs. **7B** and 7C present graphs showing the calculated values of relevant voltages and currents as a function of time following a short circuit in the circuit shown in FIG. **7A.** The results shown graphically in FIG. **7B** demonstrate that the input and therefore the MOSFET current remain below 100 A, well below the maximum current that a small power MOSFET can experience without damage, even when a small (10 nH) inductor is used. FIG. **7C** presents the results of analogous calculations for a circuit identical to that in FIG. **7A** except that the circuit does not contain an inductor. As shown in the graphs, in this case, the input and therefore the MOSFET are above 4750 Amperes which is far above the upper limit of usability even for a high power MOSFET. These results clearly demonstrate the utility of the PPSE disclosed herein.

[0076] FIG. **7D** shows another example of the short circuit behavior of the PPSE herein disclosed, in this case, a 4 ms short circuit in the negative input signal of a 400 Hz, 115 V AC power system. As can be seen in the figure, the short circuit generates a current to the load of ~5 kA, but the input current remains constant at -13 A.

[0077] Additional advantages and benefits of the invention disclosed herein over the prior art will be clear to a person of ordinary skill in the art.

CLAIMS

What is claimed is:

1. A programmable power switching element (PPSE), wherein said PPSE comprises:

a first terminal (110);

a front power transistor (103) comprising a drain connected in series to said first terminal, a source, and a gate;

a first gate driver (104) connected to said gate of said front power transistor;

a main switching transistor (108) connected in series with said front power transistor, said main switching transistor comprising a drain, said drain connected to said source of said front power transistor;

a first reverse current blocking transistor (102), comprising a drain, a source, and a gate, said first reverse current blocking transistor connected in series with and located between said front power transistor and said main switching transistor, the gate of said first reverse current blocking transistor connected to said first gate driver;

a second gate driver (106) connected to said gate of said main switching transistor;

a shunt resistor (114) connected in series with said main switching transistor;

a second terminal (116) in series with said shunt resistor;

a charge storage capacitor (113) connected between ground and a junction located between said inductor and said shunt resistor;

a second reverse current blocking transistor (111), comprising a drain, a source, and a gate, said second reverse current blocking transistor connected in series with and located between said main switching transistor and said shunt resistor, the gate of said first reverse current blocking transistor connected to a gate driver;

an inductor (112) connected in series with said second reverse current blocking transistor and located between said second reverse current blocking transistor and said shunt resistor;

an NPN transistor (115) comprising a collector and an emitter, said collector connected to said gate of said front power transistor and said emitter connected to said second terminal via said shunt resistor and said inductor;

a current measurement element (120) comprising a bidirectional shunt voltage amplifier, said current measurement element connected in parallel with said shunt resistor; and,

a high-speed MCU **(118),** comprising a high-speed A/D converter connected to said transistors and charge storage capacitor and to said voltage amplifier.

2. The PPSE according to claim **1,** wherein said PPSE first terminal is connectable to a voltage source and said second terminal is connectable to a load.

3. The PPSE according to claim **1,** comprising a gate driver high speed memory device **(110)** configured to be reset when a voltage is created on said emitter of said NPN transistor **(115)** upon current flow through said shunt resistor **(114)** due to discharge of said storage capacitor **(113),** thereby disconnecting said transistors **(108, 111)** from a source of current.

4. The PPSE according to claim **3,** wherein said high speed memory device is configured to disconnect said transistors within 200 ns of an occurrence of a short circuit condition.

5. The PPSE according to claim **1,** wherein:

   said PPSE comprises a light source **(302);**

   said NPN transistor **(115)** is a phototransistor optically coupled to said light source; and,

   said current measurement element **(120)** is configured to measure AC current.

6. The PPSE according to claim **5,** wherein said light source comprises 2 LEDs connected in parallel in opposite directions.

7. The PPSE according to claim **1,** wherein at least one of said transistors **(102, 103, 108, 111)** is a MOSFET.

8. The PPSE according to claim **1,** wherein said gate of said first reverse current blocking transistor is connected to said first gate driver **(104).**

9. The PPSE according to claim **1,** wherein said gate of said second reverse current blocking transistor is connected to said second gate driver **(106).**

10. The PPSE according to claim **1,** wherein said inductor has an inductance of between 10 and 500 nH.

11. The PPSE according to claim **1,** wherein said charge capacitor has a capacitance of between 1 and 50 μE.

12. The PPSE according to claim **1,** wherein said NPN transistor **(115)** is characterized by an FT of at least 200 MHz.

13. The PPSE according to claim **1,** wherein said NPN transistor **(115)** is characterized by an FT of about 300 MHz.

14. The PPSE according to claim **1,** wherein said MCU is programmed to read a voltage drop across said charge storage capacitor; read a voltage rise on said current measurement element; store predetermined current limits for said system; detect a value and a waveform of current flowing through said system; and to send a signal to said front power transistor to direct said front power transistor to open or close.

15. The PPSE according to claim **1,** wherein said MCU is programmed to measure a current waveform and to correlate said current waveform with a system status.

16. The PPSE according to claim **15,** wherein said system status is selected from the group consisting of normal operation; short circuit; and motor stall.

17. The PPSE according to claim **1,** wherein said MCU comprises:

  flash memory;

  RAM;

  non-volatile memory;

  at least one charge pump driver;

  UART;

  SPI;

  an analog to digital converter; and,

  a board level interface.

18. The PPSE to claim **1,** wherein said electronic fuse comprises exactly one main switching transistor.

19. The PPSE according to claim **1,** wherein said electronic fuse comprises two main switching transistors connected in series source to source.

20. A PPSE comprising a circuit as shown in FIG. **1.**

21. A programmable power switching element (PPSE), wherein said PPSE comprises:

  a first terminal **(110);**

  a first main switching transistor **(141)** comprising a drain connected in series to said first terminal, a source, and a gate;

  a gate driver **(144)** connected to said gate of first main switching transistor;

a second main switching transistor (145) connected in series with said first main switching transistor, said main switching transistor comprising a drain, said drain connected to said source of said first main switching transistor;

an inductor (147) connected in series with said second main switching transistor;

a shunt resistor (149) connected in series with said inductor;

a charge storage capacitor (148) connected between ground and a junction located between said inductor and said shunt resistor;

a second terminal (116) connected in series to said shunt resistor;

an NPN transistor (150) comprising a collector and an emitter, said collector connected to said gate of said front power transistor, and said emitter connected to said second terminal via said shunt resistor and said inductor;

a current measurement element (151) comprising a voltage amplifier connected in parallel to said shunt resistor; and,

a high-speed MCU (146), comprising:

    a programmable delay unit; and,

    a high-speed A/D converter connected to said transistors, said charge storage capacitor, and to said voltage amplifier.

22. The PPSE according to claim 21, comprising a gate driver high speed memory device (110) configured to be reset when a voltage is created on said emitter of said NPN transistor (115) upon current flow through said shunt resistor (114) due to discharge of said storage capacitor (113), thereby disconnecting said transistors (108, 111) from a source of current.

23. The PPSE according to claim 22, wherein said high speed memory device is configured to disconnect said transistors within 200 ns of an occurrence of a short circuit condition.

24. The PPSE according to claim 21, wherein:

    said PPSE comprises a light source (302);

    said NPN transistor (150) is a phototransistor optically coupled to said light source; and,

    said current measurement element (151) is configured to measure AC current.

25. The PPSE according to claim 21, wherein at least one of said switching transistors (141, 145) is a MOSFET.

26. The PPSE according to claim 21, wherein said inductor has an inductance of between 10 and 500 nH.

27. The PPSE according to claim **21,** wherein said charge capacitor has a capacitance of between 1 and 50 μE.

28. The PPSE according to claim **21,** wherein said NPN transistor **(115)** is characterized by an FT of at least 200 MHz.

29. The PPSE according to claim **21,** wherein said NPN transistor **(115)** is characterized by an FT of about 300 MHz.

30. The PPSE according to claim **21,** wherein said MCU is programmed to read a voltage drop across said charge storage capacitor; read a voltage rise on said current measurement element; store predetermined current limits for said system; detect a value and a waveform of current flowing through said system; and to send a signal to said front power transistor to direct said front power transistor to open or close.

31. The PPSE according to claim **21,** wherein said MCU is programmed to measure a current waveform and to correlate said current waveform with a system status.

32. The PPSE according to claim **31,** wherein said system status is selected from the group consisting of normal operation; short circuit; and motor stall.

33. The PPSE according to claim **21,** wherein said MCU comprises:

    flash memory;

    RAM;

    non-volatile memory;

    at least one charge pump driver;

    UART;

    SPI;

    an analog to digital converter; and,

    a board level interface.

34. A PPSE comprising a circuit as shown in FIG. **4.**

35. The PPSE according to any one of claims **1 - 34,** wherein said electronic fuse is characterized by standard fuse dimensions.

36. The PPSE according to any one of claims **1 - 34,** wherein said electronic fuse is configured to fit in a housing selected from the group consisting of a standard fuse holder and a PCB-mountable housing.

37. A Programmable Power Switching System (PPSS) comprising:

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an energy source (200);

a plurality of PPSEs according to any one of claims 1 - 34 connected to said energy
source; and,

an MCU (204) configured to transmit to and receive from signals from said MCUs of
said plurality of PPSEs.

38. The PPSS according to claim 37, wherein said energy source is a battery.

39. A Programmable Power Switching System (PPSS) comprising:

an energy source (200);

a plurality of PPSEs according to claim 35 connected to said energy source; and,

an MCU (204) configured to transmit to and receive from signals from said MCUs of
said plurality of PPSEs.

40. The PPSS according to claim 39, wherein said energy source is a battery.

41. A Programmable Power Switching System (PPSS) comprising:

an energy source (200);

a plurality of PPSEs according to claim 36 connected to said energy source; and,

an MCU (204) configured to transmit to and receive from signals from said MCUs of
said plurality of PPSEs.

42. The PPSS according to claim 41, wherein said energy source is a battery.

43. A method for determining a location of a short circuit in a system comprising a voltage
source and at least one branch current load, said method comprising:

obtaining a PPSE according to any one of claims 1 - 34;

inserting said electronic fuse into said system between said voltage source and said at
least one branch current load;

determining an initial voltage V_0 across said charge storage capacitor;

determining an electrical resistance of said system $R\!\!\!/_4$ as a function of distance from
said electronic fuse;

determining a capacitance C of said system;

using said electronic fuse to open said circuit upon occurrence of said short circuit;

determining a voltage across said charge storage capacitor at at least one point in time t
following said step of using said electronic fuse to open said circuit;

determining a resistance R according to $V_t = V_0 e^{-t/RC}$, where V_t is the voltage across
said charge storage capacitor at time t; and,

determining said location by calculating $R/R^\wedge$.

44. A method for determining a location of a short circuit in a system comprising a voltage source and at least one branch current load, said method comprising:

obtaining a PPSE according to claim 35;

inserting said electronic fuse into said system between said voltage source and said at least one branch current load;

determining an initial voltage V_b across said charge storage capacitor;

determining an electrical resistance of said system R_d as a function of distance from said electronic fuse;

determining a capacitance C of said system;

using said electronic fuse to open said circuit upon occurrence of said short circuit;

determining a voltage across said charge storage capacitor at at least one point in time t following said step of using said electronic fuse to open said circuit;

determining a resistance R according to $V_t = V_0 e^{\sim t/RC}$, where V_t is the voltage across said charge storage capacitor at time t; and,

determining said location by calculating $R/R^\wedge$.

45. A method for determining a location of a short circuit in a system comprising a voltage source and at least one branch current load, said method comprising:

obtaining a PPSE according to claim 36;

inserting said electronic fuse into said system between said voltage source and said at least one branch current load;

determining an initial voltage V_b across said charge storage capacitor;

determining an electrical resistance of said system $R_{¾}$ as a function of distance from said electronic fuse;

determining a capacitance C of said system;

using said electronic fuse to open said circuit upon occurrence of said short circuit;

determining a voltage across said charge storage capacitor at at least one point in time t following said step of using said electronic fuse to open said circuit;

determining a resistance R according to $V_t = V_0 e^{-t/RC}$, where V_t is the voltage across said charge storage capacitor at time t; and,

determining said location by calculating R/R_d.

46. A method for determining a location of a short circuit in a system comprising a voltage source and at least one branch current load, said method comprising:
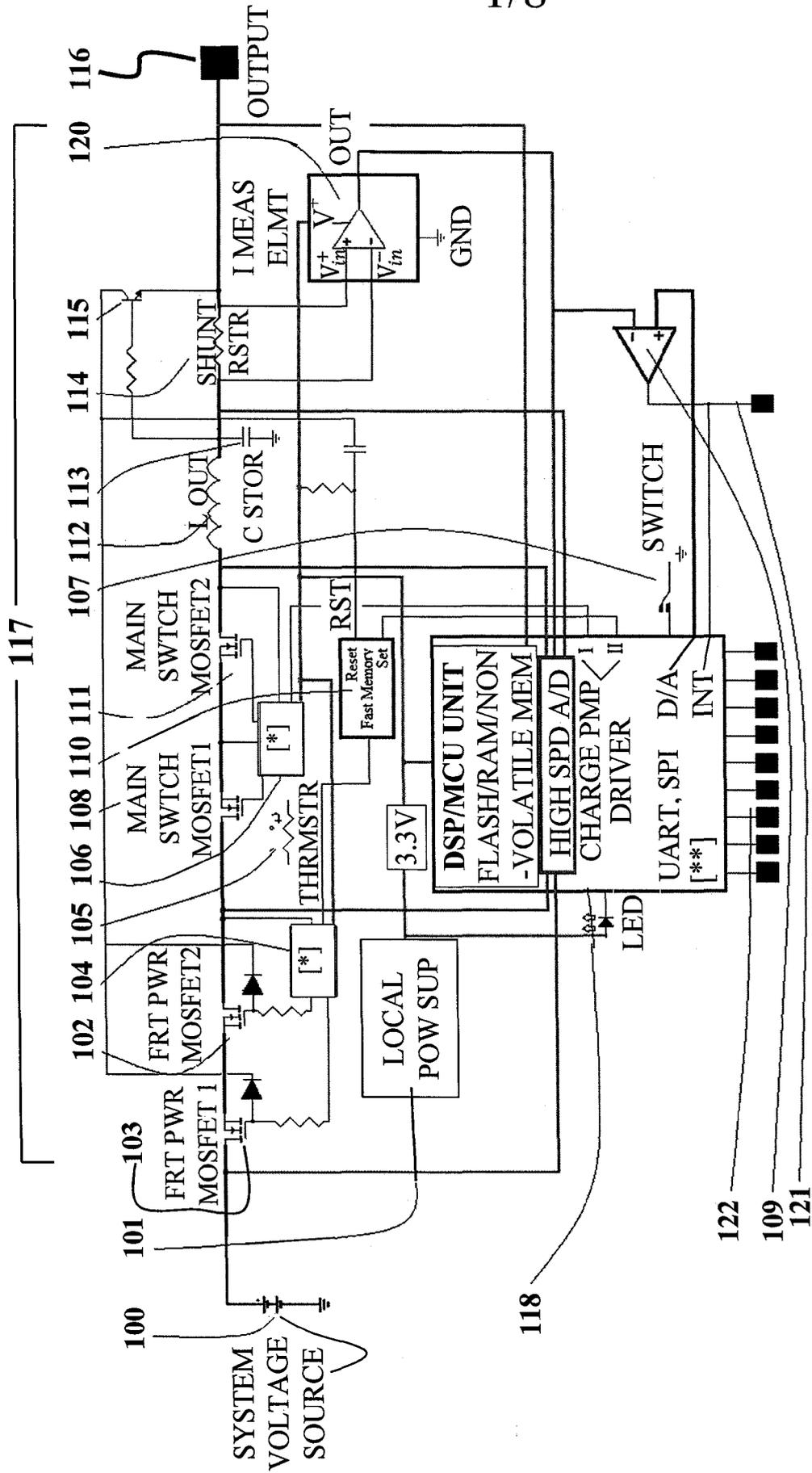
obtaining a PPSE according to any one of claims **1 - 34;**

inserting said electronic fuse into said system between said voltage source and said at least one branch current load;

determining an electrical resistance of said system **Rd** as a function of distance from said electronic fuse;

providing a pulse-width modulated (PWM) input signal, said PWM input signal characterized by a predetermined duty cycle, thereby producing an output voltage;

measuring a short-circuit current;

determining a total resistance **R** from said short-circuit current and said output voltage; and,

determining said location by calculating **R/Rd.**

47. A method for determining a location of a short circuit in a system comprising a voltage source and at least one branch current load, said method comprising:

obtaining a PPSE according to claim **35;**

inserting said electronic fuse into said system between said voltage source and said at least one branch current load;

determining an electrical resistance of said system **Rd** as a function of distance from said electronic fuse;

providing a pulse-width modulated (PWM) input signal, said PWM input signal characterized by a predetermined duty cycle, thereby producing an output voltage;

measuring a short-circuit current;

determining a total resistance **R** from said short-circuit current and said output voltage; and,

determining said location by calculating **R/Rd.**

48. A method for determining a location of a short circuit in a system comprising a voltage source and at least one branch current load, said method comprising:

obtaining a PPSE according to claim **36;**

inserting said electronic fuse into said system between said voltage source and said at least one branch current load;

determining an electrical resistance of said system **Rd** as a function of distance from said electronic fuse;

providing a pulse-width modulated (PWM) input signal, said PWM input signal characterized by a predetermined duty cycle, thereby producing an output voltage;

measuring a short-circuit current;

determining a total resistance R from said short-circuit current and said output voltage; and,
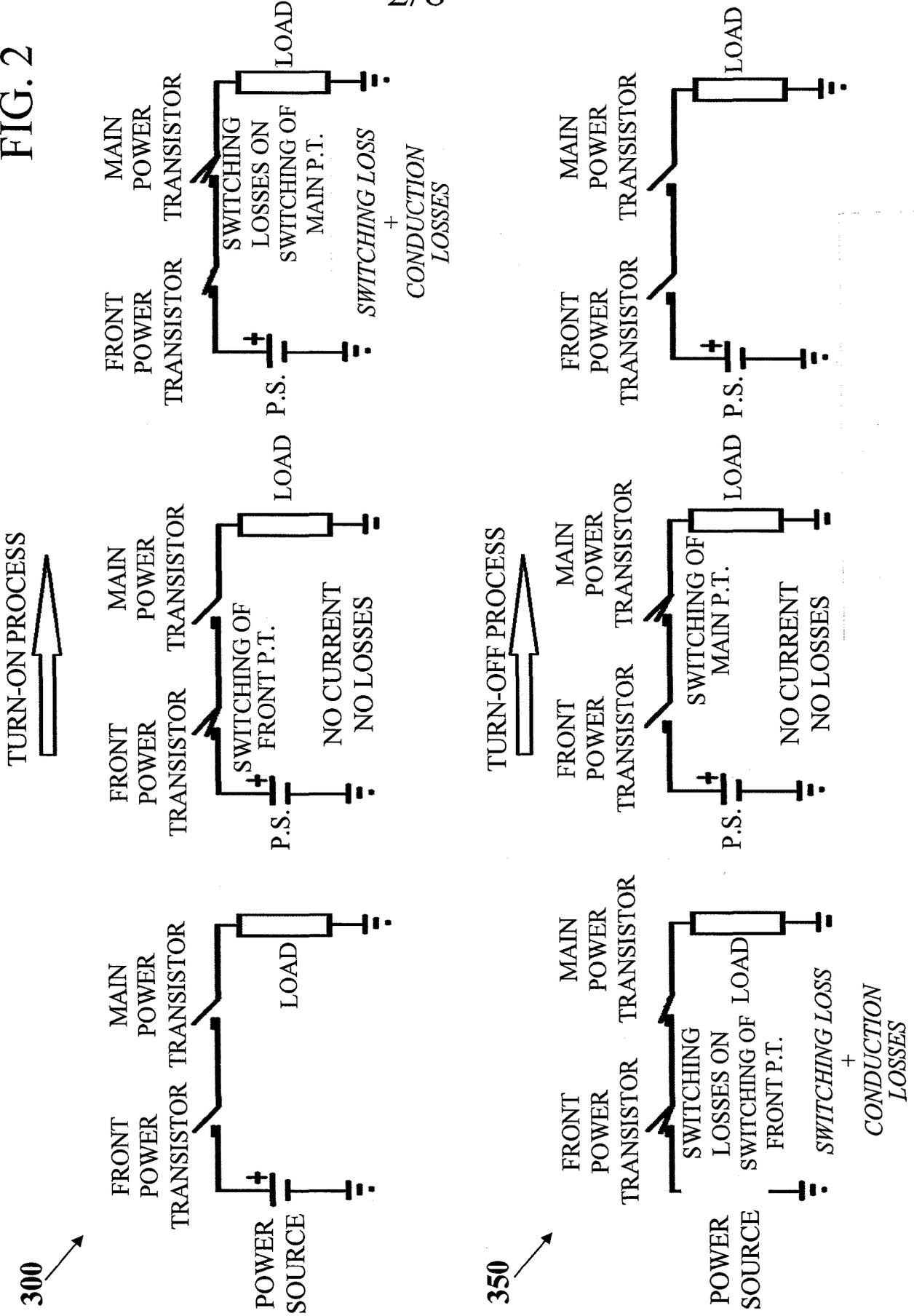
determining said location by calculating R/R_d.

49. A method for identifying and isolating an unstable power on-off situation in a system comprising a voltage source and at least one branch current load, said method comprising:

obtaining a PPSE according to any one of claims **1 - 34;**

inserting said electronic fuse into said system between said voltage source and said at least one branch current load; and,

providing a pulse-width modulated (PWM) input signal, said PWM input signal characterized by a predetermined duty cycle, thereby producing a voltage ramp-up characterized by a known rise time.

50. A method for identifying and isolating an unstable power on-off situation in a system comprising a voltage source and at least one branch current load, said method comprising:

obtaining a PPSE according to claim **35;**

inserting said electronic fuse into said system between said voltage source and said at least one branch current load; and,

providing a pulse-width modulated (PWM) input signal, said PWM input signal characterized by a predetermined duty cycle, thereby producing a voltage ramp-up characterized by a known rise time.

51. A method for identifying and isolating an unstable power on-off situation in a system comprising a voltage source and at least one branch current load, said method comprising:

obtaining a PPSE according to claim **36;**

inserting said electronic fuse into said system between said voltage source and said at least one branch current load; and,

providing a pulse-width modulated (PWM) input signal, said PWM input signal characterized by a predetermined duty cycle, thereby producing a voltage ramp-up characterized by a known rise time.

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FIG. 1

[*] GATE DRIVER CHARGE PUMP
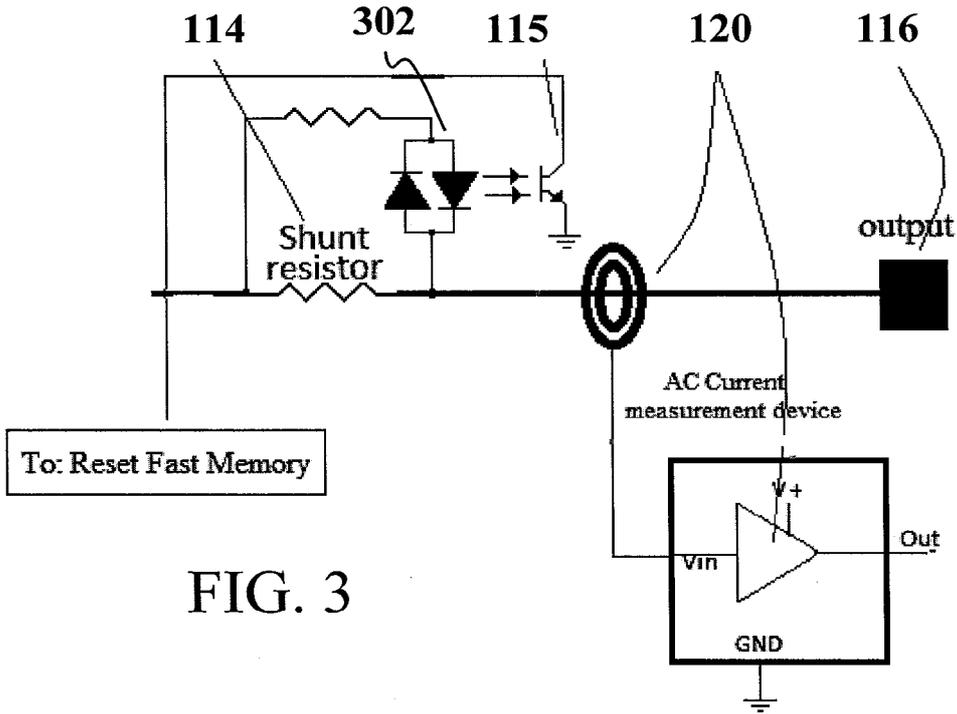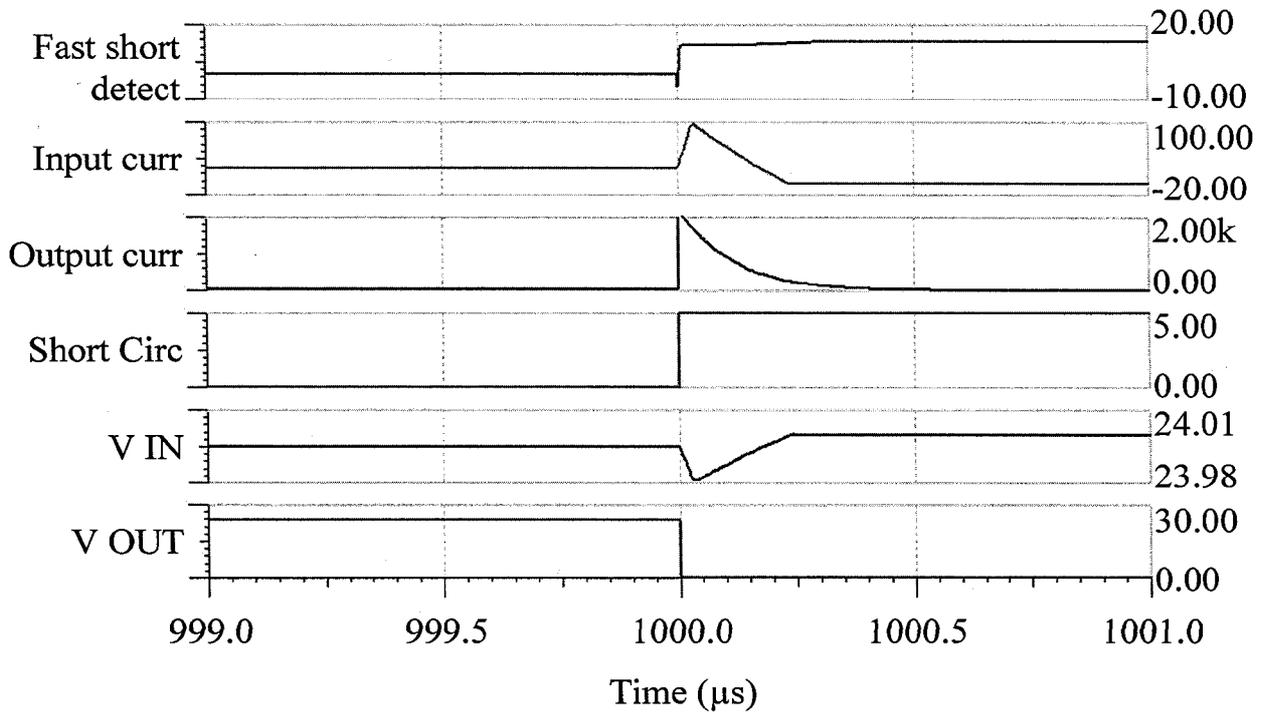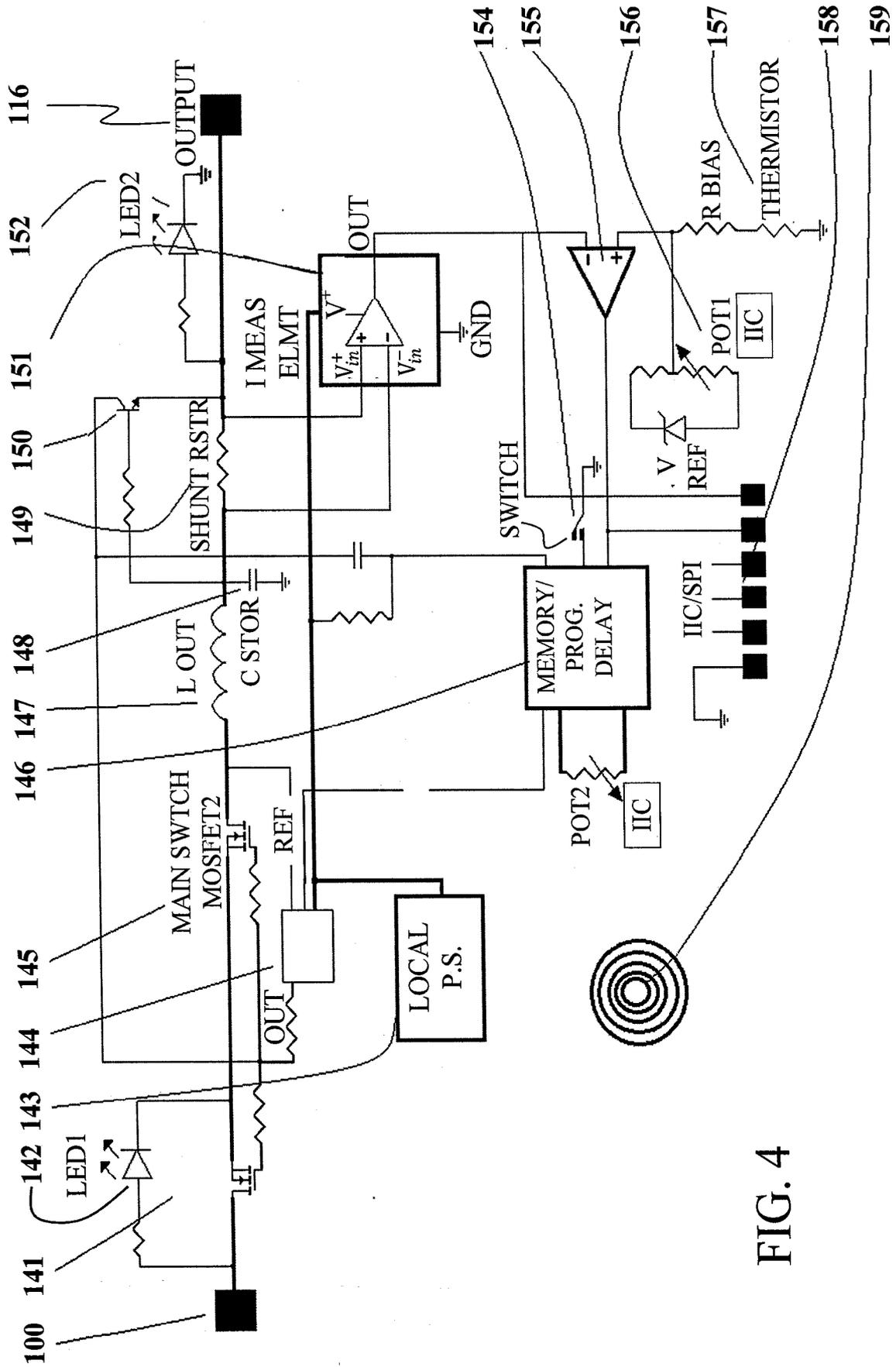[**] BOARD LEVEL INTERFACE

FIG. 2

FIG. 3

114 **302** **115** **120** **116**

Shunt resistor

AC Current measurement device

To: Reset Fast Memory

V +

Vin

Out

GND

output

Fast short detect ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯ 20.00 / -10.00

Input curr ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯ 100.00 / -20.00

Output curr ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯ 2.00k / 0.00

Short Circ ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯ 5.00 / 0.00

V IN ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯ 24.01 / 23.98

V OUT ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯ 30.00 / 0.00

999.0   999.5   1000.0   1000.5   1001.0

Time (μs)

FIG. 8B

FIG. 4

201

SYSTEM LEVEL CONNECTOR

202

V
SOURCE ⏚200

204

WiFi

CURR
LIM
POT.
SERIAL
BUS

SYSTEM LEVEL CONNECTOR

203

FIG. 5A

SYSTEM LEVEL CONNECTOR

204

| DSP Core I |
| DSP Core II |

| Flash Memory |
| Eeprom memory |

| High speed RAM |
| memory |

| CAN BUS |
| UART RS232 & 485-422 |
| Ethernat |

| Accurate |
| timing |

100 nSec
12 bits A/D
n Channels

Capacitor Voltage measurement
Current wave form measurement

FIG. 5B

10uSec
12 bits A/D
n channels

Thermistors Measurement
Voltage input measurement

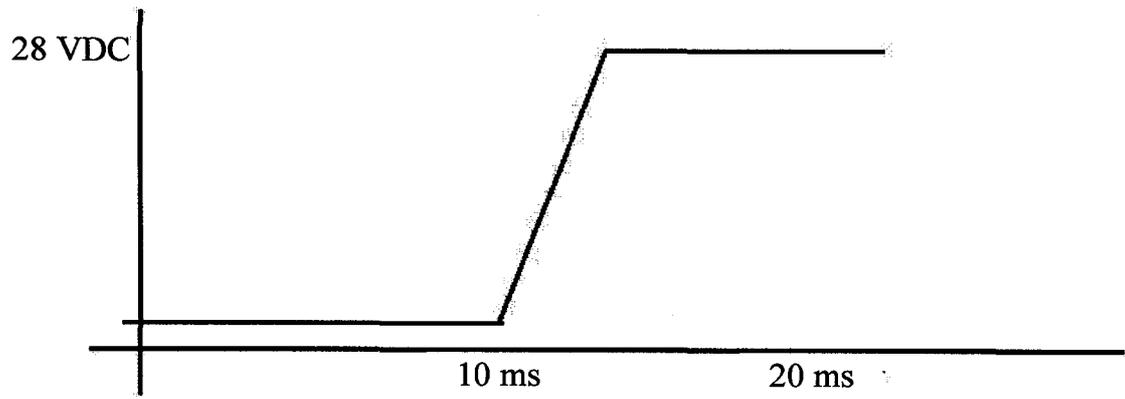Serial BUS IIC
or SPI or alike
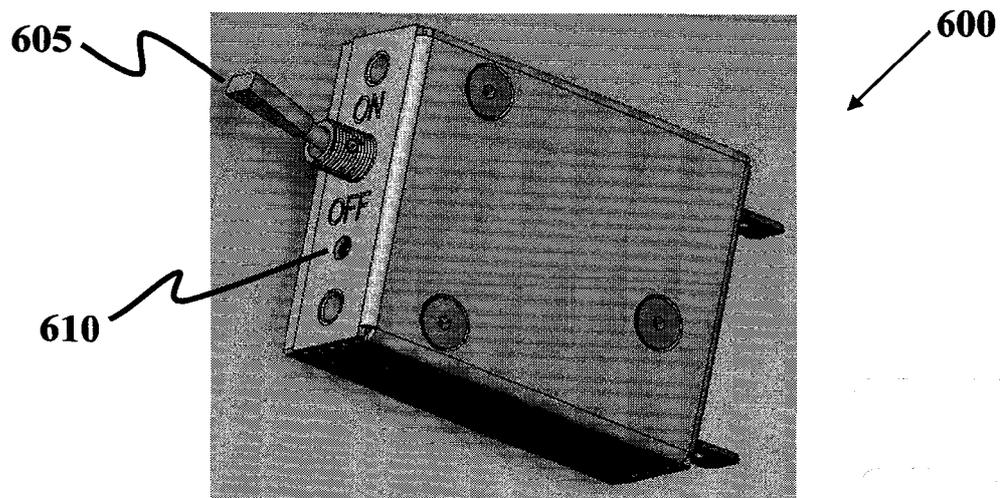Flags and
digial IO

Current limt pot. serial BUS

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FIG. 7A

FIG. 7B

FIG. 6A

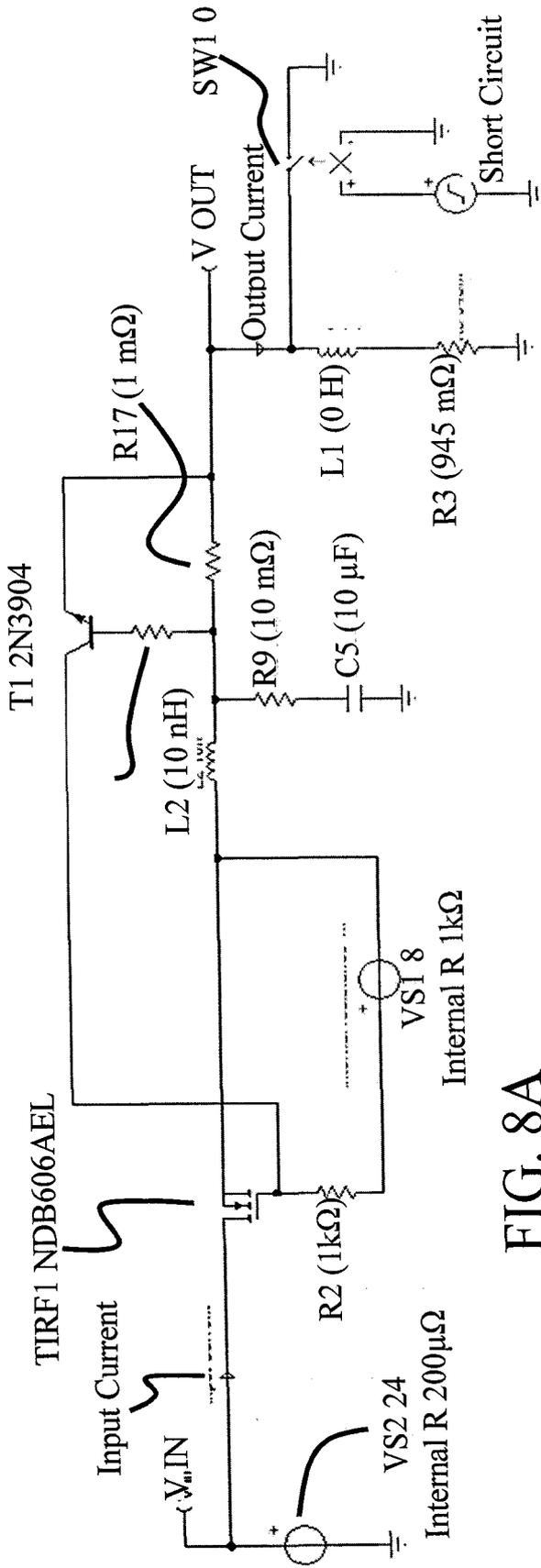FIG. 8A
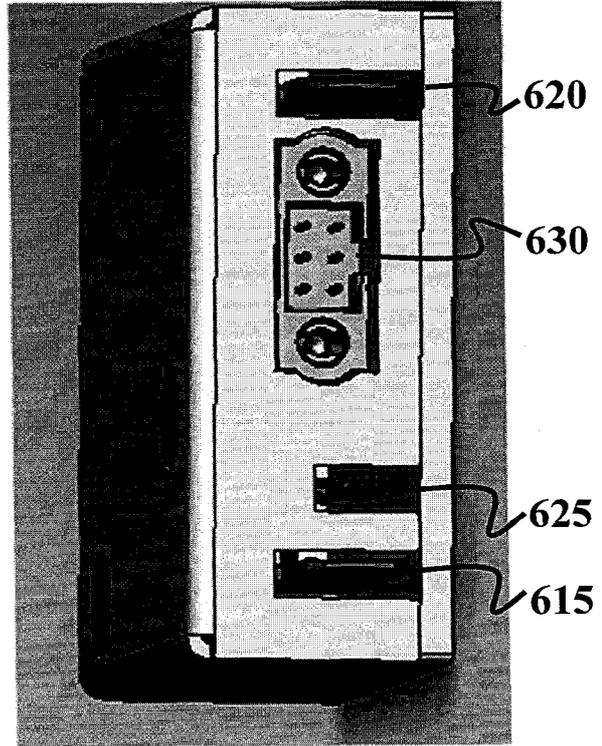
FIG. 6B
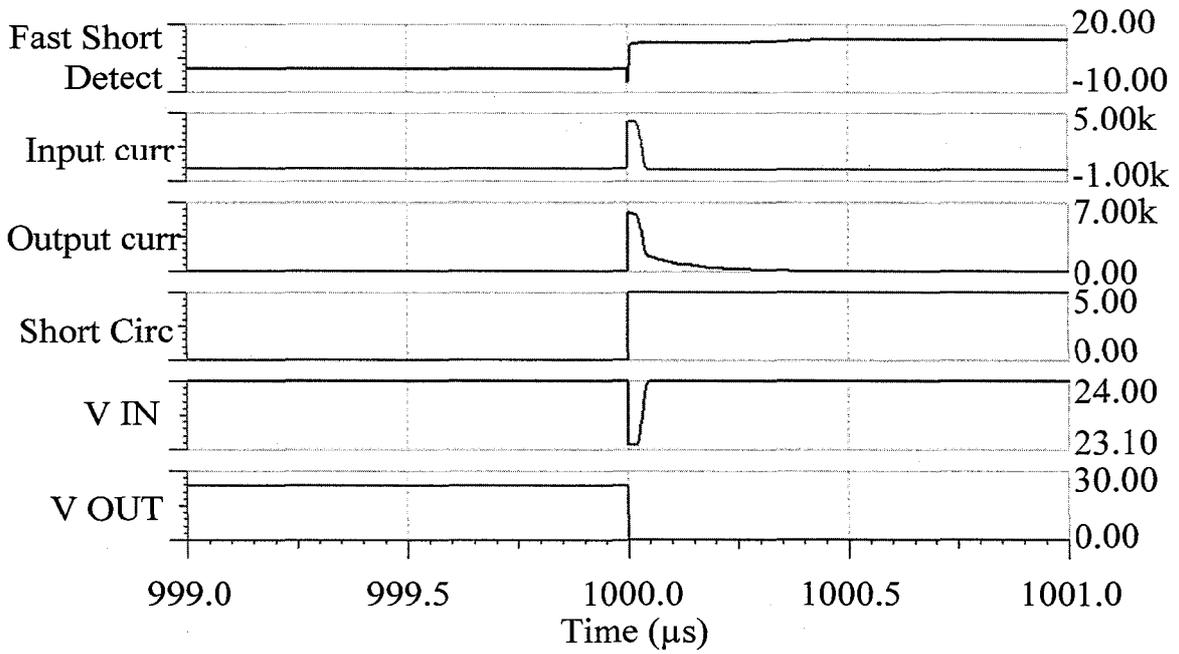
FIG. 8C
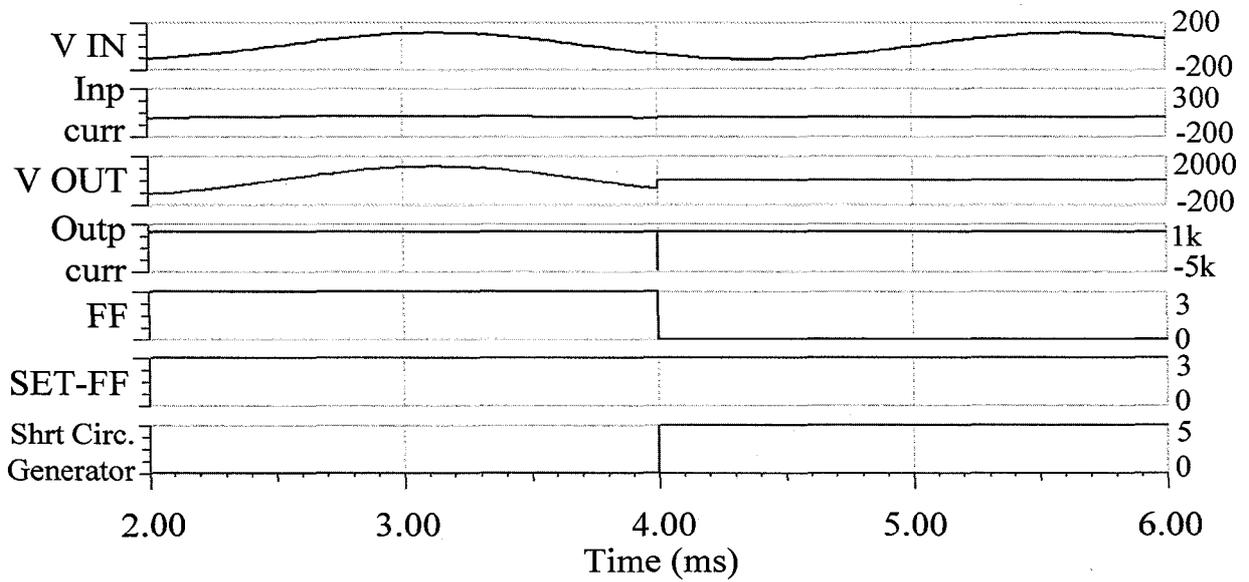
FIG. 8D

INTERNATIONAL SEARCH REPORT

A.	CLASSIFICATION OF SUBJECT MATTER

IPC (2016.01) H02H 9/02

According to International Patent Classification (IPC) or to both national classification and IPC

B.	FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC (2016.01) H02H 9/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, **where** practicable, search terms used)
Databases consulted: THOMSON INNOVATION, Esp@cenet, Google Patents, Google Scholar, FamPat database
Search terms used: Electronic fuse, E-fuse, PPSE, inrush/surge current

C.	DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013049686 A1 ERHART MICHAEL [AT]; MAGNA E CAR SYSTEMS GMBH & CO [AT] 28 Feb 2013 (2013/02/28) Fig 1	1-5 1
A	CN 101692574 A YICHANG ZHUONENG TECHNOLOGY CO 07 Apr 2010 (2010/04/07) Fig 1	1-5 1
A	US 20122573 11 A1 BURNS LAWRENCE M [US]; FISHER DAVID [US]; R2 SEMICONDUCTOR INC [US] 11 Oct 2012 (2012/10/1 1) Fig 10	1-5 1
A	WO 9725761 A1 LVAD TECHNOLOGY INC [US]; KROLL MARK W [US] 17 Jul 1997 (1997/07/17) Fig 1	1-5 1

☐ Further documents are listed in the continuation of Box C.	☒ See patent family annex.

* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "0" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family

Date of the actual completion of the international search 03 Jul 2016	Date of mailing of the international search report 17 Jul 2016

Name and mailing address of the ISA: Israel Patent Office Technology Park, Bldg.5, Malcha, Jerusalem, 9695101, Israel Facsimile No. 972-2-5651616	Authorized officer COHAY Mattan Telephone No. 972-2-565161 1

Form PCT/ISA/210 (second sheet) (January 2015)

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		EP 2562896	A3	06 Nov 2013
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		EP 2517342	A2	31 Oct 2012
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		US 8233250	B2	31 Jul 2012
		WO 2011079155	A2	30 Jun 2011
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