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[Continued on next page]

(54) **Title:** AN ION SENSITIVE FIELD EFFECT TRANSISTOR

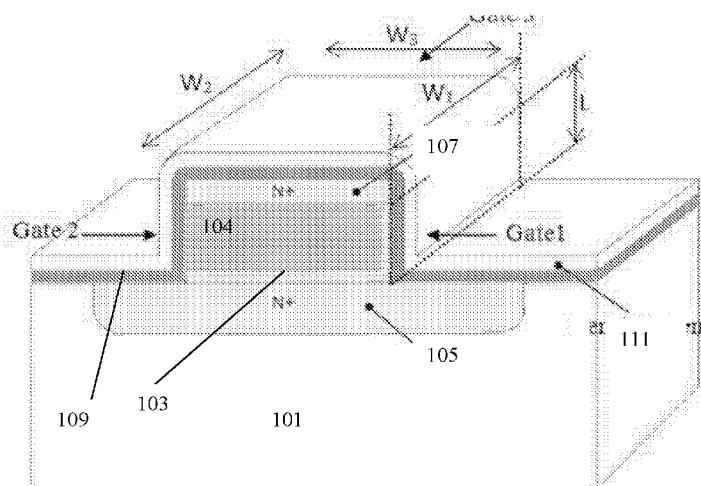


Figure 1

(57) **Abstract:** The present invention relates to an ion sensitive field effect transistor comprising: a semiconductor substrate (101); a channel region (103) having adopted polysilicon layer (104) of at least 5e16 per cubic centimeter for conducting the current, formed over the semiconductor substrate (101); a drain region (105); a source region (107), wherein the source region (107) and the drain region (105) vertically connected to the channel region (103); a gate insulating layer (109); and a sensing membrane layer (111); characterized in that the gate insulating layer (109) and the sensing membrane layer (111) are formed along substantially all of the side walls of the channel region (103) to create a vertical multi-gate electrodes.

**Declarations under Rule 4.17:**

- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

- as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))

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Description

Title of Invention: AN ION SENSITIVE FIELD EFFECT TRANSISTOR

[1] **FIELD OF INVENTION**

[2] The present invention relates to an ion sensitive field effect transistor (ISFET).

[3] **BACKGROUND OF THE INVENTION**

[4] Silicon-based chemical sensors are quite popular technology nowadays because of their advantages which are simplicity in function, fast response, small size, rigid design, and projected low cost. Additionally, the silicon technology is a good platform for system integration of chemical sensors because of the process compatibility with integrated circuit (IC) technology. Ion sensitive field effect transistor (ISFET) pH sensor is a silicon based device. A conventional ISFET structure is similar to Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) but without gate electrode deposited on gate insulator exposing the insulator layer (sensing membrane) to an electrolyte solution. The basic idea of an ISFET is to remove the metal plate of an MOSFET and expose the oxide insulator to an electrolyte. This insulator will then interact with the solution and creates an electrolyte-insulator interfacial potential which is directly modulate the channel conductivity between the source and the drain terminal. Basically the amount of current flowing through the channel between the source and the drain is a measure of the amount of inversion charge in the channel which, by charge neutrality of the entire device, the inversion charge must be equal to the amount of charges on the upper side of the insulator layer. It can be seen as a charge sensor device. To ensure high signal-to-noise ratio (SNR), sufficient sensing area must be exposed to the electrolyte. Currently the planar membrane has limited exposed area to the ions in the sample to be tested hence limiting the sensitivity and efficiency of the device. Miniaturization of ISFET for integrated micro and nano-sensor system will further reduce the gate size and minimize the sensing area which will degrade the sensor signal.

[5] One of the examples is EP 1706734 which relates to an ion sensitive field effect transistor pH sensor is provided with an improved sensor gate configuration. Specifically, a tantalum oxide-sensing gate is disposed on top of an alumina layer. The tantalum oxide-sensing gate provides advantageous sensitivity, while the alumina barrier layer increases sensor longevity in situations where the sensor is exposed to caustic cleaning processes such as Clean In Place processes.

[6] Miniaturization of ISFET for integrated micro and nano-sensor system would further reduce the gate size and minimize the sensing area which would also degrade the

sensor signal.

[7] Therefore there is a need for an invention which provides solution to the problem.

[8] **SUMMARY OF THE INVENTION**

[9] According to an aspect of the present invention, the present invention provides an ion sensitive field effect transistor comprising: a semiconductor substrate (101); a channel region (103) having doped polysilicon layer of at least 5×10^{16} per cubic centimeter for conducting the current, formed over the semiconductor substrate (101); a drain region (105); a source region (107), wherein the source region (107) and the drain region (105) vertically connected to the channel region (103); a gate insulating layer (109); and a sensing membrane layer (111); characterized in that the gate insulating layer (109) and the sensing membrane layer (111) are formed along substantially all of the side walls of the channel region (103) to create a vertical multigate electrodes.

[10] The above provision is advantageous as the polysilicon layer is used as an active region predetermined channel for a transistor to build vertical field effect transistor. The present invention provides ISFET with multi-dimensional sensing membrane (111). It is an improvement of the current ISFET design which uses planar structure for the sensing membrane. The built-up of the multi-gate vertical ISFET of the present invention increases the membrane's surface area thus improving the sensitivity of the device.

[11] **BRIEF DESCRIPTION OF THE DRAWINGS**

[12] **Figure 1** illustrates cross section view of the present invention.

[13] **Figure 2** illustrates flowchart of a method for producing the present invention.

[14] **Figure 3** illustrates procedural diagrams of the method for producing the present invention.

[15] **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[16] The present invention relates to field effect transistors particularly to vertical multi-gate ion sensitive field effect transistors and a method of producing them. Referring to **Figure 1**, generally, the present invention provides an ion sensitive field effect transistor comprising: a semiconductor substrate (101); a channel region (103) having doped polysilicon layer (104) of at least 5×10^{16} per cubic centimeter for conducting the current, formed over the semiconductor substrate (101); a drain region (105); a source region (107), wherein the source region (107) and the drain region (105) vertically connected to the channel region (103); a gate insulating layer (109); and a sensing membrane layer (111); characterized in that the gate insulating layer (109) and the sensing membrane layer (111) are formed along substantially all of the side walls of the channel region (103) to create a vertical multigate electrodes. The sensing membrane layer (111) further comprising silicon nitride and metal oxides in which the metal oxides further comprising Aluminium Oxide; Tantalum Pentoxide; and Hafnium

Oxide, or the like.

- [17] The present invention comprises of polysilicon layer (104) implanted with high doping n-type or p-type layer on top for source region and light doping with opposite type dopant at the bottom. The transistor is designed in vertical order, which the drain region (105) is created by ion implantation in silicon substrate (101).
- [18] Generally, the method for manufacturing a multigate electrode ion sensitive field effect transistor comprising: providing semiconductor substrate (201); forming a drain region (203); forming a channel region (205); forming a source region (207); forming a gate insulating layer on the channel region (209); forming a sensing membrane layer on the gate insulating layer (211); and forming special contact holes to connect source and the channel region together (213). The flowchart of the method is illustrated in **Figure 2**.
- [19] Detailed explanations on the process flow with diagram is illustrated in **Figure 3**, in which the process is started with Step 1. Step 1 is n-type ion implantation on silicon substrate (101) to create drain region (105). The dopant ion used is arsenic or phosphorus. Step 2 is polysilicon deposition. Lightly doped p-type polysilicon layer (104) is used for channel region (103). Step 3 is ion implantation on polysilicon surface for source region (107). The same dopant type and dose as drain region (105) is used. Step 4 is polysilicon gate etch to define active or channel region (103) for the ISFET. The channel region (103) can be fabricated by micro or nano-fabrication techniques, which can be by lithographic patterning, pattern transfer or by thin film deposition and etching methods. Step 5 is gate oxidation/gate insulating layer (109) and sensing membrane layer (111) deposition on polysilicon (104) and sidewall. Both of these layers are performed consecutively with typically same dielectric thickness. Membranes, which are used as sensor elements themselves or as filters, are key component in many types of sensing devices. There are many types of sensing membrane for FET-based chemical sensor for wide range of sensing applications. The role of a chemical coating in a potentiometric sensor is to make the device selective and sensitive to analytes of interest. As for example in biosensor, enzymes and antibodies based membrane are often used to render a sensor biocompatible or as an inert matrix for active sensor components. But only the inorganic gate materials can be made easily, and the technology is compatible with standard IC technology. For gate oxidation, monocrystalline and polycrystalline silicon surface were oxidized at high temperature, dry process (thermal growing of SiO₂) to receive target thickness of SiO₂ layer. Afterwards, for pH sensors a chemosensitive silicon nitride layer is deposited from two gaseous phases in Low Pressure Chemical Vapor Deposition (LPCVD) process. The silicon nitride is formed in the pyrolytic reaction between dichlorosilane and ammonia at high temperature and typically low pressure. Step 6 is when contact

holes are created and followed by metallization steps. Special contact for source and polysilicon is created to short the source and channel substrate (PSUB) in single contact hole.

- [20] Although the invention has been described with reference to particular embodiment, it is to be understood that the embodiment is merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiment that other arrangements may be devised without departing from the scope of the present invention as defined by the appended claims.

Claims

- [Claim 1] A multigate electrode ion sensitive filed effect transistor comprising:
 a semiconductor substrate (101);
 a channel region (103) having doped polysilicon layer (104) of at least 5×10^{16} per cubic centimeter for conducting the current, formed over the semiconductor substrate (101);
 a drain region (105);
 a source region (107), wherein the source region (107) and the drain region (105) vertically connected to the channel region (103);
 a gate insulating layer (109); and
 a sensing membrane layer (111);
 characterized in that
 the gate insulating layer (109) and the sensing membrane layer (111) are formed along substantially all of the side walls of the channel region (103) to create a vertical multigate electrodes.
- [Claim 2] An ion sensitive filed effect transistor as claimed in Claim 1, wherein the sensing membrane layer (111) further comprising silicon nitride and metal oxides.
- [Claim 3] An ion sensitive filed effect transistor as claimed in Claim 2, wherein the metal oxide further comprising: Aluminium Oxide; Tantalum Pentoxide; and Hafnium Oxide.
- [Claim 4] A method for manufacturing a multigate electrode ion sensitive filed effect transistor comprising:
 providing semiconductor substrate (201);
 forming a drain region (203);
 forming a channel region (205);
 forming a source region (207);
 forming a gate insulating layer on the channel region (209);
 forming a sensing membrane layer on the gate insulating layer (211);
 and
 forming special contact holes to connect source and the channel region together (213).
- [Claim 5] A method for manufacturing a multigate electrode ion sensitive filed effect transistor as claimed in Claim 4, wherein the step of forming a drain region (203) further comprising implanting ion into the semiconductor substrate.
- [Claim 6] A method for manufacturing a multigate electrode ion sensitive filed

effect transistor as claimed in Claim 4, wherein the step of forming a channel region (207) further comprising forming a doped polysilicon electrode on the semiconductor substrate.

[Claim 7] A method for manufacturing a multigate electrode ion sensitive field effect transistor as claimed in Claim 4, wherein the step of forming a source region (207) further comprising implanting ion into the polysilicon electrode surface.

[Claim 8] A method for manufacturing a multigate electrode ion sensitive field effect transistor as claimed in Claim 4, wherein the special contact holes are formed on the polysilicon electrode.

[Claim 9] A method for manufacturing a multigate electrode ion sensitive field effect transistor as claimed in Claim 4 or Claim 6, wherein the channel region is formed by micro or nano-fabrication technique.

[Claim 10] A method for manufacturing a multigate electrode ion sensitive field effect transistor as claimed in Claim 9, wherein the micro or nano-fabrication technique can be of: lithographic patterning, or pattern transfer, or thin film deposition and etching methods.

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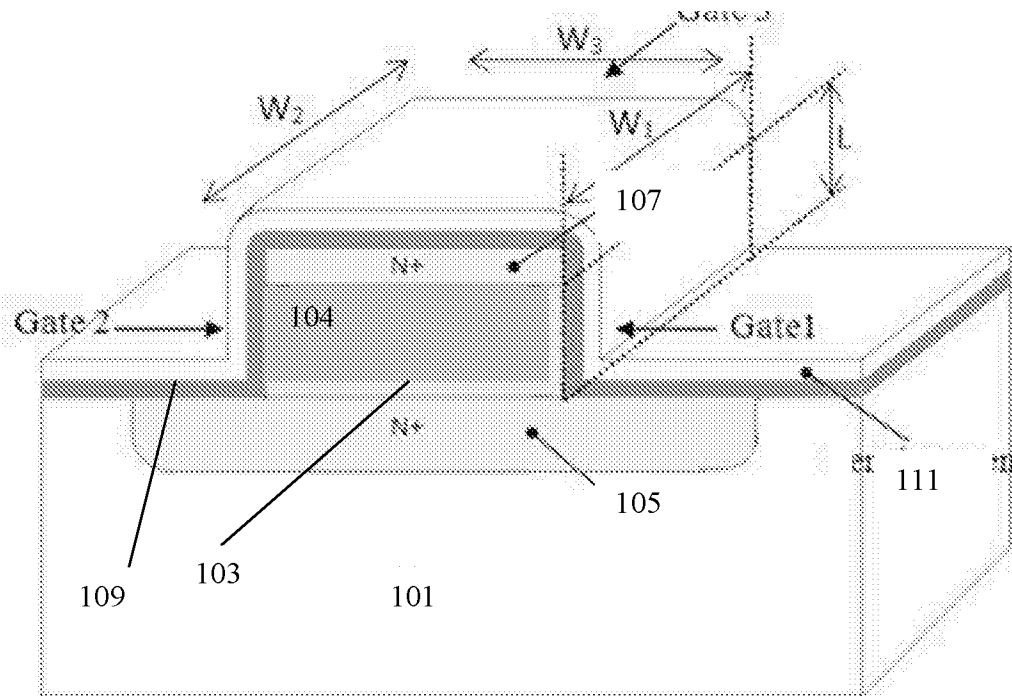
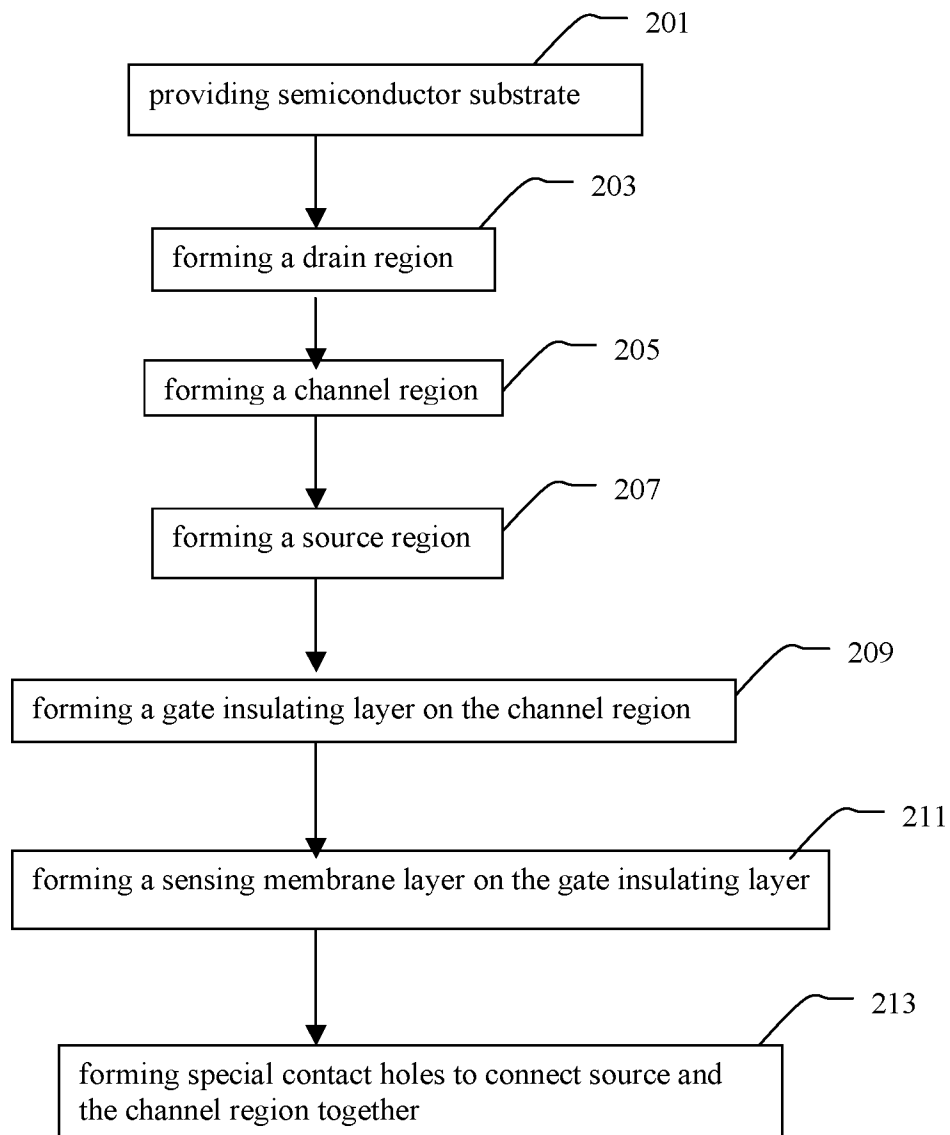
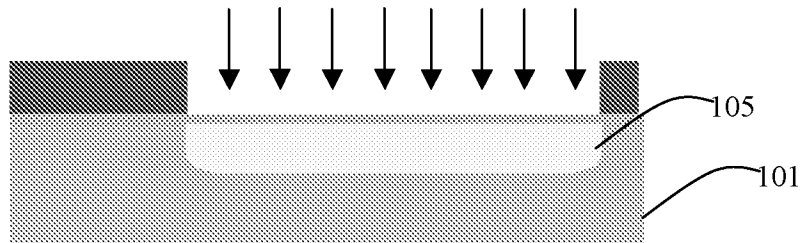


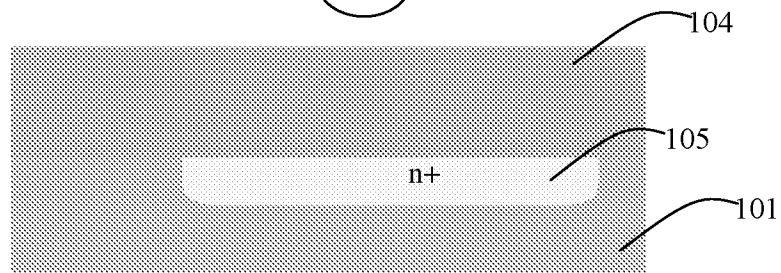
Figure 1

2/4**Figure 2**

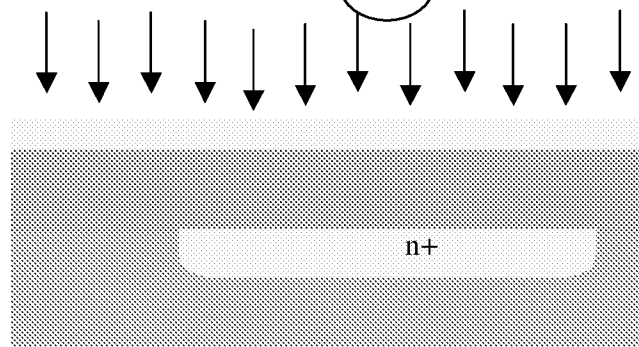
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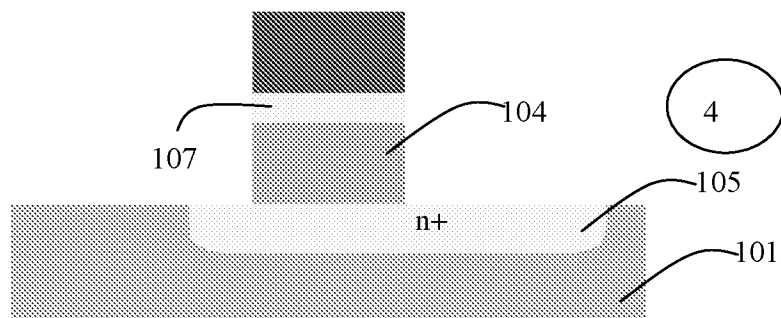
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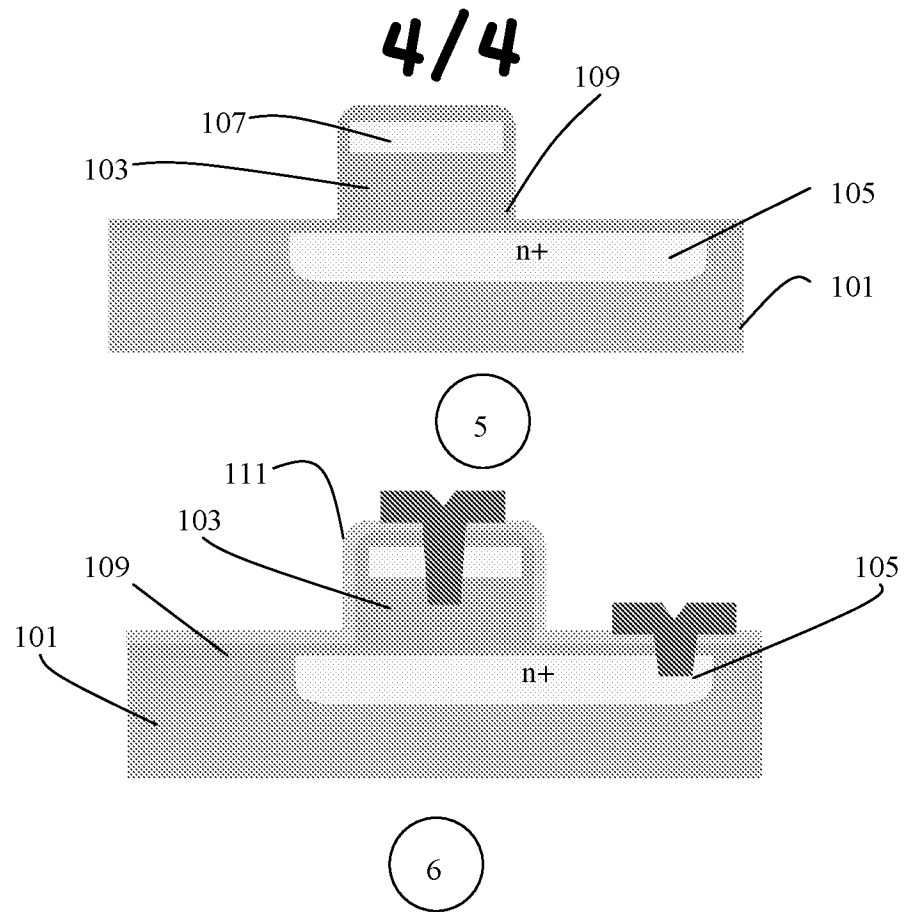


Figure 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2013/000269

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01N27/414 H01L29/78
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01N H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data, COMPENDEX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2012/154027 A1 (MIMOS BHD [MY]; BIEN DANIEL CHIA SHENG [MY]; OTHMAN MASURI [MY]; ABDUL) 15 November 2012 (2012-11-15) the whole document	1-10
A	----- Hong-Kun Lyu ET AL: "Formation of a Vertical MOSFET for Charge Sensing in a Si Micro-Fluidic Channel Chin-Sung Park and Geunbae Lim", Journal of the Korean Physical Society, 31 January 2004 (2004-01-31), pages 162-166, XP055112661, Retrieved from the Internet: URL: http://www.kps.or.kr/home/kor/journal/library/downloadPdf.asp?articleid=%7B09297AE9-AD67-4D9A-ADBC-907F49219536%7D . [retrieved on 2014-04-08] the whole document ----- -/-	1-10



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

8 April 2014

Date of mailing of the international search report

15/04/2014

Name and mailing address of the ISA/

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Stussi, Elisa

INTERNATIONAL SEARCH REPORT

International application No
PCT/MY2013/000269

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CHENG-HSIN CHEN ET AL: "A novel vertical MOSFET with bMPI structure for 1T-DRAM application", NEXT-GENERATION ELECTRONICS (ISNE), 2010 INTERNATIONAL SYMPOSIUM ON, IEEE, PISCATAWAY, NJ, USA, 18 November 2010 (2010-11-18), pages 133-135, XP031836197, ISBN: 978-1-4244-6693-1 the whole document	1-10
A	----- US 2010/126885 A1 (IECHI HIROYUKI [JP] ET AL) 27 May 2010 (2010-05-27) the whole document	1-10
A	----- WO 2009/045091 A2 (MIMOS BERHAD [MY]; SYONO MOHD ISMAHADI [MY]; ABDUL RANI ROZINA [MY]) 9 April 2009 (2009-04-09) the whole document -----	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/MY2013/000269

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WO 2009045091	A2	09-04-2009	NONE