

- [54] **CRT DISPLAY SYSTEM WITH CIRCLE DRAWING**
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340/324 AD

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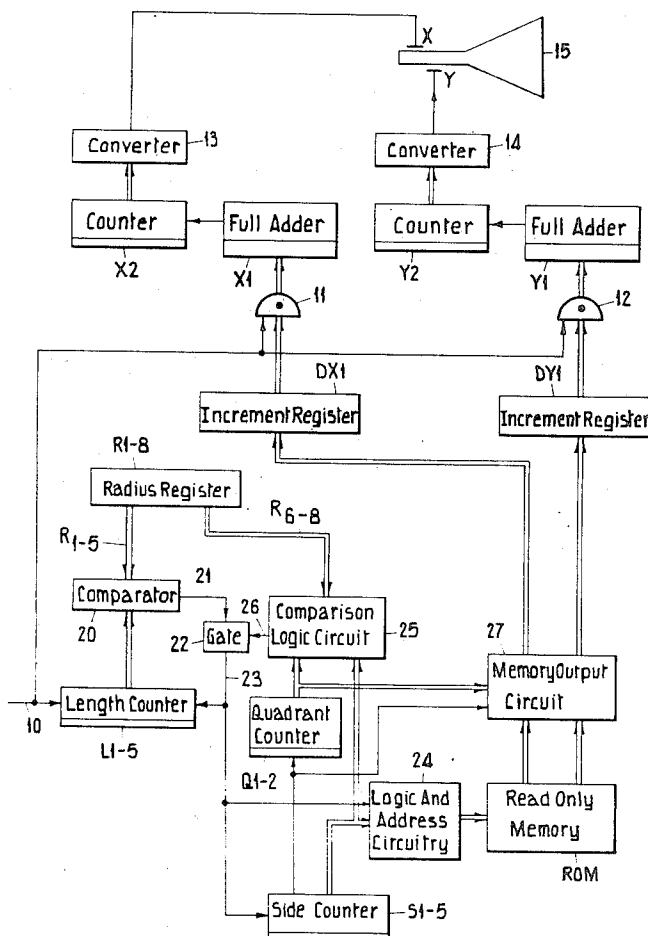
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[57] **ABSTRACT**

A display system of the CRT type wherein a desired curved line is produced from signals representing the co-ordinates of points spaced along the lengths of the lines to be displayed including means for generating signals representing the co-ordinates of points spaced along the lengths of a succession of adjoining straight lines each of which is of a predetermined length and at a predetermined angle such that the display produced from said signals approximates to a desired curved line. In a particular arrangement the display produced is a many-sided polygon and thus approximates to a circle.

10 Claims, 2 Drawing Figures



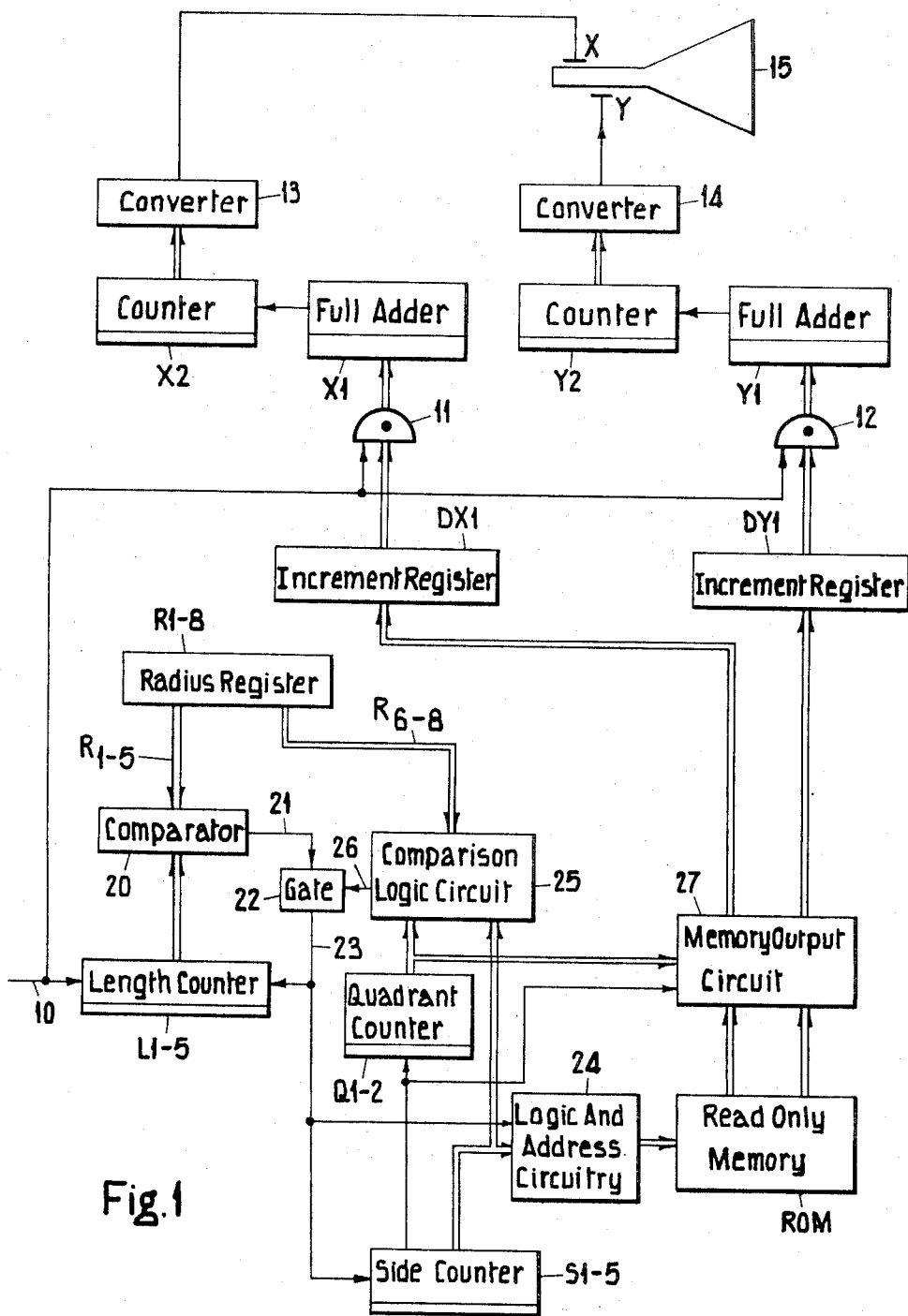


Fig. 1

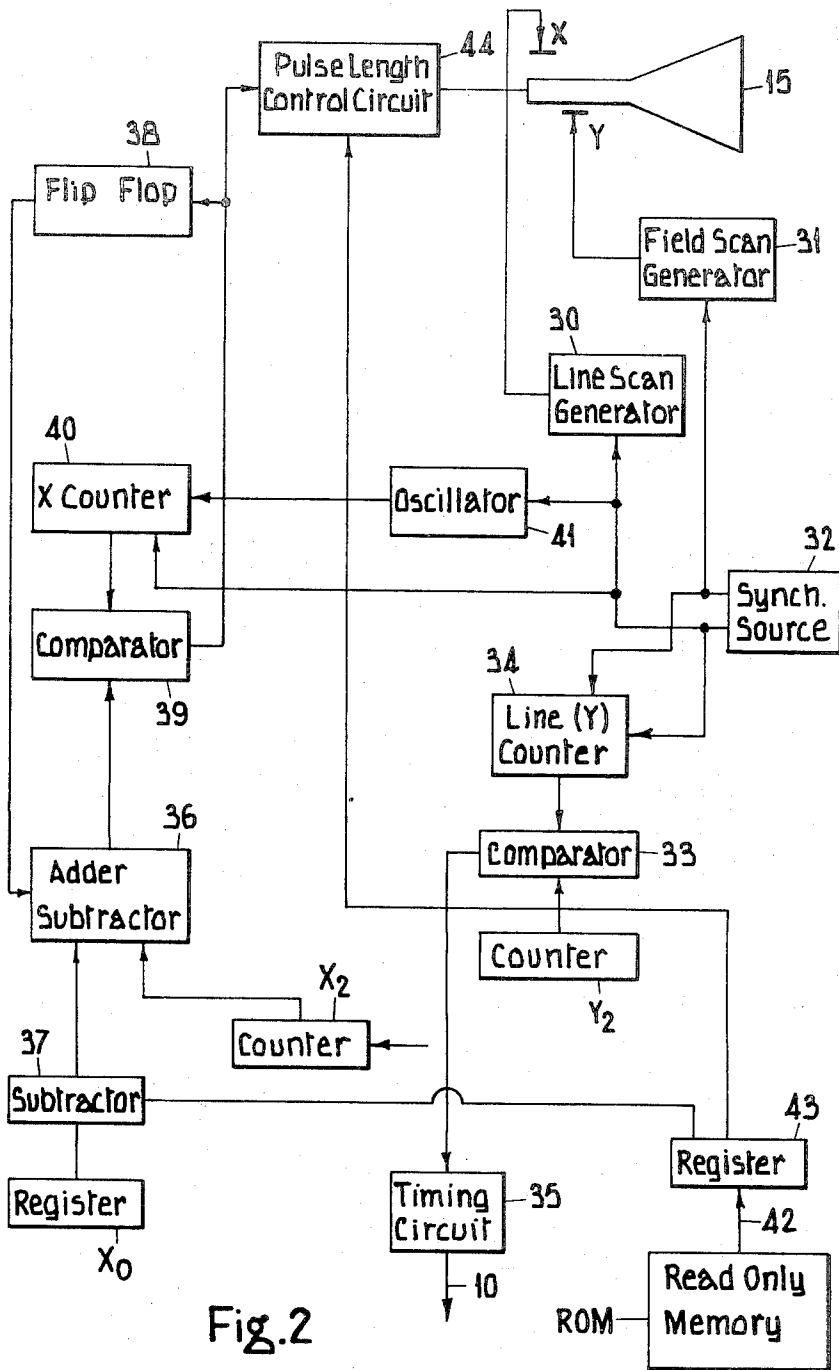


Fig. 2

CRT DISPLAY SYSTEM WITH CIRCLE DRAWING

The present invention relates to display systems of the CRT (cathode ray tube) type in which a DDA (digital differential analyzer) technique is used for defining the lines to be displayed.

By a display system of the CRT type is meant a display system using for its display device a conventional CRT or any other display device capable of producing a display equivalent to that produced by a conventional CRT, for example, a solid state matrix display device.

With the DDA technique, the lines to be displayed are produced from signals representing the co-ordinates of points spaced along the lengths of the lines.

In a typical DDA arrangement two digital registers (X and Y registers) are used, one for the X displacement and one for the Y displacement, each feeding a respective digital-to-analog converter. The X and Y registers are each constructed as adders, and have increments dx and dy added into them at regular intervals, so that their contents define a succession of points forming the line to be displayed. The increments are normally chosen so that the sum of their squares is constant (thus ensuring equal spacing of the points and hence uniform brightness for the line), their ratio being the instantaneous slope of the line.

For drawing straight lines, the increments dx and dy are of course constant, whilst for curved lines increments dx and dy must be varied. In known systems this is achieved by noting that the required increments are proportional to certain trigonometrical functions. For example, in the case of a circle the required increments are proportional to $\sin \theta$ and $\cos \theta$ respectively, where θ increases by a small constant for each successive point on the circle; each of these is proportional to the integral of the other (with a sign reversal in one case), and the increments dx and dy can therefore be varied continuously by interconnecting the two increment registers in a double integrating loop.

We have found, however, that such a system suffers from various disadvantages. For example, in the case of a circle one drawback is that in the most natural implementation, the quantity which defines the radius of the circle is proportional to the reciprocal of the radius. Thus to draw a series of circles with constantly increasing radii, a series of reciprocals has to be calculated; and the spacing between large circles will be inconveniently large. Another drawback is that the integrating loop will involve rounding errors. This means that a circle may not join up exactly, and its size and centre will vary in an apparently irregular and unpredictable manner.

It is an object of the present invention to provide a display system of the kind referred to above wherein these drawbacks are overcome.

According to the present invention a display system of the CRT type in which the lines to be displayed are produced from signals representing the co-ordinates of points spaced along the lengths of the lines to be displayed includes means for generating signals representing the co-ordinates of points spaced along the lengths of a succession of adjoining straight lines each of which is of a predetermined length and at a predetermined angle such that the display produced from said signals approximates to a desired curved line.

Preferably adjacent points in each straight line are equally spaced and circuit means are provided for varying the number of points in a selection, which may be all, of said straight lines, thereby to vary the size of said curved line without altering its shape.

In a preferred arrangement in accordance with the invention said display producing means comprises first storage means for storing in respect of each straight line information defining the difference in position of adjacent points in that straight line; co-ordinate register means for holding information defining the co-ordinates of a point; and circuit means for periodically supplying information from said storage means to said register means so that information defining the co-ordinates of each point in turn appears in said register means, the image produced on the screen of the display device of the system being a representation of the points defined by the information appearing in said register means.

In one particular form of said preferred arrangement said circuit means comprises second storage means for storing information defining the desired length of each straight line; length counting means for indicating the actual length of the straight line currently being drawn; comparator means, responsive to outputs from the second storage means and the length counting means, for producing an output when the line currently being drawn is of the desired length; line counting means responsive to the output of said comparator, for indicating which straight line is currently being drawn; logic circuit means for selecting the information supplied from said first storage means to said register means in dependence on the count of said line counting means; and means for applying input pulses to said length counting means so that information defining the co-ordinates of each point in turn appears in said register means, in the order the points occur along said curved line.

One particular application of a system according to the invention is for producing a display of a circle. In such an application, the displayed straight lines are all of substantially the same length and each adjacent pair of lines are at the same angle to one another so as to form a substantially regular many-sided polygon so that the display produced from the generated signals approximates to a circle.

In such an arrangement the polygon preferably has an integral number of sides in each quadrant, said first storage means stores information only in respect of points in which the sides in one octant of the polygon and said first storage means is connected to said register means via output circuit means for controlling the information supplied to the register means from said first storage means to obtain information defining the co-ordinates of the points in the sides of the other seven octants of the polygon in said register means.

One system in accordance with the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is an overall block diagram of the system; and
FIG. 2 is a block diagram of the system modified for raster operation.

In this system the lines to be displayed are produced from signals representing the X and Y co-ordinates of points spaced along the lengths of the lines. Referring to FIG. 1, the X and Y co-ordinates of the points are caused to appear in turn in main X and Y registers re-

spectively. Each of the main X and Y registers consists of two sections, X1 and X2 for the X register. The lower section, X1, is constructed as a full adder and register, while the upper section, X2, is constructed as a counter. The increments dx and dy which are required to update periodically the numbers in the main X and Y registers are held in increment registers DX1 and DY1 respectively. The increment dx is never large enough to affect the upper section X2 directly; this section X2 is incremented only by overflows from the lower section X1. Additions of the increment dx into the register section X1 are controlled by a gate 11, fed with pulses on line 10 at constant intervals. The Y register is similar, with a corresponding gate 12. The upper halves X2 and Y2 of the X and Y registers feed respective digital-to-analog converters 13 and 14, whose outputs drive the X and Y deflection systems of a CRT 15.

The above described circuits constitute the DDA part of the system and can be used in conventional manner to draw simple straight lines symbols.

Additional circuitry for drawing circles is provided which is shown in the lower part of FIG. 1. This circuitry controls the DDA part of the system to draw a many-sided polygon on the screen of the display device of the system approximating to a desired circle. The main elements of this circuitry are an 8-bit radius register R1-8, a five-bit side counter S1-5, a five-bit side length counter L1-5, a two-bit quadrant counter Q1-2, and a read-only memory ROM. The functions of these elements are indicated by their names: the radius register contains an eight-bit word indicative of the radius of the desired circle, and hence of the length of the sides of the polygon, to be drawn; the side counter contains a count indicating which side of the polygon is currently being drawn: the side length counter contains a count indicating length of the side currently being drawn; the quadrant counter indicates which of four quadrants of the polygon is currently being drawn; and the read-only memory contains the various increments dx and dy for the sides, in a permanently stored form.

Consider first the operation of the system when all sides of the polygon are to be of the same length. The side length is defined by five bits contained in the most significant stages, R1-5, of the radius register. The timing pulses on line 10 are fed to the side length counter L1-5, whose contents are compared with the side length in R1-5 by a comparator 20. On equality being achieved, an output signal on line 21 is fed through a gate 22 to line 23 to reset the side length counter L1-5, line 23 also feeding the side counter S1-5 to increment its count by 1. Thus the side counter S1-5 will remain at the same count for the necessary number of timing pulses.

The side counter S1-5 feeds logic and address circuitry 24 for the read-only memory ROM. The side counter completes a full counting cycle in each quadrant and its overflow is fed to the quadrant counter Q1-2, so that the quadrant counter is in effect an extension of two more stages to the side counter. The contents of the side counter are decoded by the circuitry 24 to select the next required location in the memory ROM, so that the new increments dx and dy can be set in the increment registers DX1 and DY1 when the next side is reached. The signal on line 23 may be used to control the timing of the operation of the memory ROM. The output of the memory ROM is fed to an output circuit 27, controlled by the outputs

from the quadrant counter and the most significant stage of the side counter in a manner described later, before being supplied to the increment registers DX1 and DY1.

It will be appreciated that the radius of the circle drawn may be varied in steps corresponding to a change of one point in the length of every side by altering the number stored in the stages R1-5 of the radius register.

The manner in which the radius of the circle may be varied in intermediate steps will now be described generally. The lower three stages R6-8 of the radius register feed a comparison logic circuit 25 together with the side counter S1-5. This circuit 25 contains logic circuitry, controlled from the radius register, which recognises certain counts of the side counter (the counts recognised depend on the contents of the radius register), and produces an output on line 26 for those counts. Line 26 feeds the gate circuit 22, and when energized, prevents the signal from comparator 20 from passing through for one time period. This may be achieved, for example, by arranging for comparator 20 to produce two outputs, "equality" and "excess", gating only the first, and combining the two. Hence, when circuit 25 produces an output the "equality" output of comparator 20 is blocked by gate 22 and an output does not appear on line 23 until the comparator 20 produces an "excess" output. This results in events being delayed by 1 time period for those sides for which an output signal is produced by circuit 25, so that the corresponding side of the polygon is one point larger.

The system will now be described in more detail, for drawing polygons with 100 sides. The number 100 is chosen because it is a multiple of 4, and therefore gives four identical quadrants each having an integral number of sides, and therefore being symmetrical about the 45° line. In addition, with 100 sides, the ratio of radius to circumference is almost exactly 4/25, so that an increase of 1 point on each side corresponds closely to an increase of 16 points in radius.

In a simple form of the system, the number of sides selected for an increase of 1 point in their lengths may be any one of 8 multiples of 3 from 0 to 21 in each quadrant; this is achieved by choosing one set of three sides, one set of six sides, and one set of 12 sides, all mutually exclusive, and selecting the appropriate combination of sets. By using one extra side in the last set, however, a better approximation is achieved. It is however preferred to achieve a still better approximation by using one extra side in the second set in the first and third quadrants and one extra side in the third set in the second and fourth quadrants.

The sets of three, six and 12 sides are selected by the circuitry 25 under the control of the stages R6-8 of the radius register; the set of three sides is selected if R8 is true, the set of six sides if R7 is true, and the set of 12 sides if R6 is true. To understand how they are selected, the operation of the side counter must first be stated in more detail. This counter has five stages, but counts only 25 sides (per quadrant); seven of the normal 32 counts must therefore be deleted. The deleted counts are chosen to be 13 to 19, i.e. binary 01101 to 10011 inclusive. The counter logic is constructed accordingly, so that count 01100 is followed by count 10100; this is achieved by recognizing the state 011xx (where "x" indicates "don't care") and using this to inhibit the next count pulse to the bottom stage of the counter, and to

enable the next count pulse directly to the fourth stage.

The set of 3 sides per quadrant is now defined as those sides whose counts have the pattern yy100, where yy is not 10; this pattern appears three times in the full count of 25 sides. The sets of six and 12 sides are similarly defined as those whose counts have patterns xxx10 and xxxx1 respectively, these patterns occurring six and 12 times respectively in the full count of 25 sides. To inset one extra side into the first or second set depending on quadrant, the same pattern 10100 is used, using the quadrant counter outputs as well.

The details of the read-only memory and its addressing will now be considered more fully. As so far described, the four quadrants of the polygon are identical. It is convenient for the polygon to have vertices at the junctions between quadrants. A total of 25 pairs of increments will then be required for each quadrant; those for the second, third and fourth quadrants can be obtained from those for the first by merely changing the sign of dx between vertically adjacent quadrants and of dy between horizontally adjacent quadrants. The contents of the quadrant counter Q1-2 is utilised by the ROM output circuit 27 to achieve this. Each quadrant, it will be further observed, is symmetrical about the 45° line. Hence, the dx and dy increments for the sides 14 to 25 are the same as the dy and dx increments sides 12 to 1 respectively; for side 13 the dx and dy increments are equal. Thus only the pairs of increments for the first 13 sides of a quadrant need be stored, and the increments for the last 12 sides can be obtained by interchanging the dx and dy increments for the first 12 sides. The read-only memory ROM therefore consists of 13 storage locations, each of which contains a pair of increments dx and dy. The address circuitry 24 operates to decode the contents of the lowest four stages of the side counter S1-5 normally up to and including side 13 (count 01100), and then to decode to the complement of the contents of the lowest four stages for the remaining counts (10100 upwards to 11111). This conversion is controlled by the most significant stage of the side counter, which is 0 for the first 13 sides and 1 for the last 12. It is easily seen that the sum of the counts for two corresponding sides, one in the first 12 and the other in the last 12, is always 11111. The output circuitry 27 of the ROM is controlled by the quadrant counter Q1-2 to insert negative signs into the increments dx and dy in the appropriate quadrants, and by the quadrant counter and the output of the most significant stage of the side counter to interchange the increments dx and dy when required.

The position of the circle on the CRT face is determined by inserting appropriate initial values in the registers X2 and Y2.

It can be realized that, by minor modifications to the control system, it is possible to draw arcs of circles directly, without having to take the full time required to draw a complete circle and to black out the spot for the unwanted portions.

For very small circles, of fewer than 100 points, the system may be modified so that the side counter S1-5 counts in larger steps. Such circles will then be drawn with fewer than 100 sides. For example, only 12 sides could be used per quadrant, of 1 or 2 points length as appropriate, to obtain circles down to half the size of the smallest 100-side circle, and so on.

For large circles, more accurate radius control than described above can be obtained by inserting one or more extra points; preferably an even number are introduced, in diametrically opposite sides, so that the polygon closes up properly. This can be achieved by using the high-order stages of the radius register, i.e. stages R1 to R4, to feed further circuitry in the logical circuitry 25, inserting an extra point in selected sides when the circle is large. The circuitry already discussed for block 25 is capable of inserting extra points into a total of 22 (12 + 6 + 3 + 1) sides per quadrant; this leaves three sides of the 25 per quadrant which can have extra points inserted into them for large circles without interfering with the normal fine adjustment of circle size.

This technique for drawing circles is also compatible with operation in a raster mode. In this mode, the spot on the CRT face is caused to trace out a TV-type raster, and information is displayed by controlling the brightness of the spot. It is sometimes desirable to use this mode, e.g. for displaying a TV picture, and to be able to superimpose symbolic information on this picture. It is therefore desirable to be able to use the circle drawing circuitry to draw circles when the system is operating in the raster mode. To achieve this, the system shown in FIG. 2 may be used; only the parts of the system of FIG. 1 where modification is required are shown in FIG. 2.

Referring to FIG. 2, a line scan generator 30 and a frame waveform generator 31 are provided for causing the spot on the CRT face to follow the TV-type raster, the lines being horizontal. The scan generators 30 and 31 are synchronised by field and line synchronising pulses derived from a source 32. The counter section Y2 of the Y deflection register is initially filled with the Y co-ordinate of the topmost point of the circle to be drawn; the X co-ordinate of this point is stored in a separate register X0, however, instead of the counter section X2 of the X deflection register. The contents of Y2 are compared in a comparator 33 with the Y co-ordinate of the line currently being scanned, which is produced in a line counter 34 to which the line synchronising pulses are fed, the counter 34 being reset at the end of each field by a field synchronising pulse. The comparator 33 controls a timing circuit 35 which generates timing pulses applied to line 10; the timing circuit 35 generates pulses for as long as the contents of register Y2 are different from the Y co-ordinate of the line currently being scanned. Thus the timing pulses on line 10 will appear in bursts, each burst carrying the circle generation system forward from the Y co-ordinate of one raster line to the next, the system then waiting until the next line begins.

The contents of registers X0 and X2 are fed to an adder-subtractor 36, the X0 register contents being fed via a subtractor 37 whose purpose will be explained later, but which for the present will be ignored. The adder-subtractor 36 is controlled by a bistable flip-flop 38 which is set at the beginning of each raster line to control the adder-subtractor to subtract the contents of X2 from the contents of X0; thus the output of the adder-subtractor represents the X co-ordinate of the left-hand side of the circle being generated. When this difference is equal to the instantaneous value of the X co-ordinate of the spot being scanned on the CRT face, as determined by a signal emitted from a comparator 39, a pulse is fed to the video input to the CRT to cause the

spot to be brightened. The output of comparator 39 is also fed to the flip-flop 38 to change its state; the adder-subtractor 36 now forms the sum of the contents of registers X0 and X2, and this sum is compared with the X co-ordinate of the spot, a second pulse being produced by comparator 39 on equality. Thus on each line of the raster, two bright-up pulses are produced, corresponding to the two sides of the circle. The circle is thus produced by the circle generating system generating a half-circle, with the other half being produced by, in effect, reflecting the directly generated half-circle in its vertical diameter. A signal representing the X co-ordinate of the spot being scanned on the CRT face is fed to the comparator 38 from a counter 40 which counts the cycles of oscillation produced by an oscillator 41 operating under control of the line synchronising pulses at a multiple of the line scanning frequency corresponding to the desired horizontal definition of the system.

Means (not shown) may of course be provided for inhibiting the bright-up pulses above and below the circle, to obviate the possibility of any streaks above or below it.

As so far described, the points forming the circle will be identical and will appear with equal vertical spacing, and thus with a spacing which varies around the circumference, being densest at the sides of the circle. To produce a continuous circle of uniform brightness the length of the bright-up pulses and hence the corresponding 'points', is varied the pulse length increasing as the space between points on the circle increases, that is, as the angle which the side of the polygon being drawn makes with the horizontal decreases. For this purpose, the read-only memory ROM stores a bright-up length word as well as the two increments dx and dy for each side of the polygon. When increments are read out, the bright-up length word is also read out on line 42 and fed to a register 43 which controls a pulse length control circuit 44, the output pulses from comparator 39 being fed to the circuit 44 to initiate the bright-up pulses.

In addition, half the pulse length in register 43 is subtracted in subtractor 37 from the contents of register X0, the resultant being fed to the adder/subtractor 36. As a result, the output of comparator 39 for each point occurs before that point, as defined by the contents of the counter X2, by an amount equal to half the length of the bright-up pulse for that point. Hence, the bright-up pulses produce images on the CRT centred on the points defined by the contents of the counter X2.

In an alternative arrangement (not illustrated) for obtaining a circle of uniform brightness the intensity, instead of the length, of the bright-up pulses is controlled by words stored in the read-only memory ROM. With this arrangement the output of the comparator 39 is fed to the CRT via a brightness control circuit controlled by the bright-up intensity words in the read-only memory, and the subtractor 37 is not required.

Although the system has been described with reference to circles, it is obvious that it can be used for any curved line symbol. It is more convenient to keep all the straight lines representing the curved line symbol of equal length, to simplify the problem of varying the size of the curved line symbol, although it would be possible to use straight lines whose lengths were integral multiples of a standard length. It would also be possible, in a system which operates in conjunction with a general purpose digital computer, to replace the read-only

memory with its permanently stored increments by a set of sub-routines stored in the main memory of the computer; the appropriate sub-routine for a desired curved line symbol would then be entered when required, and the increments calculated again each time the symbol is drawn.

We claim:

1. A display system of the CRT type, in which lines to be displayed are produced from signals representing the co-ordinates of points spaced along the lengths of the lines to be displayed, including means for generating signals representing the co-ordinates of points spaced along the lengths of a succession of adjoining straight lines each of which is of a predetermined length and at a predetermined angle such that the display produced from said signals approximates to a desired curved line; said signal generating means comprising:

- a. first storage means for storing in respect of each straight line information defining the difference in position of adjacent points in that straight line and hence defining the angle of that line
- b. second storage means for storing information defining the desired length of each straight line;
- c. length counting means for indicating the actual length of the straight line currently being drawn;
- d. comparator means, responsive to outputs from the second storage means and the length counting means, for producing an output when the line currently being drawn is of the desired length;
- e. line counting means, responsive to the output of said comparator, for indicating which straight line is currently being drawn;
- f. co-ordinate register means for holding information defining the co-ordinates of a point;
- g. logic circuit means for selecting and supplying information from said first storage means to said register means in dependence on the count of said line counting means; and
- h. means for applying input pulses to said length counting means so that information defining the co-ordinates of each point in turn appears in said register means, in the order the points occur along said curved line, the image produced on the screen of the display device of the system being a representation of the points defined by the information appearing in said register means.

2. A system according to claim 1 wherein the information stored in said first and second storage means is such that the display produced from the generated signals is a substantially regular many-sided polygon and thus approximates to a circle.

3. A system according to claim 2 wherein the display produced is a polygon having an integral number of sides in each quadrant, said first storage means stores information in respect of points in the sides in one octant of the polygon; and said first storage means is connected to said register means via output circuit means for controlling the information supplied to the register means from said first storage means to obtain information defining the co-ordinates of the points in the sides of the other seven octants of the polygon in said register means.

4. A system according to claim 2 wherein said second storage means stores a number defining the radius of the circle, and second logic circuit means is provided for increasing the number of points in every side of the

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polygon by the same amount in response to an increase in the more significant part of the number and for increasing the number of points in a fractional selection only of the sides of the polygon in response to an increase in the less significant part of the number.

5. A system according to claim 1 wherein adjacent points in each straight line are equally spaced and second logic circuit means are provided for varying the number of points in a selection, which may be all, of said straight lines, thereby to vary the size of said curved line without altering its shape.

6. A system according to claim 4 wherein an increase in the number of points in a side of said fractional selection is effected by delaying the output of the comparator for that side by one input pulse period.

7. A system according to claim 4 wherein said fractional selection is determined by comparing said less significant part of the number stored in the second storage means and the count of said side counting means.

8. A system according to claim 1 including a deflec-

tion system associated with the display device and means for applying the output of said signal generating means to said deflection system so as to produce images on the screen of the display at positions corresponding to the points defined by the output of said signal generating means.

9. A system according to claim 1 including a deflection system for scanning the screen of the display device in a raster, and means for utilizing the output of the signal generating means to brighten-up portions of the raster lines corresponding to the points defined by the output signal of said generating means.

10. A system according to claim 9 including means for controlling the length of the brightened-up portions of the raster lines in dependence on the spacing of the points defined by the output of the signal generating means, thereby to render each straight line image of substantially the same overall brightness.

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