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Strasse 28, 01069 Dresden (DE).(81) Designated States (unless otherwise indicated, for every
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BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
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(54) Title: CHARGE STORAGE FERROELECTRIC MEMORY HYBRID AND ERASE SCHEME

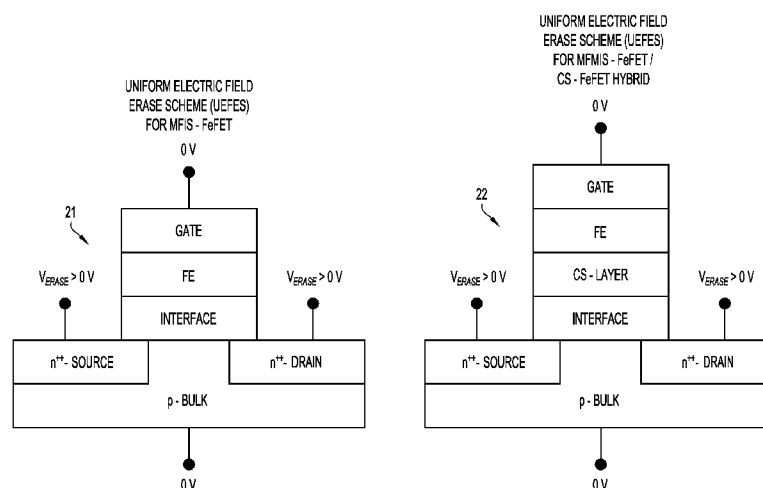


FIG.2

(57) **Abstract:** A technique for erasing a ferroelectric field effect transistor (FeFET) memory circuit comprising a plurality memory cells comprising FeFETs is described. Each FeFET comprises a gate stack, a source, a drain, a channel and a bulk substrate region, where the gate stack comprises a gate and a ferroelectric layer disposed between the gate and the channel. A positive or a negative voltage is applied to the source and drain regions of at least one FeFET memory cell depending on the channel type. The gate and bulk substrate regions are held at a ground state during said applying of the positive voltage to the source and drain regions of the FeFET memory cell to cause erasure of the at least one FeFET memory cell. In addition, a FeFET is described with a charge storage layer disposed adjacently to the ferroelectric layer within the gate stack.

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2015/055594

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C11/22
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 01/69602 A2 (SYMETRIX CORP [US]) 20 September 2001 (2001-09-20)	19,25-27
A	page 13, line 29 - page 15, line 10; figures 2, 4	1
X	US 6 122 191 A (HIROSE RYAN T [US] ET AL) 19 September 2000 (2000-09-19)	19,25-27
A	column 22, line 64 - column 23, line 55; figures 14B, 16B column 25, line 38 - column 26, line 29	1
A	US 2005/117419 A1 (HOSHINO KOZO [JP] ET AL) 2 June 2005 (2005-06-02) paragraphs [0077], [0101] - [0107]; figures 5, 6	1-5,19



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

9 December 2015

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10/03/2016

Name and mailing address of the ISA/

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2015/055594

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-16, 19-27

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2015/055594

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
WO 0169602	A2	20-09-2001	US 6370056 B1 WO 0169602 A2	09-04-2002 20-09-2001
US 6122191	A	19-09-2000	US 6122191 A US 6363011 B1	19-09-2000 26-03-2002
US 2005117419	A1	02-06-2005	JP 2005166741 A US 2005117419 A1	23-06-2005 02-06-2005

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-16, 19-27

A method of erasing a ferroelectric field effect transistor (FeFET) memory circuit comprising a plurality of FeFET memory cells, each FeFET comprising a gate stack, a source, a drain, a channel and a bulk substrate region, wherein the gate stack comprises a gate and a ferroelectric layer disposed between the gate and the channel.

2. claims: 17, 18

A method of inhibiting programming of a ferroelectric field effect transistor (FeFET) memory circuit comprising a plurality memory cells comprising FeFETs, each FeFET comprising a gate stack, a source, a drain, a channel and a bulk substrate region, wherein the gate stack comprises a gate and a ferroelectric layer disposed between the gate and the channel.
