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(54) Title: SELECTIVE ETCHING BETWEEN SILICON-AND-GERMANIUM-CONTAINING MATERIALS WITH VARYING GERMANIUM CONCENTRATIONS

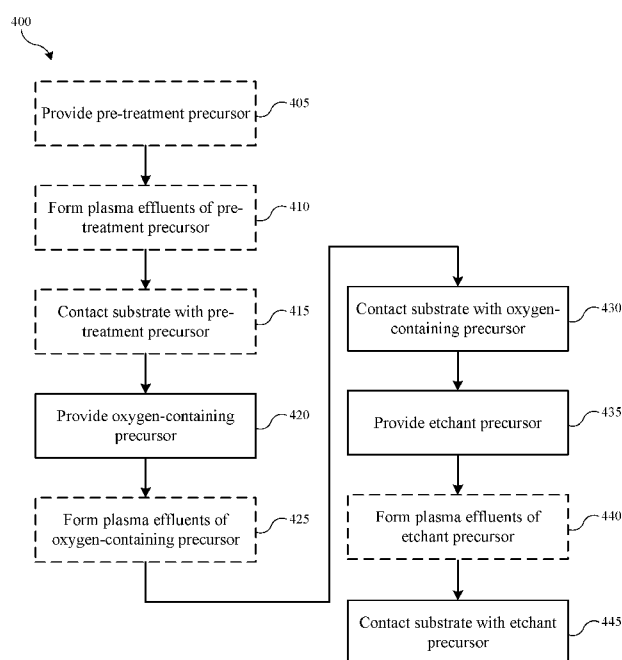


FIG. 4

(57) Abstract: Exemplary semiconductor processing methods may include providing a pre-treatment precursor to a processing region of a semiconductor processing chamber. A first layer of silicon-and-germanium-containing material and a second layer of silicon-and-germanium-containing material may be disposed on a substrate housed within the processing region. A native oxide may be present on the first layer and the second layer. The methods may include contacting the substrate with the pre-treatment precursor to remove the native oxide. The methods may include providing an oxygen-containing precursor to the processing region. The methods may include contacting the substrate with the oxygen-containing precursor to oxidize at least a portion of the second layer. The methods may include providing an etchant precursor to the processing region. The methods may include contacting the substrate with the etchant precursor to selectively etch the first layer of silicon-and-germanium-containing material.

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SELECTIVE ETCHING BETWEEN SILICON-AND-GERMANIUM-CONTAINING MATERIALS WITH VARYING GERMANIUM CONCENTRATIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

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[0001] This application claims the benefit and priority of U.S. Patent Application No. 18/223,156, filed July 18, 2023, entitled “SELECTIVE ETCHING BETWEEN SILICON-AND-GERMANIUM-CONTAINING MATERIALS WITH VARYING GERMANIUM CONCENTRATIONS”, which is hereby incorporated by reference in its entirety.

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TECHNICAL FIELD

[0002] The present technology relates to semiconductor processes and equipment. More specifically, the present technology relates to selectively etching silicon-and-germanium-containing material in vertical structures.

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BACKGROUND

[0003] Integrated circuits are made possible by processes which produce intricately patterned material layers on substrate surfaces. Producing patterned material on a substrate requires controlled methods for removal of exposed material. Chemical etching is used for a variety of purposes including transferring a pattern in photoresist into underlying layers, thinning layers, or thinning lateral dimensions of features already present on the surface. Often it is desirable to have an etch process that etches one material faster than another facilitating, for example, a pattern transfer process. Such an etch process is said to be selective to the first material. As a result of the diversity of materials, circuits, and processes, etch processes have been developed with a selectivity towards a variety of materials.

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[0004] Etch processes may be termed wet or dry based on the materials used in the process. A wet HF etch preferentially removes silicon oxide over other dielectrics and materials. However, wet processes may have difficulty penetrating some constrained trenches and also may sometimes deform the remaining material. Dry etches produced in local plasmas formed within the substrate processing region can penetrate more constrained trenches and exhibit

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less deformation of delicate remaining structures. However, local plasmas may damage the substrate through the production of electric arcs as they discharge.

[0005] Thus, there is a need for improved systems and methods that can be used to produce high quality devices and structures. These and other needs are addressed by the present
5 technology.

SUMMARY

[0006] Exemplary semiconductor processing methods may include providing a pre-treatment precursor to a processing region of a semiconductor processing chamber. A substrate may be housed within the processing region. A first layer of silicon-and-germanium-containing material and a second layer of silicon-and-germanium-containing
10 material may be disposed on the substrate. A native oxide may be present on the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material. The methods may include contacting the substrate with the pre-treatment precursor. The contacting may remove the native oxide from the first layer of
15 silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material. The methods may include providing an oxygen-containing precursor to the processing region. The methods may include contacting the substrate with the oxygen-containing precursor. The contacting may oxidize at least a portion of the second layer of silicon-and-germanium-containing material. The methods may include providing an etchant
20 precursor to the processing region. The methods may include contacting the substrate with the etchant precursor. The contacting may selectively etch the first layer of silicon-and-germanium-containing material.

[0007] In some embodiments, the first layer of silicon-and-germanium-containing material may be characterized by a first germanium concentration. The second layer of silicon-and-germanium-containing material may be characterized by a second germanium concentration.
25 The first germanium concentration may be less than the second germanium concentration. The pre-treatment precursor may be a hydrogen-containing precursor or a nitrogen-containing precursor. The hydrogen-containing precursor may be or include diatomic hydrogen (H_2) or ammonia (NH_3). The nitrogen-containing precursor may be or include diatomic nitrogen
30 (N_2) or NH_3 . The methods may include forming plasma effluents of the pre-treatment precursor. The oxygen-containing precursor may be or include diatomic oxygen (O_2) or steam (H_2O). The methods may include forming plasma effluents of the oxygen-containing

precursor. A pressure in the processing region may be maintained at less than or about 30 Torr. The contacting may etch the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material at a selectivity of greater than or about 40:1. A temperature in the processing region may be maintained at greater than or about 150 °C. Contacting the substrate with the pre-treatment precursor, contacting the substrate with the oxygen-containing precursor, and contacting the substrate with the etchant precursor may be performed on a single mainframe.

[0008] Some embodiments of the present technology may encompass semiconductor processing methods. The methods may include providing an oxygen-containing precursor to a processing region of a semiconductor processing chamber. A substrate may be housed within the processing region. A first layer of silicon-and-germanium-containing material and a second layer of silicon-and-germanium-containing material may be disposed on the substrate. The first layer of silicon-and -germanium-containing material may be characterized by a lesser germanium concentration than the second layer of silicon-and -germanium-containing material. The methods may include contacting the substrate with the oxygen-containing precursor. The contacting may oxidize at least a portion of the second layer of silicon-and-germanium-containing material. The methods may include providing a fluorine-containing precursor to the processing region. The methods may include contacting the substrate with the fluorine-containing precursor. The contacting may etch the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material at a selectivity of greater than or about 40:1.

[0009] In some embodiments, the first layer of silicon-and-germanium-containing material may be characterized by a germanium concentration of less than or about 35 at.%. The second layer of silicon-and -germanium-containing material may be or include a doped silicon-and-germanium-containing material. The oxygen-containing precursor may be or include diatomic oxygen (O₂) or steam (H₂O). The methods may include forming plasma effluents of H₂O. A native oxide may be present on the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material. The methods may include providing a pre-treatment precursor to the processing region and contacting the substrate with the pre-treatment precursor. The contacting may remove the native oxide from the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material.

[0010] Some embodiments of the present technology may encompass semiconductor processing methods. The methods may include providing a hydrogen-containing precursor or a nitrogen-containing precursor to a processing region of a semiconductor processing chamber. A substrate may be housed within the processing region. A first layer of silicon-and-germanium-containing material and a second layer of silicon-and-germanium-containing material may be disposed on the substrate. The first layer of silicon-and-germanium-containing material may be characterized by a lesser germanium concentration than the second layer of silicon-and-germanium-containing material. A native oxide may be present on the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material. The methods may include contacting the substrate with the hydrogen-containing precursor or the nitrogen-containing precursor. The contacting may remove the native oxide from the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material. The methods may include providing an oxygen-containing precursor to the processing region, wherein the oxygen-containing precursor comprises diatomic oxygen (O₂) or steam (H₂O). The methods may include contacting the substrate with the oxygen-containing precursor. The contacting may oxidize at least a portion of the second layer of silicon-and-germanium-containing material. The methods may include providing a fluorine-containing precursor to the processing region. The methods may include contacting the substrate with the fluorine-containing precursor. The contacting may selectively etch the first layer of silicon-and-germanium-containing material.

[0011] In some embodiments, a temperature in the processing region may be maintained at greater than or about 200 °C. Contacting the substrate with the fluorine-containing precursor may etch the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material at a selectivity of greater than or about 50:1.

[0012] Such technology may provide numerous benefits over conventional systems and techniques. For example, the processes may selectively oxidize one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material prior to etching operations. Additionally, the selective oxidation may permit selective etching of non-oxidized silicon-and-germanium-containing material relative to oxidized silicon-and-germanium-containing material. These and other embodiments, along with many of their

advantages and features, are described in more detail in conjunction with the below description and attached figures.

BRIEF DESCRIPTION OF THE DRAWINGS

5 **[0013]** A further understanding of the nature and advantages of the disclosed technology may be realized by reference to the remaining portions of the specification and the drawings.

[0014] FIG. 1 shows a top plan view of one embodiment of an exemplary processing system according to embodiments of the present technology.

[0015] FIG. 2A shows a schematic cross-sectional view of an exemplary processing
10 chamber according to embodiments of the present technology.

[0016] FIG. 2B shows a detailed view of a portion of the processing chamber illustrated in FIG. 2A according to embodiments of the present technology.

[0017] FIG. 3 shows a bottom plan view of an exemplary showerhead according to embodiments of the present technology.

15 **[0018]** FIG. 4 shows exemplary operations in a method according to embodiments of the present technology.

[0019] FIGS. 5A-5C show cross-sectional views of substrates being processed according to embodiments of the present technology.

[0020] Several of the figures are included as schematics. It is to be understood that the
20 figures are for illustrative purposes, and are not to be considered of scale unless specifically stated to be of scale. Additionally, as schematics, the figures are provided to aid comprehension and may not include all aspects or information compared to realistic representations, and may include superfluous or exaggerated material for illustrative purposes.

25 **[0021]** In the appended figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a letter that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the letter.

DETAILED DESCRIPTION

[0022] In transitioning to gate-all-around (GAA) transistors, many process operations are modified from more conventional fin field-effect (FinFET) transistors. Additionally, as
5 structures continue to reduce in size, the thicknesses of material layers reduce and the aspect ratios of memory holes and other structures increase, sometimes dramatically.

[0023] During GAA processing, alternating layers of material are deposited on a substrate, such as alternating layers of silicon-containing material and silicon-and-germanium-containing material. In forming the transistor, memory holes or trenches may be formed
10 through the alternating layers of material. During GAA processing, the silicon-and-germanium-containing material may be recessed from within the memory holes or trenches to form material that will serve as nanowires/nanosheets. Subsequent recessing one or more materials, including another silicon-and-germanium-containing material, may be formed within the recesses and/or memory holes or trenches.

[0024] Because of the similar materials in some GAA transistors, selectively removing one material relative to another material may become increasingly difficult. For example, multiple silicon-containing materials, including multiple silicon-and-germanium-containing materials may be used in GAA processing. In some operations, it may be desirable to remove one silicon-and-germanium-containing material, such as silicon-and-germanium-containing
20 nanowires, relative to epitaxial silicon-and-germanium-containing material and other silicon-containing materials. Conventional technologies have struggled with selectively removing one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. The non-selective removal may result in undesirable etching of some material, such as epitaxial silicon-and-germanium-containing material.

[0025] The present technology overcomes these issues by performing a selective oxidation prior to etching silicon-and-germanium-containing material, such as the silicon-and-germanium-containing nanowires. The selective oxidation may preferentially oxidize silicon-and-germanium-containing material characterized by a higher germanium concentration, such as the epitaxial silicon-and-germanium-containing material. The oxidized silicon-and-
25 germanium-containing material may be more resistant to etching compared to the non-oxidized silicon-and-germanium-containing material. Therefore, a subsequent etching operation to remove the silicon-and-germanium-containing material characterized by a lower
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germanium concentration may selectively remove the lower concentration material relative to the higher concentration material. Thus, the etching operations of the present technology may successfully remove one silicon-and-germanium-containing material while maintaining another silicon-and-germanium-containing material in addition to other silicon-containing materials.

[0026] Although the remaining disclosure will routinely identify specific etching processes utilizing the disclosed technology, it will be readily understood that the systems and methods are equally applicable to etching processes as may occur in the described chambers.

Accordingly, the technology should not be considered to be so limited as for use with etching processes or chambers alone. Moreover, although an exemplary chamber is described to provide foundation for the present technology, it is to be understood that the present technology can be applied to virtually any semiconductor processing chamber that may allow the operations described.

[0027] **FIG. 1** shows a top plan view of one embodiment of a processing system 100 of deposition, etching, baking, and curing chambers according to embodiments. In the figure, a pair of front opening unified pods (FOUPs) 102 supply substrates of a variety of sizes that are received by robotic arms 104 and placed into a low pressure holding area 106 before being placed into one of the substrate processing chambers 108a-f, positioned in tandem sections 109a-c. A second robotic arm 110 may be used to transport the substrate wafers from the holding area 106 to the substrate processing chambers 108a-f and back. Each substrate processing chamber 108a-f, can be outfitted to perform a number of substrate processing operations including the dry etch processes described herein in addition to cyclical layer deposition (CLD), atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), etch, pre-clean, degas, orientation, and other substrate processes.

[0028] The substrate processing chambers 108a-f may include one or more system components for depositing, annealing, curing and/or etching a dielectric film on the substrate wafer. In one configuration, two pairs of the processing chambers, e.g., 108c-d and 108e-f, may be used to deposit dielectric material on the substrate, and the third pair of processing chambers, e.g., 108a-b, may be used to etch the deposited dielectric. In another configuration, all three pairs of chambers, e.g., 108a-f, may be configured to etch a dielectric film on the substrate. Any one or more of the processes described may be carried out in

chamber(s) separated from the fabrication system shown in different embodiments. It will be appreciated that additional configurations of deposition, etching, annealing, and curing chambers for dielectric films are contemplated by system 100.

[0029] FIG. 2A shows a cross-sectional view of an exemplary process chamber system 200 with partitioned plasma generation regions within the processing chamber. During film etching, e.g., titanium nitride, tantalum nitride, tungsten, silicon, polysilicon, silicon oxide, silicon nitride, silicon oxynitride, silicon oxycarbide, etc., a process gas may be flowed into the first plasma region 215 through a gas inlet assembly 205. A remote plasma system (RPS) 201 may optionally be included in the system, and may process a first gas which then travels through gas inlet assembly 205. The inlet assembly 205 may include two or more distinct gas supply channels where the second channel (not shown) may bypass the RPS 201, if included.

[0030] A cooling plate 203, faceplate 217, ion suppressor 223, showerhead 225, and a pedestal 265, having a substrate 255 disposed thereon, are shown and may each be included according to embodiments. The pedestal 265 may have a heat exchange channel through which a heat exchange fluid flows to control the temperature of the substrate, which may be operated to heat and/or cool the substrate or wafer during processing operations. The wafer support platter of the pedestal 265, which may comprise aluminum, ceramic, or a combination thereof, may also be resistively heated in order to achieve relatively high temperatures, such as from up to or about 100 °C to above or about 1100 °C, using an embedded resistive heater element.

[0031] The faceplate 217 may be pyramidal, conical, or of another similar structure with a narrow top portion expanding to a wide bottom portion. The faceplate 217 may additionally be flat as shown and include a plurality of through-channels used to distribute process gases. Plasma generating gases and/or plasma excited species, depending on use of the RPS 201, may pass through a plurality of holes, shown in FIG. 2B, in faceplate 217 for a more uniform delivery into the first plasma region 215.

[0032] Exemplary configurations may include having the gas inlet assembly 205 open into a gas supply region 258 partitioned from the first plasma region 215 by faceplate 217 so that the gases/species flow through the holes in the faceplate 217 into the first plasma region 215. Structural and operational features may be selected to prevent significant backflow of plasma from the first plasma region 215 back into the supply region 258, gas inlet assembly 205, and fluid supply system 210. The faceplate 217, or a conductive top portion of the chamber, and

showerhead 225 are shown with an insulating ring 220 located between the features, which allows an AC potential to be applied to the faceplate 217 relative to showerhead 225 and/or ion suppressor 223. The insulating ring 220 may be positioned between the faceplate 217 and the showerhead 225 and/or ion suppressor 223 enabling a capacitively coupled plasma (CCP) to be formed in the first plasma region. A baffle (not shown) may additionally be located in the first plasma region 215, or otherwise coupled with gas inlet assembly 205, to affect the flow of fluid into the region through gas inlet assembly 205.

[0033] The ion suppressor 223 may comprise a plate or other geometry that defines a plurality of apertures throughout the structure that are configured to suppress the migration of ionically-charged species out of the first plasma region 215 while allowing uncharged neutral or radical species to pass through the ion suppressor 223 into an activated gas delivery region between the suppressor and the showerhead. In embodiments, the ion suppressor 223 may comprise a perforated plate with a variety of aperture configurations. These uncharged species may include highly reactive species that are transported with less reactive carrier gas through the apertures. As noted above, the migration of ionic species through the holes may be reduced, and in some instances completely suppressed. Controlling the amount of ionic species passing through the ion suppressor 223 may advantageously provide increased control over the gas mixture brought into contact with the underlying wafer substrate, which in turn may increase control of the deposition and/or etch characteristics of the gas mixture. For example, adjustments in the ion concentration of the gas mixture can significantly alter its etch selectivity, e.g., SiGe_x:SiO_x etch ratios, SiGe_x:Si etch ratios, etc. In alternative embodiments in which deposition is performed, it can also shift the balance of conformal-to-flowable style depositions for dielectric materials.

[0034] The plurality of apertures in the ion suppressor 223 may be configured to control the passage of the activated gas, i.e., the ionic, radical, and/or neutral species, through the ion suppressor 223. For example, the aspect ratio of the holes, or the hole diameter to length, and/or the geometry of the holes may be controlled so that the flow of ionically-charged species in the activated gas passing through the ion suppressor 223 is reduced. The holes in the ion suppressor 223 may include a tapered portion that faces the plasma region 215, and a cylindrical portion that faces the showerhead 225. The cylindrical portion may be shaped and dimensioned to control the flow of ionic species passing to the showerhead 225. An adjustable electrical bias may also be applied to the ion suppressor 223 as an additional means to control the flow of ionic species through the suppressor.

- [0035] The ion suppressor 223 may function to reduce or eliminate the amount of ionically charged species traveling from the plasma generation region to the substrate. Uncharged neutral and radical species may still pass through the openings in the ion suppressor to react with the substrate. It should be noted that the complete elimination of ionically charged species in the reaction region surrounding the substrate may not be performed in embodiments. In certain instances, ionic species are intended to reach the substrate in order to perform the etch and/or deposition process. In these instances, the ion suppressor may help to control the concentration of ionic species in the reaction region at a level that assists the process.
- 10 [0036] Showerhead 225 in combination with ion suppressor 223 may allow a plasma present in first plasma region 215 to avoid directly exciting gases in substrate processing region 233, while still allowing excited species to travel from chamber plasma region 215 into substrate processing region 233. In this way, the chamber may be configured to prevent the plasma from contacting a substrate 255 being etched. This may advantageously protect a variety of intricate structures and films patterned on the substrate, which may be damaged, dislocated, or otherwise warped if directly contacted by a generated plasma. Additionally, when plasma is allowed to contact the substrate or approach the substrate level, the rate at which materials may be etched increase. Accordingly, an exposed region of material may be further protected by maintaining the plasma remotely from the substrate.
- 20 [0037] The processing system may further include a power supply 240 electrically coupled with the processing chamber to provide electric power to the faceplate 217, ion suppressor 223, showerhead 225, and/or pedestal 265 to generate a plasma in the first plasma region 215 or processing region 233. The power supply may be configured to deliver an adjustable amount of power to the chamber depending on the process performed. Such a configuration may allow for a tunable plasma to be used in the processes being performed. Unlike a remote plasma unit, which is often presented with on or off functionality, a tunable plasma may be configured to deliver a specific amount of power to the plasma region 215. This in turn may allow development of particular plasma characteristics such that precursors may be dissociated in specific ways to enhance the etching profiles produced by these precursors.
- 25 [0038] A plasma may be ignited either in chamber plasma region 215 above showerhead 225 or substrate processing region 233 below showerhead 225. Plasma may be present in chamber plasma region 215 to produce the radical precursors from an inflow of, for example,
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a fluorine-containing precursor or other precursor. An AC voltage typically in the radio frequency (RF) range may be applied between the conductive top portion of the processing chamber, such as faceplate 217, and showerhead 225 and/or ion suppressor 223 to ignite a plasma in chamber plasma region 215 during deposition. An RF power supply may generate a high RF frequency of 13.56 MHz but may also generate other frequencies alone or in combination with the 13.56 MHz frequency.

[0039] FIG. 2B shows a detailed view 253 of the features affecting the processing gas distribution through faceplate 217. As shown in FIGS. 2A and 2B, faceplate 217, cooling plate 203, and gas inlet assembly 205 intersect to define a gas supply region 258 into which process gases may be delivered from gas inlet 205. The gases may fill the gas supply region 258 and flow to first plasma region 215 through apertures 259 in faceplate 217. The apertures 259 may be configured to direct flow in a substantially unidirectional manner such that process gases may flow into processing region 233, but may be partially or fully prevented from backflow into the gas supply region 258 after traversing the faceplate 217.

[0040] The gas distribution assemblies such as showerhead 225 for use in the processing chamber section 200 may be referred to as dual channel showerheads (DCSH) and are additionally detailed in the embodiments described in FIG. 3. The dual channel showerhead may provide for etching processes that allow for separation of etchants outside of the processing region 233 to provide limited interaction with chamber components and each other prior to being delivered into the processing region.

[0041] The showerhead 225 may comprise an upper plate 214 and a lower plate 216. The plates may be coupled with one another to define a volume 218 between the plates. The coupling of the plates may be so as to provide first fluid channels 219 through the upper and lower plates, and second fluid channels 221 through the lower plate 216. The formed channels may be configured to provide fluid access from the volume 218 through the lower plate 216 via second fluid channels 221 alone, and the first fluid channels 219 may be fluidly isolated from the volume 218 between the plates and the second fluid channels 221. The volume 218 may be fluidly accessible through a side of the showerhead 225.

[0042] FIG. 3 is a bottom view of a showerhead 325 for use with a processing chamber according to embodiments. Showerhead 325 may correspond with the showerhead 225 shown in FIG. 2A. Through-holes 365, which show a view of first fluid channels 219, may have a plurality of shapes and configurations in order to control and affect the flow of

precursors through the showerhead 225. Small holes 375, which show a view of second fluid channels 221, may be distributed substantially evenly over the surface of the showerhead, even amongst the through-holes 365, and may help to provide more even mixing of the precursors as they exit the showerhead than other configurations.

5 [0043] The chambers discussed previously may be used in performing exemplary methods including etching methods. Turning to **FIG. 4** is shown exemplary operations in a method 400 according to embodiments of the present technology. Prior to the first operation of the method a substrate may be processed in one or more ways before being placed within a processing region of a chamber in which method 400 may be performed. For example,
10 alternating layers of material may be formed on the substrate and then one or more memory holes or trenches may be formed through the alternating layers. The alternating layers may include any number of materials, and may include alternating layers of a silicon-containing material and a silicon-and-germanium-containing material. Although the remaining disclosure will discuss silicon-containing material and silicon-and-germanium-containing
15 material, any other known materials used in these two layers may be substituted for one or more of the layers. One material in the alternating layers, such as the silicon-and-germanium-containing material may be recessed. In the recess, an oxygen-containing material may be formed followed by a spacer material. Further, an epitaxial material, such as a second silicon-and-germanium-containing material, may be formed in the one or more
20 memory holes or trenches. Some or all of these operations may be performed in chambers or system tools as previously described, or may be performed in different chambers on the same system tool, which may include the chamber in which the operations of method 400 are performed.

[0044] The method 400 may include providing a treatment precursor, such as a pre-
25 treatment precursor or pre-etching precursor, to a semiconductor processing chamber at optional operation 405. In some embodiments, an inert precursor may be provided with the treatment precursor. An exemplary chamber may be chamber 200 previously described, which may include one or both of the RPS unit 201 or first plasma region 215. A plasma may be formed at optional operation 410, which may form plasma effluents of the treatment
30 precursor. The substrate may be contacted with the treatment precursor or, if formed, the plasma effluents of the treatment precursor at optional operation 415. The contacting at optional operation 415 may remove a native oxide that is present on the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-

containing material on the substrate. The operations to develop the structure may include removing or etching one or more materials. To increase selectivity during the removal or etching, the method 400 may include providing an oxygen-containing precursor to the processing region at operation 420, optionally forming plasma effluents of the oxygen-containing precursor at optional operation 425, and contacting the substrate with the oxygen-containing precursor, or plasma effluents thereof, at operation 430. The contacting at operation 430 may oxidize at least a portion of the second layer of silicon-and-germanium-containing material, which may be epitaxial silicon-and-germanium-containing material. Subsequent an amount of oxidation, method 400 may include providing an etchant precursor to the processing region at operation 435, optionally forming plasma effluents of the etchant precursor at optional operation 440, and contacting the substrate with the etchant precursor at operation 445. The contacting at operation 445 may selectively etch the first layer of silicon-and-germanium-containing material, which may be a silicon-and-germanium-containing material nanowire in a GAA transistor.

15 **[0045]** Method 400 may involve selectively oxidizing one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. The one silicon-and-germanium-containing material may be selectively oxidized to a greater degree relative to another silicon-and-germanium-containing material due to the germanium concentrations of the materials. The silicon-and-germanium-containing material to be oxidized may be characterized by a higher germanium concentration, and therefore may preferentially oxidize over the other silicon-and-germanium-containing material. By selectively oxidizing one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material, a subsequent etch operation may selectively remove the silicon-and-germanium-containing material that remains unoxidized or less oxidized than the other silicon-and-germanium-containing material. Accordingly, in GAA transistors, for example, the lower germanium-containing silicon-and-germanium-containing nanowire may be etched or released selectively to the higher germanium-containing silicon-and-germanium-containing epitaxial material. The method 400 may allow for the selective oxidation and subsequent selective removal of one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material.

[0046] Precursors provided to the processing region in the method 400 at optional operation 405 may include a treatment precursor, such as a pre-treatment precursor or pre-etching precursor, as well as optionally an inert precursor. An exemplary treatment precursor

may be a hydrogen-containing precursor, a nitrogen-containing precursor, or combinations thereof, which may be flowed into the processing region. The hydrogen-containing precursor may be or include, for example, molecular hydrogen (H₂), ammonia (NH₃), or any other hydrogen-containing precursor used or useful in semiconductor processing. The nitrogen-
5 containing precursor may be or include, for example, molecular nitrogen (N₂), ammonia (NH₃), or any other nitrogen-containing precursor used or useful in semiconductor processing. The treatment precursor may be provided with an inert precursor in some embodiments. The inert precursor may be or include, for example, argon, helium, xenon, or other noble, inert, or useful precursors. The inert precursor may be used to dilute the
10 treatment precursor or to assist in distributing the treatment precursor throughout the processing region.

[0047] If formed at optional operation 410, the plasma effluents of the treatment precursor and the inert precursor, if present, may be generated at a plasma power of less than or about 5,000 W, and may be generated at less than or about 4,750 W, less than or about 4,500 W,
15 less than or about 4,250 W, less than or about 4,000 W, less than or about 3,750 W, less than or about 3,500 W, less than or about 3,250 W, less than or about 3,000 W, less than or about 2,750 W, less than or about 2,500 W, less than or about 2,250 W, less than or about 2,000 W, less than or about 1,750 W, less than or about 1,500 W, less than or about 1,250 W, less than or about 1,000 W, less than or about 750 W, less than or about 500 W, less than or about 250
20 W, or less.

[0048] The substrate may be contacted with the plasma effluents of the treatment precursor at optional operation 415 for a sufficient period of time to remove native oxide on the silicon-and-germanium-containing material. In embodiments, the period of time may be greater than or about 3 seconds, greater than or about 5 seconds, greater than or about 10 seconds, greater
25 than or about 20 seconds, greater than or about 30 seconds, greater than or about 40 seconds, greater than or about 50 seconds, greater than or about 1 minute, greater than or about 2 minutes, greater than or about 3 minutes, greater than or about 5 minutes, or higher. The period of time may be sufficient to remove greater than or about 85% of the native oxide from the silicon-and-germanium-containing material, and greater than or about 90%, greater
30 than or about 95%, greater than or about 97%, greater than or about 99%, greater than or about 99.9%, or higher, or all of the native oxide may be removed from the silicon-and-germanium-containing material.

[0049] In embodiments, method 400 may include providing an oxygen-containing precursor to the processing region of the semiconductor processing chamber at operation 420. In some embodiments, an inert precursor may be provided with the oxygen-containing precursor. The oxygen-containing precursor may be or include, for example, molecular oxygen (O₂), steam (H₂O), hydrogen peroxide (H₂O₂), or any other oxygen-containing precursor used or useful in semiconductor processing. The inert precursor may be or include, for example, argon, helium, xenon, or other noble, inert, or useful precursors. The inert precursor may be used to dilute the oxygen-containing precursor, which may further reduce oxidation rates to control the oxidation and the selectivity of the oxidation, or to assist in distributing the oxygen-containing precursor throughout the processing region. Additionally, a flow rate ratio of the oxygen-containing precursor and, if present, the inert precursor may be adjusted to tune oxidative effect of the oxygen-containing precursor and/or oxidation selectivity.

[0050] A flow rate of the oxygen-containing precursor and the inert precursor, if present, may be sufficient to selectively oxidize one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. In embodiments, a flow rate of the oxygen-containing precursor to the processing region may be greater than or about 1 sccm, and may be greater than or about 10 sccm, greater than or about 50 sccm, greater than or about 100 sccm, greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 1,000 sccm, greater than or about 1,500 sccm, greater than or about 2,000 sccm, greater than or about 2,500 sccm, greater than or about 3,000 sccm, greater than or about 3,500 sccm, greater than or about 4,000 sccm, or higher. Additionally, a flow rate of the inert precursor, which may dilute and/or distribute the oxygen-containing precursor or plasma effluents thereof may be greater than or about 100 sccm, and may be greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 750 sccm, greater than or about 1,000 sccm, greater than or about 2,500 sccm, greater than or about 5,000 sccm, greater than or about 7,500 sccm, greater than or about 10,000 sccm, or higher.

[0051] In some embodiments, plasma effluents of the oxygen-containing precursor may be generated at optional operation 425. As discussed, the plasma effluents may be generated in the processing region. However, it is contemplated that plasma effluents may not be formed of the oxygen-containing precursor and a plasma-free or thermal oxidation may be performed. For example, when the oxygen-containing precursor is O₂ or H₂O, the plasma effluents may oxidize all silicon-and-germanium-containing materials on the substrate.

Accordingly, a subsequent etch to remove one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material may not be able to etch any of the oxidized silicon-and-germanium-containing material. In embodiments where plasma effluents of the oxygen-containing precursor are formed, the plasma effluents of the oxygen-containing precursor and the inert precursor, if present, may be generated at a plasma power of less than or about 5,000 W, and may be generated at less than or about 4,750 W, less than or about 4,500 W, less than or about 4,250 W, less than or about 4,000 W, less than or about 3,750 W, less than or about 3,500 W, less than or about 3,250 W, less than or about 3,000 W, less than or about 2,750 W, less than or about 2,500 W, less than or about 2,250 W, less than or about 2,000 W, less than or about 1,750 W, less than or about 1,500 W, less than or about 1,250 W, less than or about 1,000 W, less than or about 750 W, less than or about 500 W, less than or about 250 W, or less. Compared to the pre-treatment precursor, plasma effluents of the oxygen-containing precursor may be generated at a lower plasma power. By generating plasma effluents of the post-treatment at a lower plasma power, oxidation may be better controlled and bombardment/damage to the substrate and materials deposited thereon may be limited.

[0052] Method 400 may include contacting the substrate with the oxygen-containing precursor, or plasma effluents thereof, at operation 430. The contacting may continue for a sufficient period of time to oxidize at least one of the multiple silicon-and-germanium-containing materials on the substrate. In embodiments, the period of time may be greater than or about 3 seconds, greater than or about 5 seconds, greater than or about 10 seconds, greater than or about 20 seconds, greater than or about 30 seconds, greater than or about 40 seconds, greater than or about 50 seconds, greater than or about 1 minute, greater than or about 2 minutes, greater than or about 3 minutes, greater than or about 5 minutes, or higher. Similarly, the period of time may be less than or about 5 minutes, less than or about 3 minutes, less than or about 2 minutes, less than or about 1 minute, less than or about 50 seconds, less than or about 40 seconds, less than or about 30 seconds, less than or about 20 seconds, less than or about 10 seconds, less than or about 5 seconds, less than or about 3 seconds, or less.

[0053] By contacting the substrate with the oxygen-containing precursor, germanium and/or silicon in silicon-and-germanium-containing material may bond with oxygen to oxidize a portion of the silicon-and-germanium-containing material. Without being bound by any particular theory, it is believed that germanium may more readily bond with oxygen, and

silicon-and-germanium-containing material with a higher germanium concentration may oxidize easier than neighboring silicon-and-germanium-containing material with a lower germanium concentration. Additionally, it is believed Si-Ge bonds in the silicon-and-germanium-containing material may break easier than Si-Si bonds in neighboring silicon-containing material, and the silicon-and-germanium-containing material may oxidize easier than neighboring silicon-containing material. Additionally, by operating at temperature and/or pressure ranges discussed below, the silicon-and-germanium-containing material with a higher germanium concentration may be more readily oxidized.

[0054] At operation 435, method 400 may include providing an etchant precursor to the processing region of the semiconductor processing chamber. In some embodiments, an inert precursor may be provided with the etchant precursor. The etchant precursor may be a halogen-containing precursor or any other precursor able to etch silicon-and-germanium-containing material. For example, the etchant precursor may be or include, for example, diatomic fluorine (F₂), nitrogen trifluoride (NF₃), hydrogen fluoride (HF), or any other fluorine-containing precursor used or useful in semiconductor processing. The inert precursor may be or include, for example, argon, helium, xenon, or other noble, inert, or useful precursors. The inert precursor may be used to dilute the etchant precursor, which may further reduce etching rates to control the etch and the selectivity of the etch, or to assist in distributing the etchant precursor throughout the processing region. Additionally, a flow rate ratio of the etchant precursor and, if present, the inert precursor may be adjusted to tune etching selectivity.

[0055] A flow rate of the etchant precursor and the inert precursor, if present, may be sufficient to selectively etch one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. In embodiments, a flow rate of the etchant precursor to the processing region may be greater than or about 1 sccm, and may be greater than or about 10 sccm, greater than or about 50 sccm, greater than or about 100 sccm, greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 1,000 sccm, greater than or about 1,500 sccm, greater than or about 2,000 sccm, greater than or about 2,500 sccm, greater than or about 3,000 sccm, greater than or about 3,500 sccm, greater than or about 4,000 sccm, or higher. Additionally, a flow rate of the inert precursor, which may dilute and/or distribute the etchant precursor or plasma effluents thereof may be greater than or about 100 sccm, and may be greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 750 sccm, greater than or about 1,000 sccm, greater than or about

2,500 sccm, greater than or about 5,000 sccm, greater than or about 7,500 sccm, greater than or about 10,000 sccm, or higher.

[0056] In some embodiments, plasma effluents of the etchant precursor may be generated at optional operation 440. As discussed, the plasma effluents may be generated in the processing region. In embodiments plasma effluents of the oxygen-containing precursor and the inert precursor, if present, may be generated at a plasma power of less than or about 5,000 W, and may be generated at less than or about 4,750 W, less than or about 4,500 W, less than or about 4,250 W, less than or about 4,000 W, less than or about 3,750 W, less than or about 3,500 W, less than or about 3,250 W, less than or about 3,000 W, less than or about 2,750 W, less than or about 2,500 W, less than or about 2,250 W, less than or about 2,000 W, less than or about 1,750 W, less than or about 1,500 W, less than or about 1,250 W, less than or about 1,000 W, less than or about 750 W, less than or about 500 W, less than or about 250 W, or less.

[0057] Method 400 may include contacting the substrate with the etchant precursor, or plasma effluents thereof, at operation 445. The contacting may continue for a sufficient period of time to etch at least one of the multiple silicon-and-germanium-containing materials on the substrate. In embodiments, the period of time may be greater than or about 3 seconds, greater than or about 5 seconds, greater than or about 10 seconds, greater than or about 20 seconds, greater than or about 30 seconds, greater than or about 40 seconds, greater than or about 50 seconds, greater than or about 1 minute, greater than or about 2 minutes, greater than or about 3 minutes, greater than or about 5 minutes, or higher. Similarly, the period of time may be less than or about 5 minutes, less than or about 3 minutes, less than or about 2 minutes, less than or about 1 minute, less than or about 50 seconds, less than or about 40 seconds, less than or about 30 seconds, less than or about 20 seconds, less than or about 10 seconds, less than or about 5 seconds, less than or about 3 seconds, or less.

[0058] By contacting the substrate with the etchant precursor, the non-oxidized silicon-and-germanium-containing material may be selectively removed relative to other materials on the substrate, including the oxidized silicon-and-germanium-containing material. Without being bound by any particular theory, it is believed that the oxidized silicon-and-germanium-containing material may be more resistant to the etchant precursor compared to the non-oxidized silicon-and-germanium-containing material. Therefore, the non-oxidized silicon-and-germanium-containing material may be selectively removed compared to the oxidized

silicon-and-germanium-containing material. As such, in GAA transistors, the non-oxidized and lower germanium concentration silicon-and-germanium-containing material, such as SiGe nanowires, may be selectively removed relative to the oxidized and higher germanium concentration silicon-and-germanium-containing material, such as epitaxial SiGe material.

5 [0059] In embodiments, operations 405-415 may be performed in the same semiconductor processing chamber as operations 420-430, or the substrate may be transferred to a second processing region of a second semiconductor processing chamber to selectively oxidize one silicon-and-germanium-containing material on the substrate at operations 420-430. However, the second semiconductor processing chamber may be on the same processing system or
10 mainframe, such as processing system 100, as the semiconductor processing chamber used during operations 405-415. Additionally, operations 430-445 may be performed in the same semiconductor processing chamber as operations 405-415 and/or operations 420-430, or the substrate may be transferred to a third processing region of a third semiconductor processing chamber to selectively etch one silicon-and-germanium-containing material on the substrate
15 at operations 435-445. However, the third semiconductor processing chamber may be on the same processing system or mainframe, such as processing system 100, as the semiconductor processing chamber used during operations 405-415 and/or operations 420-430. Accordingly, contacting the substrate with the pre-treatment precursor, contacting the substrate with the oxygen-containing precursor, and contacting the substrate with the etchant
20 precursor may be performed on a single mainframe.

[0060] Process conditions may also impact the operations performed in method 400 as well as other etching methods according to the present technology. Each of the operations of method 400 may be performed during a constant temperature in embodiments, while in some embodiments the temperature may be adjusted during different operations. For example, the
25 substrate, pedestal, or chamber temperature may be maintained between about 25 °C and about 500 °C in embodiments. The temperature may also be maintained at less than or about 480 °C, less than or about 460 °C, less than or about 440 °C, less than or about 420 °C, less than or about 400 °C, less than or about 380 °C, less than or about 360 °C, less than or about 350 °C, less than or about 340 °C, less than or about 330 °C, less than or about 320 °C, less
30 than or about 310 °C, less than or about 300 °C, less than or about 280 °C, less than or about 260 °C, less than or about 240 °C, less than or about 220 °C, less than or about 200 °C, or less. In embodiments, the temperature may also be maintained at greater than or about or about 100 °C, greater than or about or about 120 °C, greater than or about or about 140 °C,

greater than or about or about 150 °C, greater than or about or about 160 °C, greater than or about or about 180 °C, greater than or about or about 200 °C, greater than or about or about 220 °C, greater than or about or about 240 °C, greater than or about or about 260 °C, greater than or about or about 280 °C, greater than or about or about 300 °C, greater than or about or about 320 °C, greater than or about or about 340 °C, greater than or about or about 360 °C, greater than or about or about 380 °C, greater than or about or about 400 °C, greater than or about or about 420 °C, greater than or about or about 440 °C, greater than or about or about 460 °C, greater than or about or about 480 °C, greater than or about or about 500 °C, or higher. Temperature may affect the quality of the oxidation process, and higher temperature may allow for better oxidation of the silicon-and-germanium-containing material. Higher temperature may also produce higher reactivity between the etchant precursor and the silicon-and-germanium-containing material. Similarly, lower temperatures may slow the removal of the silicon-and-germanium-containing material due to poor reactivity. Thus, in some embodiments, maintaining a temperature at greater than or about 150 °C may provide better oxidation and/or increased removal of the silicon-and-germanium-containing material.

[0061] The pressure within the chamber may also affect the operations performed, and in embodiments the pressure within the semiconductor processing chamber may be maintained at greater than about 1 Torr, greater than or about 2 Torr, greater than or about 3 Torr, greater than or about 4 Torr, greater than or about 5 Torr, greater than or about 7.5 Torr, greater than or about 10 Torr, greater than or about 12.5 Torr, greater than or about 15 Torr, greater or about 17.5 Torr, greater than or about 20 Torr, or more. Each of the operations of method 400 may be performed during a constant pressure in embodiments, while in some embodiments the pressure may be adjusted during different operations. In embodiments a pressure greater or about 1 Torr may result in stronger oxidation of one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. Accordingly, a lower pressure may result in weaker oxidation and, therefore, may require additional time for sufficient or desired oxidation. However, to maintain precise selectivity of the oxidation, the pressure within the chamber may also be maintained at less than or about 30 Torr, and may be maintained at less than or about 28 Torr, less than or about 26 Torr, less than or about 24 Torr, less than or about 22 Torr, less than or about 20 Torr, less than or about 18 Torr, less than or about 16 Torr, less than or 14 Torr, less than or about 12 Torr, less than or about 10 Torr, or less.

[0062] The contacting may etch one layer of silicon-and-germanium-containing material relative to another layer of silicon-and-germanium-containing material at a selectivity of greater than or about 40:1. For example, the non-oxidized layer of silicon-and-germanium-containing material may be etched at a selectivity of greater than or about 42:1 relative to the oxidized layer of silicon-and-germanium-containing material, such as greater than or about 44:1, greater than or about 46:1, greater than or about 48:1, greater than or about 50:1, greater than or about 52:1, greater than or about 54:1, greater than or about 56:1, greater than 58:1, or more.

[0063] Turning to **FIGS. 5A-5C** are shown cross-sectional views of structure 500 being processed according to embodiments of the present technology. As illustrated in **FIG. 5A**, structure 500 may include a substrate 505 that may have a plurality of stacked layers overlying the substrate, which may be silicon-containing material, silicon-and-germanium-containing material, or other substrate materials. The alternating layers of material may include materials suitable for GAA transistors, such as silicon-containing material 510 alternating with first silicon-and-germanium-containing material 515. The first silicon-and-germanium-containing material 515 may be or include material that will be recessed and/or removed to produce nanowires/nanosheets in GAA transistors. Although illustrated with only 7 layers of material, exemplary structures may include any number of layers. Memory holes or trenches may be defined through the stacked structure to the level of substrate 505. Memory holes or trenches may be defined by sidewalls that may be composed of the alternating layers of silicon-containing material 510 and first silicon-and-germanium-containing material 515. After recessing the first silicon-and-germanium-containing material 515, an oxygen-containing material 520 and a spacer material 525 may be formed in the recesses. As illustrated in **FIG. 5A**, the oxygen-containing material 520 may line the silicon-containing material 510 and the first silicon-and-germanium-containing material 515 defining the recess. The spacer material 525 may then be deposited in the remaining area where the first silicon-and-germanium-containing material 515 was previously. A second silicon-and-germanium-containing material 530 may then be formed in the memory holes or trenches defined through the stacked structure.

[0064] In embodiments, the second silicon-and-germanium-containing material 530, which may be epitaxially grown, may be characterized by a germanium concentration greater than the first silicon-and-germanium-containing material 515. For example, the first silicon-and-germanium-containing material 515 may be characterized by a germanium concentration of

less than or about 35 at.%, and may be characterized by a germanium concentration of less than or about 32.5 at.%, less than or about 30 at.%, less than or about 27.5 at.%, less than or about 25 at.%, less than or about 22.5 at.%, less than or about 20 at.%, less than or about 17.5 at.%, less than or about 15 at.%, or less. Conversely, the second silicon-and-germanium-containing material 530 may be characterized by a germanium concentration greater than or about 35 at.%, and may be characterized by a germanium concentration of greater than or about 37.5 at.%, greater than or about 40 at.%, greater than or about 42.5 at.%, greater than or about 45 at.%, greater than or about 47.5 at.%, greater than or about 50 at.%, greater than or about 52.5 at.%, greater than or about 55 at.%, greater than or about 57.5 at.%, greater than or about 60 at.%, or more. Additionally, the second silicon-and-germanium-containing material 530 may be a doped material. In embodiments, the second silicon-and-germanium-containing material 530 may be doped with, for example, boron.

[0065] FIG. 5B may illustrate the structure after some operations of methods according to the present technology have been performed, such as discussed with respect to FIG. 4 above. Contacting the substrate with the oxygen-containing precursor, such as at operation 430 of method 400, may oxidize at least a portion of the second layer of silicon-and-germanium-containing material 535. The portion of the second layer of silicon-and-germanium-containing material 535 may be an oxidized silicon-and-germanium-containing material. The portion of the second layer of silicon-and-germanium-containing material 535 may be in contact with the oxygen-containing material 520 and/or the spacer material 525. As previously discussed with regard to methods according to the present technology, such as discussed with respect to FIG. 4 above, the second layer of silicon-and-germanium-containing material 530 may selectively oxidize relative to the first layer of silicon-and-germanium-containing material 515 due to the increased germanium concentration of the second layer of silicon-and-germanium-containing material 530. The spacer material 525 may be porous. Accordingly, during a subsequent etch to remove the first silicon-and-germanium-containing material 515, etchant species may penetrate the spacer material 525 and reach the second layer of silicon-and-germanium-containing material 530. Without the portion of the second layer of silicon-and-germanium-containing material 535 blocking the etchant species, some of the second layer of silicon-and-germanium-containing material 530 may be etched.

[0066] FIG. 5C illustrates the structure after further operations of methods according to the present technology have been performed, such as discussed with respect to FIG. 4 above. An

etching operation may be performed to remove the silicon-and-germanium-containing material 515. The etching may remove the first silicon-and-germanium-containing material 515 to form nanowires/nanosheets of the silicon-containing material 510 useful in GAA applications. Structure 500 may show minimal or zero etching of the second layer of silicon-and-germanium-containing material 530 due to the selective oxidation of the portion of the second layer of silicon-and-germanium-containing material 535.

[0067] In the preceding description, for the purposes of explanation, numerous details have been set forth in order to provide an understanding of various embodiments of the present technology. It will be apparent to one skilled in the art, however, that certain embodiments may be practiced without some of these details, or with additional details.

[0068] Having disclosed several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the embodiments. Additionally, a number of well-known processes and elements have not been described in order to avoid unnecessarily obscuring the present technology. Accordingly, the above description should not be taken as limiting the scope of the technology. Additionally, methods or processes may be described as sequential or in steps, but it is to be understood that the operations may be performed concurrently, or in different orders than listed.

[0069] Where a range of values is provided, it is understood that each intervening value, to the smallest fraction of the unit of the lower limit, unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Any narrower range between any stated values or unstated intervening values in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of those smaller ranges may independently be included or excluded in the range, and each range where either, neither, or both limits are included in the smaller ranges is also encompassed within the technology, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

[0070] As used herein and in the appended claims, the singular forms “a”, “an”, and “the” include plural references unless the context clearly dictates otherwise. Thus, for example, reference to “a precursor” includes a plurality of such precursors, and reference to “the

material” includes reference to one or more materials and equivalents thereof known to those skilled in the art, and so forth.

[0071] Also, the words “comprise(s)”, “comprising”, “contain(s)”, “containing”, “include(s)”, and “including”, when used in this specification and in the following claims, are
5 intended to specify the presence of stated features, integers, components, or operations, but they do not preclude the presence or addition of one or more other features, integers, components, operations, acts, or groups.

CLAIMS:

1. A semiconductor processing method comprising:
providing a pre-treatment precursor to a processing region of a semiconductor processing chamber, wherein a substrate is housed within the processing region, wherein a
5 first layer of silicon-and-germanium-containing material and a second layer of silicon-and-germanium-containing material are disposed on the substrate, and wherein a native oxide is present on the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material;
contacting the substrate with the pre-treatment precursor, wherein the
10 contacting removes the native oxide from the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material;
providing an oxygen-containing precursor to the processing region;
contacting the substrate with the oxygen-containing precursor, wherein the contacting oxidizes at least a portion of the second layer of silicon-and-germanium-
15 containing material;
providing an etchant precursor to the processing region; and
contacting the substrate with the etchant precursor, wherein the contacting selectively etches the first layer of silicon-and-germanium-containing material.
2. The semiconductor processing method of claim 1, wherein:
20 the first layer of silicon-and-germanium-containing material is characterized by a first germanium concentration;
the second layer of silicon-and-germanium-containing material is characterized by a second germanium concentration; and
the first germanium concentration is less than the second germanium
25 concentration.
3. The semiconductor processing method of claim 1, wherein the pre-treatment precursor comprises a hydrogen-containing precursor or a nitrogen-containing precursor.
4. The semiconductor processing method of claim 3, wherein:
30 the hydrogen-containing precursor comprises diatomic hydrogen (H₂) or ammonia (NH₃); and

the nitrogen-containing precursor comprises diatomic nitrogen (N_2) or NH_3 .

5. The semiconductor processing method of claim 1, further comprising:
forming plasma effluents of the pre-treatment precursor.

6. The semiconductor processing method of claim 1, wherein the oxygen-
5 containing precursor comprises diatomic oxygen (O_2) or steam (H_2O).

7. The semiconductor processing method of claim 1, further comprising:
forming plasma effluents of the oxygen-containing precursor.

8. The semiconductor processing method of claim 1, wherein a pressure
in the processing region is maintained at less than or about 30 Torr.

10 9. The semiconductor processing method of claim 1, wherein the
contacting etches the first layer of silicon-and-germanium-containing material relative to the
second layer of silicon-and-germanium-containing material at a selectivity of greater than or
about 40:1.

10. The semiconductor processing method of claim 1, wherein a
15 temperature in the processing region is maintained at greater than or about 150 °C.

11. The semiconductor processing method of claim 1, wherein contacting
the substrate with the pre-treatment precursor, contacting the substrate with the oxygen-
containing precursor, and contacting the substrate with the etchant precursor is performed on
a single mainframe.

20 12. A semiconductor processing method comprising:
providing an oxygen-containing precursor to a processing region of a
semiconductor processing chamber, wherein a substrate is housed within the processing
region, wherein a first layer of silicon-and-germanium-containing material and a second layer
of silicon-and-germanium-containing material are disposed on the substrate, and wherein the
25 first layer of silicon-and-germanium-containing material is characterized by a lesser
germanium concentration than the second layer of silicon-and-germanium-containing
material;

contacting the substrate with the oxygen-containing precursor, wherein the contacting oxidizes at least a portion of the second layer of silicon-and-germanium-containing material;

providing a fluorine-containing precursor to the processing region; and

5 contacting the substrate with the fluorine-containing precursor, wherein the contacting etches the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material at a selectivity of greater than or about 40:1.

13. The semiconductor processing method of claim 12, wherein the first
10 layer of silicon-and-germanium-containing material is characterized by a germanium concentration of less than or about 35 at. %.

14. The semiconductor processing method of claim 12, wherein the second layer of silicon-and-germanium-containing material comprises a doped silicon-and-germanium-containing material.

15 15. The semiconductor processing method of claim 12, wherein the oxygen-containing precursor comprises diatomic oxygen (O₂) or steam (H₂O).

16. The semiconductor processing method of claim 15, further comprising: forming plasma effluents of H₂O.

17. The semiconductor processing method of claim 12, wherein a native
20 oxide is present on the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material, the method further comprising:

providing a pre-treatment precursor to the processing region; and

 contacting the substrate with the pre-treatment precursor, wherein the contacting removes the native oxide from the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing
25 material.

18. A semiconductor processing method comprising:

 providing a hydrogen-containing precursor or a nitrogen-containing precursor to a processing region of a semiconductor processing chamber, wherein a substrate is housed
30 within the processing region, wherein a first layer of silicon-and-germanium-containing

material and a second layer of silicon-and-germanium-containing material are disposed on the substrate, wherein the first layer of silicon-and-germanium-containing material is characterized by a lesser germanium concentration than the second layer of silicon-and-germanium-containing material, and wherein a native oxide is present on the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material;

contacting the substrate with the hydrogen-containing precursor or the nitrogen-containing precursor, wherein the contacting removes the native oxide from the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material;

providing an oxygen-containing precursor to the processing region, wherein the oxygen-containing precursor comprises diatomic oxygen (O_2) or steam (H_2O);

contacting the substrate with the oxygen-containing precursor, wherein the contacting oxidizes at least a portion of the second layer of silicon-and-germanium-containing material;

providing a fluorine-containing precursor to the processing region; and
contacting the substrate with the fluorine-containing precursor, wherein the contacting selectively etches the first layer of silicon-and-germanium-containing material.

19. The semiconductor processing method of claim 18, wherein a temperature in the processing region is maintained at greater than or about 200 °C.

20. The semiconductor processing method of claim 18, wherein contacting the substrate with the fluorine-containing precursor etches the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material at a selectivity of greater than or about 50:1.

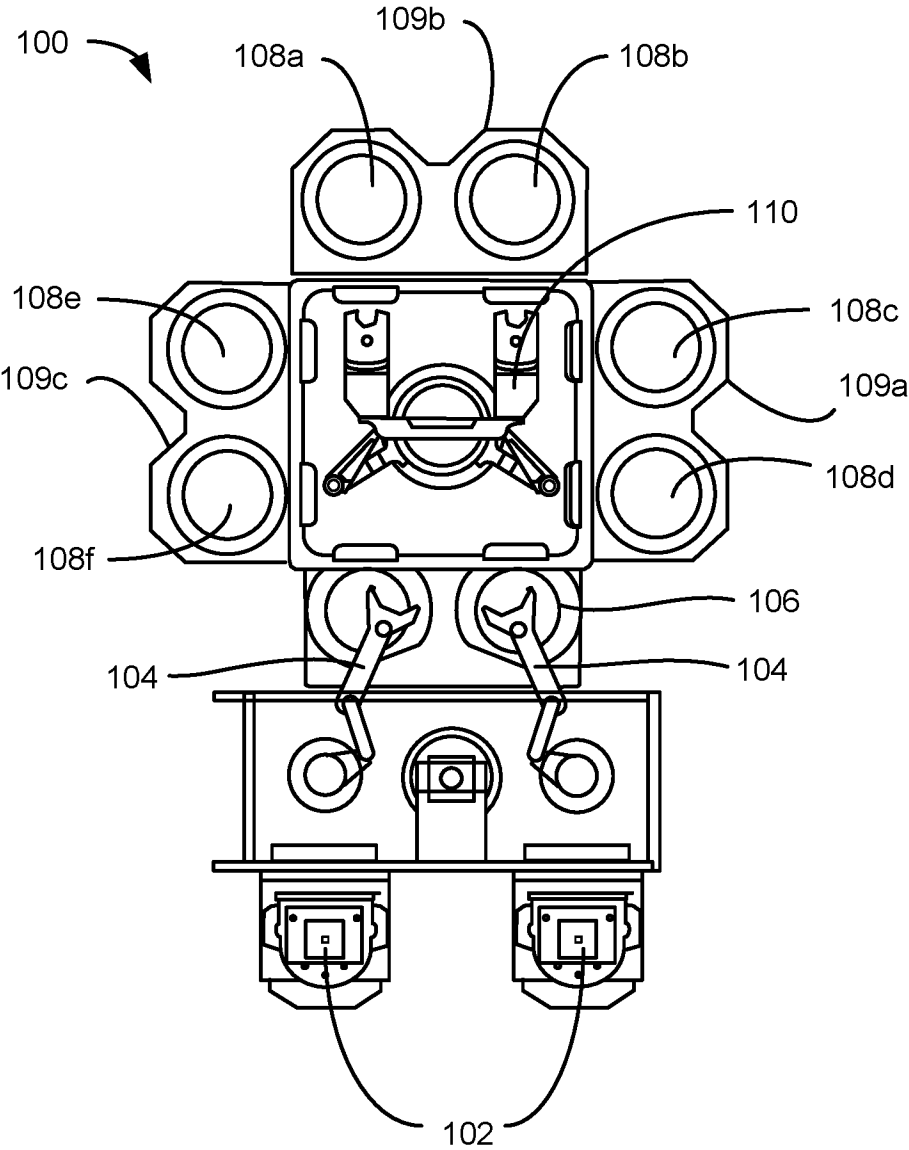
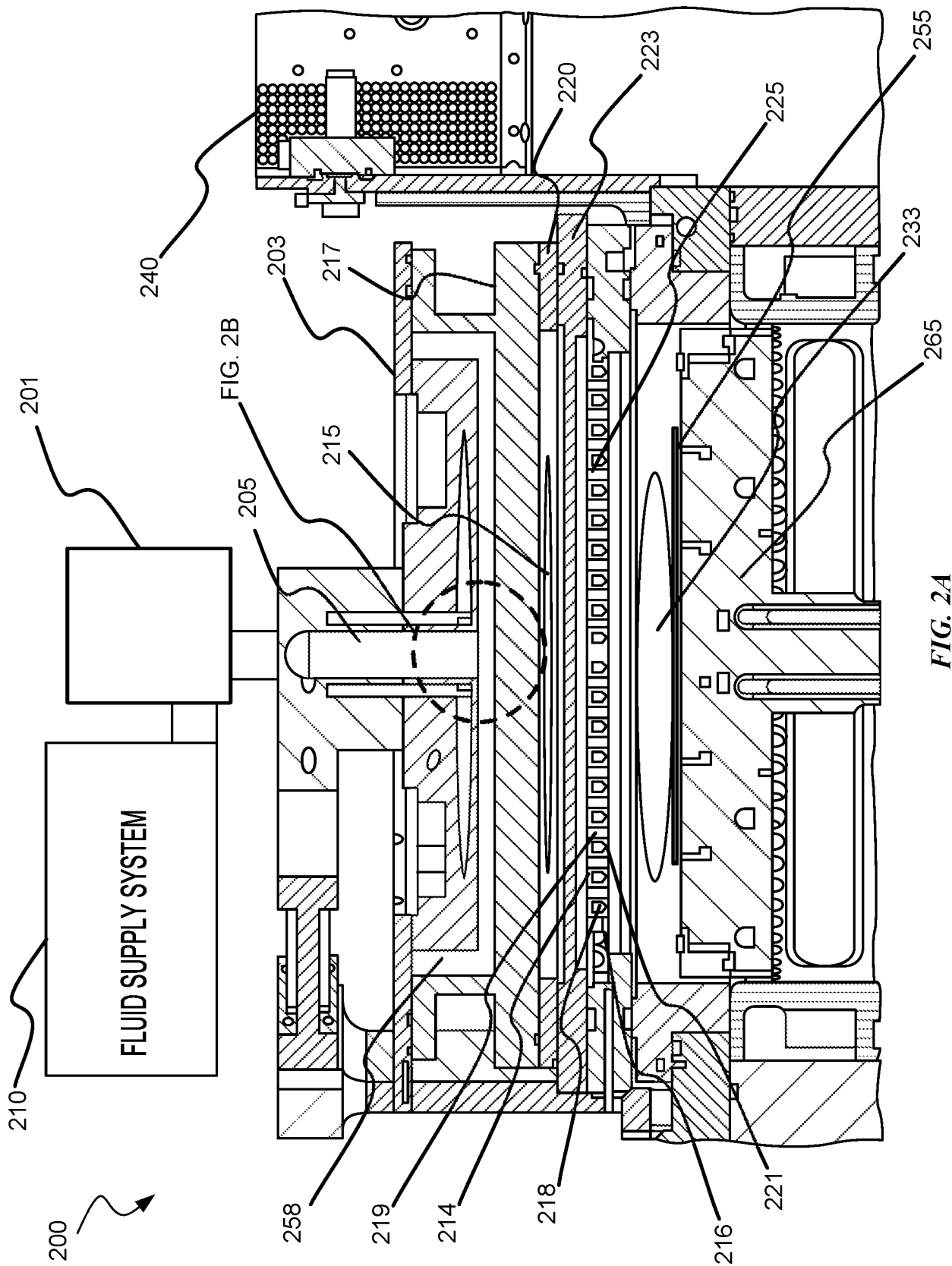


FIG. 1



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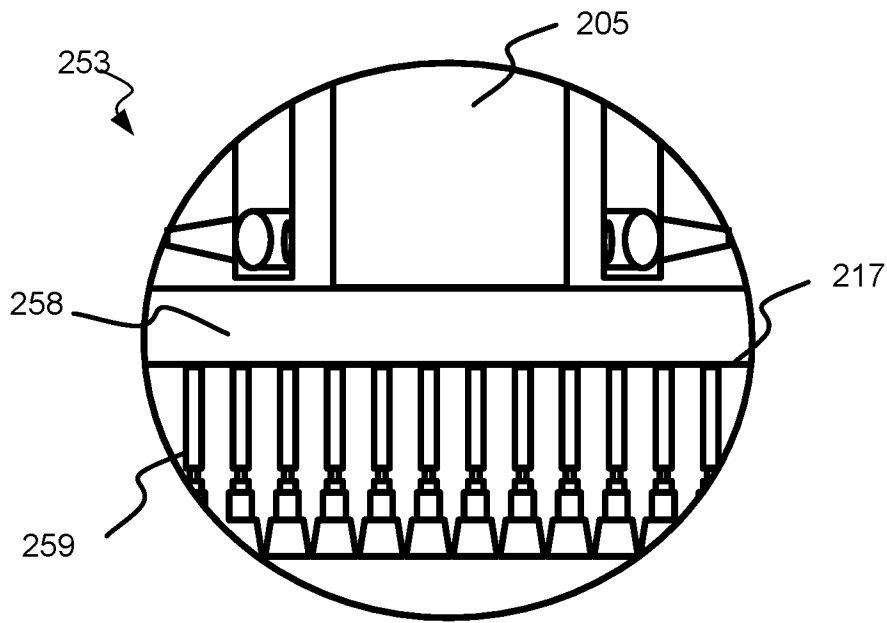


FIG. 2B

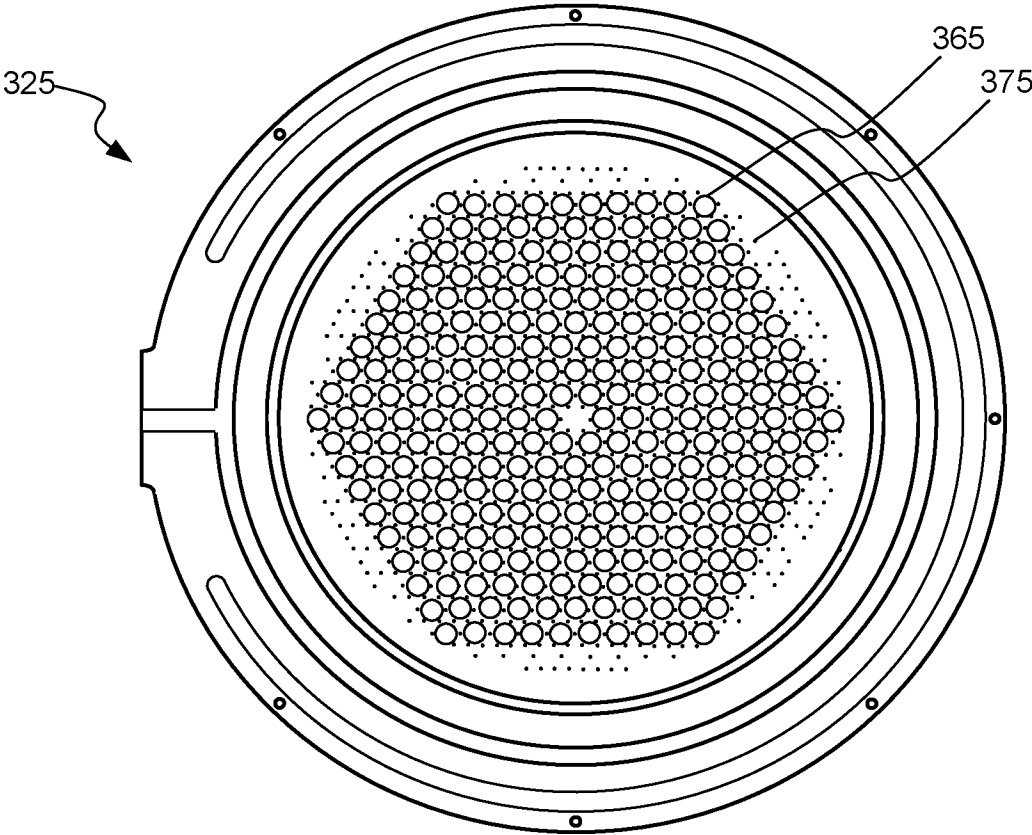


FIG. 3

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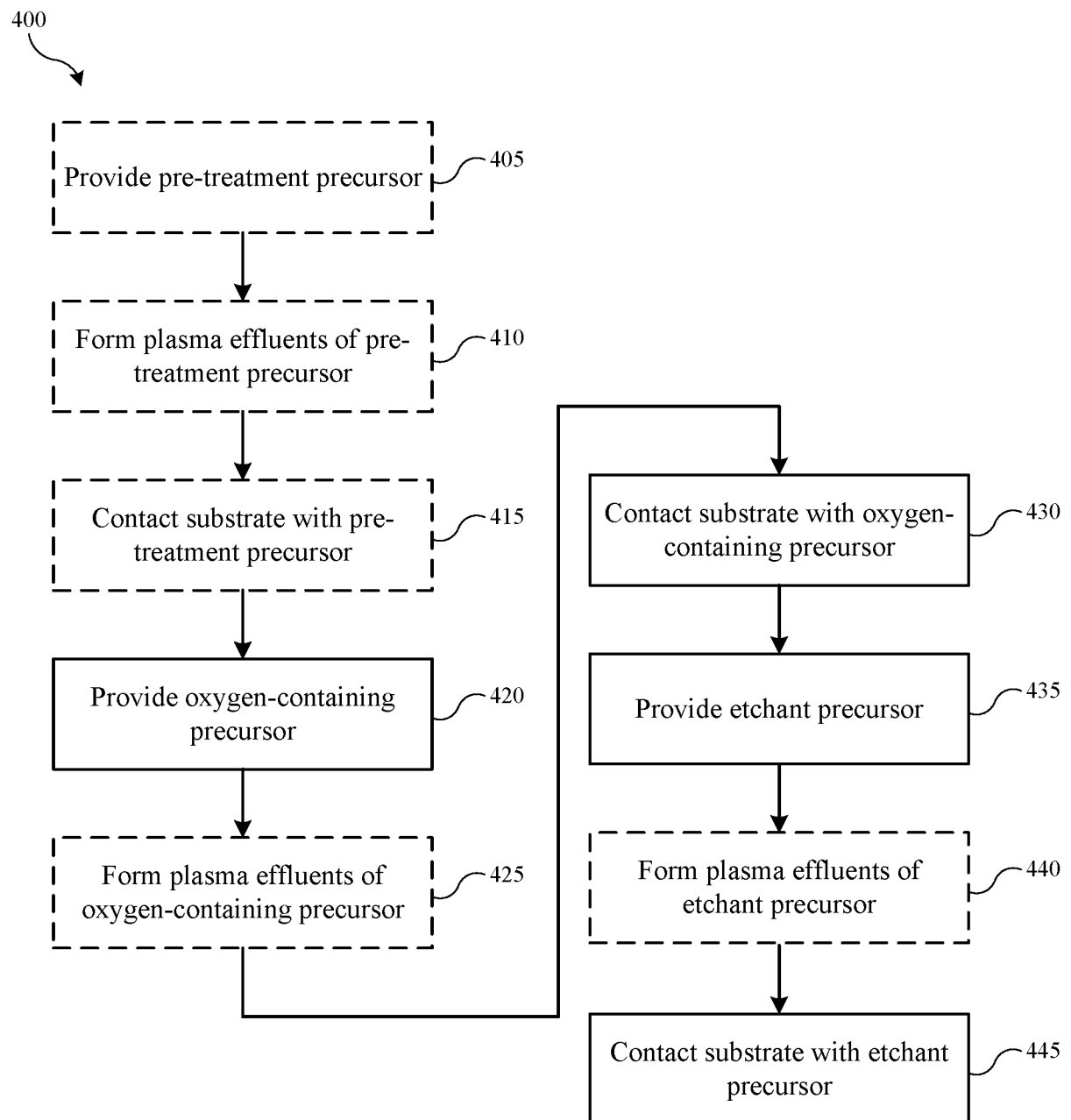
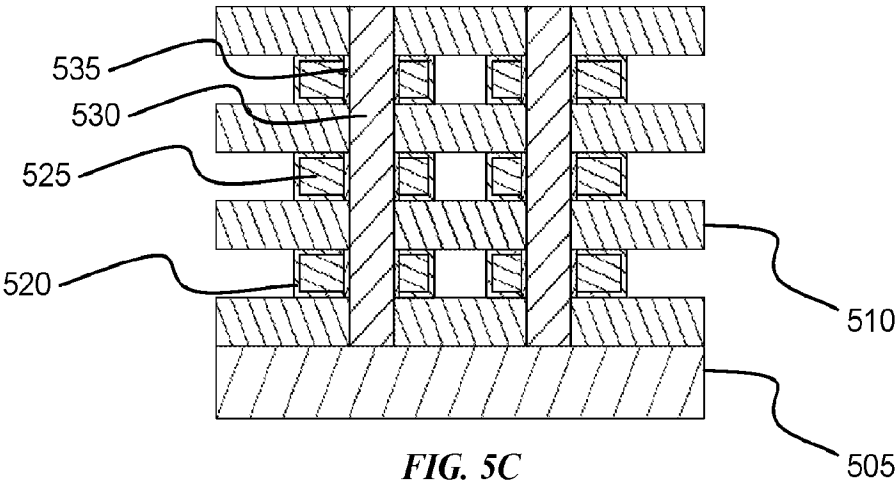
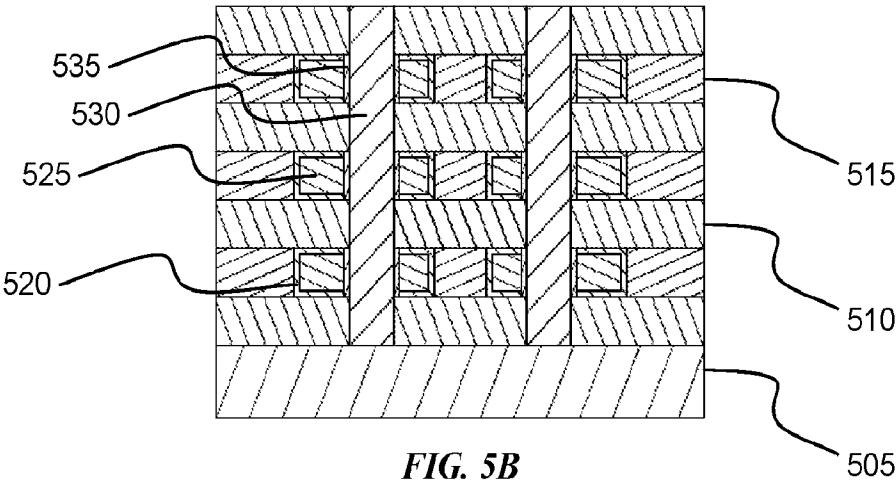
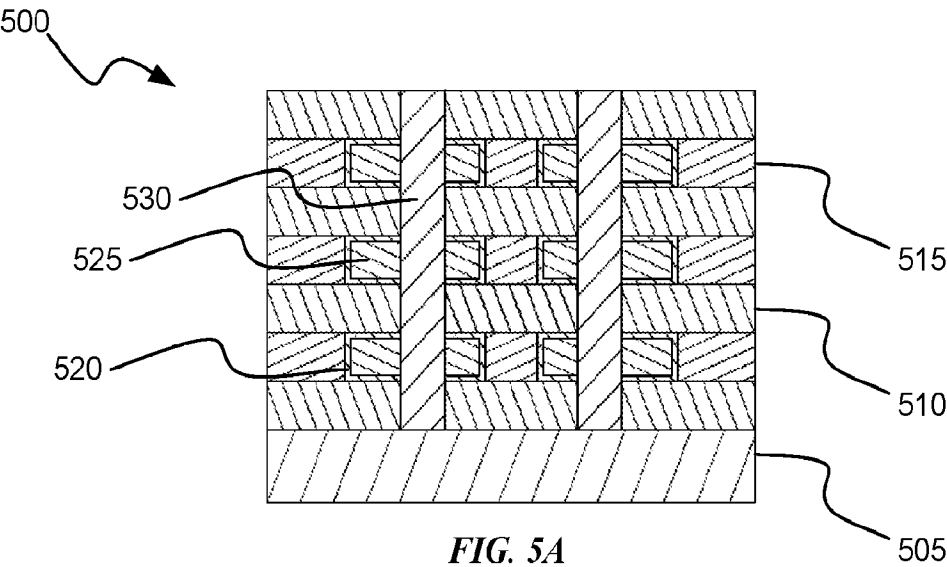


FIG. 4



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2023/085979

A. CLASSIFICATION OF SUBJECT MATTER H01L 21/3065(2006.01)i; H01L 21/311(2006.01)i; H01L 21/02(2006.01)i; H01L 21/67(2006.01)i According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L 21/3065(2006.01); H01J 37/32(2006.01); H01L 21/02(2006.01); H01L 21/302(2006.01); H01L 21/311(2006.01) Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Korean utility models and applications for utility models Japanese utility models and applications for utility models Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) eKOMPASS(KIPO internal) & Keywords: selectively etching, silicon and germanium containing material, germanium concentration, oxidation		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2020-0098575 A1 (TOKYO ELECTRON LIMITED) 26 March 2020 (2020-03-26) See paragraphs [0029]-[0033] and figures 1-3.	1-20
A	US 2019-0228981 A1 (TOKYO ELECTRON LIMITED) 25 July 2019 (2019-07-25) See paragraphs [0070]-[0071] and figures 8A-8B.	1-20
A	US 2023-0124597 A1 (TOKYO ELECTRON LIMITED) 20 April 2023 (2023-04-20) See claims 15, 21 and figures 3A-3E.	1-20
A	WO 2022-264380 A1 (HITACHI HIGH-TECH CORPORATION) 22 December 2022 (2022-12-22) See paragraphs [0034]-[0042] and figures 5A-5F.	1-20
A	US 2022-0238309 A1 (TOKYO ELECTRON LIMITED) 28 July 2022 (2022-07-28) See the entire document.	1-20
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "D" document cited by the applicant in the international application "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 25 April 2024		Date of mailing of the international search report 26 April 2024
Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon 35208, Republic of Korea Facsimile No. +82-42-481-8578		Authorized officer LEE, Kang Ha Telephone No. +82-42-481-5003

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

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