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Canadian Intellectual Property Office

CA 3127581 A1 2020/10/22

(21) 3 127 581

(12) DEMANDE DE BREVET CANADIEN
CANADIAN PATENT APPLICATION

(13) A1

(86) Date de dépôt PCT/PCT Filing Date: 2019/04/19
(87) Date publication PCT/PCT Publication Date: 2020/10/22
(85) Entrée phase nationale/National Entry: 2021/07/22
(86) N° demande PCT/PCT Application No.: US 2019/028403
(87) N° publication PCT/PCT Publication No.: 2020/214189

(51) Cl.Int./Int.Cl. *B41J 2/045* (2006.01),
B41J 2/14 (2006.01)

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(54) Titre : DISPOSITIFS D'EJECTION DE FLUIDE COMPRENANT UNE PREMIERE MEMOIRE ET UNE SECONDE MEMOIRE

(54) Title: FLUID EJECTION DEVICES INCLUDING A FIRST MEMORY AND A SECOND MEMORY

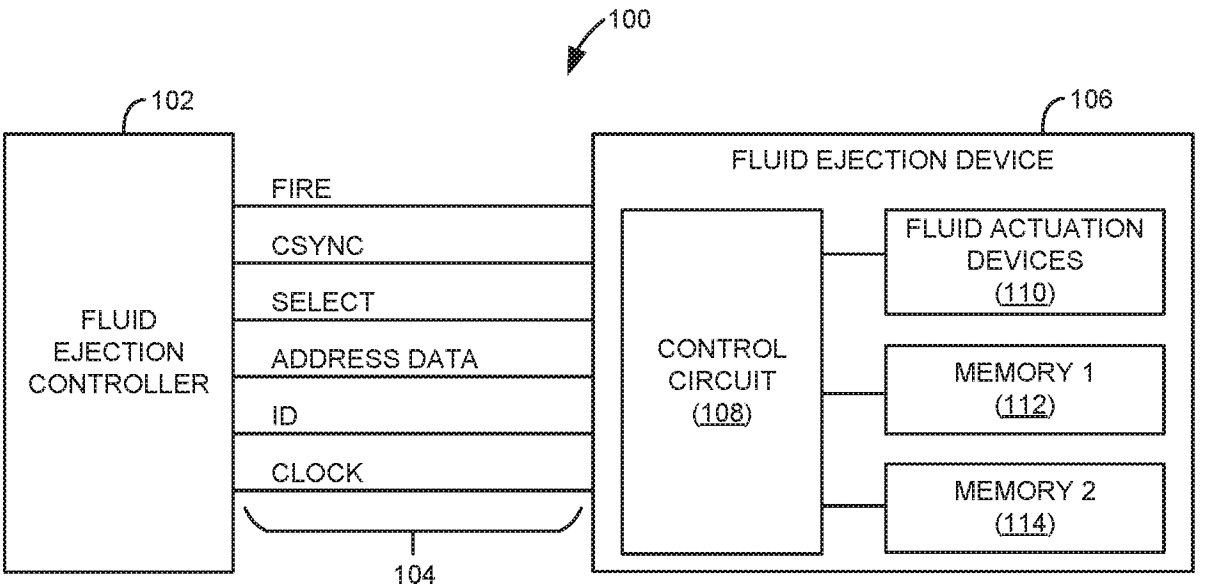


Fig. 1

(57) Abrégé/Abstract:
An integrated circuit to drive a plurality of fluid actuation devices includes a plurality of first data lines, a second data line, a first memory element, and a second memory element. The first memory element is enabled in response to first data on the plurality of first data lines. The second memory element is enabled in response to second data on the second data line.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 October 2020 (22.10.2020)

WIPO | PCT

(10) International Publication Number
WO 2020/214189 A1

(51) International Patent Classification:
B41J 2/045 (2006.01) *B41J 2/14* (2006.01)

(21) International Application Number:
PCT/US2019/028403

(22) International Filing Date:
19 April 2019 (19.04.2019)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to the identity of the inventor (Rule 4.17(i))*
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:
— *with international search report (Art. 21(3))*

(54) Title: FLUID EJECTION DEVICES INCLUDING A FIRST MEMORY AND A SECOND MEMORY

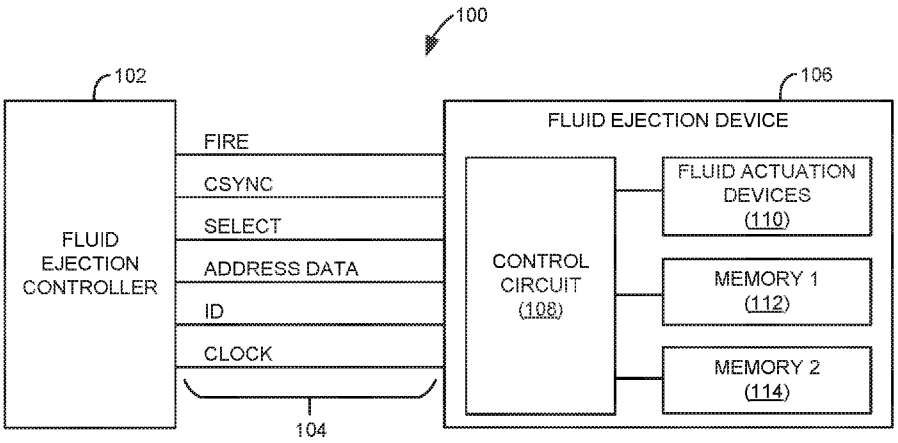


Fig. 1

(57) Abstract: An integrated circuit to drive a plurality of fluid actuation devices includes a plurality of first data lines, a second data line, a first memory element, and a second memory element. The first memory element is enabled in response to first data on the plurality of first data lines. The second memory element is enabled in response to second data on the second data line.

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FLUID EJECTION DEVICES INCLUDING A FIRST MEMORY AND A SECOND MEMORY

Background

[0001] An inkjet printing system, as one example of a fluid ejection system, may include a printhead, an ink supply which supplies liquid ink to the printhead, and an electronic controller which controls the printhead. The printhead, as one example of a fluid ejection device, ejects drops of ink through a plurality of nozzles or orifices and toward a print medium, such as a sheet of paper, so as to print onto the print medium. In some examples, the orifices are arranged in at least one column or array such that properly sequenced ejection of ink from the orifices causes characters or other images to be printed upon the print medium as the printhead and the print medium are moved relative to each other.

Brief Description of the Drawings

[0002] Figure 1 is a block diagram illustrating one example of a fluid ejection system.

[0003] Figure 2 is a schematic diagram illustrating one example of a fluid ejection device.

[0004] Figure 3 is a block diagram illustrating one example of a circuit including a first memory and a second memory of a fluid ejection device.

[0005] Figure 4 is a block diagram illustrating another example of a circuit including a first memory and a second memory of a fluid ejection device.

[0006] Figure 5 is a schematic diagram illustrating one example of a circuit including a memory element of a fluid ejection device.

[0007] Figure 6 is a schematic diagram illustrating another example of a circuit including a memory element of a fluid ejection device.

[0008] Figure 7A is a schematic diagram illustrating one example of a circuit including a plurality of memory elements of a fluid ejection device.

[0009] Figure 7B is a schematic diagram illustrating another example of a circuit including a plurality of memory elements of a fluid ejection device.

[0010] Figures 8A-8B are schematic diagrams illustrating one example of a circuit including a plurality of memory elements and a plurality of fluid actuation devices of a fluid ejection device.

[0011] Figure 9A is a schematic diagram illustrating one example of a circuit including a first memory, a second memory, and fluid actuation devices.

[0012] Figure 9B is a schematic diagram illustrating another example of a circuit including a first memory, a second memory, and fluid actuation devices.

[0013] Figures 10A and 10B are timing diagrams illustrating one example of the operation of the circuit of Figure 9B.

[0014] Figures 11A and 11B are timing diagrams illustrating another example of the operation of the circuit of Figure 9B.

[0015] Figure 12 is a block diagram illustrating one example of a fluid ejection system.

[0016] Figures 13A-13D are flow diagrams illustrating one example of a method for accessing a first memory and a second memory of a fluid ejection device.

[0017] Figures 14A-14B are flow diagrams illustrating one example of a method for accessing a memory of a fluid ejection device.

[0018] Figures 15A-15B are flow diagrams illustrating another example of a method for accessing a memory of a fluid ejection device.

Detailed Description

[0019] In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific examples in which the disclosure may be practiced. It is to be understood that other examples may be utilized and structural or logical

changes may be made without departing from the scope of the present disclosure. The following detailed description, therefore, is not to be taken in a limiting sense, and the scope of the present disclosure is defined by the appended claims. It is to be understood that features of the various examples described herein may be combined, in part or whole, with each other, unless specifically noted otherwise.

[0020] As used herein a "logic high" signal is a logic "1" or "on" signal or a signal having a voltage about equal to the logic power supplied to an integrated circuit (e.g., between about 1.8 V and 15 V, such as 5.6 V). As used herein a "logic low" signal is a logic "0" or "off" signal or a signal having a voltage about equal to a logic power ground return for the logic power supplied to the integrated circuit (e.g., about 0 V).

[0021] A printhead for use in a printing system may include nozzles that are activated to cause printing fluid droplets to be ejected from respective nozzles. Each nozzle includes a fluid actuation device. The fluid actuation devices when activated cause a printing fluid droplet to be ejected by the corresponding nozzles. In one example, each fluid actuation device includes a heating element (e.g., a thermal resistor) that when activated generates heat to vaporize a printing fluid in a firing chamber of a nozzle. The vaporization of the printing fluid causes expulsion of a droplet of the printing fluid from the nozzle. In other examples, each fluid actuation device includes a piezoelectric element. When activated, the piezoelectric element applies a force to eject a printing fluid droplet from a nozzle. In other examples, other types of fluid actuation devices may be used to eject a fluid from a nozzle.

[0022] A printing system can be a two-dimensional (2D) or three-dimensional (3D) printing system. A 2D printing system dispenses printing fluid, such as ink, to form images on print media, such as paper media or other types of print media. A 3D printing system forms a 3D object by depositing successive layers of build material. Printing fluids dispensed from the 3D printing system may include ink, as well as agents used to fuse powders of a layer of build material, detail a layer of build material (such as by defining edges or shapes of the layer of build material), and so forth.

[0023] As used herein, the term "printhead" refers generally to a printhead die or an assembly that includes multiple dies mounted on a support structure. A die (also referred to as an "integrated circuit die") includes a substrate on which is provided various layers to form nozzles and/or control circuitry to control ejection of a fluid by the nozzles.

[0024] Although reference is made to a printhead for use in a printing system in some examples, it is noted that techniques or mechanisms of the present disclosure are applicable to other types of fluid ejection devices used in non-printing applications that are able to dispense fluids through nozzles. Examples of such other types of fluid ejection devices include those used in fluid sensing systems, medical systems, vehicles, fluid flow control systems, and so forth.

[0025] As devices, including printhead dies or other types of fluid ejection dies, continue to shrink in size, the number of signal lines used to control circuitry of a device may affect the overall size of the device. A large number of signal lines may lead to using a large number of signal pads (referred to as "bond pads") that are used to electrically connect the signal lines to external lines. Adding features to fluid ejection devices may lead to the use of an increased number of signal lines (and corresponding bond pads), which may take up valuable die space. Examples of additional features that may be added to a fluid ejection device include memory devices.

[0026] Accordingly, disclosed herein are various example circuits of a fluid ejection device (that includes one die or multiple dies) that may share control and data lines to allow for a reduction in the number of signal lines of the fluid ejection device. As used herein, the term "line" refers to an electrical conductor (or alternatively, multiple electrical conductors) that may be used to carry a signal (or multiple signals).

[0027] Figure 1 is a block diagram illustrating one example of a fluid ejection system 100. Fluid ejection system 100 includes a fluid ejection controller 102 and a fluid ejection device 106. Fluid ejection controller 102 is communicatively coupled to fluid ejection device 106 through a plurality of control lines 104. Fluid ejection device 106 may include a control circuit 108, fluid actuation devices 110, a first memory 112, and a second memory 114. Control circuit 108 is

electrically coupled to the fluid actuation devices 110, the first memory 112, and the second memory 114.

[0028] Fluid ejection controller 102 is separate from the fluid ejection device 106. Fluid ejection controller 102 may include a processor, an application-specific integrated circuit (ASIC), or other suitable logic circuitry for controlling fluid ejection device 106 through control lines 104. For example, in a printing system, the fluid ejection controller 102 may be a printhead drive controller that is part of the printing system, while the fluid ejection device 106 may be a printhead integrated circuit die that is part of a print cartridge (that includes ink or another agent) or part of another structure.

[0029] Fluid actuation devices 110 of fluid ejection device 106 may include an array of nozzles that are selectively controllable to dispense fluid. First memory 112 may include an ID memory used to store identification data and/or other information about the fluid ejection device 106, such as to uniquely identify the fluid ejection device 106. Second memory 114 may include a fire memory used to store data relating to fluid actuation devices 110, where the data may include any or some combination of the following, as examples: die location, region information, drop weight encoding information, authentication information, data to enable or disable selected fluid actuation devices, and so forth.

[0030] First memory 112 and second memory 114 may be implemented with different types of memories to form a hybrid memory arrangement. First memory 112 may be implemented with a non-volatile memory, such as an electrically programmable read-only memory (EPROM). Second memory 114 may be implemented with a non-volatile memory, such as a fuse memory, where the fuse memory includes an array of fuses that may be selectively blown (or not blown) to program data into the second memory 114. Although specific examples of types of memories are listed above, it is noted that in other examples, the first memory 112 and the second memory 114 may be implemented with other types of memories. In some examples, the first memory 112 and the second memory 114 may be implemented with the same type of memory.

[0031] In one example, fluid actuation devices 110, first memory 112, and second memory 114 of fluid ejection device 106 may be formed on a common die (i.e., a fluid ejection die). In another example, fluid actuation devices 110 may be implemented on one die (i.e., a fluid ejection die), while first memory 112 and second memory 114 may be implemented on a separate die (or respective separate dies). For example, first memory 112 and second memory 114 may be formed on a second die that is separate from the fluid ejection die, or alternatively, first memory 112 and second memory 114 may be formed on respective different dies separate from the fluid ejection die. In other examples, part of first memory 112 may be on one die, and another part of first memory 112 may be on another die. Likewise, part of second memory 114 may be on one die, and another part of second memory 114 may be on another die.

[0032] Control circuit 108 controls the operation of fluid actuation devices 110, first memory 112, and second memory 114 based on the control signals received through control lines 104. The control lines 104 include a fire line, a CSYNC line, a select line, an address data line, an ID line, a clock line, and other lines. In other examples, there may be multiple fire lines, and/or multiple select lines, and/or multiple address data lines. Control circuit 108 may select fluid actuation devices 110 or second memory 114 based on an ID signal on the ID line. The ID line may also be used to access first memory 112 for read and/or write operations. Memory elements of the first memory 112 may be addressed based on select and data signals on the select and address data lines.

[0033] The fire line is used to control activation of the fluid actuation devices 110 when the fluid actuation devices 110 are selected by the control circuit 108 in response to a first logic level on the ID line. A fire signal on the fire line when set to a first logic level causes a respective fluid actuation device (or fluid actuation devices) to be activated if such fluid actuation device (or fluid actuation devices) are addressed based on select and data signals on the select and address data lines. If the fire signal is set to a second logic level different from the first logic level, then the fluid actuation device (or fluid actuation devices) are not activated. The fire line may also be used to access

the second memory 114 for read and/or write operations when the second memory 114 is selected by the control circuit 108 in response to a second logic level on the ID line. Memory elements of the second memory 114 may be addressed based on select and data signals on the select and address data lines.

[0034] The CSYNC signal is used to initiate an address (referred to as Ax and Ay) in the fluid ejection device 106. The select line may be used to select certain fluid actuation devices or memory elements. The address data line may be used to carry an address bit (or address bits) to address a specific fluid actuation device or memory element (or a specific group of fluid actuation devices or group of memory elements). The clock line may be used to carry a clock signal for control circuit 108.

[0035] In accordance with some implementations of the present disclosure, to enhance flexibility and to reduce the number of input/output (I/O) pads that have to be provided on the fluid ejection device 106, each of the fire line and the ID line performs both primary and secondary tasks. As noted above, the primary task of the fire line is to activate selected fluid actuation device(s) 110. The secondary task of the fire line is to communicate data of the second memory 114. In this manner, a data path may be provided between the fluid ejection controller 102 and the second memory 114 (over the fire line), without having to provide a separate data line between the fluid ejection controller 102 and the fluid ejection device 106.

[0036] The primary task of the ID line is to communicate data of the first memory 112. The secondary task of the ID line is to cause the control circuit 108 to enable either the fluid actuation devices 110 or the second memory 114. In this way, a common fire line may be used to control activation of the fluid actuation devices 110 and to communicate data of the second memory 114, where the ID line may be used to select when the fluid actuation devices 110 are controlled by the fire line and when the fire line may be used to communicate data of the second memory 114.

[0037] Figure 2 is a schematic diagram illustrating one example of fluid ejection device 106 of Figure 1 in more detail. Fluid ejection device 106 includes fluid

actuation devices 110, first memory 112, second memory 114, latches 130 and 132, a shift register decoder 134, an address generator 136, a fire line 140, an ID line 142, and switches 144, 146, 148, and 150. In one example, fire line 140 and ID line 142 are part of control lines 104 of Figure 1. Latches 130 and 132, shift register decoder 134, address generator 136, and switches 144, 146, 148, and 150 may be part of control circuit 108 of Figure 1.

[0038] ID line 142 is electrically coupled to an input of latch 130, an input of latch 132, and to first memory 112. Fire line 140 is electrically coupled to one side of switch 146 and to fluid actuation devices 110. The output of latch 130 is electrically coupled to the control input of switch 146. The other side of switch 146 is electrically coupled to second memory 114. The output of latch 132 is electrically coupled to the control input of switch 148. Switch 148 is electrically coupled between second memory 114 and a common or ground node 152. Switch 150 is electrically coupled between fluid actuation devices 110 and a common or ground node 152. An output of address generator 136 is electrically coupled to the control input of switch 148 and the control input of switch 150. An output of shift register 134 is electrically coupled to the control input of switch 144. Switch 144 is electrically coupled between first memory 112 and a common or ground node 152.

[0039] First memory 112 may include a plurality of memory elements. Switch 144 may include a plurality of switches, where each switch corresponds to one of the memory elements of first memory 112. Shift register decoder 134 selects a memory element of first memory 112 for read and/or write access by closing the switch 144 corresponding to the selected memory element. Shift register decoder 134 disables memory elements of first memory 112 by opening the switches 144 corresponding to the disabled memory elements. With a memory element of first memory 112 selected by shift register decoder 134, the memory element may be accessed for read and/or write operations through ID line 142.

[0040] Latch 130 receives the ID signal on ID line 142, latches the logic level of the ID signal, and controls switch 146 based on the latched value. In response to a first logic level (e.g., a logic high) of the latched value, latch 130 turns on switch 146. In response to a second logic level (e.g., a logic low) of the latched

value, latch 130 turns off switch 146. With switch 146 closed, second memory 114 is enabled for read and/or write access through fire line 140. With switch 146 open, second memory 114 is disabled.

[0041] Second memory 114 may include a plurality of memory elements. Switch 148 may include a plurality of switches, where each switch corresponds to one of the memory elements of second memory 114. Switch 150 may include a plurality of switches, where each switch corresponds to one of the fluid actuation devices 110. Latch 132 receives the ID signal on ID line 142, latches the inverted logic level of the ID signal, and controls switch 148 based on the latched value. In response to a first logic level (e.g., a logic high) of the latched value, latch 132 disables switch 148 (i.e., prevents switch 148 from being turned on). In response to second logic level (e.g., a logic low) of the latched value, latch 132 enables switch 148 (i.e., allows switch 148 to be turned on).

[0042] Address generator 136 generates address signals Ax and Ay for selecting a memory element of second memory 114 or a fluid actuation device 110. The selection of a memory element of second memory 114 or a fluid actuation device 110 may also be based on a data signal (D2) on an address data line. Accordingly, as shown in Figure 2 and described in more detail below, switch 148 may be controlled based on ID x D2 x AxAy and switch 150 may be controlled based on ID' x D2 x AxAy. With switch 150 open, switch 146 closed, and switch 148 closed, second memory 114 may be accessed for read and/or write operations through fire line 140. With switch 146 open, switch 148 open, and switch 150 closed, fluid actuation devices 110 may be activated through fire line 140.

[0043] Figure 3 is a block diagram illustrating one example of a circuit 200 including a first memory and a second memory of a fluid ejection device. In one example, circuit 200 is part of an integrated circuit to drive a plurality of fluid actuation devices. Circuit 200 includes a first memory 112 and a second memory 114. First memory 112 includes a plurality of first memory elements 212_1 to 212_M, where "M" is any suitable number of memory elements. Second memory 114 includes a plurality of second memory elements 214_1 to 214_N, where "N" is any suitable number of memory elements. First memory 112 and

second memory 114 may include the same number of memory elements or different numbers of memory elements.

[0044] Circuit 200 also includes a plurality of first data ($D1_1$ to $D1_3$) lines 216_1 to 216_3 and a second data (D2) line 218. The first data lines 216_1 to 216_3 are electrically coupled to first memory 112, and the second data line 218 is electrically coupled to second memory 114. In one example, first data lines 216_1 to 216_3 and second data line 218 are part of the address data lines of control lines 104 of Figure 1. In this example, a memory element 212 of first memory 112 is enabled in response to first data on the plurality of first data lines 216_1 to 216_3, and a memory element 214 of second memory 114 is enabled in response to second data on the second data line 218.

[0045] Figure 4 is a block diagram illustrating another example of a circuit 230 including a first memory and a second memory of a fluid ejection device. In one example, circuit 230 is part of an integrated circuit to drive a plurality of fluid actuation devices. Circuit 230 includes first memory 112 and second memory 114 as previously described and illustrated with reference to Figure 3. Circuit 230 also includes an ID line 142, a first select (S4) line 236, and a second select (S5) line 238. The first select line 236 is electrically coupled to first memory 112, and the second select line 238 and the ID line 142 are electrically coupled to the second memory 114. In this example, a memory element 212 of first memory 112 is enabled in response to a first logic level on the first select line 236, and a memory element 214 of second memory 114 is enabled in response to a first logic level on the second select line 238 and a first logic level on the ID line.

[0046] In one example, circuit 200 of Figure 3 may be combined with circuit 230 of Figure 4. Therefore, first memory 112 may be accessed based on an address generated by the first data $D1_1$, $D1_2$, and $D1_3$ (e.g., via a shift register decoder 134 of Figure 1), while second memory 114 may be accessed based on an address generated by second data D2. The first data and the second data may be fully independent from each other. In addition, first memory 112 may be enabled in response to the S4 select signal, while second memory 114 may be enabled in response to the S5 select signal. The S4 select signal and

the S5 select signal may be staggered. In this way, corruption on the ID signal due to a shift register (e.g., shift register decoder 134 of Figure 1) may be avoided.

[0047] Figure 5 is a schematic diagram illustrating one example of a circuit 250 including a memory element of a fluid ejection device. In one example, circuit 250 is part of an integrated circuit to drive a plurality of fluid actuation devices. Circuit 250 includes a fire line 140, an ID line 142, a memory element 252, a latch 254, and a discharge path 256. Fire line 140 is electrically coupled to memory element 252. ID line 142 is electrically coupled to an input of latch 254. An output of latch 254 is electrically coupled to an input of discharge path 256. Discharge path 256 is electrically coupled between memory element 252 and a common or ground node 152.

[0048] Discharge path 256 keeps memory element 252 from floating when memory element 252 is not enabled for read and/or write access. In this example, latch 254 disables the discharge path in response to a first logic level (e.g., a logic high) on the ID line 142 and enables the discharge path in response to a second logic level (e.g., a logic low) on the ID line. When memory element 252 is enabled, discharge path 256 is disabled and memory element 252 may be accessed through fire line 140 for read and/or write operations. In one example, latch 254 provides latch 132 of Figure 2, discharge path 256 is part of the control input to switch 148, and memory element 252 is a memory element of second memory 114 of Figure 2.

[0049] Figure 6 is a schematic diagram illustrating another example of a circuit 270 including a memory element of a fluid ejection device. In one example, circuit 270 is part of an integrated circuit to drive a plurality of fluid actuation devices. Circuit 270 includes a fire line 140, an ID line 142, a memory element 252, a latch 272, and a switch 274. Switch 274 is electrically coupled between fire line 140 and memory element 252. The input of latch 272 is electrically coupled to the ID line 142. The output of latch 272 is electrically coupled to the control input of switch 274. Memory element 252 is electrically coupled to a common or ground node 152.

[0050] In this example, latch 272 enables (i.e., turns on) switch 274 in response to a first logic level (e.g., a logic high) on the ID line 142 and disables (i.e., turns off) switch 274 in response to a second logic level (e.g., a logic low) on the ID line. With switch 274 enabled, the fire line 140 is electrically connected to memory element 252. With switch 274 disabled, fire line 140 is electrically disconnected from memory element 252. With switch 274 enabled, memory element 252 may be accessed through fire line 140 for read and/or write operations. In one example, latch 272 provides latch 130 of Figure 2, switch 274 provides switch 146 of Figure 2, and memory element 252 is a memory element of second memory 114 of Figure 2.

[0051] Figure 7A is a schematic diagram illustrating one example of a circuit 300 including a plurality of memory elements of a fluid ejection device. In one example, circuit 300 is part of an integrated circuit to drive a plurality of fluid actuation devices. Circuit 300 includes a fire line 140, a plurality of memory elements 214_1 to 214_N, a first switch 304, and a plurality of second switches 308_1 to 308_N. Switch 304 is electrically coupled between the fire line 140 and a first side of each memory element 214_1 to 214_N. The control input of switch 304 is electrically coupled to a control (Vy) signal line 302. One side of each second switch 308_1 to 308_N is electrically coupled to a second side of a respective memory element 214_1 to 214_N. The other side of each second switch 308_1 to 308_N is electrically coupled to a common or ground node 152. The control input of each second switch 308_1 to 308_N is electrically coupled to a control (X_1 to X_N) signal line 306_1 to 306_N, respectively.

[0052] The Vy control signal may be based on the ID signal (e.g., on ID line 142). Control signals X_1 to X_N may be based on the ID signal (e.g., on ID line 142), the D2 data signal (e.g., on D2 data line 218), and the Ax and Ay address signals (e.g., from address generator 136). In this example, a memory element 214_1 to 214_N may be enabled by turning on switch 304 in response to the Vy signal and turning on at least one respective second switch 308_1 to 308_N in response to a respective X_1 to X_N signal. With a memory element 214_1 to 214_N enabled, the enabled memory element may be accessed for read and/or write operations through fire line 140. In one example, first switch 304 provides

switch 146 of Figure 2, and each second switch 308_1 to 308_N provides a switch 148 of Figure 2.

[0053] Figure 7B is a schematic diagram illustrating another example of a circuit 320 including a plurality of memory elements of a fluid ejection device. In one example, circuit 320 is part of an integrated circuit to drive a plurality of fluid actuation devices. Circuit 320 is similar to circuit 300 previously described and illustrated with reference to Figure 7A, except that in circuit 320 a first transistor 324 is used in place of first switch 304 and a plurality of second transistors 328_1 to 328_N are used in place of second switches 308_1 to 308_N. First transistor 324 has a source-drain path electrically coupled between the fire line 140 and a first side of each memory element 214_1 to 214_N. Each second transistor 328_1 to 328_N has a source-drain path electrically coupled between a respective memory element 214_1 to 214_N and a common or ground node 152. The gate of each second transistor 328_1 to 328_N is electrically coupled to a control signal line 306_1 to 306_N, respectively.

[0054] In this example, a memory element 214_1 to 214_N may be enabled by turning on first transistor 324 in response to a logic high Vy signal and turning on at least one respective second transistor 328_1 to 328_N in response to a respective logic high X_1 to X_N signal. With a memory element 214_1 to 214_N enabled, the enabled memory element may be accessed for read and/or write operations through fire line 140. In one example, first transistor 324 provides switch 146 of Figure 2, and each second transistor 328_1 to 328_N provides a switch 148 of Figure 2.

[0055] Figures 8A-8B are schematic diagrams illustrating one example of a circuit 350 including a plurality of memory elements and a plurality of fluid actuation devices of a fluid ejection device. In one example, circuit 350 is part of an integrated circuit to drive a plurality of fluid actuation devices. Circuit 350 includes circuit 320 previously described and illustrated with reference to Figure 7B. In addition, as illustrated in Figure 8A, circuit 350 includes a plurality of fluid actuation devices 352_1 to 352_N and a plurality of third switches (e.g., third transistors) 358_1 to 358_N. Each fluid actuation device 352_1 to 352_N is electrically coupled between the fire line 140 and one side of the source-drain path of a

respective third transistor 358_1 to 358_N. The other side of the source-drain path of each third transistor 358_1 to 358_N is electrically coupled to a common or ground node 152. The gate of each third transistor 358_1 to 358_N is electrically coupled to a control (Y_1 to Y_N) signal line 356_1 to 356_N, respectively.

[0056] As illustrated in Figure 8B, circuit 350 also includes an address generator 136 and a decoder 360. Outputs of address generator 136 are electrically coupled to inputs of decoder 360 through an Ax address signal line 362 and an Ay address signal line 364. Other inputs to decoder 360 are electrically coupled to ID line 142 and second data line 218. First outputs of decoder 360 are electrically coupled to the gates of second transistors 328_1 to 328_N through control signal lines 306_1 to 306_N, respectively. Second outputs of decoder 360 are electrically coupled to the gates of third transistors 358_1 to 358_N through control signal lines 356_1 to 356_N, respectively.

[0057] Ax and Ay are output by address generator 136, such as in response to a select signal on the select line and a CSYNC signal on the CSYNC line. In one example, decoder 360 receives an address (e.g., D2, Ax, Ay) to turn on a respective second transistor 328_1 to 328_N or a respective third transistor 358_1 to 358_N in response to the address. In another example, in response to a first logic level (e.g., a logic high) on the ID line 142, decoder 360 turns on a respective second transistor 328_1 to 328_N in response to the address, and in response to a second logic level (e.g., a logic low) on the ID line 142, decoder 360 turns on a respective third transistor 358_1 to 358_N in response to the address to enable a respective fluid actuation device 352_1 to 352_N. With a fluid actuation device 352_1 to 352_N enabled, the enabled fluid actuation device may be activated through fire line 140. In one example, each third transistor 358_1 to 358_N provides a switch 150 of Figure 2.

[0058] Figure 9A is a schematic diagram illustrating one example of a circuit 400 including a first memory 112, a second memory 114, and fluid actuation devices 110 in more detail. In one example, circuit 400 is part of an integrated circuit to drive a plurality of fluid actuation devices. While first memory 112 includes a plurality of memory elements, just one memory element 212 is shown in Figure 9A. Likewise, while second memory 114 includes a plurality of memory

elements, just one memory element 214 is shown in Figure 9A, and while fluid actuation devices 110 include a plurality of fluid actuation devices, just one fluid actuation device 352 is shown in Figure 9A.

[0059] Circuit 400 includes a fire line 140, an ID line 142, first data lines 216_1 to 216_3, a second data line 218, select lines 236 and 238, an Ax address signal line 362, an Ay address signal line 364, a shift register decoder 134, and transistors 324, 328, and 358 as previously described. In addition, circuit 400 includes a buffer 408, an inverter 410, and transistors 402, 404, 406, 412, 414, 416, 418, 420, 422, 432, 434, 436, 438, 440, and 442. In one example, transistors 402, 404, and 406 may provide a switch 144 of Figure 2. Buffer 408 may provide latch 130 of Figure 2 or latch 272 of Figure 6. Inverter 410 may provide latch 132 of Figure 2 or latch 254 of Figure 5. Transistor 416 may provide part of discharge path 256 of Figure 5 for first memory 114. Transistor 436 may provide a discharge path for fluid actuation devices 110. Transistors 412, 414, 418, 420, 422, 432, 434, 438, 440, and 442 may provide part of decoder 360 of Figure 8B.

[0060] First inputs of shift register decoder 134 are electrically coupled to first data lines 216_1 to 216_3. A second input of shift register decoder 134 is electrically coupled to first select (S4) line 236. Outputs of shift register decoder 134 are electrically coupled to the gates of transistors 402, 404, and 406. Transistors 402, 404, and 406 are electrically coupled in series between memory element 212 and a common or ground node 152. When the transistors 402, 404, and 406 are turned on, memory element 212 is addressed, such that data of memory element 212 may be accessed via the ID line 142.

[0061] Shift register decoder 134 includes shift registers connected to each of the first data lines 216_1 to 216_3 to input address data bits to the shift register decoder 134. Each shift register includes a series of shift register cells, which may be implemented as flip-flops, other storage elements, or any sample and hold circuits (such as circuits to pre-charge and evaluate address data bits) that can hold their values until the next selection of the storage elements. The output of one shift register cell in the series can be provided to the input of the next shift register cell to perform data shifting through the shift register. The

address data bits provided through each shift register is connected to the gate of a respective one of the transistors 402, 404, and 406.

[0062] By using shift registers in the shift register decoder 134, a small number of data lines 216_1 to 216_3 may be used to select a larger address space. For example, each shift register may include eight (or any other number of) shift register cells. With three address data bits ($D1_1$, $D1_2$, and $D1_3$) input to the shift register decoder 134 that includes three shift registers, each of length eight, then the address space that may be addressed by the shift register decoder 134 is 512 bits (instead of just eight bits if the three address bits are used without using the shift registers of the shift register decoder 134). The output of shift register decoder 134 may be enabled in response to a first logic level on the first select (S4) line 236 and disabled in response to a second logic level on the first select (S4) line 236.

[0063] Buffer 408 is electrically coupled between the ID line 142 and the gate of transistor 324 through a Vy node 409. Inverter 410 is electrically coupled between the ID line 142 and the gate of transistor 416 through a Vx node 411. One side of the source-drain path of transistor 416 is electrically coupled to a common or ground node 152. The other side of the source-drain path of transistor 416 is electrically coupled to one side of the source-drain path of transistor 414, one side of the source-drain path of transistor 418, one side of the source-drain path of transistor 420, and one side of the source-drain path of transistor 422. The other side of the source-drain path of each transistor 418, 420, and 422 is electrically coupled to a common or ground node 152. The gate of transistor 418 is electrically coupled to the second data line 218. The gate of transistor 420 is electrically coupled to the Ax address signal line 362. The gate of transistor 422 is electrically coupled to the Ay address signal line 364. The gate of transistor 414 is electrically coupled to the second select (S5) line 238. The other side of the source-drain path of transistor 414 is electrically coupled to one side of the source-drain path of transistor 412 and the gate of transistor 328. The other side of the source-drain path and the gate of transistor 412 are electrically coupled to the first select (S4) line 236.

[0064] The gate of transistor 436 is electrically coupled to the ID line 142. One side of the source-drain path of transistor 436 is electrically coupled to a common or ground node 152. The other side of the source-drain path of transistor 436 is electrically coupled to one side of the source-drain path of transistor 434, one side of the source-drain path of transistor 438, one side of the source-drain path of transistor 440, and one side of the source-drain path of transistor 442. The other side of the source-drain path of each transistor 438, 440, and 442 is electrically coupled to a common or ground node 152. The gate of transistor 438 is electrically coupled to the second data line 218. The gate of transistor 440 is electrically coupled to the Ax address signal line 362. The gate of transistor 442 is electrically coupled to Ay address signal line 364. The gate of transistor 434 is electrically coupled to the second select (S5) line 238. The other side of the source-drain path of transistor 434 is electrically coupled to one side of the source-drain path of transistor 432 and the gate of transistor 358. The other side of the source-drain path and the gate of transistor 432 are electrically coupled to the first select (S4) line 236.

[0065] Two separate decoders are used to control the respective transistors 328 and 358 that are connected to the memory element 214 and the fluid activation device 352, respectively. The gate of transistor 328 is connected to a first decoder that includes transistors 412, 414, 418, 420, and 422. The gate of transistor 358 is connected to a second decoder that includes transistors 432, 434, 438, 440, and 442. The S4 select signal may be activated earlier in time than the S5 select signal. The combination of Ax, Ay, D2, S4, and S5 form the address input to the first decoder and the second decoder.

[0066] When the ID signal on ID line 142 is at a first logic level (e.g., logic high), transistor 436 turns on and causes the gate of transistor 358 to remain discharged (i.e., disables the gate of transistor 358), such that the fluid activation device 352 is maintained deactivated. In addition, when the ID signal is at the first logic level (e.g., logic high), transistor 324 is turned on by buffer 408 and transistor 416 is turned off by inverter 410, such that when transistor 328 is turned on based on an address input to the first decoder, memory

element 214 may be accessed for read and/or write operations through fire line 140.

[0067] When the ID signal on ID line 142 is at a second logic level (e.g., a logic low), transistor 436 turns off, such that when transistor 358 is turned on based on an address input to the second decoder, fluid actuation device 352 may be activated through fire line 140. In addition, when the ID signal is at the second logic level (e.g., logic low), transistor 324 is turned off by buffer 408 and transistor 416 is turned on by inverter 410. With transistor 416 turned on, the gate of transistor 328 remains discharged (i.e., the gate of transistor 328 is disabled), such that memory element 214 is maintained deselected.

[0068] Figure 9B is a schematic diagram illustrating another example of a circuit 450 including a first memory 112, a second memory 114, and fluid actuation devices 110. In one example, circuit 450 is part of an integrated circuit to drive a plurality of fluid actuation devices. Circuit 450 is similar to circuit 400 previously described and illustrated with reference to Figure 9A, except that in circuit 450, transistors 452, 454, 456, 458, 460, and 462 are used in place of buffer 408; and transistors 468, 470, and 472 are used in place of inverter 410.

[0069] Transistor 460 and transistor 462 are electrically coupled in series between a node 459 and a common or ground node 152. The gate of transistor 462 is electrically coupled to the ID line 142, and the gate of transistor 460 is electrically coupled to the S4 select line 236. Transistor 458 has a source-drain path electrically coupled between the S3 select line 234 and the node 459. The gate of transistor 458 is electrically coupled to the S3 select line 234. Transistor 454 and transistor 456 are electrically coupled in series between the gate of transistor 324 and a common or ground node 152. The gate of transistor 456 is electrically coupled to the node 459. The gate of the transistor 454 is electrically coupled to the S5 select line 238. Transistor 452 has a source-drain path electrically coupled between the S4 select line 236 and the gate of transistor 324. The gate of transistor 452 is electrically coupled to the S4 select line 236.

[0070] Transistor 470 and transistor 472 are electrically coupled in series between the gate of transistor 416 and a common or ground node 152. The gate of transistor 472 is electrically coupled to the ID line 142. The gate of

transistor 470 is electrically coupled to the S4 select line 236. Transistor 468 has a source-drain path electrically coupled between the S3 select line 234 and the gate of transistor 416. The gate of transistor 468 is electrically coupled to the S3 select line 234.

[0071] The S3 select signal may be activated earlier in time than the S4 select signal. The S4 select signal may be activated earlier in time than the S5 select signal. With the ID signal on ID line 142 at a first logic level (e.g., a logic high), a second logic level (e.g., a logic low) is latched on Vx node 411 in response to the S3 and S4 select signals. With the ID signal at a second logic level (e.g., a logic low), a first logic level (e.g., a logic high) is latched on Vx node 411 in response to the S3 and S4 select signals.

[0072] With the ID signal on ID line 142 at a first logic level (e.g., a logic high), a second logic level (e.g., a logic low) is latched on node 459 in response to the S3 and S4 select signals. With the ID signal at a second logic level (e.g., a logic low), a first logic level (e.g., a logic high) is latched on node 459 in response to the S3 and S4 select signals. With a first logic level (e.g., a logic high) on node 459, a second logic level (e.g., a logic low) is latched on Vy node 409 in response to the S4 and S5 select signals. With a second logic level (e.g., a logic low) on node 459, a first logic level (e.g., a logic high) is latched on Vy node 409 in response to the S4 and S5 select signals. Accordingly, with the ID signal on ID line 142 at a first logic level (e.g., a logic high), a first logic level (e.g., a logic high) is latched on Vy node 409 in response to the S3, S4, and S5 select signals. With the ID signal at a second logic level (e.g., a logic low), a second logic level (e.g., a logic low) is latched on Vy node 409 in response to the S3, S4, and S5 select signals.

[0073] Figures 10A and 10B are timing diagrams illustrating one example of the operation of the circuit 450 of Figure 9B. Figure 10A illustrates a timing diagram 500a for when a memory element 214 is enabled, and Figure 10B illustrates a timing diagram 500b for when a fluid actuation device 352 is enabled. Timing diagrams 500a and 500b include the CSYNC signal, an S1 select signal, an S2 select signal, an S3 select signal on S3 select line 234, an S4 select signal on S4 select line 236, an S5 select signal on S5 select line 238, a clock signal, a

$D1_1$ data signal on $D1_1$ data line 216_1, a $D1_2$ data signal on $D1_2$ data line 216_2, a D2 data signal on D2 data line 218, an ID signal on ID line 142, a Vx signal on Vx node 411, and a fire signal on fire line 140.

[0074] The S1 through S5 select signals are sequentially activated. The S1 and S2 select signals may be used by first memory 112, such as to control shift register decoder 134. As shown in Figure 10A at 502, when the ID signal is logic high when the S4 signal is logic high, Vx is logic low. Thus, when the S5 signal is logic high, the discharge path for memory element 214 is off and the memory element 214 is enabled for read and/or write access via the fire signal as indicated at 504. As shown in Figure 10B at 506, when the ID signal is logic low when the S4 signal is logic high, Vx is logic high. Thus, when the S5 signal is logic high, the discharge path for memory element 214 is on and memory element 214 is disabled. With memory element 214 disabled, the fluid actuation device 352 may be enabled and may be activated via the fire signal as indicated at 508.

[0075] In one example, as shown in Figures 10A and 10B, the ID signal and the fire signal may not be turned on (i.e., logic high) at the same time. Accordingly, the ID signal is latched to provide Vx when the S4 signal is logic high to prepare for the fire signal when S5 is logic high. This also ensures that either the gate of transistor 328 for memory element 214 or the gate of transistor 358 for fluid actuation device 352 has a discharge path to avoid a floating condition when unselected. A floating condition should be avoided to prevent corruption of the data stored in second memory 114.

[0076] Figures 11A and 11B are timing diagrams illustrating another example of the operation of the circuit of Figure 9B. Figure 11A illustrates a timing diagram 550a for when a memory element 214 is enabled, and Figure 11B illustrates a timing diagram 550b for when a fluid actuation device 352 is enabled. Timing diagrams 550a and 550b include the CSYNC signal, an S1 select signal, an S2 select signal, an S3 select signal on S3 select line 234, an S4 select signal on S4 select line 236, an S5 select signal on S5 select line 238, a clock signal, a $D1_1$ data signal on $D1_1$ data line 216_1, a $D1_2$ data signal on $D1_2$ data line 216_2, a

D2 data signal on D2 data line 218, an ID signal on ID line 142, a Vy signal on Vy node 409, and a fire signal on fire line 140.

[0077] As shown in Figure 11A at 552, when the ID signal is logic high when the S4 signal is logic high, Vy is logic high when the S5 signal is logic high. With Vy logic high, the memory element 214 is enabled for read and/or write access via the fire signal as indicated at 554. As shown in Figure 11B at 556, when the ID signal is logic low when the S4 signal is logic high, Vy is logic low when the S5 signal is logic high. With Vy logic low, the memory element 214 is disabled and isolated from the fire signal. With memory element 214 disabled, the fluid actuation device 352 may be enabled and may be activated via the fire signal as indicated at 558.

[0078] In one example, as shown in Figures 11A and 11B, the ID signal and the fire signal may not be turned on (i.e., logic high) at the same time. Accordingly, the ID signal is latched to provide Vy when the S4 signal is logic high to prepare for the fire signal when S5 is logic high. Transistor 324 also serves as an isolator between the fire signal and memory element 214 when a fluid actuation device 352 is activated. This may prevent memory element 214 from being subjected to high voltage at high frequency, which may improve the reliability of memory element 214.

[0079] Figure 12 is a block diagram illustrating one example of a fluid ejection system 600. Fluid ejection system 600 includes a fluid ejection assembly, such as printhead assembly 602, and a fluid supply assembly, such as ink supply assembly 610. In the illustrated example, fluid ejection system 600 also includes a service station assembly 604, a carriage assembly 616, a print media transport assembly 618, and an electronic controller 620. While the following description provides examples of systems and assemblies for fluid handling with regard to ink, the disclosed systems and assemblies are also applicable to the handling of fluids other than ink.

[0080] Printhead assembly 602 includes at least one printhead or fluid ejection die 606, such as fluid ejection device 106 of Figure 1, which ejects drops of ink or fluid through a plurality of orifices or nozzles 608. In one example, the drops are directed toward a medium, such as print media 624, so as to print onto print

media 624. In one example, print media 624 includes any type of suitable sheet material, such as paper, card stock, transparencies, Mylar, fabric, and the like. In another example, print media 624 includes media for three-dimensional (3D) printing, such as a powder bed, or media for bioprinting and/or drug discovery testing, such as a reservoir or container. In one example, nozzles 608 are arranged in at least one column or array such that properly sequenced ejection of ink from nozzles 608 causes characters, symbols, and/or other graphics or images to be printed upon print media 624 as printhead assembly 602 and print media 624 are moved relative to each other.

[0081] Ink supply assembly 610 supplies ink to printhead assembly 602 and includes a reservoir 612 for storing ink. As such, in one example, ink flows from reservoir 612 to printhead assembly 602. In one example, printhead assembly 602 and ink supply assembly 610 are housed together in an inkjet or fluid-jet print cartridge or pen. In another example, ink supply assembly 610 is separate from printhead assembly 602 and supplies ink to printhead assembly 602 through an interface connection 613, such as a supply tube and/or valve.

[0082] Carriage assembly 616 positions printhead assembly 602 relative to print media transport assembly 618, and print media transport assembly 618 positions print media 624 relative to printhead assembly 602. Thus, a print zone 626 is defined adjacent to nozzles 608 in an area between printhead assembly 602 and print media 624. In one example, printhead assembly 602 is a scanning type printhead assembly such that carriage assembly 616 moves printhead assembly 602 relative to print media transport assembly 618. In another example, printhead assembly 602 is a non-scanning type printhead assembly such that carriage assembly 616 fixes printhead assembly 602 at a prescribed position relative to print media transport assembly 618.

[0083] Service station assembly 604 provides for spitting, wiping, capping, and/or priming of printhead assembly 602 to maintain the functionality of printhead assembly 602 and, more specifically, nozzles 608. For example, service station assembly 604 may include a rubber blade or wiper which is periodically passed over printhead assembly 602 to wipe and clean nozzles 608 of excess ink. In addition, service station assembly 604 may include a cap that

covers printhead assembly 602 to protect nozzles 608 from drying out during periods of non-use. In addition, service station assembly 604 may include a spittoon into which printhead assembly 602 ejects ink during spits to ensure that reservoir 612 maintains an appropriate level of pressure and fluidity, and to ensure that nozzles 608 do not clog or weep. Functions of service station assembly 604 may include relative motion between service station assembly 604 and printhead assembly 602.

[0084] Electronic controller 620 communicates with printhead assembly 602 through a communication path 603, service station assembly 604 through a communication path 605, carriage assembly 616 through a communication path 617, and print media transport assembly 618 through a communication path 619. In one example, when printhead assembly 602 is mounted in carriage assembly 616, electronic controller 620 and printhead assembly 602 may communicate via carriage assembly 616 through a communication path 601. Electronic controller 620 may also communicate with ink supply assembly 610 such that, in one implementation, a new (or used) ink supply may be detected.

[0085] Electronic controller 620 receives data 628 from a host system, such as a computer, and may include memory for temporarily storing data 628. Data 628 may be sent to fluid ejection system 600 along an electronic, infrared, optical or other information transfer path. Data 628 represent, for example, a document and/or file to be printed. As such, data 628 form a print job for fluid ejection system 600 and includes at least one print job command and/or command parameter.

[0086] In one example, electronic controller 620 provides control of printhead assembly 602 including timing control for ejection of ink drops from nozzles 608. As such, electronic controller 620 defines a pattern of ejected ink drops which form characters, symbols, and/or other graphics or images on print media 624. Timing control and, therefore, the pattern of ejected ink drops, is determined by the print job commands and/or command parameters. In one example, logic and drive circuitry forming a portion of electronic controller 620 is located on printhead assembly 602. In another example, logic and drive circuitry forming a portion of electronic controller 620 is located off printhead assembly 602.

[0087] Figures 13A-13D are flow diagrams illustrating one example of a method 700 for accessing a first memory and a second memory of a fluid ejection device. In one example, method 700 may be implemented by fluid ejection system 100 of Figure 1. As illustrated in Figure 13A, at 702 method 700 includes sequentially generating a first select signal and a second select signal. At 704, method 700 includes enabling a first memory element in response to the first select signal and first data on a plurality of first data lines. At 706, method 700 includes enabling a second memory element in response to the second select signal and second data on a second data line.

[0088] As illustrated in Figure 13B, at 708 method 700 may further include generating an address signal. In this case, enabling the second memory element may include enabling the second memory element in response to the second select signal, the second data on the second data line, and the address signal.

[0089] As illustrated in Figure 13C, at 710 method 700 may further include generating a signal on an ID line. At 712, method 700 may further include enabling a fluid actuation device in response to the second select signal and a first logic level on the ID line. In this case, enabling the second memory element may include enabling the second memory element in response to the second select signal and a second logic level on the ID line.

[0090] As illustrated in Figure 13D, at 714 method 700 may further include accessing the first memory element via the ID line with the first memory element enabled. At 716, method 700 may further include accessing the second memory element via a fire line with the second memory element enabled.

[0091] Figures 14A-14B are flow diagrams illustrating one example of a method 800 for accessing a memory of a fluid ejection device. In one example, method 800 may be implemented by fluid ejection system 100 of Figure 1. As illustrated in Figure 14A, at 802 method 800 includes electrically connecting, via a first switch, a first side of each memory element of a plurality of memory elements to a fire line in response to a first logic level on an ID line and electrically disconnecting, via the first switch, the first side of each memory element of the plurality of memory elements from the fire line in response to a second logic

level on the ID line. At 804, method 800 includes electrically connecting, via a respective second switch of a plurality of second switches, a second side of a respective memory element of the plurality of memory elements to a common node in response to an address signal.

[0092] In one example, the first switch includes a first transistor and the plurality of second switches include a plurality of second transistors. As illustrated in Figure 14B, at 806 method 800 may further include accessing a respective memory element of the plurality of memory elements via the fire line with the respective memory element electrically connected between the fire line and the common node.

[0093] Figures 15A-15B are flow diagrams illustrating another example of a method 900 for accessing a memory of a fluid ejection device. In one example, method 900 may be implemented by fluid ejection system 100 of Figure 1. As illustrated in Figure 15A, at 902 method 900 includes generating an ID signal on an ID line. At 904, method 900 includes sequentially generating a first select signal and a second select signal. At 906, method 900 includes latching the ID signal in response to the first select signal. At 908, method 900 includes enabling a memory element in response to the latched ID signal having a first logic level. At 910, method 900 includes accessing the memory element via a fire line in response to the second select signal with the memory element enabled.

[0094] In one example, enabling the memory element includes electrically connecting the memory element to the fire line in response to the latched ID signal having the first logic level. In another example, latching the ID signal includes inverting the ID signal and latching the inverted ID signal in response to the first select signal; and enabling the memory element includes turning off a discharge path coupled to the memory element in response to the latched inverted ID signal having a second logic level.

[0095] As illustrated in Figure 15B, at 912 method 900 may further include enabling a fluid actuation device in response to the ID signal having a second logic level. At 914, method 900 may further include activating the fluid actuation

device via the fire line in response to the second select signal with the fluid actuation device enabled.

[0096] Although specific examples have been illustrated and described herein, a variety of alternate and/or equivalent implementations may be substituted for the specific examples shown and described without departing from the scope of the present disclosure. This application is intended to cover any adaptations or variations of the specific examples discussed herein. Therefore, it is intended that this disclosure be limited only by the claims and the equivalents thereof.

CLAIMS

1. An integrated circuit to drive a plurality of fluid actuation devices, the integrated circuit comprising:

a plurality of first data lines;

a second data line;

a first memory element to be enabled in response to first data on the plurality of first data lines; and

a second memory element to be enabled in response to second data on the second data line.

2. The integrated circuit of claim 1, further comprising:

a shift register decoder to enable the first memory element in response to the first data on the plurality of first data lines.

3. The integrated circuit of claim 1 of 2, further comprising:

a transistor to enable the second memory element in response to the second data on the second data line.

4. The integrated circuit of any of claims 1-3, further comprising:

an ID line;

wherein the first memory element is accessed via the ID line with the first memory element enabled, and

wherein the second memory element is enabled in response to the second data on the second data line and a first logic level on the ID line.

5. The integrated circuit of claim 4, further comprising:

a fluid actuation device enabled in response to a second logic level on the ID line.

6. The integrated circuit of any of claims 1-5, wherein the first memory element comprises a non-volatile memory element and the second memory element comprises a non-volatile memory element.

7. An integrated circuit to drive a plurality of fluid actuation devices, the integrated circuit comprising:

an ID line;

a first select line;

a second select line;

a first memory element enabled in response to a first logic level on the first select line; and

a second memory element enabled in response to a first logic level on the second select line and a first logic level on the ID line.

8. The integrated circuit of claim 7, further comprising:

a fire line electrically coupled to the second memory element,

wherein the first memory element is accessed via the ID line with the first memory element enabled, and

wherein the second memory element is accessed via the fire line with the second memory element enabled.

9. The integrated circuit of claim 7 or 8, further comprising:

a fluid actuation device enabled in response to a first logic level on the second select line and a second logic level on the ID line.

10. The integrated circuit of claim 9, further comprising:

a fire line electrically coupled to the second memory element and the fluid actuation device,

wherein the first memory element is accessed via the ID line with the first memory element enabled,

wherein the second memory element is accessed via the fire line with the second memory element enabled; and

wherein the fluid actuation device is activated via the fire line with the fluid actuation device enabled.

11. The integrated circuit of any of claims 7-10, further comprising:

a plurality of first data lines; and

a second data line,

wherein the first memory element is enabled in response to first data on the plurality of first data lines and a first logic level on the first select line, and

wherein the second memory element is enabled in response to second data on the second data line, a first logic level on the second select line, and a first logic level on the ID line.

12. The integrated circuit of any of claims 7-11, wherein the first memory element comprises an erasable programmable read-only memory element and the second memory element comprises a programmable fuse.

13. An inkjet cartridge comprising a printhead including an integrated circuit of any of claims 7-12.

14. A method for accessing a first memory and a second memory of a fluid ejection device, the method comprising:

sequentially generating a first select signal and a second select signal;

enabling a first memory element in response to the first select signal and first data on a plurality of first data lines; and

enabling a second memory element in response to the second select signal and second data on a second data line.

15. The method of claim 14, further comprising:

generating an address signal,

wherein enabling the second memory element comprises enabling the second memory element in response to the second select signal, the second data on the second data line, and the address signal.

16. The method of claim 14 or 15, further comprising:

generating a signal on an ID line; and

enabling a fluid actuation device in response to the second select signal and a first logic level on the ID line,

wherein enabling the second memory element comprises enabling the second memory element in response to the second select signal and a second logic level on the ID line.

17. The method of claim 16, further comprising:

accessing the first memory element via the ID line with the first memory element enabled; and

accessing the second memory element via a fire line with the second memory element enabled.

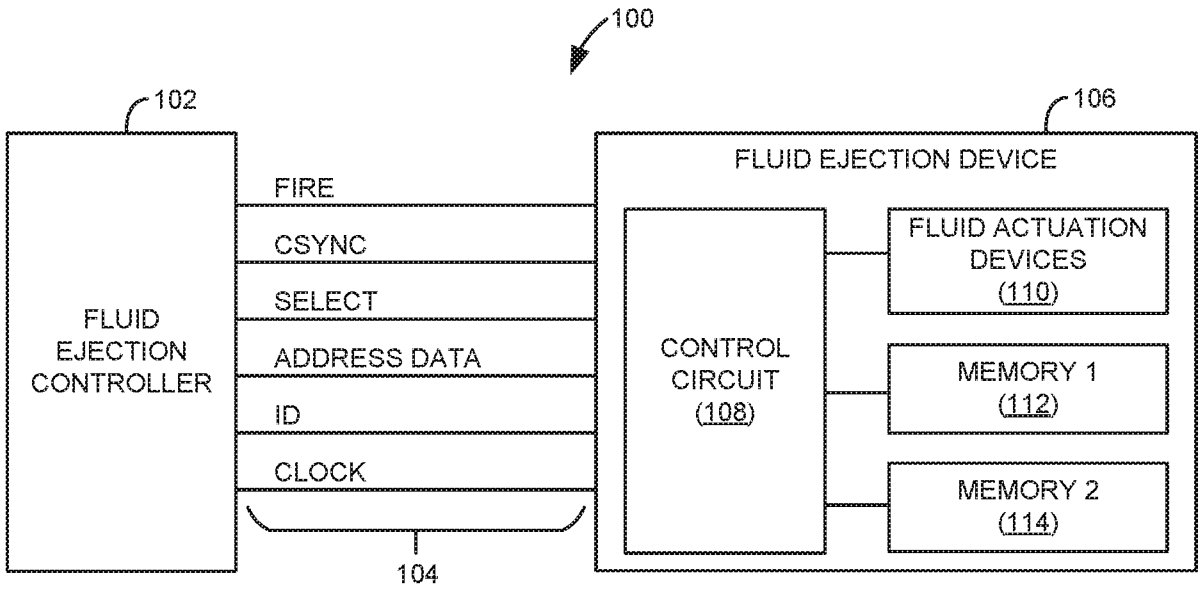

100
102
106
FLUID EJECTION DEVICE
FLUID EJECTION CONTROLLER
FIRE
CSYNC
SELECT
ADDRESS DATA
ID
CLOCK
104
CONTROL CIRCUIT (108)
FLUID ACTUATION DEVICES (110)
MEMORY 1 (112)
MEMORY 2 (114)

Fig. 1

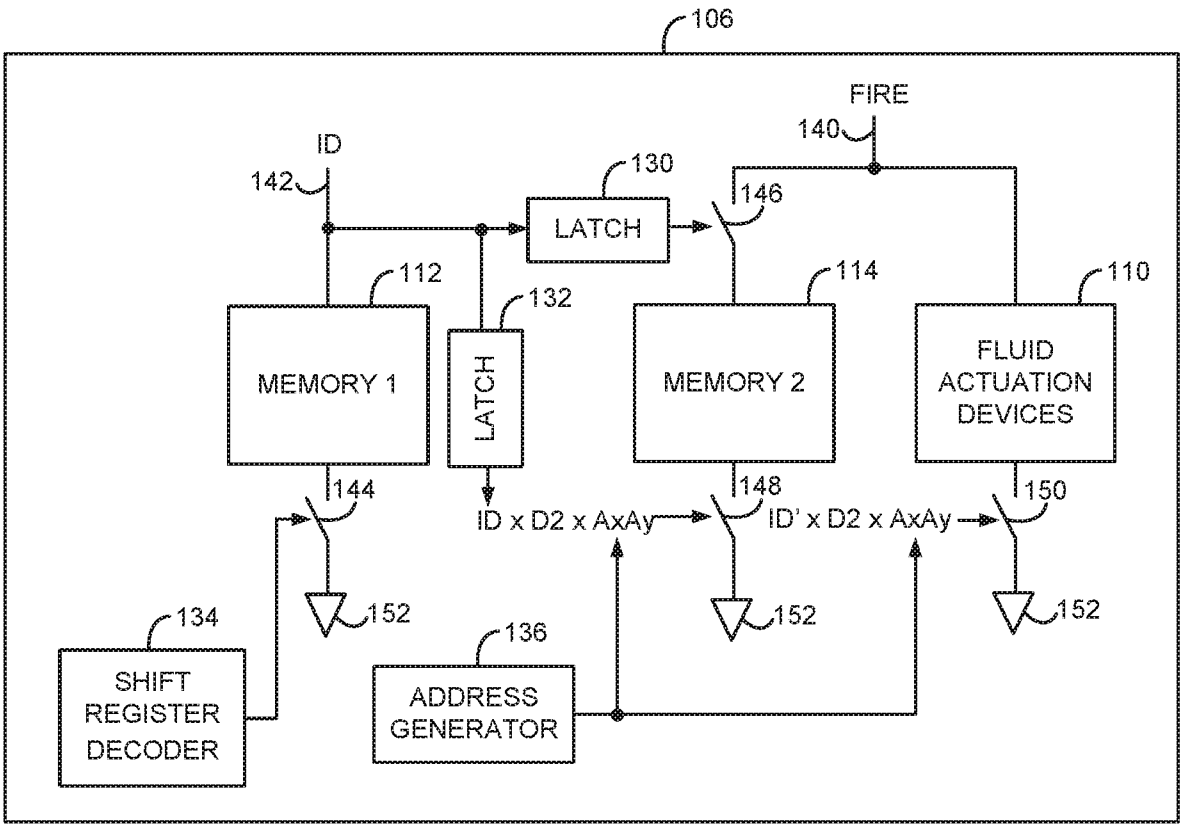

106
FIRE
140
ID
142
130
LATCH
146
112
132
114
110
MEMORY 1
LATCH
MEMORY 2
FLUID ACTUATION DEVICES
144
ID x D2 x AxAy
148
ID' x D2 x AxAy
150
152
152
152
134
SHIFT REGISTER DECODER
136
ADDRESS GENERATOR

Fig. 2

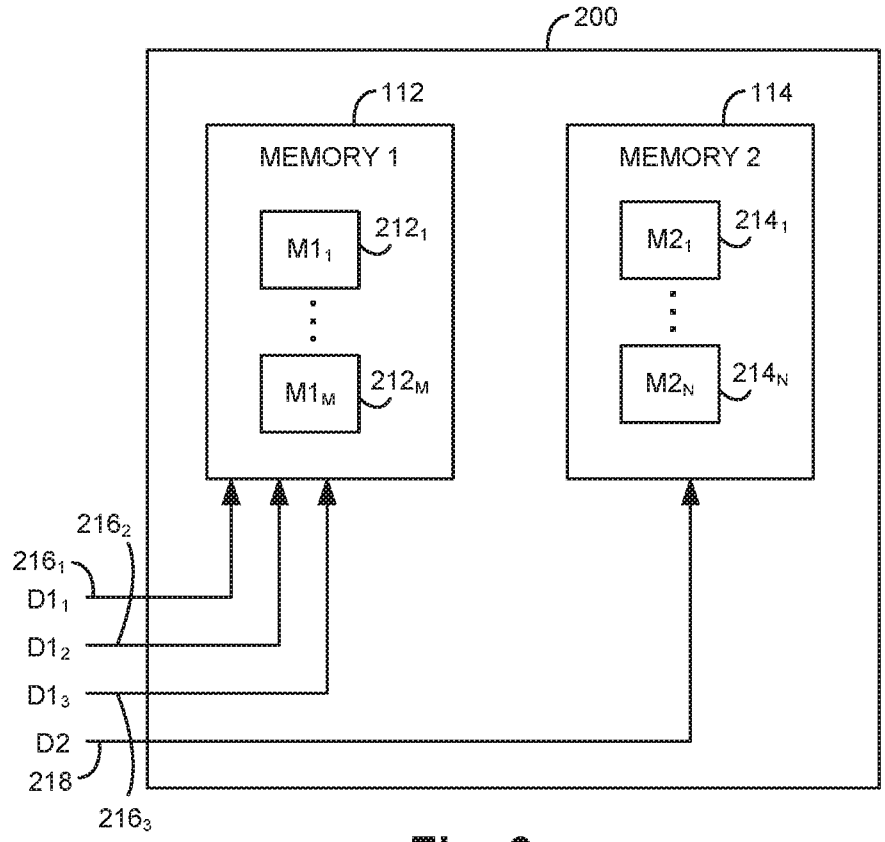

200
112
MEMORY 1
M1$_1$
212$_1$
M1$_M$
212$_M$
114
MEMORY 2
M2$_1$
214$_1$
M2$_N$
214$_N$
216$_2$
216$_1$
D1$_1$
D1$_2$
D1$_3$
D2
218
216$_3$

Fig. 3

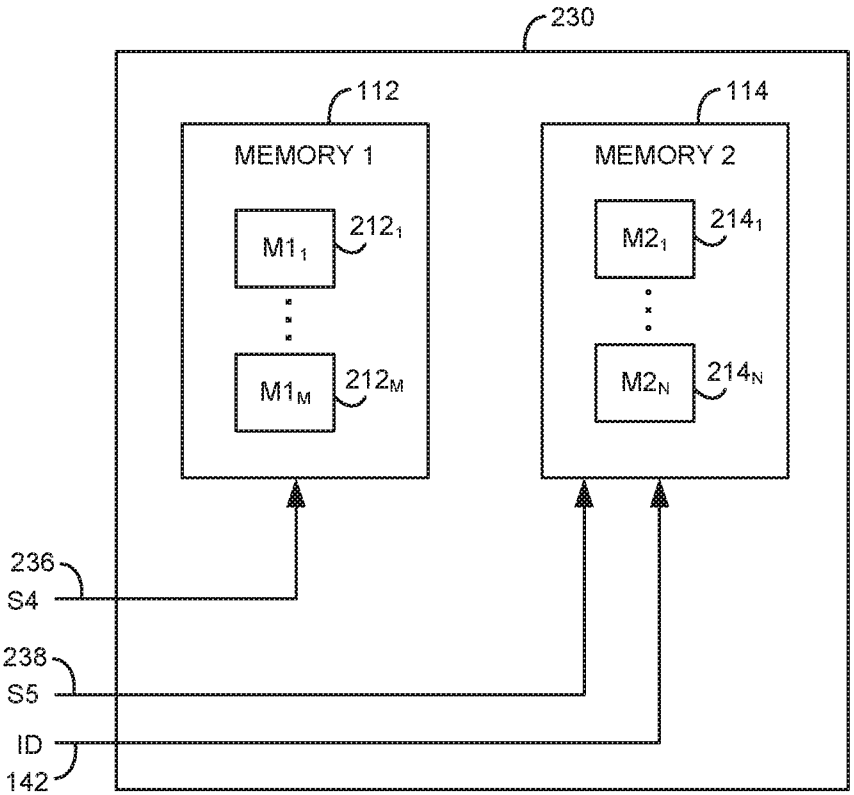

230
112
MEMORY 1
M1$_1$
212$_1$
M1$_M$
212$_M$
114
MEMORY 2
M2$_1$
214$_1$
M2$_N$
214$_N$
236
S4
238
S5
ID
142

Fig. 4

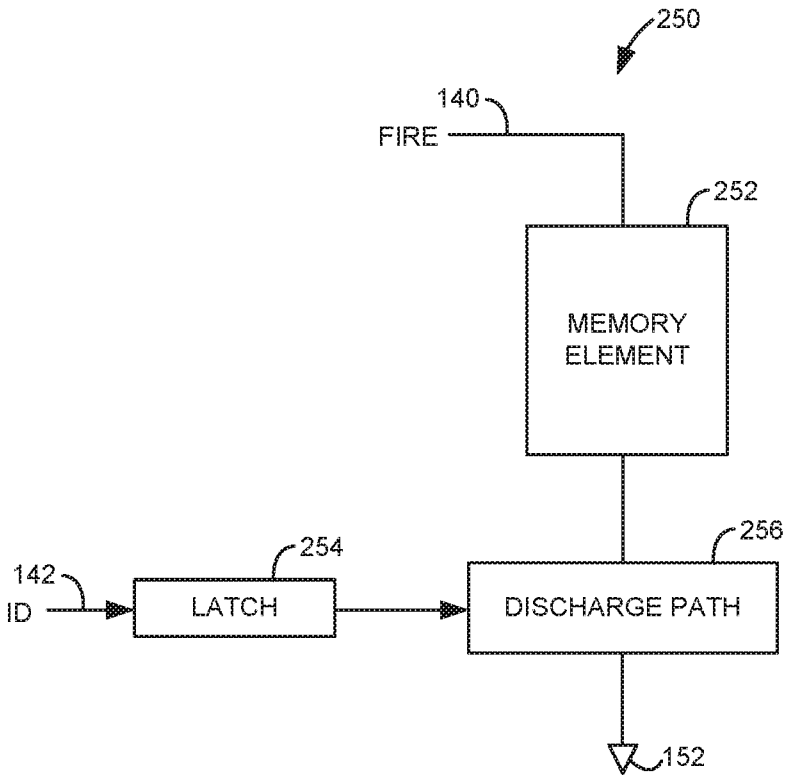

250
140
FIRE
252
MEMORY ELEMENT
256
254
142
ID
LATCH
DISCHARGE PATH
152

Fig. 5

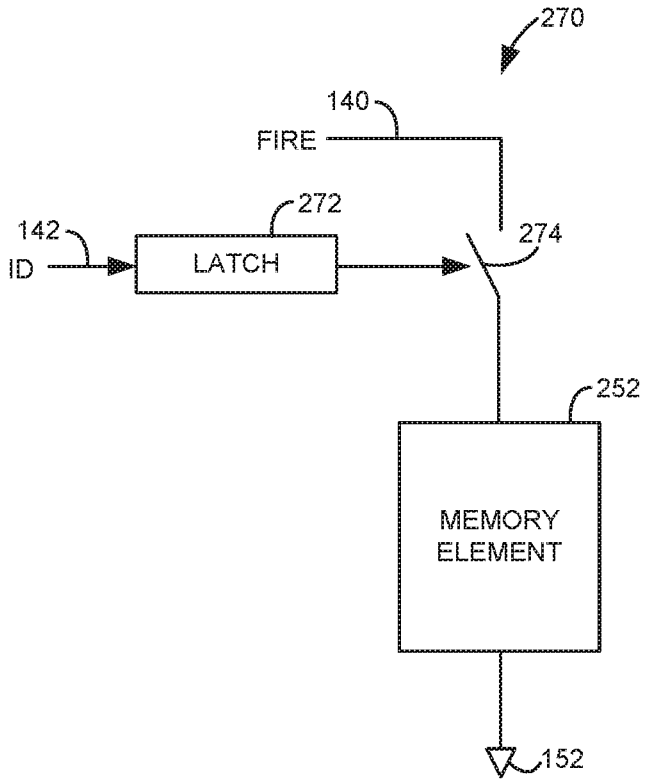

270
140
FIRE
272
142
ID
LATCH
274
252
MEMORY ELEMENT
152

Fig. 6

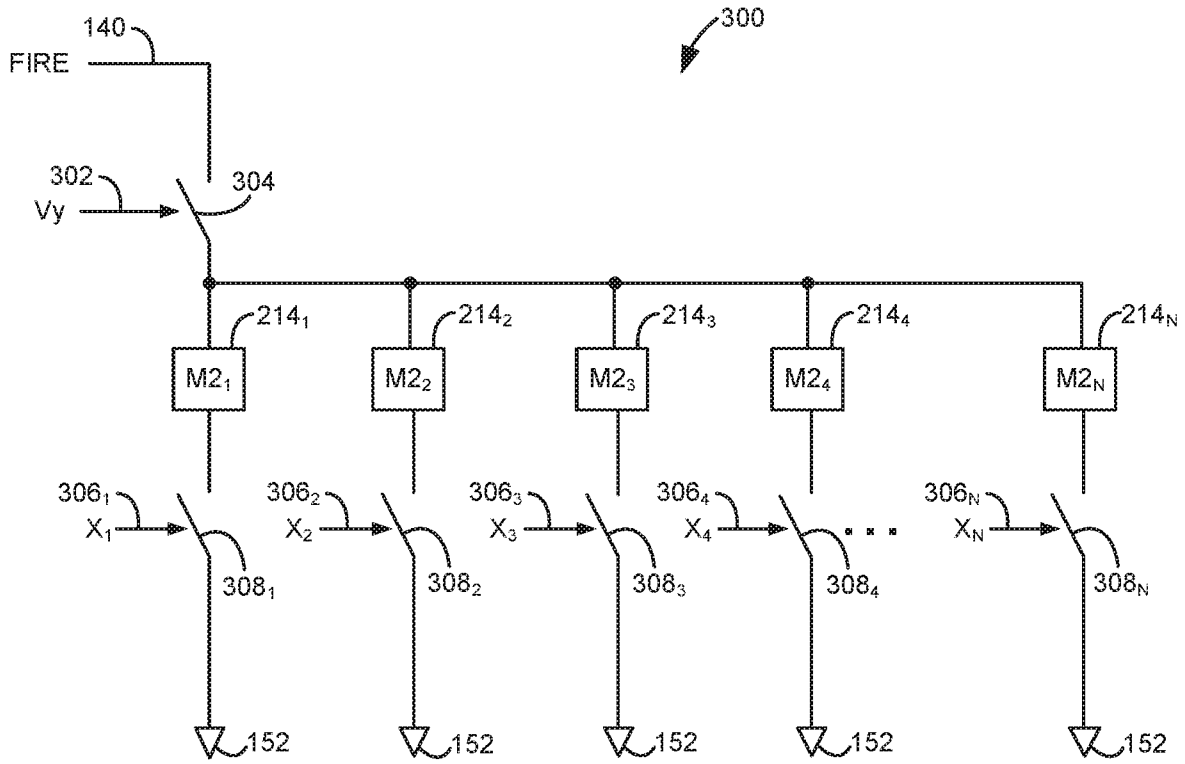

140
FIRE
300
302
Vy
304
214$_1$
214$_2$
214$_3$
214$_4$
214$_N$
M2$_1$
M2$_2$
M2$_3$
M2$_4$
M2$_N$
306$_1$
X$_1$
306$_2$
X$_2$
306$_3$
X$_3$
306$_4$
X$_4$
306$_N$
X$_N$
308$_1$
308$_2$
308$_3$
308$_4$
308$_N$
152

Fig. 7A

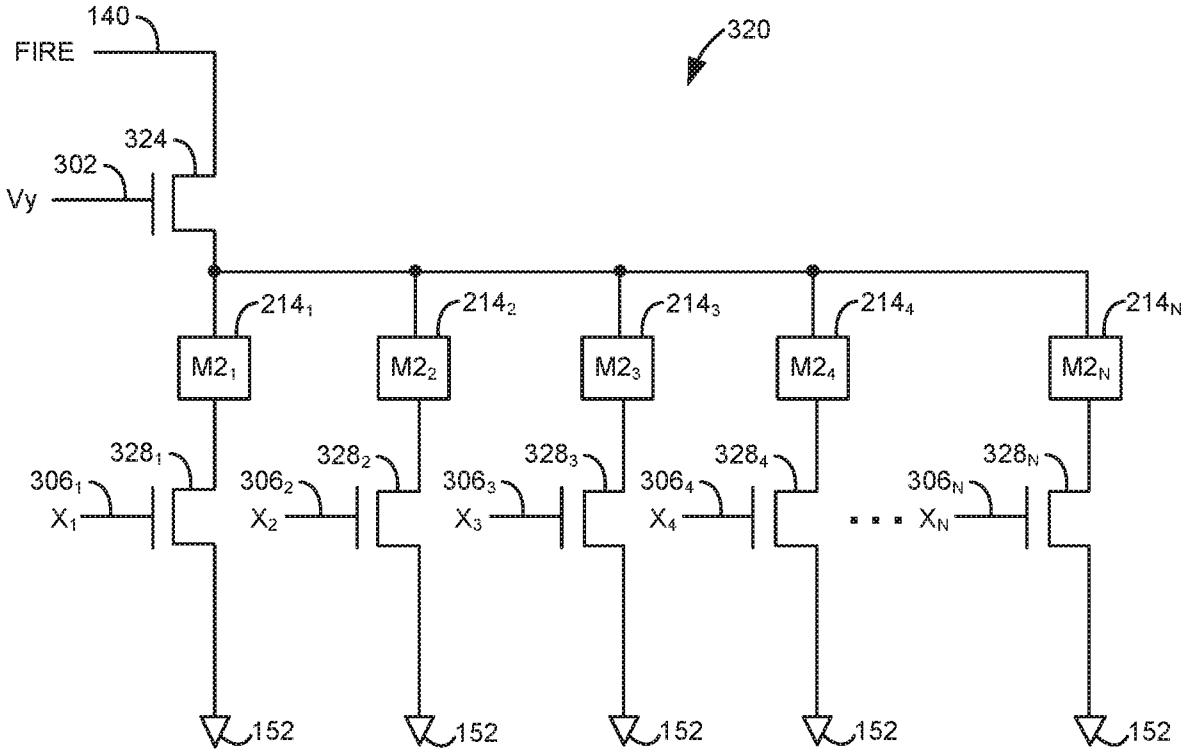

140
FIRE
320
324
302
Vy
214$_1$
214$_2$
214$_3$
214$_4$
214$_N$
M2$_1$
M2$_2$
M2$_3$
M2$_4$
M2$_N$
328$_1$
328$_2$
328$_3$
328$_4$
328$_N$
306$_1$
X$_1$
306$_2$
X$_2$
306$_3$
X$_3$
306$_4$
X$_4$
306$_N$
X$_N$
152

Fig. 7B

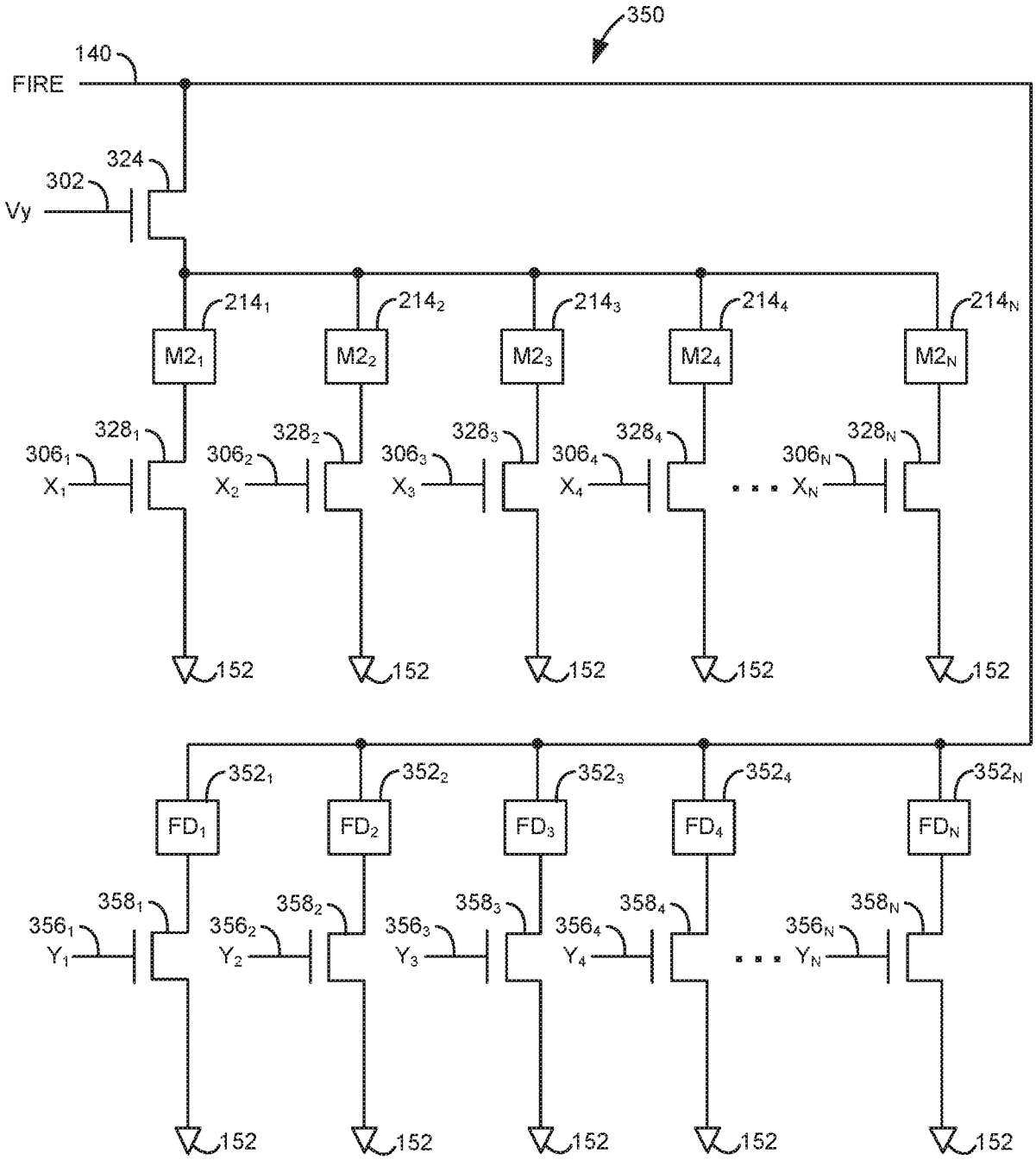

350
140
FIRE
324
302
Vy
214$_1$
214$_2$
214$_3$
214$_4$
214$_N$
M2$_1$
M2$_2$
M2$_3$
M2$_4$
M2$_N$
328$_1$
328$_2$
328$_3$
328$_4$
328$_N$
306$_1$
306$_2$
306$_3$
306$_4$
306$_N$
X$_1$
X$_2$
X$_3$
X$_4$
X$_N$
152
352$_1$
352$_2$
352$_3$
352$_4$
352$_N$
FD$_1$
FD$_2$
FD$_3$
FD$_4$
FD$_N$
358$_1$
358$_2$
358$_3$
358$_4$
358$_N$
356$_1$
356$_2$
356$_3$
356$_4$
356$_N$
Y$_1$
Y$_2$
Y$_3$
Y$_4$
Y$_N$

Fig. 8A

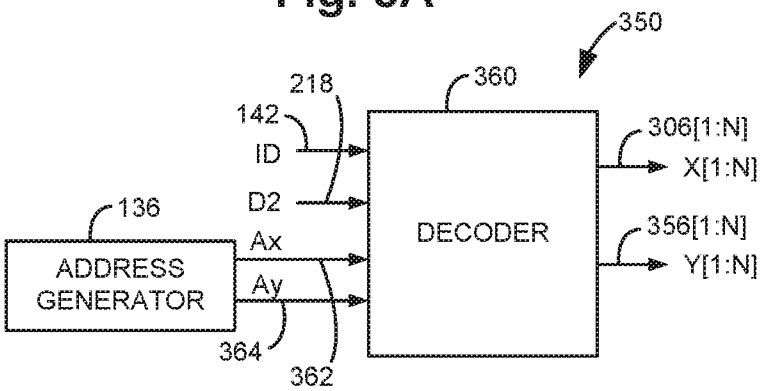

350
360
218
142
ID
D2
136
ADDRESS GENERATOR
Ax
Ay
364
362
DECODER
306[1:N]
X[1:N]
356[1:N]
Y[1:N]

Fig. 8B

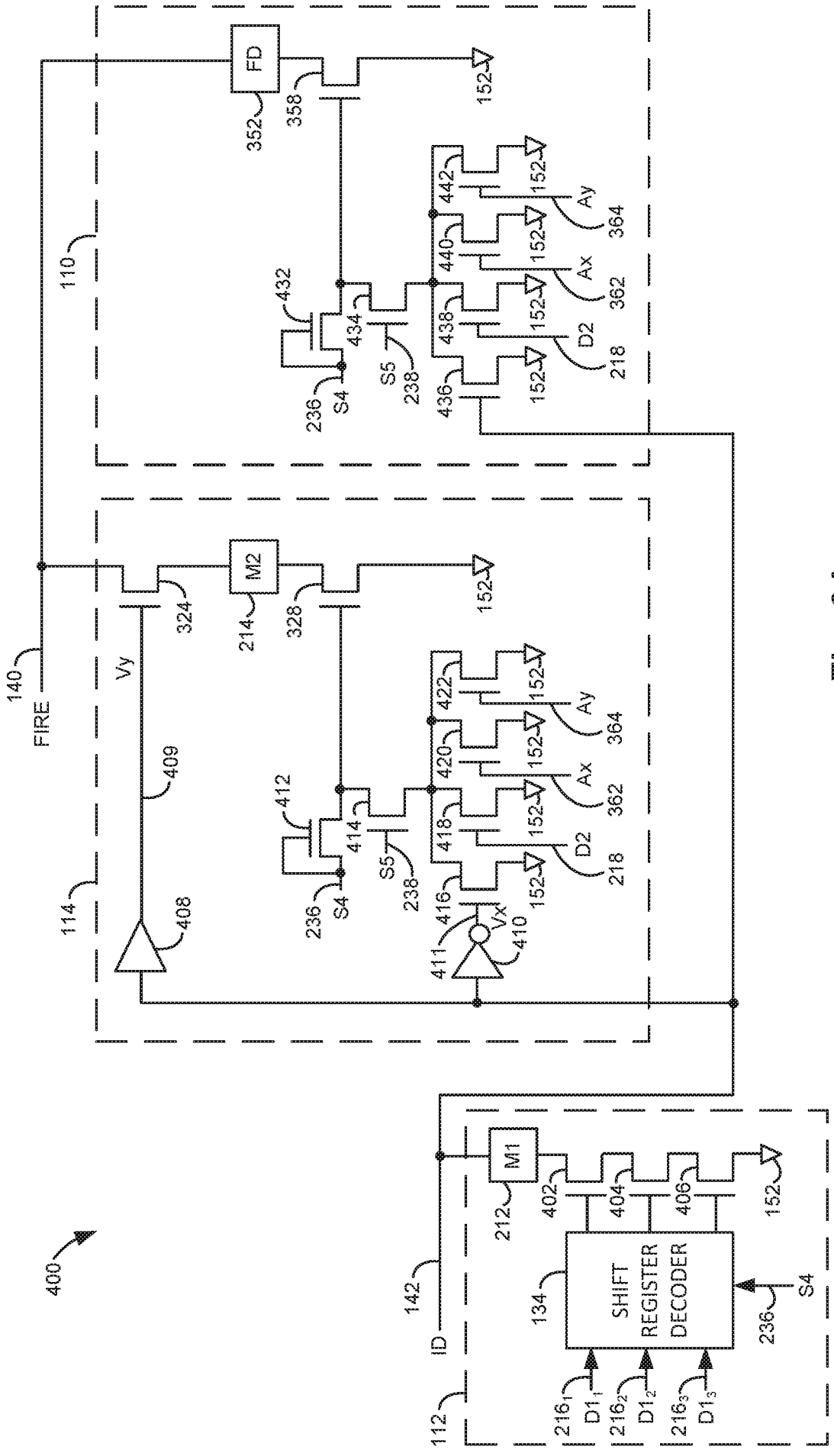

400
112
142
ID
212
M1
402
404
406
152
134
SHIFT REGISTER DECODER
236
S4
216$_1$
D1$_1$
216$_2$
D1$_2$
216$_3$
D1$_3$
110
114
140
FIRE
Vy
324
214
M2
328
409
408
Vx
410
411
412
414
416
418
420
422
S5
238
236
S4
D2
218
Ax
362
Ay
364
352
FD
358
432
434
436
438
440
442

Fig. 9A

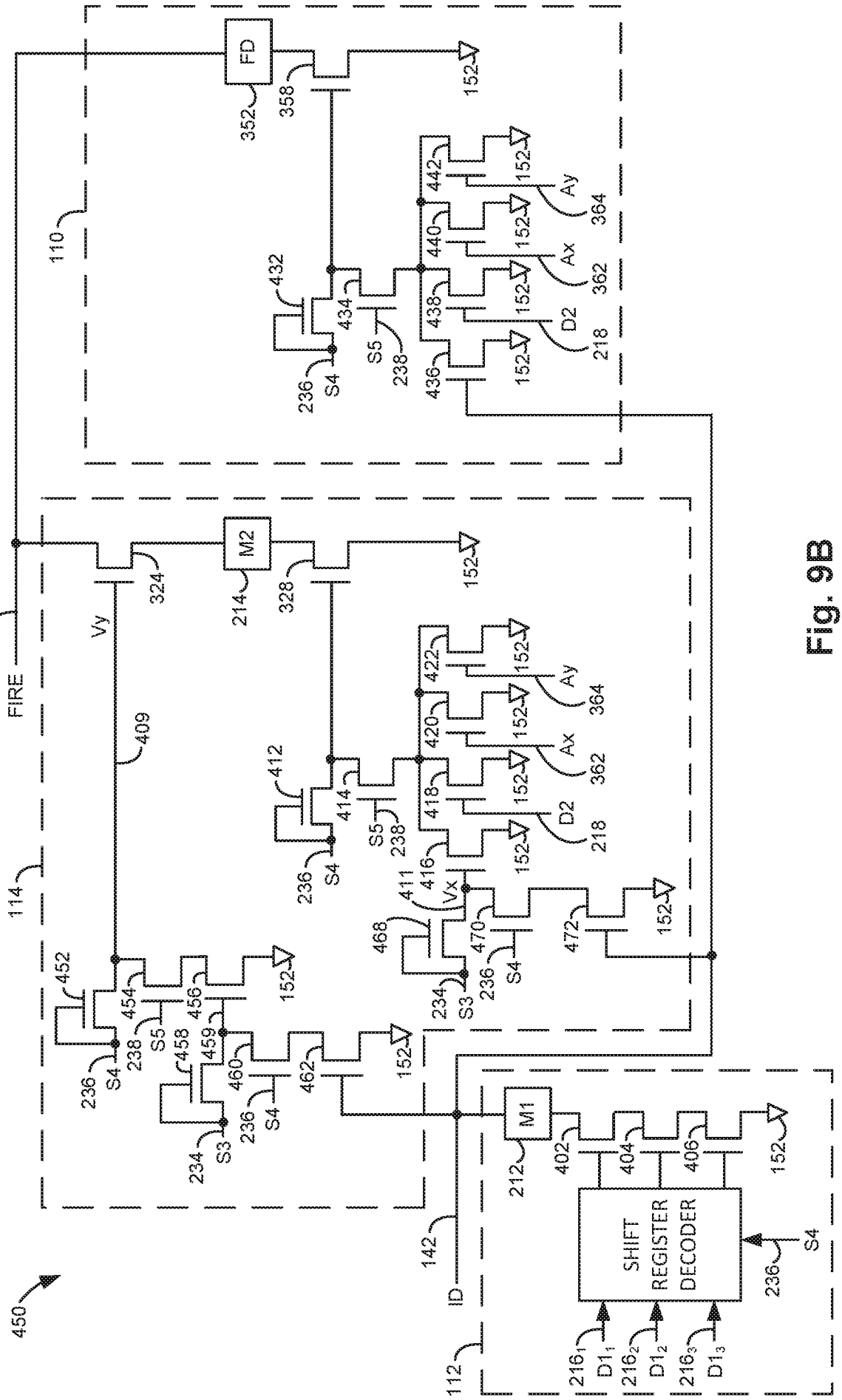

450
112
142
ID
216
D1
SHIFT REGISTER DECODER
212
M1
402
404
406
152
236
S4
234
S3
460
462
458
459
454
456
452
238
S5
114
409
Vy
324
214
M2
328
140
FIRE
110
352
FD
358
432
434
436
438
440
442
Ax
Ay
362
364
218
D2
412
414
416
418
420
422
411
Vx
468
470
472

Fig. 9B

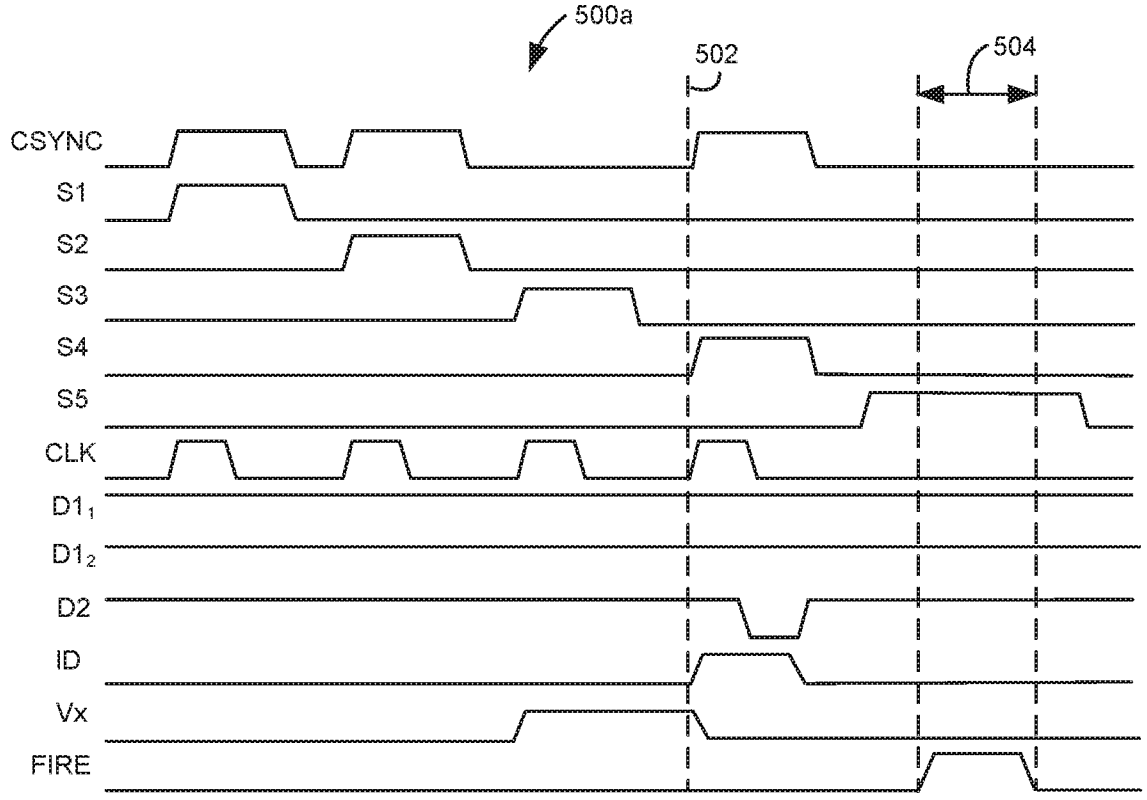


Fig. 10A

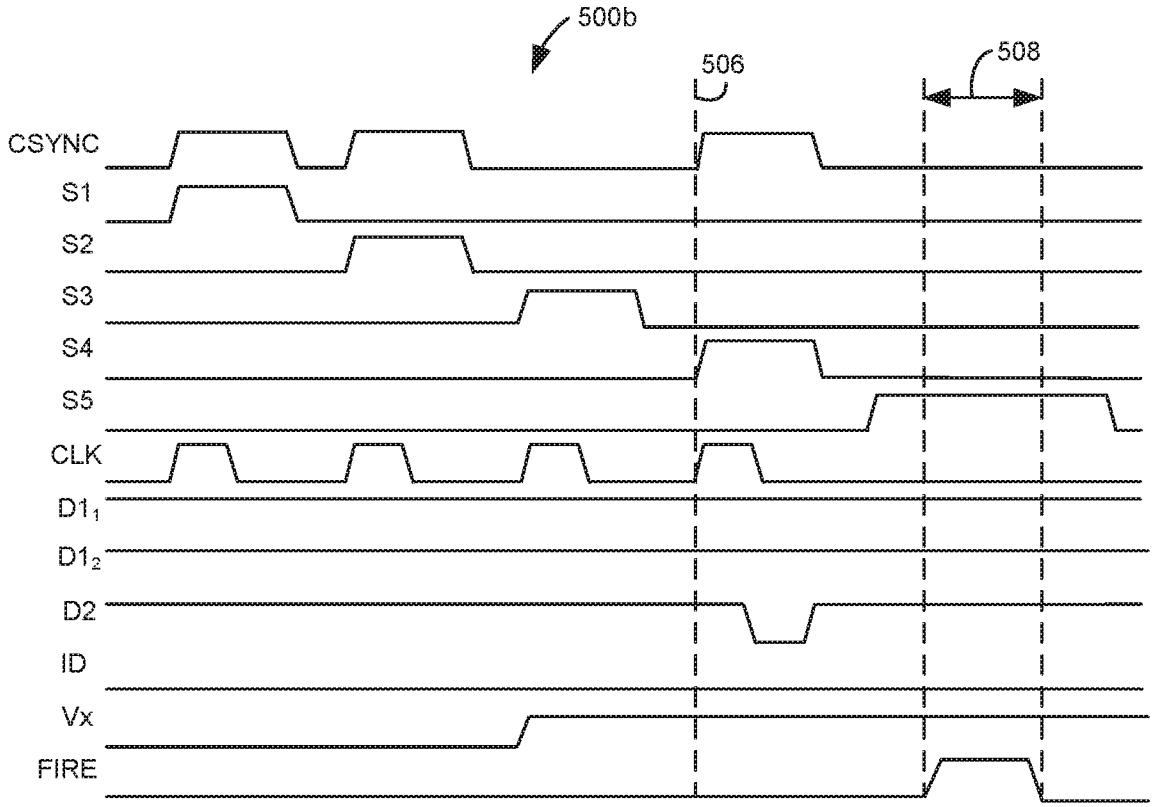


Fig. 10B

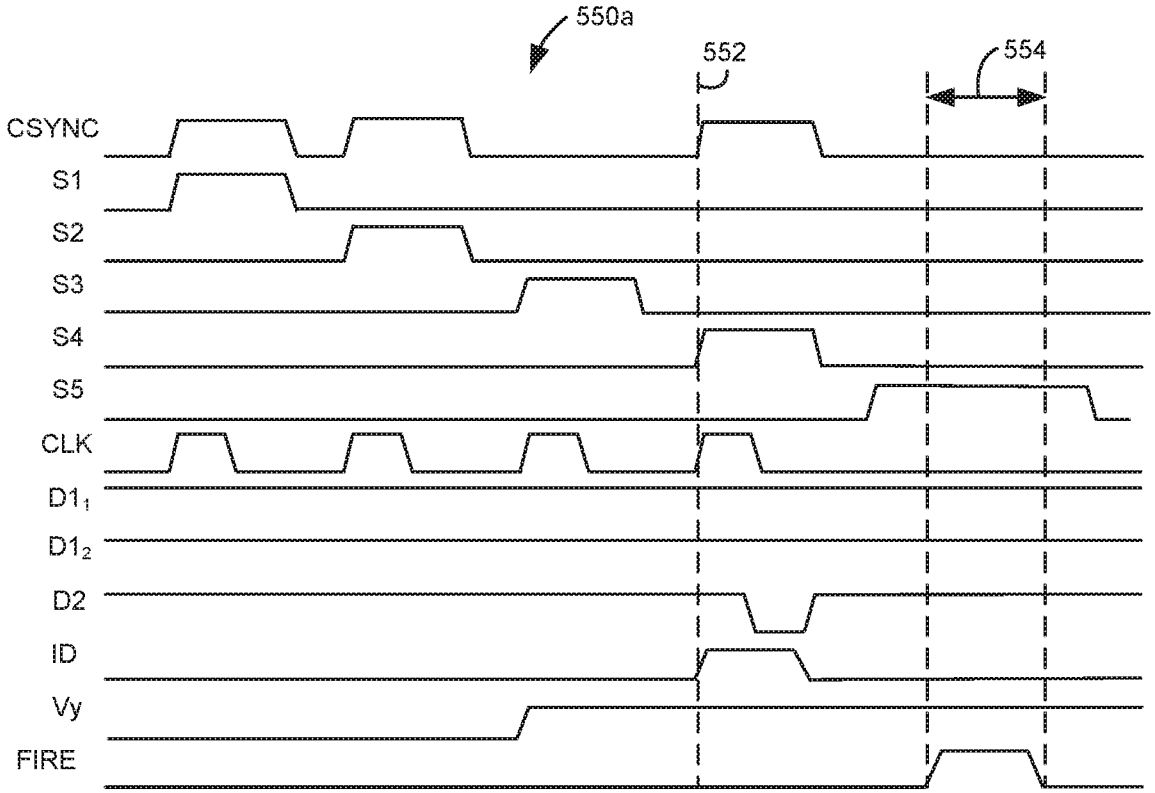


Fig. 11A

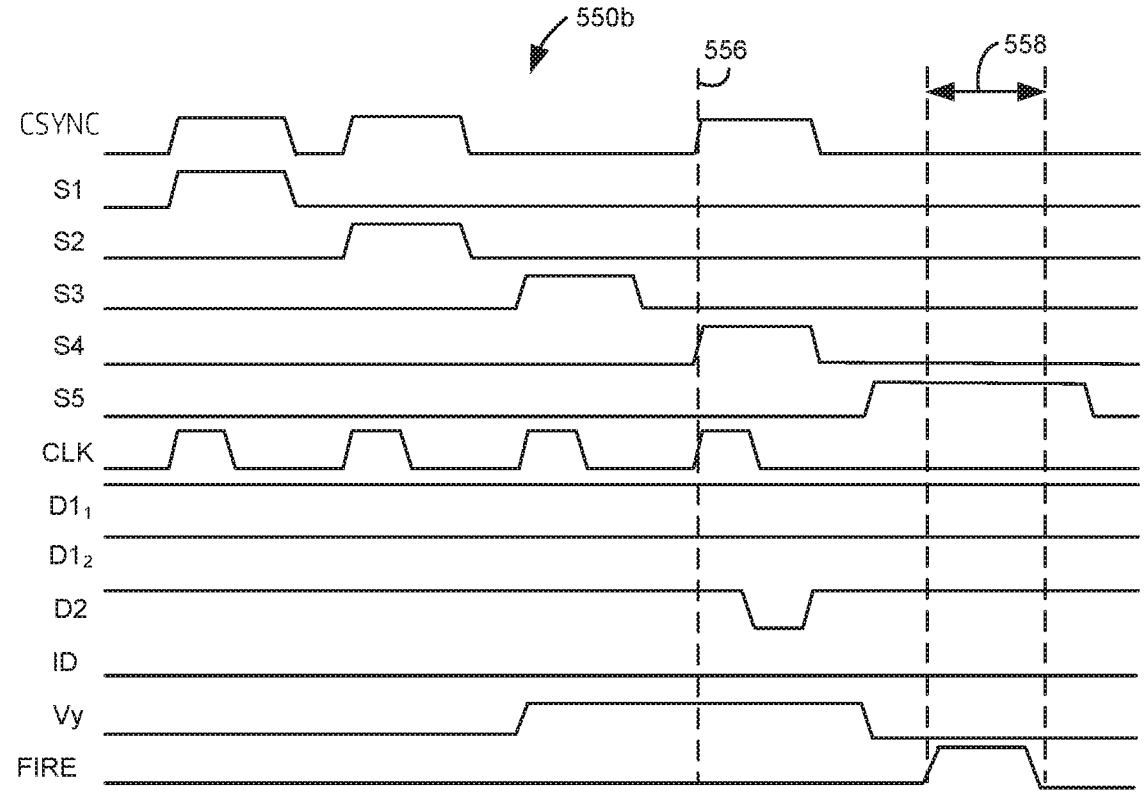


Fig. 11B

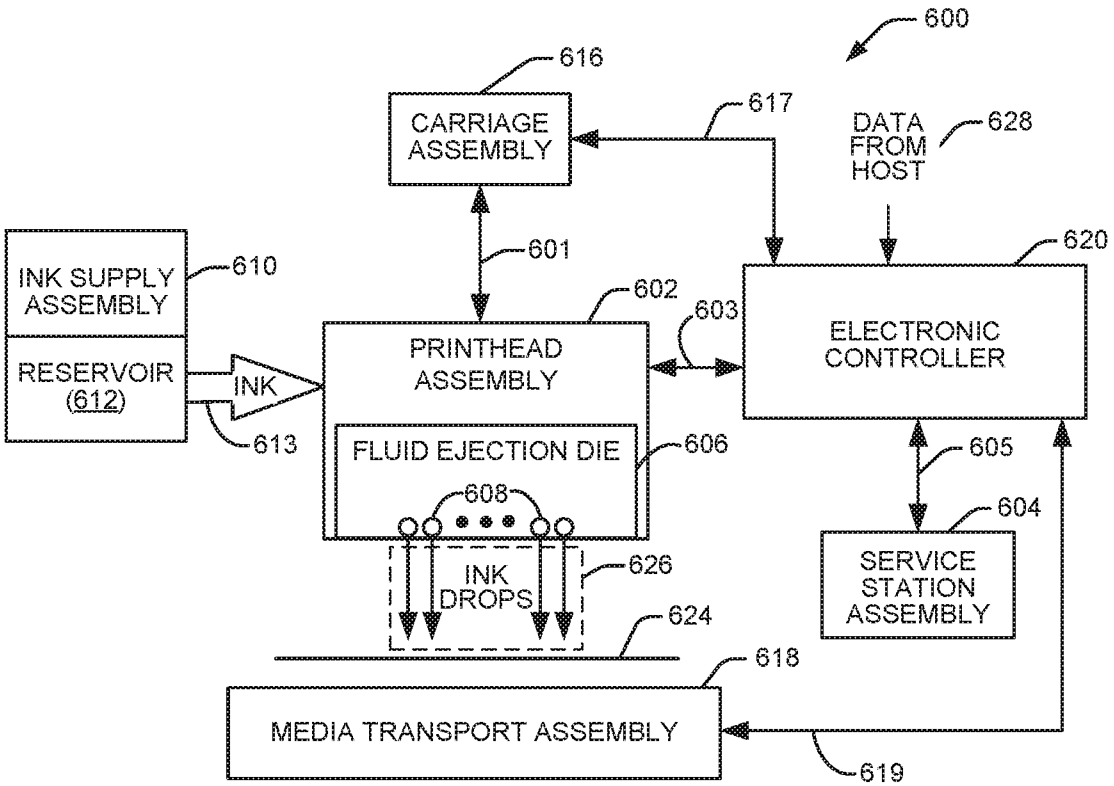

600
616
CARRIAGE ASSEMBLY
617
DATA FROM HOST
628
601
620
INK SUPPLY ASSEMBLY
610
602
603
PRINTHEAD ASSEMBLY
ELECTRONIC CONTROLLER
RESERVOIR (612)
INK
613
FLUID EJECTION DIE
606
605
608
604
SERVICE STATION ASSEMBLY
INK DROPS
626
624
618
MEDIA TRANSPORT ASSEMBLY
619

Fig. 12

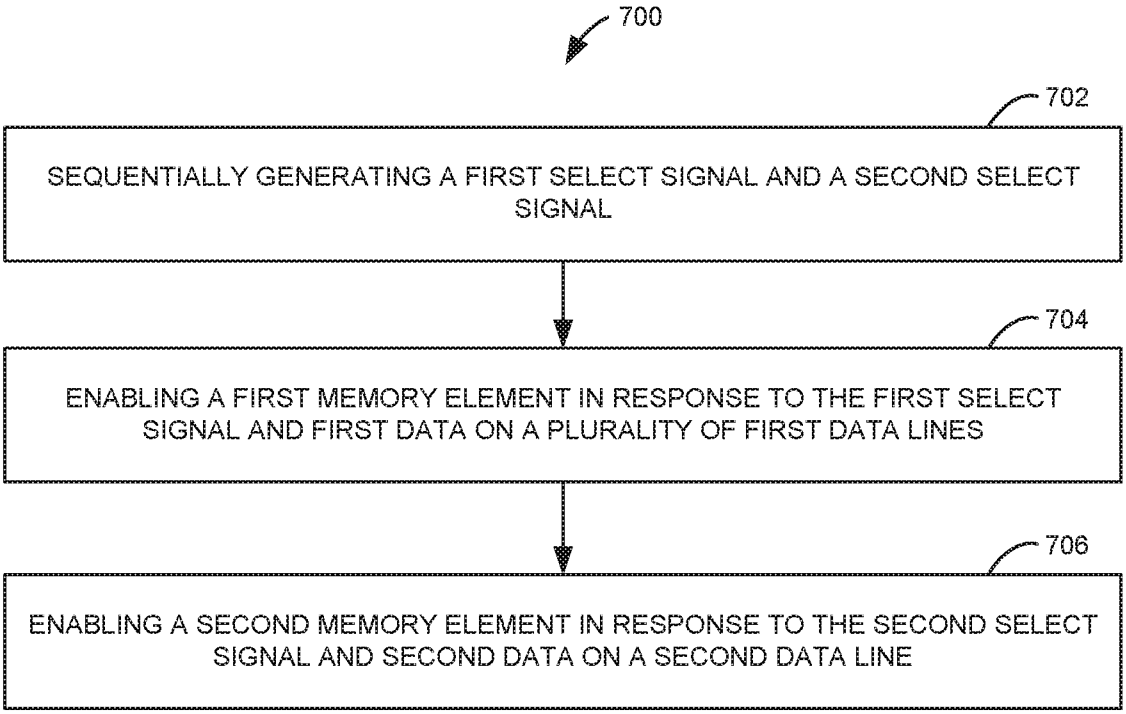


Fig. 13A

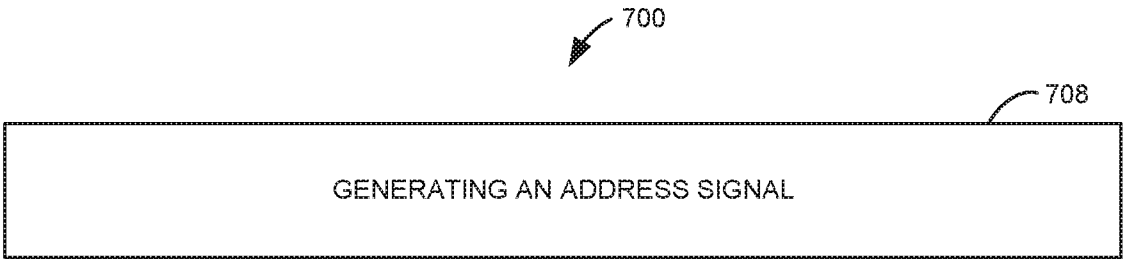


Fig. 13B

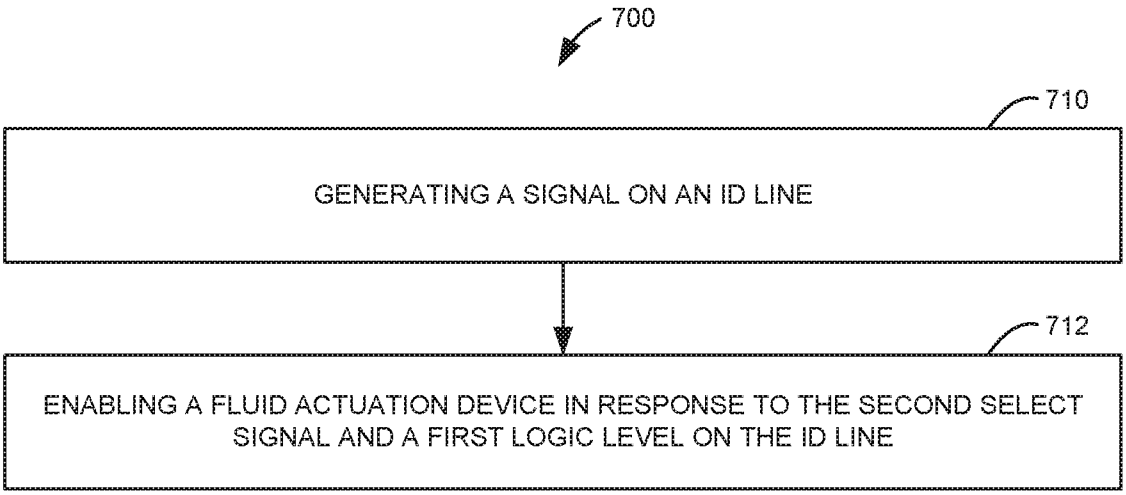


Fig. 13C

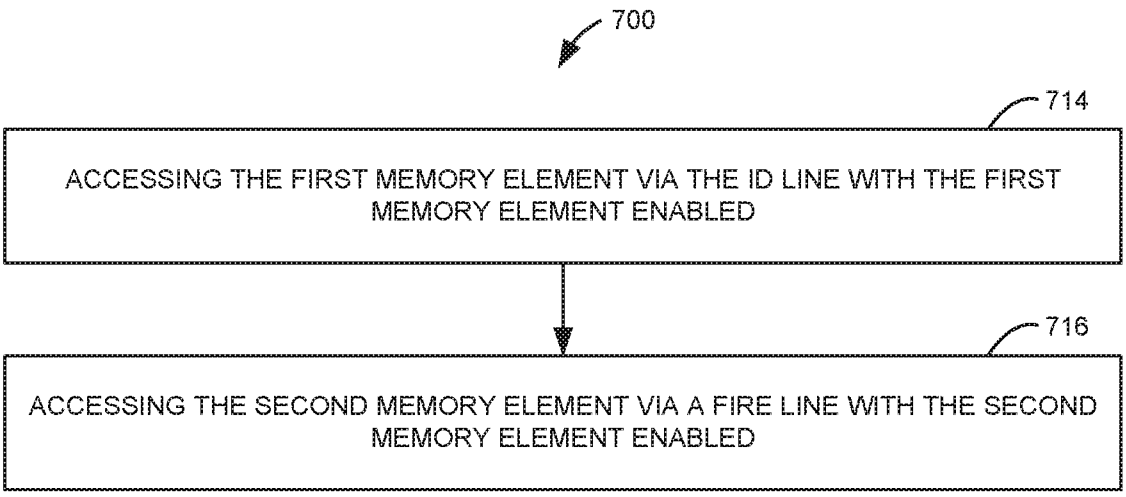


Fig. 13D

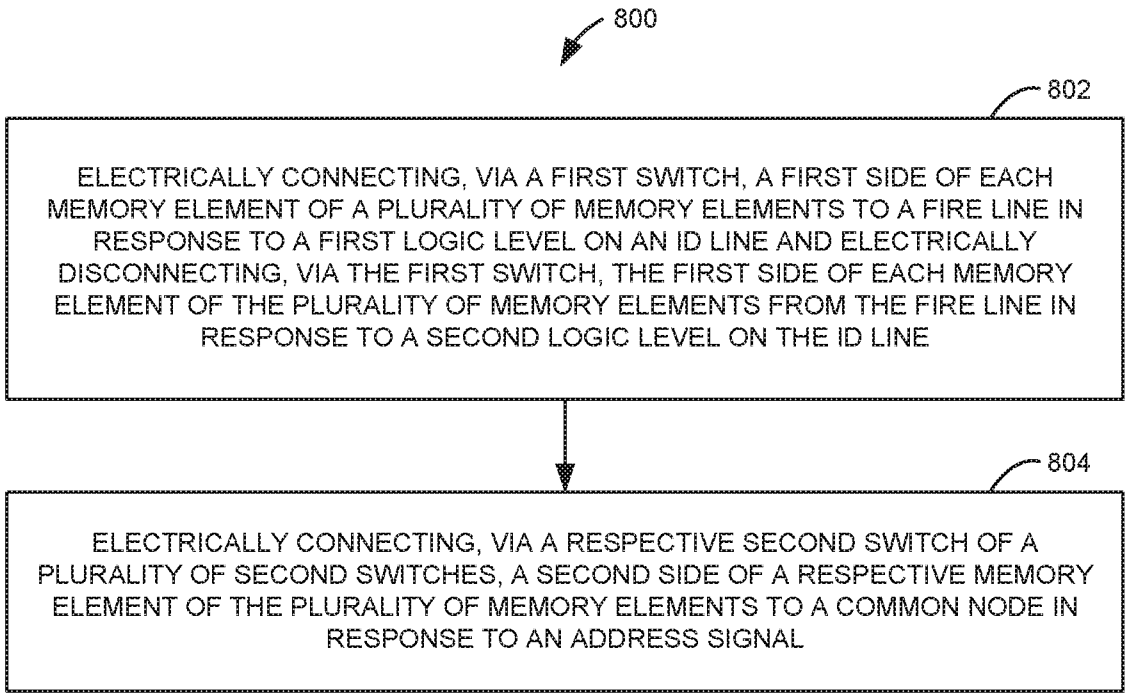


Fig. 14A

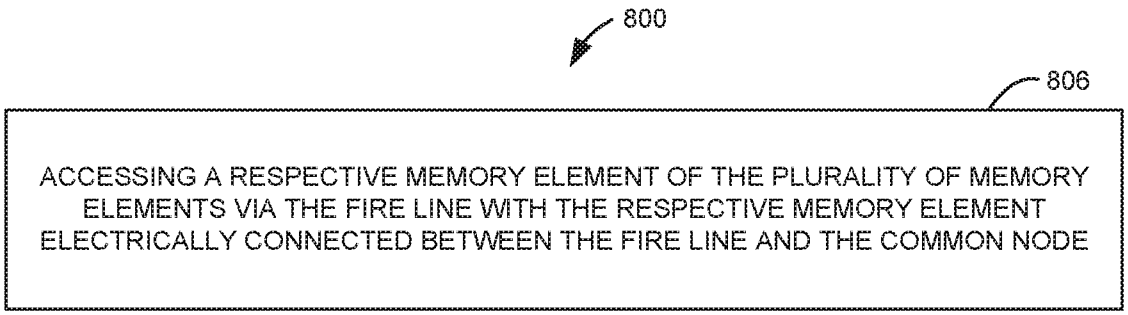


Fig. 14B

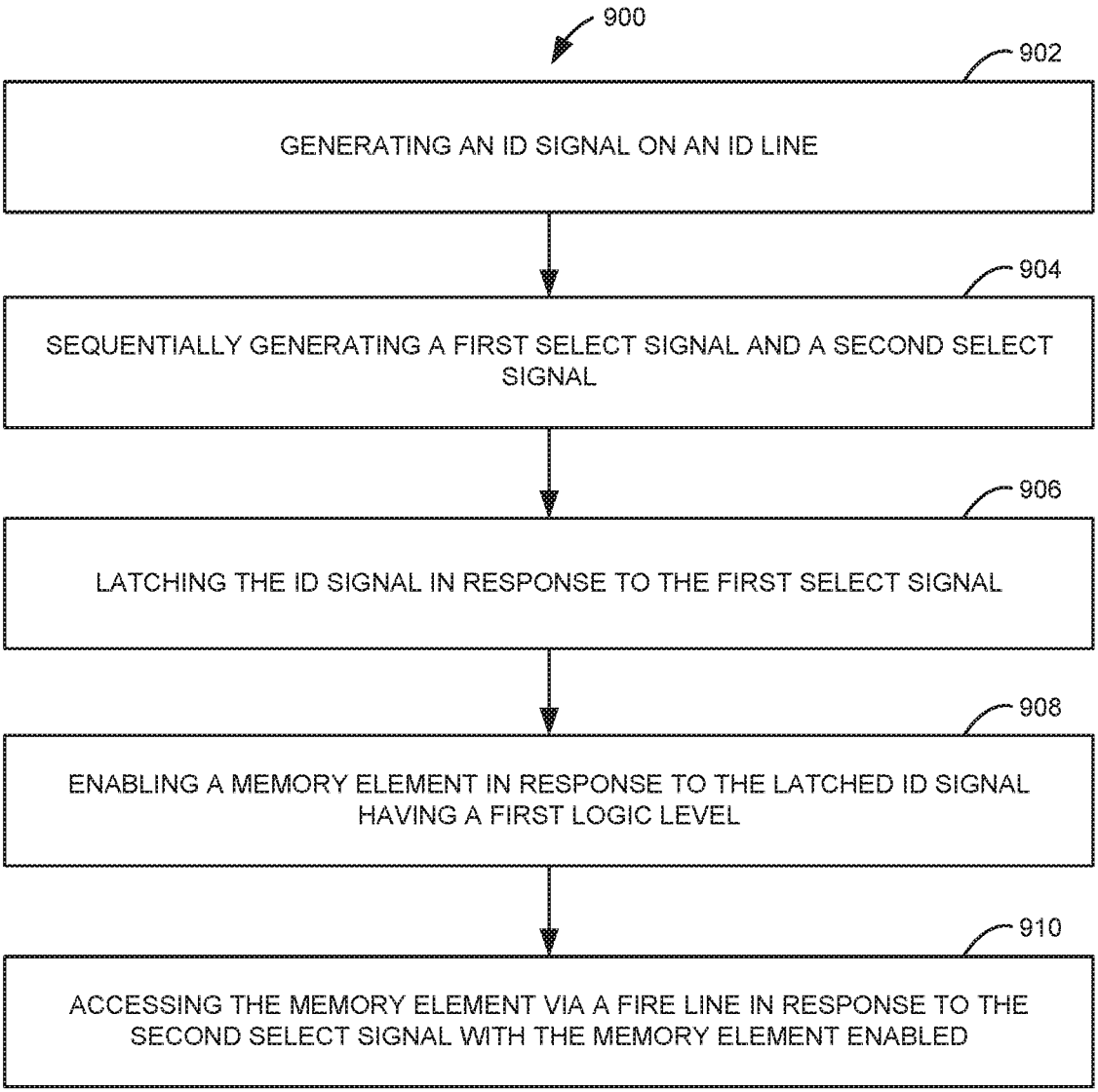


Fig. 15A

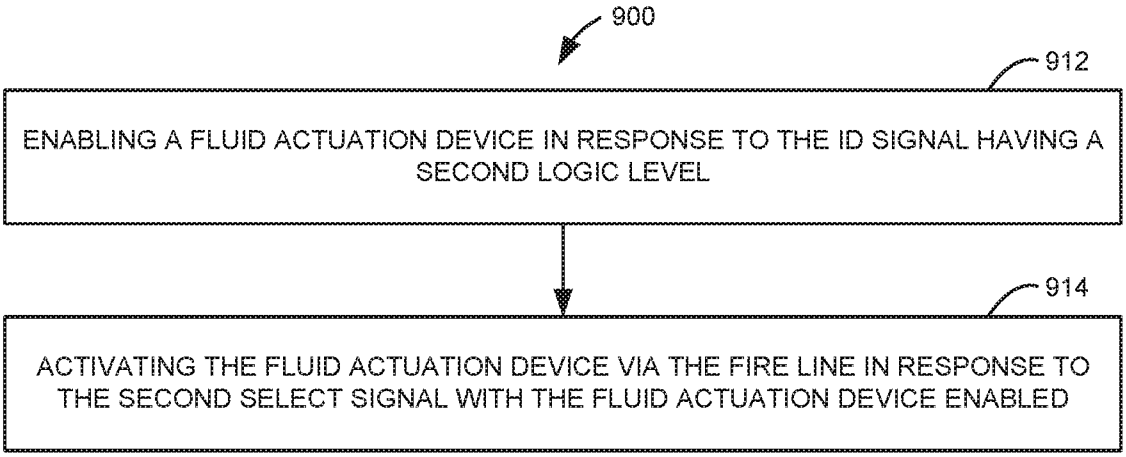


Fig. 15B

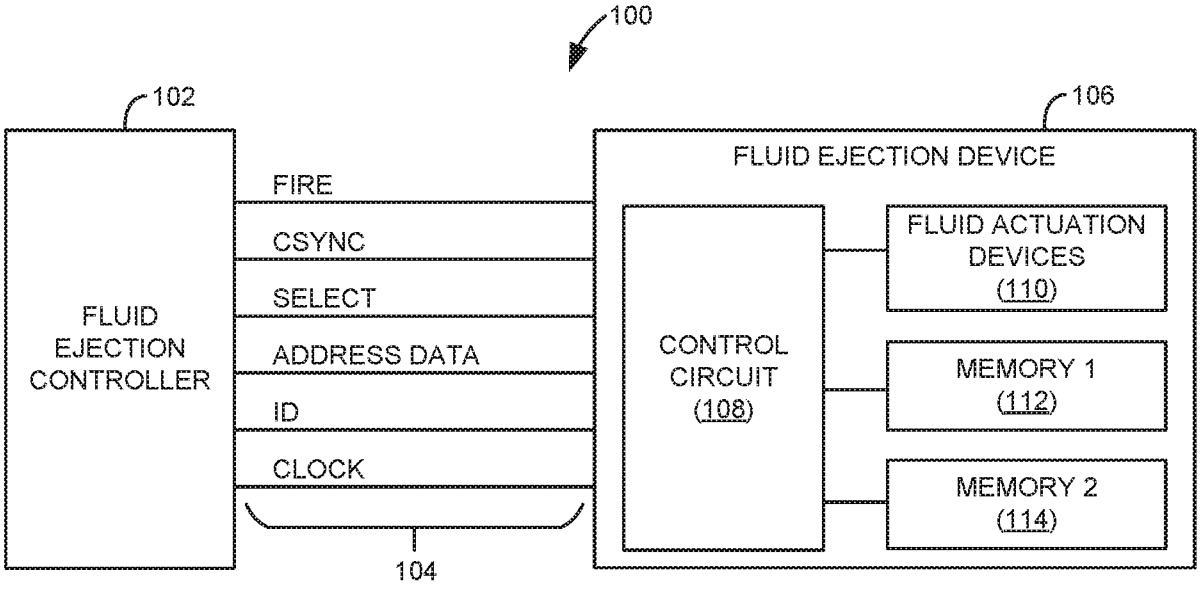

100
102
106
FLUID EJECTION DEVICE
FLUID EJECTION CONTROLLER
FIRE
CSYNC
SELECT
ADDRESS DATA
ID
CLOCK
104
CONTROL CIRCUIT (108)
FLUID ACTUATION DEVICES (110)
MEMORY 1 (112)
MEMORY 2 (114)

Fig. 1