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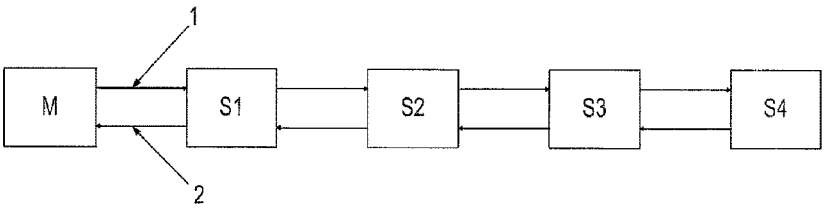
(54) Titre : PROCEDE D'INTEGRATION D'UN AUTRE ABONNE DE BUS DANS UN SYSTEME DE BUS, ET SYSTEME DE BUS

(54) Title: METHOD FOR INTEGRATING A FURTHER BUS SUBSCRIBER INTO A BUS SYSTEM, AND BUS SYSTEM



(57) Abrégé/Abstract:
A method for integrating a further bus subscriber into a bus system, and bus system, having a master module and bus subscribers arranged in series, having the chronologically successive method steps of: a first method step involving the further bus subscriber sending a data packet to the master module in order to register with the master module, a second method step involving a bus subscriber arranged between the further bus subscriber and the master module stopping the data packet and checking whether the bus system has already been given clearance, a third method step involving the bus subscriber forwarding the data packet to the master module if the bus system has hitherto not been given clearance, or a, in particular alternative, third method step, when the bus system has already been given clearance, involving the bus subscriber storing the data packet and waiting until the clearance for the bus system is cancelled, and, after the clearance has been cancelled, forwarding the stored data packet to the master module.

Abstract:

A method for integrating a further bus subscriber into a bus system, and a bus system, having a master module and subscribers disposed in series, having the temporally consecutive method steps: in a first method step, the further bus subscriber transmits a data packet to the master module in order to log in to the master module, and in a second method step, a bus subscriber disposed between the further bus subscriber and the master module stops the data packet and checks whether the bus system has already received a release, and in a third method step, the first bus subscriber forwards the data packet to the master module if the bus system has not yet received a release, or in a third, in particular an alternative, method step, if the bus system has already received a release, the bus subscriber stores the data packet and waits until the release of the bus system is revoked and after the release has been revoked, forwards the stored data packet to the master module.

METHOD FOR INTEGRATING A FURTHER BUS SUBSCRIBER INTO A BUS SYSTEM, AND BUS SYSTEM

Technical Field

The present invention relates to a method for integrating a further bus subscriber into a bus system, and to a bus system.

Background

The German patent DE 10 2005 056 294 A1 shows a method for allocating addresses to bus subscribers of a bus system, and a plant.

From the European patent EP 1 124 351 A2, a communications protocol for nodes of a daisy chain is known as the most proximate related art.

From the German patent DE 102 15 720 A1, a data bus network is known.

From the European patent EP 0 807 887 A2, a method for addressing a number of peripheral modules of the central unit in a BUS line system is known.

From the German patent DE 196 47 668 A1, a slave station, master station, BUS system, and a method for operating a BUS system is known.

Summary

Therefore, the present invention is based on the objective of further developing a method for integrating a further bus subscriber into a bus system and a bus system, in which the security is to be improved.

According to the present invention, the objective in the method for integrating a further bus subscriber into a bus system is achieved according to the features herein described, and in the bus system, the objective is achieved according to the features herein described.

Important features of the present invention in the method for integrating a further bus subscriber into a bus system, including a master module and bus subscribers disposed

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in series, are that the present method has the following temporally consecutive method steps:

In a first method step, the further bus subscriber sends a data packet to the master module in order to log in to the master module,

and in a second method step, a bus subscriber disposed between the further bus subscriber and the master module stops the data packet and checks whether the bus system has already received a release,

and in a third method step, the bus subscriber forwards the data packet to the master module if the bus system has not yet received a release,

or in a third, in particular an alternative, method step, if the bus system has already received a release, the bus subscriber stores the data packet and waits until the release of the bus system is revoked, and after the release was revoked, forwards the stored data packet to the master module.

This has the advantage that a further bus subscriber, in particular a bus subscriber that requires a longer period of time for the activation, is easily able to be integrated into the bus system retroactively.

In the production mode, i.e. after a granted release, no bus subscriber is advantageously admitted to the bus system.

The admission to the bus system is advantageously blocked with the aid of the bus subscriber situated between the master module and the further bus subscriber, so that the loading of the master module is reduced. This improves the security.

In an advantageous manner, the further bus subscriber is automatically admitted to the bus system in a new startup of the bus system.

In an advantageous embodiment, the master module asks the bus subscribers to log in to the master module in order to initialize the bus system, and in a following method step, a first bus subscriber disposed downstream from the master module logs in to the master module, and in a subsequent method step, the first bus subscriber waits for

a predefined period of time to see whether a second bus subscriber downstream from the first bus subscriber logs in to the master module. This has the advantage that the bus subscribers reduce the loading of the master module. This improves the security.

The predefined period of time is advantageously adaptable to the bus subscribers, so that there is a sufficient wait to allow a bus subscriber that needs a longer period of time for the activation to be logged in securely as well.

In an advantageous embodiment, the first bus subscriber closes the bus system if no second bus subscriber logs in to the master module within the predefined period of time. This has the advantage that the bus system automatically initializes itself with the aid of the present method. The bus system recognizes which one is the bus subscriber most remote from the master module, and this bus subscriber automatically closes the bus system. This relieves an operator of the bus system inasmuch as the operator does not have to connect a terminating impedance within the system. The security is therefore improved.

In an advantageous embodiment, a second bus subscriber logs in to the master module within the predefined period of time and waits a further predefined period of time to see whether a third bus subscriber disposed downstream from the second bus subscriber logs in to the master module, and the second bus subscriber closes the bus system if no third bus subscriber logs in to the master module within the further predefined period of time. This has the advantage that the bus system automatically initializes itself with the aid of the present method. The bus system recognizes which one of the bus subscribers is the one most remote from the master module, and this bus subscriber automatically closes the bus system. This relieves an operator of the bus system inasmuch as the operator does not have to connect a terminating impedance within the system. This improves the security.

In an advantageous embodiment, the release is granted and/or revoked by a control superordinate to the master module. This has the advantage that with the aid of the release, the bus system obtains an external release in an additional method step after a successful initialization. Only after the release does the bus system transition to a production mode in which the bus subscribers are controlled by the master module.

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In an advantageous embodiment, the temporally successive method steps are carried out for the allocation of addresses to the bus subscribers:

In a method step, the master module allocates a first address to a first bus subscriber and transmits this first address to the first bus subscriber, the first address in particular being a natural number n, the first address in particular being O or 1,

and in a following method step, the first bus subscriber increments the first address by one and allocates it to a second bus subscriber as the second address and transmits this second address to the second bus subscriber, the second address in particular being the natural number (n+1),

and in a further method step, the second bus subscriber logs in to the master module with its second address.

This has the advantage that the assignment of the addresses to the bus subscribers takes place automatically. As a result, the initialization of the bus system is able to be executed in a secure and rapid manner.

During the addressing, a data packet advantageously passes an inactive bus subscriber so that the next active bus subscriber of the bus system receives the address and uses it to log in to the master module.

In an advantageous embodiment, in a fourth method step, the second bus subscriber increments the second address by one and allocates this address to a third bus subscriber as the third address and transmits this third address to the third bus subscriber, the third address in particular being the natural number (n+2), and in a fifth method step, the third bus subscriber logs in to the master module using its third address. This has the advantage that each bus subscriber, in particular each active bus subscriber, is automatically able to be addressed with the aid of the present method.

In an advantageous embodiment, the address m is allocated to an m^{th} bus subscriber in a further method step, and the m^{th} bus subscriber logs in to the master module using the address m, m being a natural number, and m in particular being unequal to n, m in particular being equal to 15, and the m^{th} bus subscriber allocates the address m to a

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bus subscriber downstream from the m^{th} bus subscriber, and transmits the address m to the downstream bus subscriber, the m^{th} bus subscriber in particular not incrementing the address, (m-1) being the maximally possible number of bus subscribers in the bus system. This has the advantage that the number of the bus subscribers is able to be limited. Data packets do not become too long in this way, and the transmission speed is improved. The number of bus subscribers is advantageously automatically restricted.

In an advantageous embodiment, the master module aborts the method and transmits an error report when a bus subscriber using the address m logs in to the master module. This has the advantage that the bus system automatically recognizes when too many bus subscribers are logging in. The error report is advantageously sent to a superordinate control. In an advantageous manner, the master module generates a warning signal, in particular a warning tone or a warning light.

In an advantageous embodiment, the temporally successive method steps are carried out for the emergency shutdown of the bus system:

In a first method step, a bus subscriber and/or the master module recognize(s) an error status,

and in a second method step, the bus subscriber and/or the master module transmit(s) an emergency signal to all bus subscribers and to the master module,

and in a third method step, a further bus subscriber receives the emergency signal, immediately forwards it to an adjacent bus subscriber and simultaneously evaluates it,

and in a fourth method step, the further bus subscriber shuts itself down.

This has the advantage that all bus subscribers of the bus system are able to be shut down within a short period of time. The emergency signal is advantageously not fully evaluated right away but is simultaneously forwarded to all bus subscribers and to the master module as soon as it has been identified as an emergency signal.

In an advantageous embodiment, the emergency signal interrupts a data packet. This has the advantage that the emergency signal is immediately sent to all bus

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subscribers and to the master module as soon as the error status has been identified. In an advantageous manner, there is no need to wait until the data packet has been transmitted in its entirety. As a result, a rapid shutdown of all bus subscribers is possible, and the security is improved.

In an advantageous embodiment, the transmission of the interrupted data packet is not continued and the interrupted data packet is discarded. This has the advantage that an error that occurs in the data packet due to the interruption has no effect on the bus system. The security is therefore improved.

In an advantageous embodiment, all data packets have an identical length, in particular signal length, and the length of the emergency signal, in particular the signal length, is shorter than the length of the data packets. This has the advantage that the emergency signal is able to be transmitted faster than a data packet. As a result, the security is improved.

In an advantageous embodiment, two consecutive data packets are temporally spaced apart from each other by a transmission pause, and the emergency signal interrupts a transmission pause. This has the advantage that the emergency signal may be transmitted immediately and independently of the status of the data line. The emergency signal is advantageously transmittable at any time, regardless of whether a data packet happens to be transmitted or a transmission pause exists at the time when the emergency signal is transmitted.

The emergency signal is advantageously shorter than the transmission pause.

In an advantageous embodiment, the bus system has two data lines, the bus subscriber and/or the master module transmitting the emergency signal simultaneously with the aid of both data lines. This has the advantage that the emergency signal reaches all bus subscribers in a communications ring faster when it is transmitted with the aid of the two data lines in two opposite directions than when the emergency signal is transmitted by only one data line in one direction.

Important features of the present invention in the bus system, in which a further bus subscriber is able to be integrated into the bus system with the aid of a method for integrating a further bus subscriber as previously described and/or as recited in one of

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the patent claims directed to the method for integrating a further bus subscriber, are that the bus system has a master module and bus subscribers, which are disposed in series, and the master module and the bus subscribers are connected to one another with the aid of at least one data line.

This has the advantage that a further bus subscriber, in particular a bus subscriber that needs a longer period of time for the activation, is easily integratable into the bus system retroactively.

In the production mode, i.e. after a granted release, no bus subscriber is advantageously admitted to the bus system.

In an advantageous manner, the admittance to the bus system is blocked with the aid of a bus subscriber disposed between the master module and the further bus subscriber so that the loading of the master module is reduced. This increases the security.

In an advantageous manner, the further bus subscriber is automatically admitted to the bus system in a new startup of the bus system.

In an advantageous embodiment, the bus system has at least one first data line and one second data line. This offers the advantage that a data packet is able to be sent from the master module to the bus subscribers with the aid of the first data line, and a data packet is able to be sent from a respective bus subscriber to the master module with the aid of the second data line, in particular at the same time. The speed of the data transmission is thus increased and the security improved. For the closing of the bus system, the first data line is advantageously connected to the second data line by the last bus subscriber, in particular short-circuited. The first and the second data line thus form a communications ring.

In an advantageous embodiment, a data packet is transmittable from the master module to the bus subscribers using the first data line. This has the advantage that the first data line and the second data line may be disposed in parallel. In an advantageous manner, data packets are transmittable from the master module to the bus subscribers at any time with the aid of the first data line. As a result, the data transmission from the master module to the bus subscribers will not be interrupted in

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order to transmit a respective data packet from an individual bus subscriber to the master module.

In an advantageous embodiment, a respective data packet may be transmitted from an individual bus subscriber to the master module with the aid of the second data line. This has the advantage that the first data line and the second data line may be placed in parallel. In an advantageous manner, data packets are transmittable by a respective bus subscriber to the master module at any time via the second data line. As a result, the data transmission from the bus subscribers to the master module will not be interrupted in order to transmit a data packet from the master module to an individual bus subscriber.

In an advantageous embodiment, the respective data line has at least one data cable in each case, and each bus subscriber is connected by a respective data cable to the bus subscriber upstream or downstream from it or to the master module. This has the advantage that the respective data line may have a modular development. As a result, a further bus subscriber is easily connected to the bus system with the aid of a further data cable.

In an advantageous embodiment, each data cable has two mating plug connector parts and each bus subscriber has a first plug connector part for the connection to the respective upstream bus subscriber with the aid of an individual data cable, and each bus subscriber has a second plug connector part for the connection to the respective downstream bus subscriber. This has the advantage that the bus subscribers of the bus system are easily connected to each other in a reversible manner. As a result, a further bus subscriber is easily connectable to the bus system, or a bus subscriber is easily separated from its upstream bus subscriber and/or from its downstream bus subscriber.

In an advantageous embodiment, the respective data cable of the first data line and the respective data cable of the second data line are disposed between two adjacent bus subscribers in a cable sheath, the cable sheath in particular surrounding the data cables in the circumferential direction, in particular enveloping them. This has the advantage of reducing the wiring expense. The first and the second data line are advantageously connected by a shared plug connector part so that only one plug connector part has to be plugged into the bus subscriber in order to connect a bus

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subscriber to its upstream or downstream bus subscriber. The plug connection is advantageously implementable in a manner that prevents a polarity reversal.

In an advantageous embodiment, a supply line and/or a ground lead for the bus subscribers is disposed in the cable sheath. This has the advantage of reducing the wiring expense. The data cables and the supply line and/or the ground lead are advantageously connected to a shared plug connector part so that only one plug connector part has to be plugged into the bus subscriber in order to connect a bus subscriber to its upstream or downstream bus subscriber. The plug connection is advantageously implementable in a manner that prevents a polarity reversal.

In an advantageous embodiment, each bus subscriber has a switch, which is connected to a respective data line, the switch being developed to interrupt the data transmission along the respective data line. This has the advantage that the individual bus subscriber is developed to use the switch to stop data packets that are not meant to reach the master module. In this way the bus subscriber relieves the load of the master module.

In an advantageous embodiment, each bus subscriber has a time-measuring means. This has the advantage that the time-measuring means allows the individual bus subscriber to measure a time span within which a further bus subscriber responds to a data packet, and in particular sends a further data packet. Thus, the further data packet is able to be evaluated as a function of this time span, and in particular is able to be blocked by the switch. This relieves the loading of the master module.

In an advantageous embodiment, each bus subscriber has a logic circuit, and the logic circuit in particular makes it possible to evaluate data packets of the master module and/or of the bus subscribers. This offers the advantage that the switch and/or the time-measuring means is/are able to be actuated with the aid of the logic circuit, in particular as a function of a data packet.

In an advantageous manner, the respective logic circuit has a storage means, which may be used for storing data packets. As a result, a data packet that was stopped by a bus subscriber may be stored by its storage means and be transmitted to the master module and/or to a bus subscriber at a later point in time.

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In an advantageous manner, the logic circuit is developed to evaluate the status of the bus system, in particular to detect whether a release was granted for the bus system.

In an advantageous embodiment, each bus subscriber has an electronic circuit, the electronic circuit including the switch and/or the time-measuring means and/or the logic circuit, the switch and/or the time-measuring means and/or the logic circuit in particular being integrated into the electronic circuit. This has the advantage that the electronic circuit may have a compact and secure development.

Further advantages result from the dependent claims. The present invention is not restricted to the feature combination of the claims. One skilled in the art will discover further meaningful combination possibilities of claims and/or individual claim features and/or features of the description and/or the figures, in particular on the basis of the stated objective and/or based on the objective resulting from a comparison with the related art.

Brief Description of the Drawings

The present invention will now be described in greater detail with the aid of figures:

Figure 1 shows a schematic representation of a bus system according to the present invention.

Figure 2 shows the time characteristic of data packets on a data bus.

Figure 3 shows the time characteristic of data packets and an emergency signal on the data bus in a first case example.

Figure 4 shows the time characteristic of data packets and an emergency signal on the data bus in a second case example.

Detailed Description

The bus system according to the present invention has a master module M and bus subscribers (S1, S2, S3, S4), which are disposed in series and connected to one another. The bus system has a first bus subscriber S1 disposed downstream from

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master module M. The bus system has a second bus subscriber S2 downstream from first bus subscriber S1, first bus subscriber S1 being situated upstream from second bus subscriber S2. Second bus subscriber S2 is disposed upstream from a third bus subscriber S3, and third bus subscriber S3 is situated downstream from second bus subscriber S2. Third bus subscriber S3 is disposed upstream from a fourth bus subscriber S4, and fourth bus subscriber S4 is disposed downstream from third bus subscriber S3.

A bus subscriber (S1, S2, S3, S4) situated downstream from another bus subscriber (S1, S2, S3, S4) is situated at a greater distance from master module M in the direction of the series arrangement than the other bus subscriber (S1, S2, S3, S4). The other bus subscriber (S1, S2, S3, S4), which is disposed at a shorter distance from master module M than the bus subscriber (S1, S2, S3, S4) in the direction of the series arrangement, is located upstream from the bus subscriber (S1, S2, S3, S4).

For example, the bus system is an industrial plant which has various devices as bus subscribers (S1, S2, S3, S4), such as drives or electronic components, e.g., drive converters for electric motors.

The data bus has a first data line 1 and a second data line 2, which in each case serially connect the bus subscribers (S1, S2, S3, S4) and master module M to one another.

With the aid of first data line 1, master module M sends data packets (3, 4) such as control commands to the bus subscribers (S1, S2, S3, S4). With the aid of second data line 2, the bus subscribers (S1, S2, S3, S4) send data packets (3, 4) such as status information to master module M.

Each bus subscriber (S1, S2, S3, S4) has a first interface and a second interface, which are preferably developed as a plug connector part in each case. Each data line (1, 2) has at least one data cable. Each data cable has a first mating plug connector part and at least one second mating plug connector part for a data transmission between the bus subscribers (S1, S2, S3, S4) along the respective data line (1, 2).

As a result, each bus subscriber (S1, S2, S3, S4) is able to be connected to a second plug connector part of an upstream bus subscriber (S1, S2, S3, S4) using a first plug

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connector part and the respective data cable, and is able to be connected by a second plug connector part and the respective data cable to a first plug connector part of a downstream bus subscriber (S1, S2, S3, S4).

The respective data cable of first data line 1 and the respective data cable of second data line 2 are preferably guided in a shared cable sheath. A supply line and/or a ground lead for the bus subscribers (S1, S2, S3, S4) is/are preferably also disposed in this cable sheath.

Each bus subscriber (S1, S2, S3, S4) has a switch, in particular as a component of an electronic circuit, which is connected to the respective data line (1, 2). The switch may be used to interrupt the data transmission along the respective data line (1, 2).

Each bus subscriber (S1, S2, S3, S4) has a time-measuring means, in particular a timer. The time-measuring means is preferably integrated into the electronic circuit of the bus subscriber (S1, S2, S3, S4).

Using the electronic circuit, the data transmission along the respective data line (1, 2) is therefore able to be interrupted after a predefined time has elapsed.

Each bus subscriber (S1, S2, S3, S4) has a logic circuit. The logic circuit is preferably integrated into the electronic circuit of the bus subscriber (S1, S2, S3, S4).

Using the logic circuit, data packets on the data bus are able to be evaluated, and the sender of a data packet, in particular, is identifiable.

In the event that a bus subscriber (S1, S2, S3, S4) is inactive, a data packet is forwarded without interruption and without a time delay through the inactive bus subscriber (S1, S2, S3, S4) to the downstream or upstream bus subscriber (S1, S2, S3, S4). A data packet passes through an inactive bus subscriber (S1, S2, S3, S4) without obstruction.

The data bus is preferably implemented in a digital form.

For the initialization of the bus system, master module M sends a request to the bus subscribers (S1, S2, S3, S4) situated downstream to log in to master module M. An

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active bus subscriber (S1, S2, S3, S4) downstream from master module M logs in to master module M and forwards the request for the login to master module M to bus subscribers (S1, S2, S3, S4) disposed downstream from it. The logged in bus subscriber (S1, S2, S3, S4) then waits for a predefined period of time to see whether a bus subscriber (S1, S2, S3, S4) downstream from it logs in to master module M.

If no downstream bus subscriber (S1, S2, S3, S4) logs in to the master module, then the last logged in bus subscriber (S1, S2, S3, S4) closes the bus system as soon as the predefined period of time has elapsed, by connecting first data line 1 and second data line 2 to each other, in particular short-circuiting them. A data packet that is transmitted with the aid of first data line 1 from master module M to the bus subscribers (S1, S2, S3, S4) is thus forwarded into second data line 2 at the final bus subscriber (S1, S2, S3, S4) and routed back to the master module.

The last bus subscriber (S1, S2, S3, S4) is the particular bus subscriber (S1, S2, S3, S4) that logs in last to master module M and has no downstream bus subscribers (S1, S2, S3, S4).

The request to log in to master module M is routed through an inactive bus subscriber (S1, S2, S3, S4) without this subscriber itself logging in to master module M.

After the bus system has been closed, a release is granted by a superordinate control or by an operator and the operation of the bus system begins.

In the event that a bus subscriber (S1, S2, S3, S4) logs in late, i.e. after the predefined period of time following the login of the last bus subscriber (S1, S2, S3, S4) has elapsed, then this bus subscriber (S1, S2, S3, S4) sends a data packet to master module M. If a release was already granted, this data packet is stopped by an upstream bus subscriber (S1, S2, S3, S4) that is logged in to master module M and will not be forwarded to master module M.

As soon as the release has been revoked, a data packet of the late bus subscriber (S1, S2, S3, S4) is forwarded to master module M and the late bus subscriber (S1, S2, S3, S4) is admitted to the bus system.

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In the event that the late bus subscriber (S1, S2, S3, S4) has no downstream bus subscribers (S1, S2, S3, S4) that are logged in to master module M, then it becomes the new last bus subscriber (S1, S2, S3, S4) and closes the bus system after waiting out the predefined period of time for the login of a bus subscriber (S1, S2, S3, S4). The predefined period of time for the login of a bus subscriber (S1, S2, S3, S4) is able to be adapted to the bus subscribers (S1, S2, S3, S4). The period of time may be selected in such a way that bus subscribers (S1, S2, S3, S4) that have a longer start-up time are securely logged in to master module M.

During the initialization of the bus system, bus addresses for the bus subscribers (S1, S2, S3, S4) are automatically assigned. For this purpose, master module M sends the bus address "1" to first bus subscriber S1. First bus subscriber S1 logs in to master module M using this bus address and increments the bus address by 1 and forwards it to the bus subscriber (S1, S2, S3, S4) disposed downstream. The downstream bus subscriber (S1, S2, S3, S4) logs in to master module M using the incremented bus address, i.e. bus address "2" in this instance, increments this bus address by 1 again and forwards it to the bus subscriber (S2, S3, S4) downstream from it.

In an effort to restrict the number of bus subscribers (S1, S2, S3, S4) in the bus system, a bus subscriber (S1, S2, S3, S4) that is given a bus address that is greater than the maximally allowed number of bus subscribers (S1, S2, S3, S4), will not further increment this bus address but forwards the same bus address to its downstream bus subscriber (S1, S2, S3, S4), which uses this bus address to log in to master module M. As soon as master module M receives a bus address that is greater than the maximally allowed number of bus subscribers (S1, S2, S3, S4), master module M aborts the initialization of the bus system and transmits an error report to a control superordinate to master module M.

If a bus subscriber (S1, S2, S3, S4) that is not yet active, i.e. an inactive bus subscriber (S1, S2, S3, S4), receives a bus address from a bus subscriber (S1, S2, S3, S4) upstream from it or from master module M, then this bus address is looped through the inactive bus subscriber (S1, S2, S3, S4) without being incremented, and is assigned to a downstream bus subscriber (S1, S2, S3, S4).

Figures 2 through 4 show the time characteristic of data packets 3 that are transmitted with the aid of a respective data line (1, 2). Each data packet 3 has a predefined length that is a function of the number of bus subscribers (S1, S2, S3, S4) of the bus system. The data transmission is interrupted for a predefined period of time between two temporally successive data packets 3, which means that two temporally successive data packets 3 are temporally spaced apart with the aid of a transmission pause 6.

As soon as a bus subscriber (S1, S2, S3, S4) or master module M detects an error, data packet 4 transmitted at that instant is immediately interrupted and an emergency signal 5 is transmitted by the respective bus subscriber (S1, S2, S3, S4) or by master module M, as illustrated in Figure 3. This emergency signal 5 causes an immediate shutdown of all bus subscribers (S1, S2, S3, S4).

The interrupted data packet 4 is immediately terminated and not further processed by the bus subscribers (S1, S2, S3, S4).

If a bus subscriber (S1, S2, S3, S4) or master module M detects an error during a transmission pause 6, then transmission pause 6 will be interrupted and an emergency signal 5 be sent by the respective bus subscriber (S1, S2, S3, S4) or by master module M, as illustrated in Figure 4. This emergency signal 5 causes an immediate shutdown of all bus subscribers (S1, S2, S3, S4).

The respective bus subscriber (S1, S2, S3, S4) transmits emergency signal 5 on both data lines (1, 2). In other words, emergency signal 5 is transmitted from the respective bus subscriber (S1, S2, S3, S4) in the direction of master module M on the second data line and is transmitted by the respective bus subscriber (S1, S2, S3, S4) away from master module M on first data line 1.

The respective bus subscribers (S1, S2, S3, S4) immediately process the emergency signal 5 and at the same time forward it to the downstream bus subscriber (S1, S2, S3, S4) so that the bus subscribers (S1, S2, S3, S4) shut down immediately. In other words, emergency signal 5 is not first stored and processed but is immediately forwarded to all bus subscribers (S1, S2, S3, S4) and to master module M.

The emergency signal 5 preferably has a temporally shorter length than the data packets (3, 4) and/or transmission pause 6.

List of Reference Numerals

M master module

S1 first bus subscriber

S2 second bus subscriber

S3 third bus subscriber

S4 fourth bus subscriber

1 first data line

2 second data line

3 data packet

4 data packet

5 emergency signal

6 transmission pause

Date Reçue/Date Received 2022-01-12

Claims

1. A method for integrating a further bus subscriber (S1, S2, S3, S4) into a bus system, comprising a master module (M) and bus subscribers (S1, S2, S3, S4) disposed in series, and having temporally consecutive method steps:

In a first method step, the further bus subscriber (S1, S2, S3, S4) sends a data packet to the master module (M) in order to log in to the master module (M),

and in a second method step, a bus subscriber (S1, S2, S3, S4) disposed between the further bus subscriber (S1, S2, S3, S4) and the master module (M) stops the data packet and checks whether the bus system has already received a release for a production mode after a successful initialization,

and in a third method step, the bus subscriber (S1, S2, S3, S4) disposed between the further bus subscriber (S1, S2, S3, S4) and the master module (M) forwards the data packet to the master module (M) if the bus system has not yet received a release,

or in an alternative third method step, if the bus system has already obtained a release, the bus subscriber (S1, S2, S3, S4) stores the data packet and waits until the release of the bus system is revoked and after the release has been revoked, forwards the stored data packet to the master module (M).

2. The method for integrating a further bus subscriber (S1, S2, S3, S4) into a bus system as recited in Claim 1,

wherein

for the initialization of the bus system, the master module (M) asks the bus subscribers (S1, S2, S3, S4) to log in to the master module (M),

in a subsequent method step, a first bus subscriber (S1) disposed downstream from the master module (M) logs in to the master module (M),

and in a subsequent method step, the first bus subscriber (S1) waits for a predefined period of time to see whether a second bus subscriber (S2) disposed downstream from the first bus subscriber (S1) logs in to the master module (M).

3. The method for integrating a further bus subscriber (S1, S2, S3, S4) into a bus system as recited in Claim 2,

wherein

the first bus subscriber (S1) closes the bus system if no second bus subscriber (S2) logs in to the master module (M) within the predefined period of time.

4. The method for integrating a further bus subscriber (S1, S2, S3, S4) into a bus system as recited in Claim 2,

wherein

a second bus subscriber (S2) logs in to the master module (M) within the predefined period of time and waits a further predefined period of time to see whether a third bus subscriber (S3) disposed downstream from the second bus subscriber (S2) logs in to the master module (M), and the second bus subscriber (S2) closes the bus system if no third bus subscriber (S3) logs in to the master module (M) within the further predefined period of time.

5. The method for integrating a further bus subscriber (S1, S2, S3, S4) into a bus system as recited in any one of Claims 1 to 4,

wherein

the release is granted and/or revoked by a control superordinate to the master module (M).

6. A bus system, where a further bus subscriber is able to be integrated into the bus system with the aid of a method as recited in any one of Claims 1 to 5,

wherein

the bus system has a master module (M) and bus subscribers (S1, S2, S3, S4) which are disposed in series,

the master module (M) and the bus subscribers (S1, S2, S3, S4) being connected to one another with the aid of at least one data line (1, 2).

7. The bus system as recited in Claim 6,

wherein

the bus system has at least one first data line (1) and one second data line (2).

8. The bus system as recited in Claim 7,

wherein

a data packet (3) is able to be transmitted with the aid of the first data line (1) from the master module (M) to the bus subscribers (S1, S2, S3, S4),

and/or

a respective data packet (3) is able to be transmitted with the aid of the second data line (2) from a respective bus subscriber (S1, S2, S3, S4) to the master module (M).

9. The bus system as recited in any one of Claims 6 to 8,

wherein

each of the respective first and second data lines (1, 2) has at least one data cable in each case, and each bus subscriber (S1, S2, S3, S4) is connected by a respective data cable to the bus subscriber (S1, S2, S3, S4) disposed upstream or downstream from it, or to the master module (M).

10. The bus system as recited in claim 9, wherein each data cable has two mating plug connector parts, and each bus subscriber (S1, S2, S3, S4) has a first plug connector part for the connection to the respective upstream bus subscriber with the aid of a respective data cable, and each bus subscriber (S1, S2, S3, S4) has a second plug connector part for the connection to the respective downstream bus subscriber.

11 The bus system as recited in Claim 10,

wherein

the respective data cable of the first data line (1) and the respective data cable of the second data line (2) are disposed between two adjacent bus subscribers (S1, S2, S3, S4) in a shared cable sheath, the cable sheath at least in part surrounds the data cables in a circumferential direction.

12. The bus system as recited in Claim 11, wherein the cable sheath envelops the data cables.

13. The bus system as recited in Claim 11, wherein a supply line and/or a ground lead for the bus subscribers (S1, S2, S3, S4) being disposed in the cable sheath.

14 The bus system as recited in any one of Claims 6 to 13,

wherein

each bus subscriber (S1, S2, S3, S4) has a switch, and the switch is connected to a respective data line (1, 2),

the switch being developed to interrupt the data transmission along the respective data line (1, 2).

15. The bus system as recited in any one of Claims 6 to 14,
wherein
each bus subscriber (S1, S2, S3, S4) has a time-measuring means.

16. The bus system as recited in any one of Claims 6 to 15,
wherein
each bus subscriber (S1, S2, S3, S4) has a logic circuit.

17. The bus system as recited in claim 16, wherein data packets of the master module (M) and/or the bus subscribers (S1, S2, S3, S4) are able to be evaluated with the aid of the logic circuit.

18 The bus system as recited in any one of Claims 6 to 13,
wherein
each bus subscriber (S1, S2, S3, S4) has an electronic circuit,
the electronic circuit having a switch and/or a time-measuring means and/or a logic circuit,
the switch being connected to a respective data line (1, 2), the switch being developed to interrupt the data transmission along the respective data line (1, 2),
wherein data packets of the master module (M) and/or the bus subscribers (S1, S2, S3, S4) are able to be evaluated with the aid of the logic circuit.

19. The bus system as recited in claim 18, wherein the switch and/or the time-measuring means and/or the logic circuit being integrated into the electronic circuit.

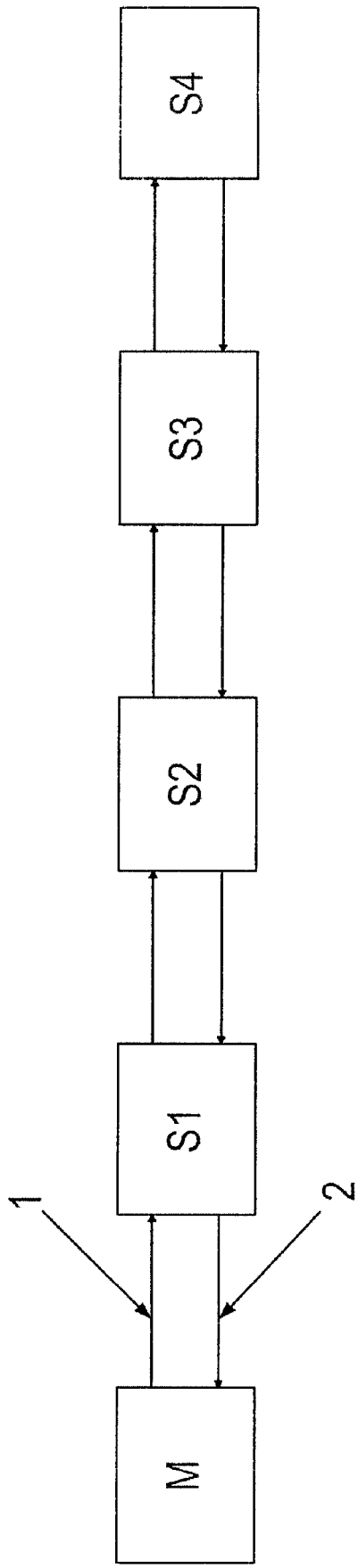


Fig. 1

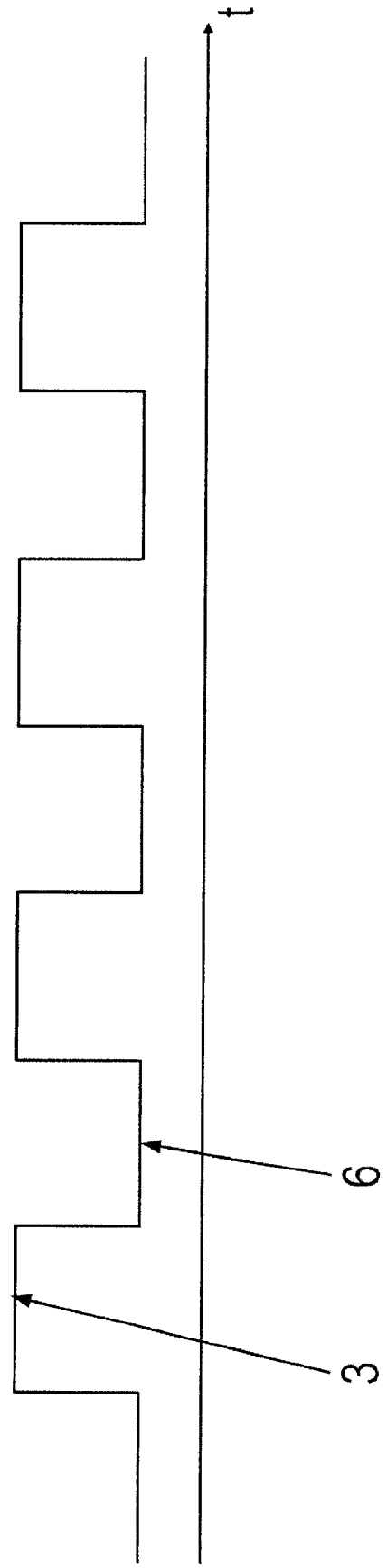


Fig. 2

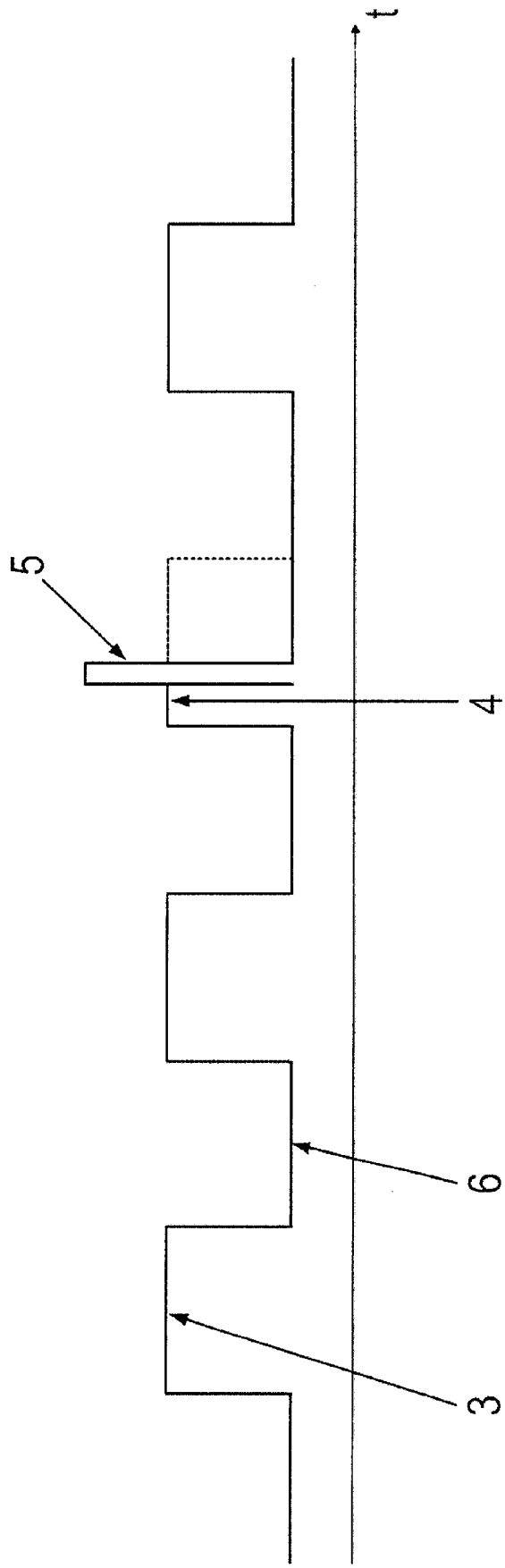


Fig. 3

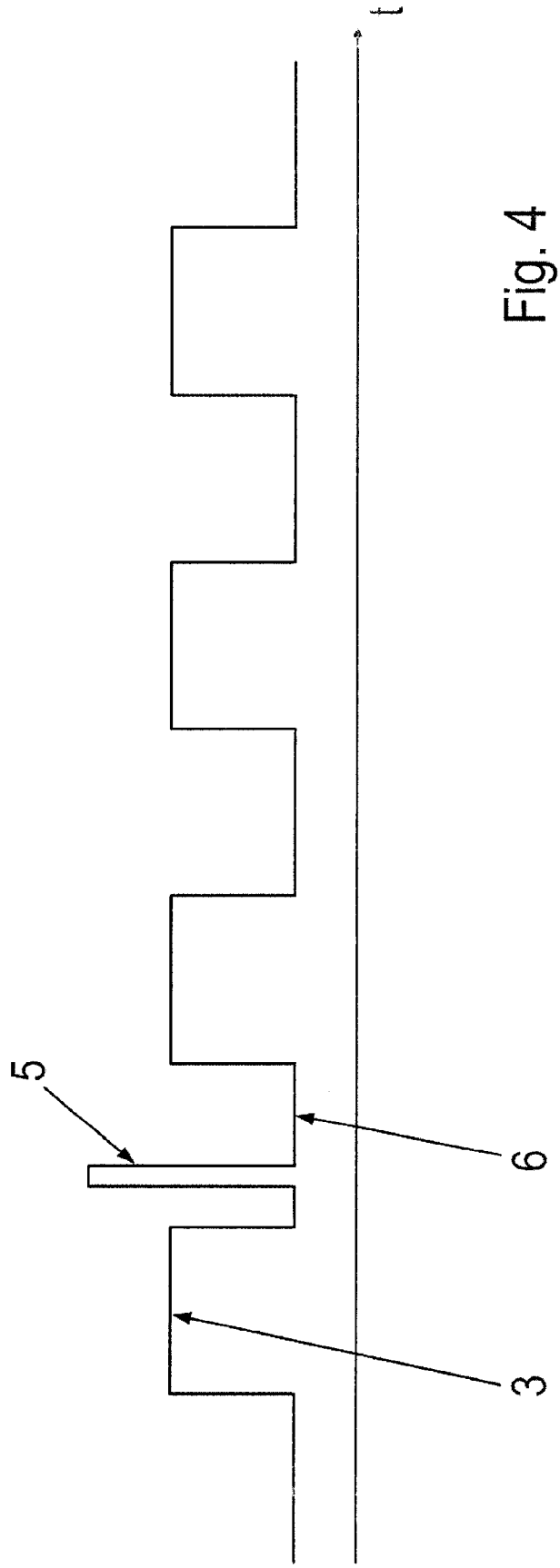
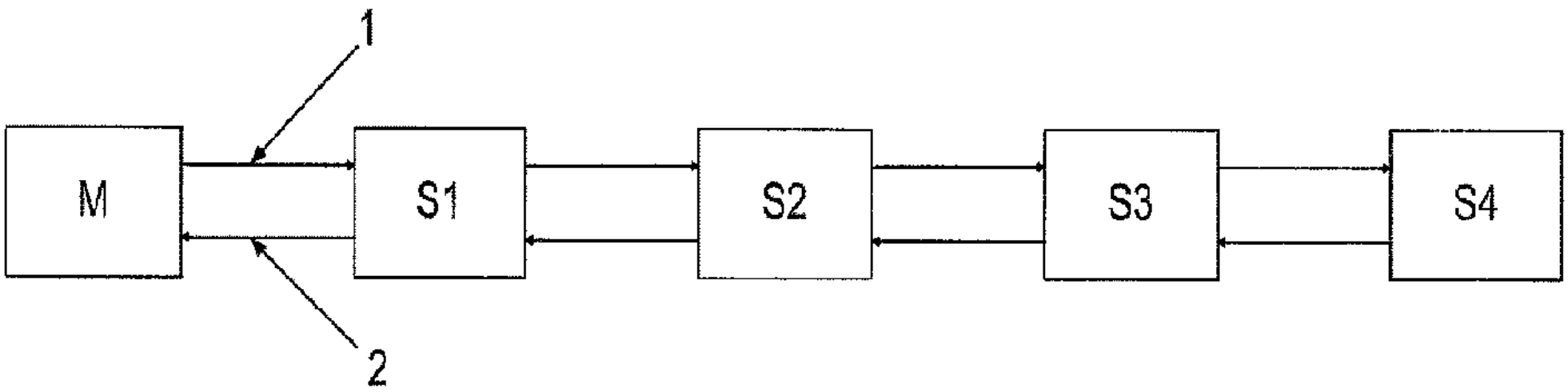


Fig. 4


1
M
S1
S2
S3
S4
2