United States Patent [19]

Watts et al.

[11] **3,771,156**

[45] **Nov. 6, 1973**

[54] **COMMUNICATION APPARATUS**

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[73] Assignee: **Sanders Associates Inc.**, Nashua, N.H.

[22] Filed: **Sept. 25, 1972**

[21] Appl. No.: **292,046**

[52] **U.S. Cl.** ..... **340/325,** 340/168 CC, 340/324 R

[51] **Int. Cl.** **G08b 5/36**

[58] **Field of Search** ..... 340/325, 168 R, 168 CC

[56] **References Cited**

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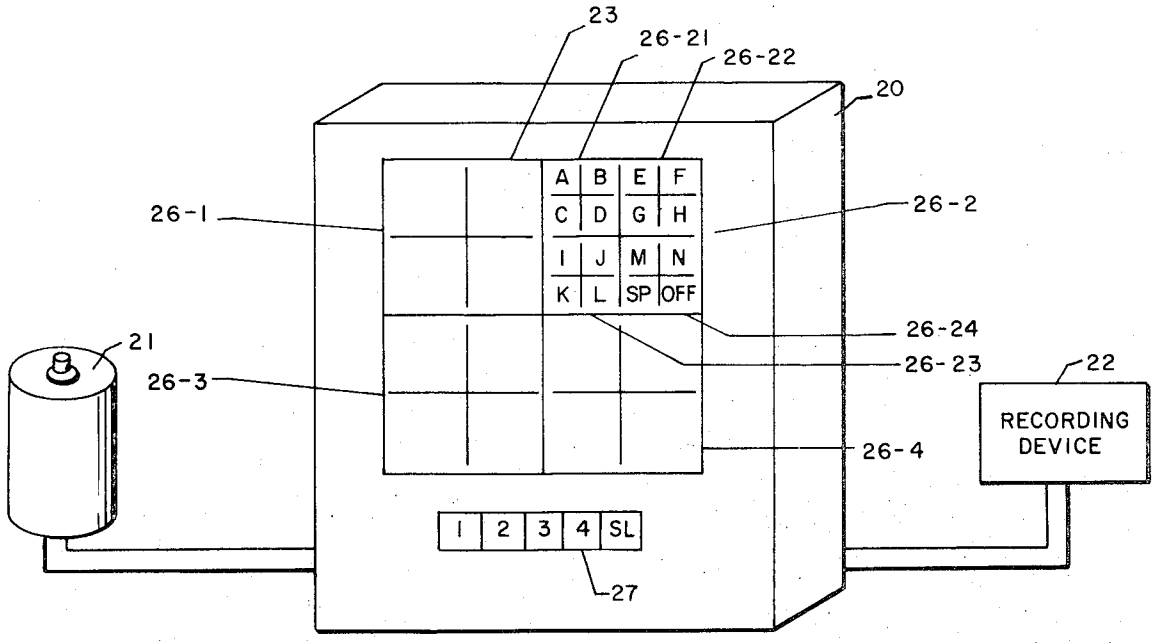
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Primary Examiner—David L. Trafton
Attorney—Louis Etlinger

[57] **ABSTRACT**

Communication apparatus in which an operator selects information items or characters which are visually displayed in groups sequentially. The operator observes the sequential display of the groups and selects the group containing the character he desires to communicate by operating a single switch mechanism in coincidence with the visual display of that group. The apparatus then sequentially displays the characters within the selected group. The operator then selects his desired character by operating the switch in coincidence with the display of that character.

13 Claims, 31 Drawing Figures



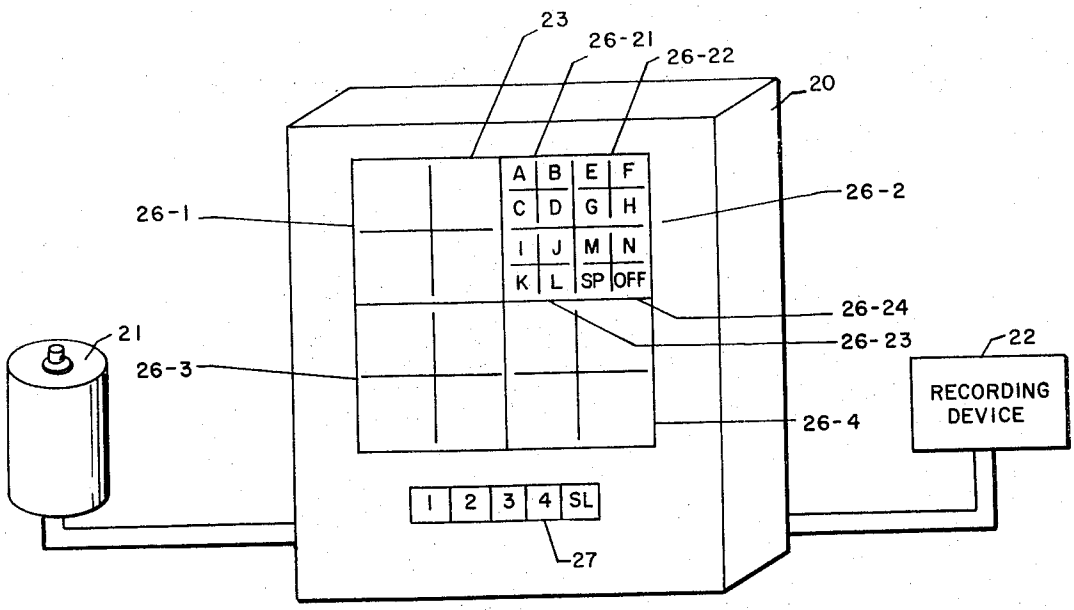


FIG. 1

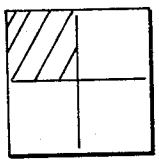


FIG. 2A

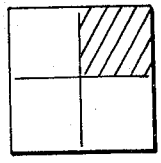


FIG. 2B

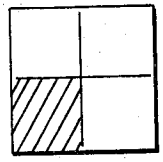


FIG. 2C

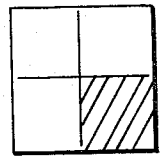


FIG. 2D

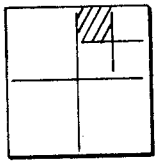


FIG. 2E

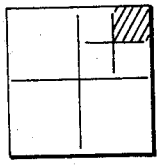


FIG. 2F

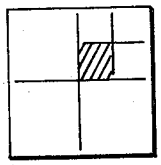


FIG. 2G

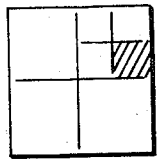


FIG. 2H

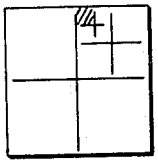


FIG. 2I

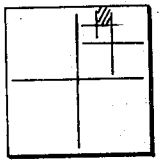


FIG 2J

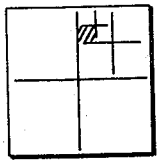


FIG. 2K

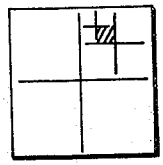


FIG. 2L

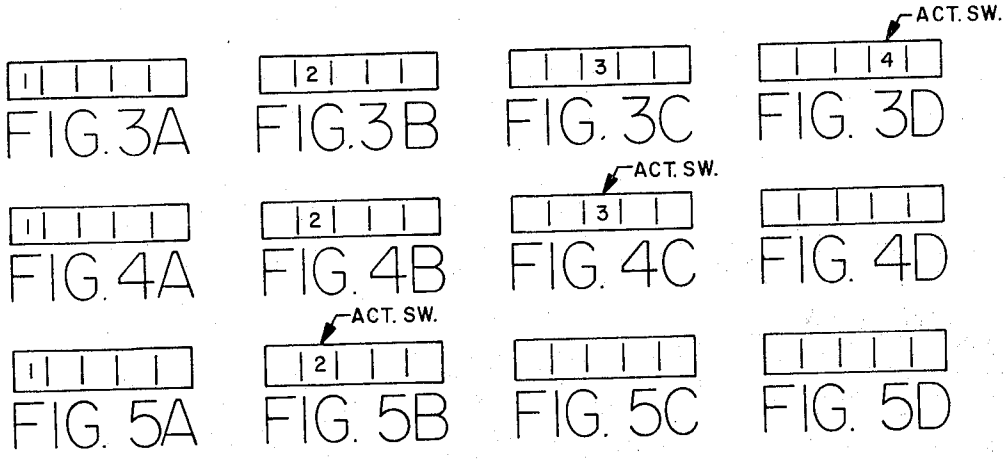


FIG. 3A FIG. 3B FIG. 3C FIG. 3D

FIG. 4A FIG. 4B FIG. 4C FIG. 4D

FIG. 5A FIG. 5B FIG. 5C FIG. 5D

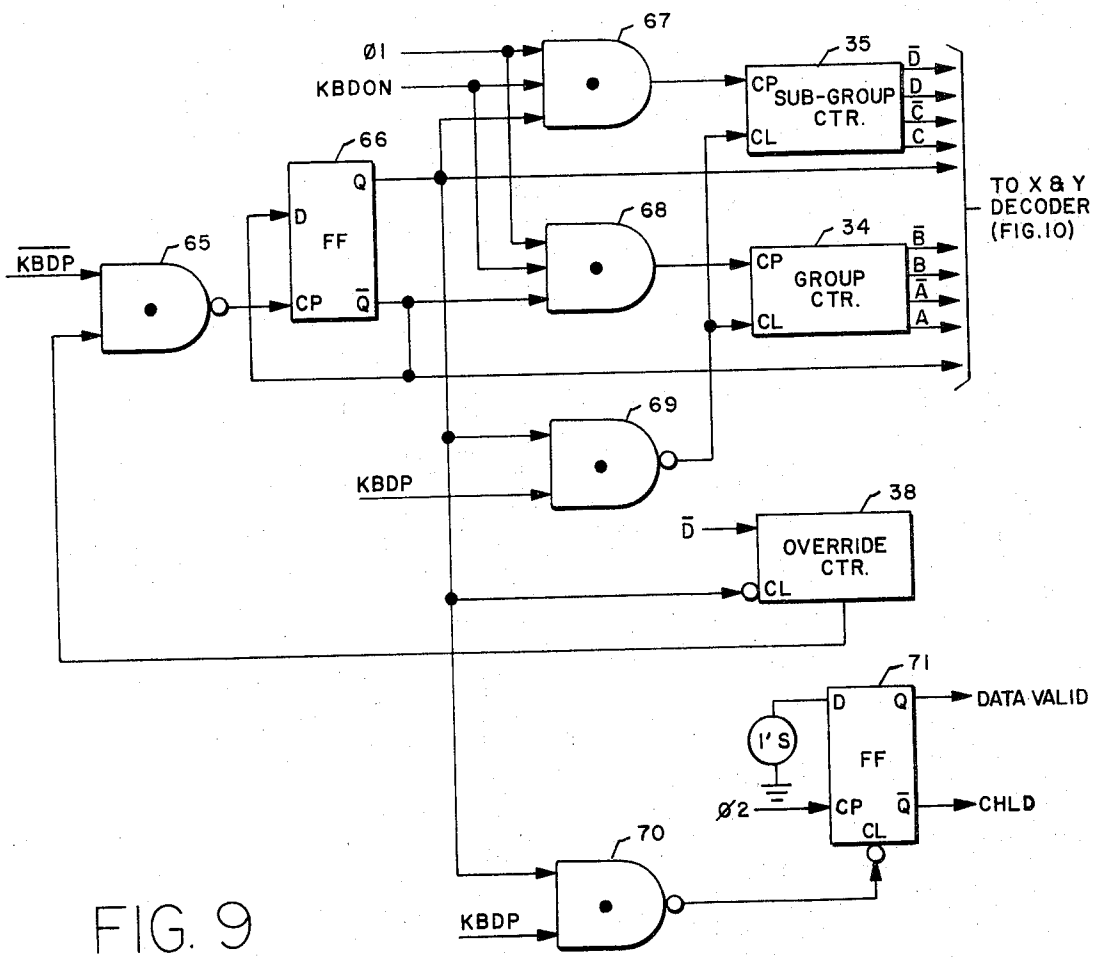


FIG. 9

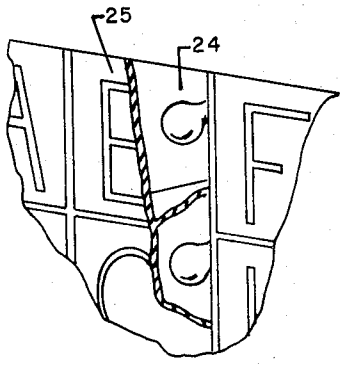


FIG. 6

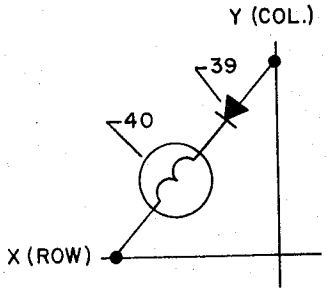


FIG. 11

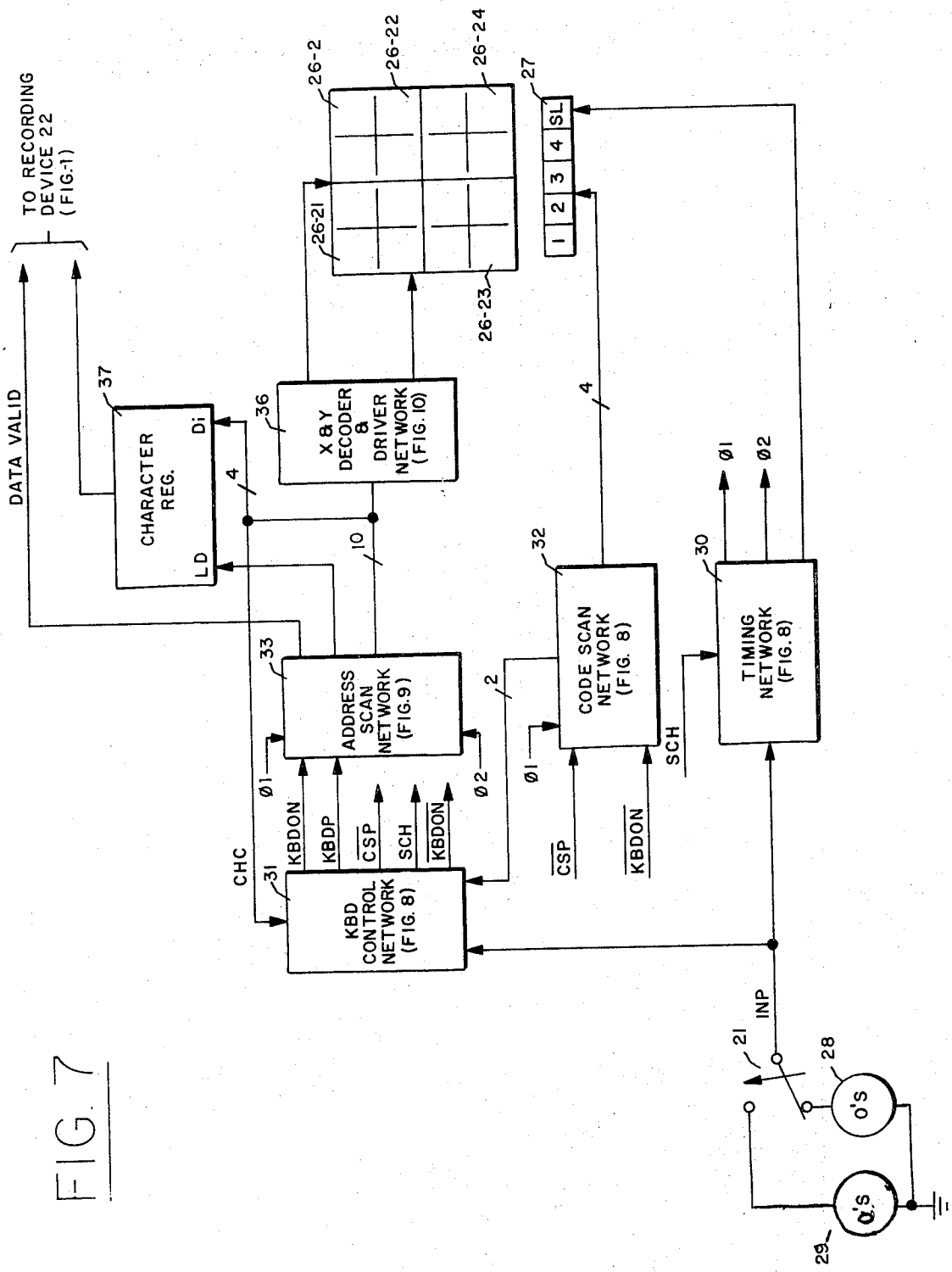

TO RECORDING DEVICE 22 (FIG.1)
DATA VALID
CHARACTER REG.
Di
LD
37
4
10
36
X & Y DECODER & DRIVER NETWORK (FIG. 10)
26-2
26-22
26-24
26-21
26-23
27
1
2
3
4
SL
ADDRESS SCAN NETWORK (FIG.9)
33
Ø1
Ø2
2
CODE SCAN NETWORK (FIG. 8)
32
TIMING NETWORK (FIG.8)
30
SCH
KBD CONTROL NETWORK (FIG. 8)
31
CHC
KBDON
KBDP
CSP
SCH
KBDON
INP
21
28
o's
Q's
29

FIG. 7

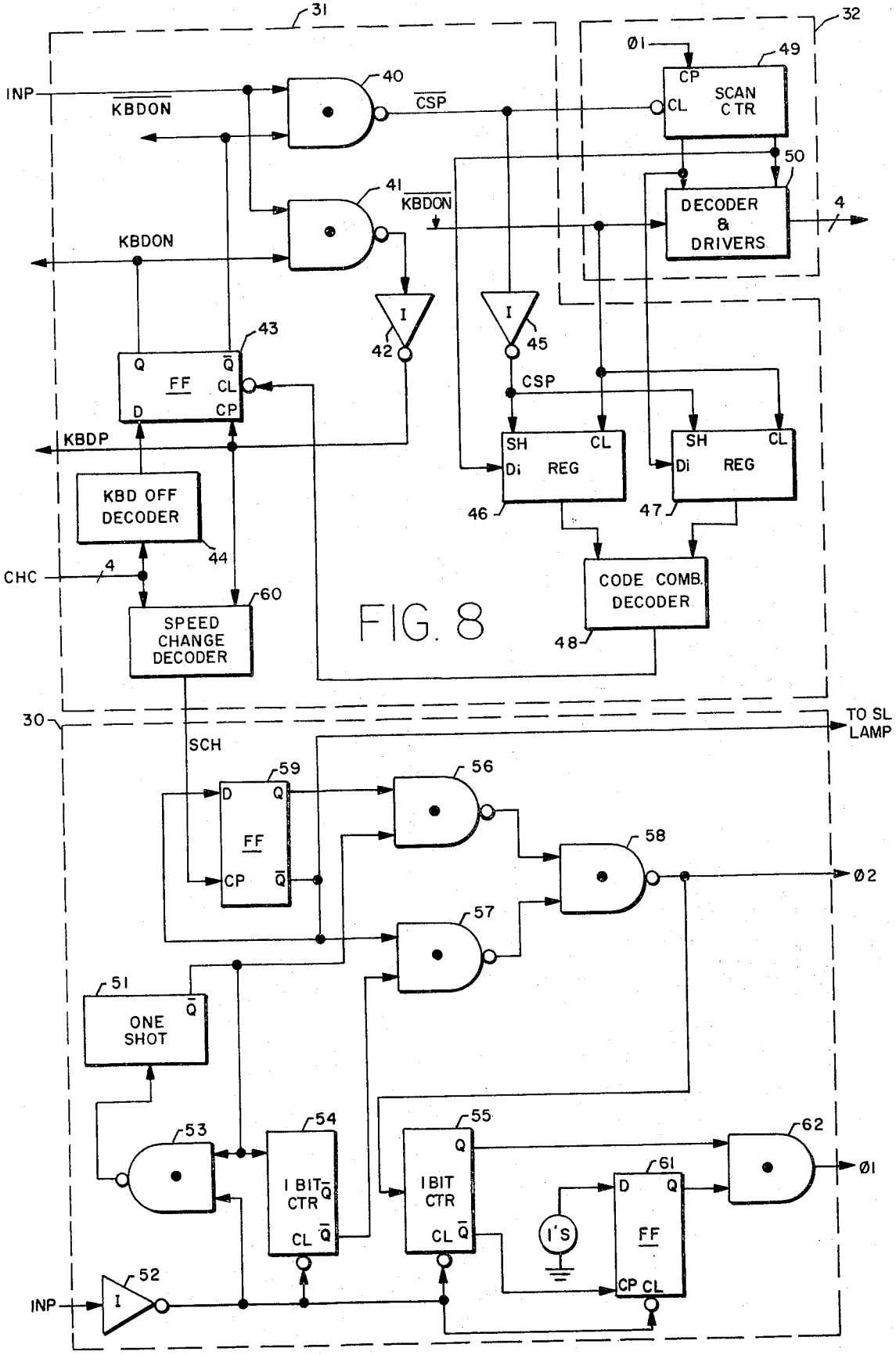

31
32
INP
KBDON
40
CSP
Ø1
49
CP
CL
SCAN CTR
50
41
KBDON
DECODER & DRIVERS
4
KBDON
I
42
I
45
43
Q
Q
FF
CL
D
CP
CSP
KBDP
SH
CL
Di
REG
SH
CL
Di
REG
46
47
KBD OFF DECODER
44
CHC
4
CODE COMB. DECODER
48
SPEED CHANGE DECODER
60
30
TO SL LAMP
SCH
59
D
Q
FF
CP
Q
56
58
Ø2
57
51
ONE SHOT
Q
53
54
I BIT CTR
Q
CL
Q
55
I BIT CTR
Q
CL
Q
62
Ø1
61
D
Q
FF
CP
CL
I'S
INP
52
I

FIG. 8

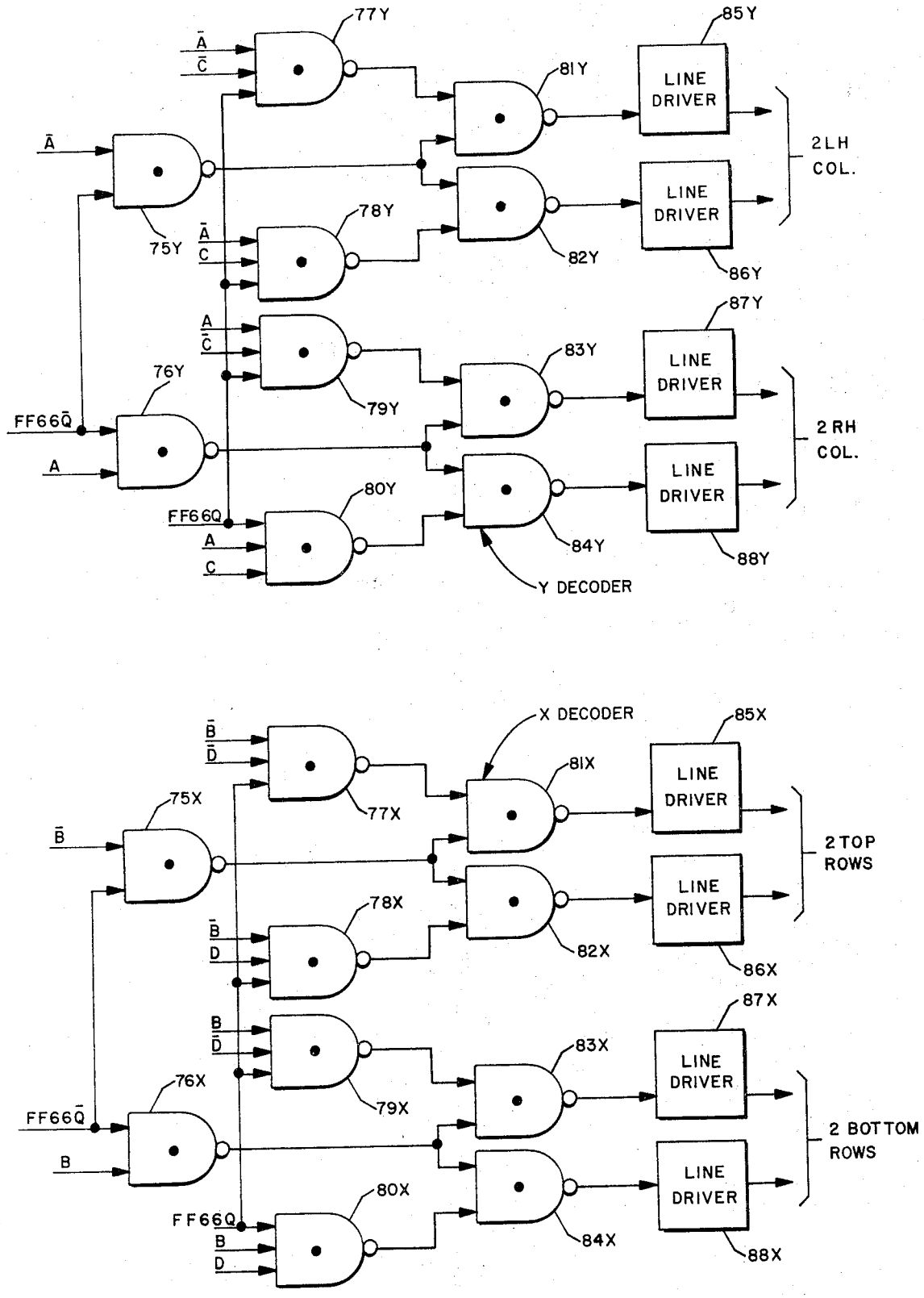

77Y
85Y
81Y
LINE DRIVER
2 LH COL.
78Y
75Y
82Y
86Y
87Y
83Y
79Y
76Y
2 RH COL.
80Y
84Y
88Y
Y DECODER
X DECODER
85X
81X
77X
75X
2 TOP ROWS
78X
82X
86X
87X
83X
79X
76X
2 BOTTOM ROWS
80X
84X
88X
FF66Q

FIG. 10

COMMUNICATION APPARATUS

BACKGROUND OF INVENTION

1. Field of Invention

This invention relates to novel and improved communication apparatus and in particular to such apparatus in which each information item selected for communication is visually displayed.

Communication apparatus is useful for communication between one person and another or between a person and a machine, as for example, an electronic data processing machine.

2. Prior Art

In the prior art, communication apparatus has been embodied in keyboard operated displays in which an operator selects information items or characters from a keyboard having a separate key for each character in the character repertoire. As each character is selected, it is displayed visually on a display screen, such as a cathode ray tube screen. This type of prior art communication device generally requires an operator with the physical ability to depress keys having different locations on the keyboard. For this reason, it is not generally of any use to handicapped personnel who have limited physical abilities, as for example, quadraphlegics, multiple sclerosis victims, cerebral palsy victims and many others.

One prior art communication device which is particularly adapted for use by handicapped personnel is described in U.S. Pat. No. 3,651,512. This device includes a display unit having a display panel with a series of compartments containing lamps. Translucent windows are located over the compartments and have messages or other similar information printed thereon. A switch unit, which in one case is hand held, having four switches allows an operator to turn the display panel on and off and to sequentially illuminate the lamps in either vertical or horizontal direction so as to select a desired message or item of information. Many handicapped personnel do not have the physical ability or power to operate or grasp the four switch control unit of this prior art device.

BRIEF SUMMARY OF INVENTION

An object of the present invention is to provide novel and improved communication apparatus.

Another object is to provide novel and improved communication apparatus that can be readily used by handicapped personnel.

Still another object is to provide communication apparatus that can be used by a handicapped individual who is unable to use his hands, or unable to speak, or is otherwise weak or ill.

Yet another object is to provide communication apparatus in which the operator can select information items through the operation of a single switch mechanism.

A further object is to provide novel and improved code responsive apparatus.

Briefly, communication apparatus embodying the invention includes a display screen for displaying the items in a set of information items, a manually operable switch, a display means and a control circuit. The display means includes a sequential group display means which is operable to sequentially display the items of the set a group at a time and further includes a sequential item display circuit which is operable to sequentially display the items of a selected group an item at a time. In the operation of the apparatus, the operator views the information items which are being sequentially displayed a group at a time. He selects a desired character by actuating the switch when the group containing that character is being displayed. The control means respond to the actuation of the switch at this time to initiate the operation of the sequential item display circuit which sequentially displays the information items within the selected group. The operator again actuates the switch when the desired item is visually displayed. The control circuit responds to the further actuation of the switch to interrupt the operation of the sequential item display circuit and to enter the selected information item into a storage device.

In accordance with one feature of the invention, the communication apparatus becomes operable only after a proper code or sequence of information items is selected by the operator. This feature is particularly attractive for use by voice operated switch users in that the user can carry on a conversation with other people without accidentally turning the communication apparatus on. This feature is embodied in code responsive apparatus which includes means for displaying during consecutive cycles a set of characters, one at a time, in sequence, a manually operable switch and a control circuit. The operator enters a predetermined code by actuating the switch in coincidence with the visual display of the characters of a predetermined code, a character at a time, in the order they appear in the code. The control circuit produces a control signal when the switch has been sequentially activated in coincidence with the visual display of all the characters of a predetermined code.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings like reference characters denote like elements of structure; and

FIG. 1 is a perspective view of visual communication apparatus embodying the present invention;

FIG. 2A through FIG. 2L are skeletal views of the display screen of the visual communication apparatus illustrating the illumination sequences of the groups and sub-groups of the characters or information items in a set;

FIGS. 3A through 3D, 4A through 4D and 5A through 5D are also skeletal views which illustrate the entry of a code into the code responsive apparatus of the present invention;

FIG. 6 is a partial and exploded perspective view of a single display element location of the visual communication apparatus shown on FIG. 1;

FIG. 7 is a block diagram of visual communication apparatus embodying the present invention;

FIG. 8 is a block diagram, in part, and a logic diagram, in part, of the keyboard control network, timing network and code scan network of the visual communication apparatus in FIG. 7;

FIG. 9 is a block diagram, in part, and a logic schematic diagram, in part, of the address counter select network of the visual communication apparatus of FIG. 7.

FIG. 10 is a block diagram, in part, and a logic schematic, in part, of the X and Y decoder and driver network of the visual communication apparatus shown in FIG. 7; and

FIG. 11 is a circuit diagram illustrating the circuit of the illuminating element at each information item location display screen.

DESCRIPTION OF THE PREFERRED EMBODIMENT

It is contemplated that communication apparatus embodying the present invention may be employed to communicate various different items of information where an item may range from a single alphanumeric character or a punctuation symbol to a message comprised of several such characters arranged in conventional word form. However by way of example, and completeness of description, the communication apparatus embodying the invention is illustrated herein for the case where each of the information items in a set are different ones of a set of alphanumeric characters together with some special control items.

With reference now to FIG. 1, communication apparatus embodying the present invention is shown to include a display console **20** having a display screen **23**, a manually operable switch **21** and an output recording device **22**. The manually operable switch may take on not only the illustrated hand held form but other forms such as foot operated, voice operated and other suitable forms. The recording device **22** may be any suitable type of recording device which makes record of characters received at its input such as a typewriter, printer, magnetic or paper tape recorder, cathode ray tube display and the like.

The display console **20** and display screen **23** may comprise any suitable display device such as a cathode ray tube, plasma display panel, X and Y addressable illuminating element array and the like. By way of example, the X and Y addressable illuminating element array has been chosen for the embodiment illustrated herein. Accordingly, the display screen **23** includes a plurality of compartments each containing an illuminating element and each having a translucent window which bears an alphanumeric character. This is best shown in the partial view of FIG. **10** which illustrates the compartment for the alphanumeric character B. The letter B, which is imprinted upon the translucent window **25**, is visible only when the associated illuminating element **24** within the compartment is illuminated.

Referring again to FIG. **1**, the alphanumeric characters or the compartments to which the characters are assigned are divided into a number of groups **26-1** to **26-4**. Each of the groups is shown to be further divided or subdivided into four subgroups. For convenience, only the characters in the group **26-2** (upper right hand quadrant) have been illustrated. Others of the alphanumeric characters and various other characters which are employed in standard character sets may be assigned to the character locations in the other three groups or quadrants.

The display console also includes an additional set **27** of dispaly compartments located below the display screen **23**. This additional set of display compartments **27** is shown in FIG. **1** to bear the numerals 1 through 4 and a speed control information item (SL). The set of characters **27** are part of the code responsive feature of the present invention which must be enabled to initiate operation of the visual communication apparatus.

Before describing the circuits of the display console and code responsive apparatus, the technique of selecting characters or how an operator uses the communication apparatus will be first described.

In the standby mode or condition of the visual communication apparatus none of the characters on the display screen **23** is illuminated. The characters in the code responsive set **27** are illuminated one at a time in sequence on a repetitive basis. The operator activates the communication apparatus by entering a predetermined character sequence or code. He does this by actuating the switch **21** in time coincidence with the visual display of the numeric characters in the set **27** during consecutive cycles. FIGS. **3A** through **3D**, **4A** through **4D** and **5A** through **5D** illustrate the entry of an exemplary code of 4 3 2. During the first sequential presentation of the numeric characters, the switch **21** is activated when the character 4 is visually displayed as shown in FIG. **3D**. During the next sequential presentation of the characters, the switch is activated when the character 3 is displayed as shown in FIG. **4C**. During the next ensuing character presentation, the switch is activated when the character 2 is displayed as shown in FIG. **5B**. When the code has been thus correctly entered, the code responsive apparatus contained within the display console **20** produces a control signal which enables the display console circuits.

Once enabled, the display console circuits are operable to sequentially illuminate the character groups **26-1**, **26-2**, **26-3** and **26-4** as shown in FIGS. **2A** through **2D**. In FIGS. **2A** through **2D** as well as FIGS. **2E** through **2L**, the sector which is illuminated is cross-hatched. As an example, if the operator desires to select the letter D, he would activate the switch **21** when the sector **26-2** is illuminated as shown both in FIG. **1** and FIG. **2B**. The subgroups **26-21**, **26-22**, **26-23** and **26-24** within groups **26-2** would then be sequentially illuminated as shown in FIGS. **2E** through **2H**. In order to select the letter D the operator would again actuate the switch **21** when the upper lefthand sector or quadrant **26-21** within the group **26-2** is illuminated as in FIG. **2E**.

The A, B, C, D and E compartments in the subgroup or sector **26-21** would then be sequentially illuminated as shown in FIGS. **2I** through **2L**. The operator would then actuate the switch **21** when the letter D compartment is illuminated as in FIG. **2L**.

If the operator has selected the wrong group or subgroup, the illuminating sequence will continue for two sequencing cycles and then return to the sequential illumination of the groups so long as the switch **21** has not been actuated. In other words, if the operator makes an erroneous selection of a group or subgroup, he merely waits for the illumination sequence to revert from the subgroup sequencing to group sequencing.

Two items of information shown in group or quadrant **26-2** are for the purpose of providing control functions. Thus, the SP information item, if selected by the operator, causes the sequencing cycle to either speed up or slow down depending upon the speed of the sequencing cycle at the time the control item SP is selected. When the sequence cycle is operating at its slower rate, the speed control item SL in the additional display compartments **27** is illuminated. The OFF control item is selected by the operator when he wants to return the visual communication apparatus to its standby mode in which the code responsive display elements **27** are sequentially illuminated.

In the description which follows a number of circuit blocks shown in the drawing are discussed. These circuit blocks contain known circuits which are actuated by bi-level electrical signals applied thereto. When the signal is at one level, (say, the high level) it represents the binary digit 1 and when it is at the other level it represents the binary digit 0. Also, to simplify the discussion, rather than speaking of an electrical signal being applied to a block or logic state, it is sometimes stated that a 1 or a 0 is applied to the block or stage.

The flip flop, shift register, counter, one-shot multivibrator, and logic gates or other blocks shown in the drawing may take on any suitable form. For example, these known circuits may be selected from any or all of the following catalogs: Fairchild Semiconductor Integrated Circuit Catalog, a catalog of Fairchild Semiconductor, Inc., Texas Instrument TTL Integrated Circuit Catalog, a catalog of Texas Instrument, Inc., and Signetics, 54 – 74 Handbook, a catalog of Signetics, Inc.

Coincidence gates are represented in the drawing with the conventional AND gate symbol having a dot therein and OR gates are represented by the conventional OR gate symbol with a + contained therein. A small circle at the output of these gates represents signal inversion such that the AND and OR gates becomes NAND and NOR gates, respectively. When a signal flow path contains more than a single lead or conductor, a slash mark is made through the path together with an adjacent number indicating the number of conductors in the path. One final note before proceeding with the description, the signal leads have in some cases been interrupted and labeled rather than shown as continuous leads so as to avoid cluttering in the drawing.

Referring now to FIG. 7, there is shown a block diagram of visual communication apparatus which embodies the present invention. The switch **21** is essentially a key type switch which provides an input signal INP to a timing network **30** and a keyboard control network **31.** In its normal position the switch **21** is connected to a source of 0's **28** such that the input signal INP normally has a vlaue of 0. When the keying switch **21** is actuated, it is connected to a source of 1's **29** so that the input signal INP has a value of 1. The timing network **30** is arranged to provide a pair of clock signals $\phi 1$ and $\phi 2$.

The keyboard control network **31** responds to the input signal INP to provide either a code select pulse $\overline{CSP}$ to a code scan network **32** or a keyboard pulse KBDP to an address scan network **33.** In the standby mode, the code scan network **32** is operative to sequentially scan the code characters **27.** It is in this standby mode that the keyboard control network **31** provides the $\overline{CSP}$ code scan network **32.** A two bit code representing the code characters (1, 2, 3, or 4), which are illuminated at the time the $\overline{CSP}$ signal is received, is coupled from the network **32** to the keyboard control network **31.** When the appropriate code or character sequence has been entered by the operator, the keyboard control network ceases to supply $\overline{CSP}$ signals and commences to supply KBDP signals in response to further input INP signals. In addition, when the character sequence or code has been correctly entered, the keyboard control network **31** produces a keyboard on KBDON signal which is also applied to the address select network **33.** The complement signal $\overline{KBDON}$ is employed to enable the code scan network during the standby mode and to disable it when the code has been correctly entered.

When enabled by the KBDON signal, the address scan network **33** provides a set of codes or binary numbers sequentially, one at a time, to an X and Y decoder and driver network **36.** The network **36** decodes the binary numbers and in response thereto provides illumination drive signals to the appropriate groups and illumination elements of the dsiplay screen. For convenience, the visual communication apparatus circuits are being illustrated for the case where the display screen is comprised of **16** display element locations or one quadrant or group of the display screen **23** of FIG. **1.** For this reason, the display screen has been labeled **26-2** in FIG. **7** and it will be assumed that the display characters or information items are the same as those shown for the display area **26-2** in FIG. **1.** Accordingly, the networks **33** and **36** will be operative to sequentially illuminate the subgroup or sector areas **26-21, 26-22, 26-23** and **26-24** and, once a particular sector is selected, will be further operative to sequentially illuminate the characters within the selected sector.

The output of the address scan network is essentially a four bit code together with its four complement signals and two additional control signals as designated by the numeral **10.** The four code signal elements represent a character code CHC which is applied to a character register **37** at its data in D_i input. The character code is loaded into the register **37** only when a character has been properly selected by the operator by means of a load signal CHLD applied to the LD input of register **37** from the address scan network **33.** This code contained in register **37** together with a data valid signal also produced by network **33** can be applied to the recording device **22** (FIG. **1**).

The character code CHC is also applied to the keyboard control network **31** which reponds thereto to interpret the selection of either of the control functions SP or OFF. When the OFF function is selected by the operator, the keyboard control network disables the KBDON signal. When the SP (speed control) function is selected by the operator, the keyboard control network **31** responds by issuing a speed change SCH signal to the timing network **30.** The timing network **30** responds to the SCH signal to either speed up or slow down the clock signal ϕ and to control the illumination of the SL lamp in additional display compartments **27.**

Referring next to FIG. **11,** there is shown a typical illumination element or crosspoint of the matrix or array of illumination elements which make up the display screen **26-2.** As shown in FIG. **11,** the crosspoint is defined by the crossing of an X (row) and Y (column) conductor. Between each of these conductors at each crosspoint is connected a diode **39** and an illuminating element (a lamp) **40.** When the decoder and driver networks **36** select an X and a Y conductor, a circuit will be completed between the selected X and Y conductors to provide current flow in the conventional sense through the lamp **40** causing it to illuminate.

Referring now to FIG. **8,** the keyboard control network **31** is shown to include a pair of NAND gates **40** and **41** which respond to the input INP signal to produce either the complement $\overline{CSP}$ of a CSP signal or the KBDP signal, respectively. When one of these gates is enabled the other is disabled and vice versa by a keyboard on/off D-type flip flop **43.**

During the standby mode, the Q and $\overline{Q}$ outputs of flip flop **43** are 0 and 1, respectively, so as to enable gate **40** and disable gate **41.** As the operator operates the switch **21** (FIG. 7) in the standby mode, each INP signal is passed by the enable gate **40** as a $\overline{CSP}$ signal to the code scan network **32.** The $\overline{CSP}$ signal is also inverted by means of an inverter **45** so as to apply a CSP signal to the shift SH inputs of a pair of registers **46** and **47.**

The code scan network **32** includes a scan counter **49** and a decoder and driver network **50** which when enabled by the $\overline{KBDON}$ signal responds to the count values of the counter **49** to sequentially illuminate the numeric characters 1, 2, 3, 4 of the additional display compartment set **27.** The $\overline{CSP}$ signal is applied to the clear CL input of the scan counter **49** and the clock signal $\phi 1$ is applied to the count input CP thereof. In the absence of an INP signal, the $\overline{CSP}$ signal is a 1 whereby counter **49** responds to the clock signal $\phi 1$ to cycle through its count values. For the case of the illustrated embodiment of the code responsive apparatus where only four code elements are to be scanned, the counter **49** may simply be a two bit counter such that there are four count values to be cycled through. The decoder and driver network **50** responds to the sequential presentation of these count values to decode and sequentially illuminate the numeric characters 1 through 4 of the additional character set **27.** To this end, the decoder may simply comprise a set of four NAND gates approximately connected to the outputs of counter **49** (including the 1's complements of these outputs) with each NAND gate being enabled by the $\overline{KBDON}$ signal. That is, the scan counter **49** is enabled at all times to cycle through its count value, but the decoder **50** responds to the count values only during the standby mode to sequentially illuminate the code elements 1 through 4. When a $\overline{CSP}$ signal is produced in response to an INP signal (actuation of the key type switch **21**), the counter **49** is cleared and begins to cycle through its count values anew.

The bits of the count outputs of the scan counter **49** are applied to the data in D_i inputs of a pair of registers **46** and **47.** The $\overline{CSP}$ signal is inverted by means of an inverter **45** so as to apply a CSP signal to the shift SH input of these registers. In operation then the count value of the scan counter **49** which exists at the time a $\overline{CSP}$ signal is generated, is shifted into the registers **46** and **47** with one bit occupying the first bit position of register **46** and the other bit occupying the first bit position of register **47.** On the next two ensuing $\overline{CSP}$ signals, two more count values are similarly shifted into the registers **46** and **47.** Assuming that the three count values now stored in the registers **46** and **47** do indeed represent the correct code, a code combination decoder **48** responds thereto to produce a 1 to 0 transition at its output. This 1 to 0 transition is applied to the clear input of flip flop **43** whereby flip flop **43** changes state. This disables the decoder and driver network **50,** clears the registers **46** and **47,** disables NAND gate **40** and enables NAND gate **41.** The KBDON signal now becomes a 1 so as to enable the address scan network (FIGS. **7** and **9**) to cause the character code CHC to change from the OFF value. The keyboard OFF decoder **44** in FIG. **8** responds thereto to produce a 1 at the D input of flp flop **43.** Accordingly, flip flop **43** will remain in this state, until the operator again selects the OFF control function. When this does happen, the decoder **44** will apply a zero to the D input of flip flop **43** and KDBP signal generated by the INP signal produced by this selection will cause the flip flop **43** to change its state. The keyboard control network is then returned to the standby mode of operation.

The design of the code combination decoder **48** is, of course, a function of the code to which the code responsive apparatus will respond. For example, for a code consisting of three consecutive count values of 11, the code combination decoder may suitably comprise a set of gates which performs a six input AND function with signal inversion (a six input NAND function) to produce a 1 to 0 transition when the third count value of 11 is selected by the operator.

The keyboard control network **31** is shown to further include a speed change decoder **60** which receives the character code CHC from the counters **34** and **35** (FIG. 7) to detect the code representing a speed change SP selection by the operator, and to produce a speed change signal SCH. Since this code is generated once per scan cycle when sub-group **26-24** has been selected (see FIG. 1), the speed change decoder is enabled by the KDBP pulse only when the operator selects the SP speed change items. The decoders **44** and **60** may comprise any suitable gating function for the codes assigned to the OFF and SP functions. For example, if the codes are 1111 and 1101, each decoder can take the simple form of a four input NAND gate with the complement of the 0 bit position being employed. In addition, the output of the SP decoding gate would be further gated with the KBDP signal via an AND gate.

Still referring to FIG. **8,** the timing network is shown to include a one shot multivibrator **51** which is connected as a gated pulse generator to produce a sequence of pulses until interrupted by the input INP signal. To this end, the INP signal is inverted by means of an inverter **52** so as to normally enable a NAND gate **53** to pass the pulse sequence from the $\overline{Q}$ output of one shot **51** to its input. When the INP signal becomes a 1, gate **53** becomes diabled so as to interrupt the pulse sequence produced by one shot **51.**

A pair of one bit counters **54** and **55** serve to divide the frequency of the pulse sequence. Both of these counters are employed during the slow operating mode and only one of these counters, **55,** is employed during the fast operating mode. A speed control flip flop **59** and a set of steering gates **56** through **58** serve to control whether just counter **55** or both counters **54** and **55** will be employed to divide the frequency of the pulse sequence produced by one shot **51.** To this end, flip flip **59** is connected as a one bit counter with its $\overline{Q}$ output being applied to its D input. The clock input CP is connected to the speed change signal SCH produced by the speed change decoder **60** in the keyboard control network **31.**

For the fast mode of operation, flip flop **59** is in the state where its Q and $\overline{Q}$ outputs are 0 and 1, respectively. This causes gate **56** to be disabled so as to apply a 1 to the input of gate **58** and gate **57** to be enabled to pass the output of counter **54** to the other input of gate **58.** The output of gate **58** then drives the count input of the counter **55.** On the other hand in the slower operating mode, the Q and $\overline{Q}$ outputs of flip flop **59** are 1 and 0, respectively. This causes gate **57** to be disabled so as to apply a 1 to one input of gate **58.** Gate **56** is enabled so as to pass the pulse sequence from the

$\bar{Q}$ output of one shot **51** to the other input of gate **58.** Accordingly, in the faster operating mode only the counter **55** is connected to divide the frequency of the pulse sequence.

The clock signal $\phi 2$ is taken from the output of the gate **58.** The clock signal $\phi 1$ is taken from the output of an AND gate **62** which gates the Q output of counter **55** with the Q output of a flip flop **61.** The flip flop **61** serves to double the normal key or quadrant dwell time after each actuating switch depression. This feature is desirable in order to avoid confusion of the operator when the keyboard recycles to the first quadrant, subquadrant or key. This gives the operator an opportunity to view his selection before the next cycling sequence in the selection process takes place. To accomplish this, flip flop **61** has its D input connected to a source of 1's and its clock input CP connected to the $\bar{Q}$ output of counter **55.** The complements of the INP signal (taken from the output of inverter **52**) serves to clear counters **54** and **55** as well as flip flop **61** whenever the INP signal has a 0 to 1 transition. This cause the Q output of flip flop **61** to be a 0 and the Q and $\bar{Q}$ outputs of counter **55** to be 0 and 1, respectively. Upon the occurrence of the next $\phi 2$ signal, the one bit counter **55** will change its state such that its Q and $\bar{Q}$ outputs become 1 and 0, respectively. Flip flop **61** does not change state at this time such that gate **62** is disabled by the 0 from the Q output of flip flop **61** so that no $\phi 1$ clock pulse is produced. When the $\phi 2$ signal again occurs, the counter **55** will change its state such that its Q and $\bar{Q}$ outputs become 0 and 1, respectively. This will cause flip flop **61** to change its state so that its Q output becomes a 1 to enable the gate **62.** For all subsequent $\phi 2$ pulses in the absence of another INP signal, the flip flop **61** does not change state such that the gate **62** is enabled to pass the pulse sequence occurring at the Q output of the counter **55** as the clock signal sequence $\phi 1$.

With reference now to FIG. **9**, the address scan network **33** includes a pair of AND gates **67** and **68** which, when enabled by the KBDON signal, steer the clock signal $\phi 1$ to a selected one of a number of counters, namely, a group counter **34** and a subgroup counter **35** depending upon the stage in the character selection process to which the operator has progressed. The outputs of the counter **34** and **35** together with the outputs of a counter select flip flop **66** constitute the ten signal elements previously referred to as being applied to the X and Y decoder **36** (FIG. **10**).

During the standby mode of operation, the counters **34** and **35** are cleared to the all 0's state and the KBDON signal is a 0 such that AND gates **67** and **68** are disabled from coupling the $\phi 1$ clock signal to either of the counters. The counter select flip flop **66** is in the state where its Q and $\bar{Q}$ ouputs are 0 and 1, respectively. When the operator has entered the correct code, the KBDON signal becomes a 1. This fully enables gate **68** to pass the $\phi 1$ clock signal to the group counter **34.** The group counter **34** begins to cycle through its four count values which are interpreted by the decoder network **36** so as to sequentially illuminate the quadrants **26-21** through **26-24** (FIGS. **1** and **7**).

When the operator selects a quadrant, a KBDP pulse will be generated. The complement $\overline{KBDP}$ is applied as one input of a NAND gate **65.** NAND gate **65** is enabled at this time by the output of an override counter **38** (which is described below). This will produce a 0 to 1 transition at the output of gate **65** which is applied to the CP clock input of flip flop **66.** Flip flop **66** then switches so that its Q and $\bar{Q}$ outputs become 1 and 0, respectively. AND gate **68** becomes disabled and AND gate **67** is now fully enabled to steer the clock signals $\phi 1$ to the CP clock input of the subgroup counter **35.**

The subgroup counter **35** now begins to cycle through its four count values which are interpreted by the X and Y decoder network **36** to sequentially illuminate the characters within the selected quadrant as determined by the count value of group counter **34.** The lower order bit ($\bar{D}$) of the subgroup counter **35** is applied to the override counter **38.** The purpose of the override counter **38** is as follows. If the operator discovers that his selection of the quadrant or group is erroneous, he does not actuate the switch **21.** The override counter **38** then counts through two sequencing cycles of the subgroup counter **35** to produce a 1 to 0 transition at its output. This 1 to 0 transition causes the output of NAND gate **65** to produce a 0 to 1 transition to thereby switch flip flop **66** to the state where its Q and $\bar{Q}$ output are 0 and 1, respectively. As described above, this state of flip flop **66** selects group counter **34** to receive the clock signals $\phi 1$ whereby the character selection process begins anew with the quadrants **26-21** through **26-24** being sequentially illuminated. The operator may now make a correct selection.

Returning now to the point in the character selection process where the operator has made a correct selection of a quadrant, the subgroup counter **35** begins to cycle through its count value. When the operator properly selects a character (within two cycles of counter **35**) a KBDP pulse will be generated. A NAND gate **69** is enabled by the 1 at the Q output of flip flop **66** to pass the KBDP pulse to the clear CL inputs of counters **34** and **35.** This causes counters **34** and **35** to return to the all 0's count value. The KBDP pulse will be passed by NAND gate **65** to produce a 0 to 1 transition at its output. This causes flip flop **66** to change state such that its Q and $\bar{Q}$ outputs become 0 and 1, respectively. The 1 to 0 transition at the Q output of flip flop **66** causes the override counter **38** to become cleared to its all 0's state. However, the override counter output which is applied to AND gate **65** is the complement of its second stage and is a 1 at this time.

The address scan network is now in condition for the character selection process to begin anew so that the operator can select another character. When it is desired to turn the visual communication apparatus off, the operator first selects the quadrant **26-24** and then selects the OFF control function while the subgroup counter **35** is cycling. This will cause the keyboard control network to produce a KBDP pulse. The OFF code is detected by the KBD OFF decoder **44** (FIG. **8**) so as to cause flip flop **43** to switch and thereby cause the KBDON signal to become a 0. This disables AND gate **67** and **68** in FIG. **9.** The $\overline{KBDP}$ pulse is passed by NAND gate **69** to clear the counters **34** and **35** to their all 0's count value. The KBDP pulse is passed by NAND gate **65** to cause flip flop **66** to change to its state where its Q and $\bar{Q}$ outputs are 0 and 1, respectively. The 1 to 0 transition at the output of flip flop **66** causes the override counter **38** to clear. The address scan network has now been returned to its standby mode.

As described above when the character selection process is at the point where the operator has selected

a quadrant and is about to select a character, the Q output of flip flop **66** is a 1. This enables a NAND gate **70.** When the operator does make a character selection at this time, a KBDP pulse is generated which is passed by NAND gate **70** as a 1 to 0 transition to the clear input of a flip flop **71.** The flip flop **71** has its D input connected to a source of 1's and its clock input CP connected to receive the $\phi 2$ clock pulse sequence. The 1 to 0 transition at its clear input at this time causes flip flop **71** to become cleared to the state where its Q and $\bar{Q}$ outputs are 0 and 1, respectively. The 0 to 1 transition at the $\bar{Q}$ output of flip flop **71** is the character load CHLD signal which causes the character code at the output of counters **34** and **35** to be loaded into the character register **37** (FIG. 7). On the next ensuing $\phi 2$ clock pulse, the flip flop **71** will switch back to the state where its Q and $\bar{Q}$ outputs are 1 and 0, respectively. The 0 to 1 transition at the Q output of flip flop **71** is the data valid signal which signals the recording device that the data contained in character register **37** is valid. The flip flop **71** will remain in this state until NAND gate **70** produces another 1 to 0 transition (at the time the operator makes another character selection).

Referring to FIG. **10,** the X and Y decoder network **36** is shown to include an X decoder and a Y decoder. The circuit elements and connections therebetween are substantially identical and corresponding circuit elements have been given identical reference numerals followed by either an X or a Y to identify to which decoder it belongs. There is one exception, however. The signal elements A, $\bar{A}$, C and $\bar{C}$ applied to circuit elements in the Y decoder are replaced with the signal elements B, $\bar{B}$, D and $\bar{D}$ respectively, in the X decoder for the corresponding circuit elements.

When the group counter **34** (FIG. **9**) is cycling, the Q and $\bar{Q}$ outputs of flip flop **66** (designated as FF**66**Q and FF**66**$\bar{Q}$, respectively in FIG. **10**) are 0 and 1, respectively. This selects a pair of NAND gates **75**Y and **76**Y in the Y decoder and a pair of NAND gates **75**X and **76**X in the X decoder which test the A and B output, respectively, of the group counter. A number of gates **81**Y through **84**Y and **81**X through **84**X are arranged in pairs to monitor the changes in signal condition at the outputs of the gates **75**Y, **76**Y, **75**X and **76**X. Thus, gates **81**Y and **82**Y both receive the output of gate **75**Y, gates **83**Y and **84**Y receive the output of gate **76**Y, and so on. The outputs of gates **81**Y and **82**Y are connected via line drivers **85**Y and **86**Y to the two left hand columns of the array **26-2** (FIG. 7). The outputs of gates **83**Y and **84**Y are connected via line drivers **87**Y and **88**Y to the two right hand columns of the display array. The outputs of gates **81**X and **82**X are connected via line drivers **85**X and **86**X to the top two rows of the display array. Finally, the outputs of gates **83**X and **84**X are coupled via line drivers **87**X and **88**X to the bottom two rows of the display array.

During the time that the group counter is cycling, the gates **81**Y through **84**Y and **81**X through **84**X are enabled by the outputs of another set of gates **77**Y through **80**Y, **77**X through **80**X, respectively. This is so since each of these gates has as an input FF**66**Q which is a 0 at this time. Accordingly, whenever the output of one of the gates **75**Y, **76**Y, **75**X or **76**X goes to 0, the outputs of its associated gate pair will become a 1. For example, when counter **34** is in its all 0's state (A=0, B=0), the outputs of gates **75**Y and **75**X will be 0's and the outputs of gate **76**Y and **76**X will be 1's. This causes the outputs of gates **81**Y, **82**Y, **81**X and **82**X to be all 1's to thereby select the upper left hand quadrant of the display array **26-2** as defined by the two left hand columns in the two top rows. For the next count value of 10 (A = 1, B = 0), the outputs of gates **76**Y and **75**X will be 0's and the outputs of gates **75**Y and **76**X will be 1's. This causes the outputs of gates **83**Y, **84**Y, **81**X and **82**X to be all 1's thereby selecting the upper right hand quadrant as defined by the two right hand columns in the two top rows. For the next two count values 01 and 11, the decoder is operative in a similar manner to select the lower left and right hand quadrants, respectively.

When a particular quadrant has been selected by the operator, the flip flop **66** changes state, such that FF**66**Q and FF**66**$\bar{Q}$ become 1 and 0, respectively. The subgroup counter **35** then begins to cycle. Gates **77**Y to **80**Y and **77**X to **80**X are all enabled by the 1 value of FF**66**Q. The output of gates **77**Y to **80**Y and **77**X to **80**X are monitored by gates **81**Y to **84**Y and **81**X to **84**X, respectively, since these latter gates are all enabled by the 1's at the outputs of the corresponding gates **75**Y, **76**Y, **75**X and **76**X which are disabled by the 0 value of FF**66**$\bar{Q}$.

As an example, suppose that the operator has selected the upper right hand quadrant. Since A = 1 and B = 0 for this case, only gates **79**Y, **80**Y, **77**X and **78**X will be enabled to monitor the C and D outputs of the subgroup counter **35.** For the subgroup count value of 00 (C = 0, D = 0), the outputs of gates **79**Y and **77**X are 0's. This causes the outputs of the associated gates **83**Y and **81**X to be 1's to thereby select for illumination the upper left hand character (E in FIG. **1**) of the selected upper right hand quadrant sector. For the subgroup count values of 10 (C = 1, D = 0), the outputs of gates **80**Y and **77**X are 0's. This causes the outputs of the corresponding gates **84**Y and **81**X to be 1's so as to select for illumination the upper right hand character (F) in the selected upper right hand quadrant. For the next two subgroup count values of 01 and 11 the decoder is operative in a similar manner to select the lower left (G) and right (H) hand characters, respectively, in the selected upper right hand quadrant. For other selected quadrants the operation of the subgroup cycling is similar with the gates which monitor the C and D outputs of the subgroup counter being determined by the count value A and B of the group counter.

What is claimed is:

1. Communication apparatus comprising:

a manually operable switch;

display means including

a. sequential group display means for sequentially displaying the items of a set of information items a group at a time, and

b. sequential time display means for sequentially displaying the items of a selected group an item at a time; and

a control network including

a. means for initiating the operation of said sequential group display means,

b. means responsive to the actuation of said switch during the visual display of a selected one of the groups to initiate the operation of the sequential item display means so as to sequentially display the information items within the selected group, and

c. means responsive to a further actuation of the switch during the visual display of a selected one of the information items to interrupt the operation of the sequential item display means.

2. Communication apparatus as set forth in claim 1 wherein said sequential group display means and said sequential item display means both operate on a cyclic basis; and

wherein said control network further includes an override means which interrupts the operation of said sequential item display means in the absence of an actuation of said switch during a predetermined number of sequential item display cycles.

3. Communication apparatus as set forth in claim 1 wherein said display means further includes a display screen upon which said items are displayed sequentially either a group or an item at a time by said sequential group and item display means, respectively, at addressable locations thereon;

wherein said sequential group and item display means include a group and item counter, respectively;

wherein said control network further includes

a timing generator which produces a clock pulse sequence; means responsive to each switch actuation to produce a

switch pulse; and

a steering control network responsive to said switch pulses to alternately enable said sequential group initiating means and said sequential item initiating means to steer said clock pulse sequence to said group and item counters; respectively, which respond thereto to sequentially generate the addresses of each group of each item within a selected group, respectively.

4. Communication apparatus as set forth in claim 3 wherein said interrupt means responds to the switch pulse produced by said further switch actuation to clear both of said counters.

5. Communication apparatus as set forth in claim 4 wherein said timing generator includes means for interrupting the generation of said clock pulse sequence for the duration of each said switch pulse.

6. Communication apparatus as set forth in claim 5 wherein said timing generator further includes means for delaying the generation of said clock pulse sequence after each switch pulse.

7. Communication apparatus as set forth in claim 6 wherein said control network further includes means responsive to the selection of one of said information items to disable said switch pulse producing means and said group and item initiating means.

8. Communication apparatus as set forth in claim 7 and further including means for displaying an additional set of symbols one at a time in sequence during consecutive cycles whenever said group and item initiating means are disabled; and

means for producing a control signal, whenever said switch has been sequentially activated in coincidence with the visual display of the symbols of a predetermined code; and

wherein said disabling means responds to said control signal to enable said switch pulse producing means and said group and item initiating means.

9. Communication apparatus as set forth in claim 8 wherein said control network further includes further means responsive to the selection of a further one of said information items to produce a speed control signal; and

wherein said timing generating means responds to said speed control signal to change the frequency of said clock pulse sequence.

10. Communication apparatus as set forth in claim 9 wherein said display screen comprises a plurality of compartments each containing an illuminating element and each having a translucent window bearing an information item which is visible when the illuminating element is illuminated, said compartments being arranged in rows and columns; and

wherein said group and item addressing means addresses said compartments by rows and columns.

11. Code responsive apparatus comprising:

means for displaying during consecutive cycles a set of characters one at a time in sequence;

a manually operable switch; and

a control circuit for producing a control signal whenever said switch has been sequentially activated in coincidence with the visual display of the characters of a predetermined code.

12. Code responsive apparatus as set forth in claim 11

wherein said display means includes a display screen upon which said characters are displayed at addressable locations; and

address generating means which generates the addresses of said characters one at a time in sequence on a cyclic basis.

13. Code responsive apparatus as set forth in claim 12

wherein said control circuit includes storage means for storing the addresses of the characters which coincide in time with the actuation of said switch; and

means for producing said control signal when said stored addresses correspond to the characters of the predetermined code.

* * * * *

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,771,156 Dated November 6, 1973

Inventor(s) Eugene R. V. Watts, et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 12, Line 56 Claim 1 change "time" to --item--.

Signed and sealed this 16th day of July 1974.

(SEAL)
Attest:

McCOY M. GIBSON, JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents