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US-A- 3 911 378
US-A- 4 827 226

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Description

This invention relates to voltage controlled oscillator circuits.

In prior art, a useful form of an oscillator circuit is a crystal oscillator circuit. Such a circuit comprises an oscillator element (e.g., quartz crystal), a pair of electrodes attached to the oscillator element, and an inverting amplifying element connected across the electrodes. Such a circuit has a resonant frequency f_R at which it will oscillate, this frequency depending in a rather complicated manner upon the effective parameters (inductance, capacitance, resistance) of the various elements, including the crystal. A separate capacitor, connected between each one of the electrodes and ground, can be added for the purpose of changing ("tuning") the resonant frequency of the circuit.

In order to vary ("pull") the resonant frequency of a crystal oscillator circuit while it is oscillating, a varactor (variable capacitor) is substituted for each capacitor. More specifically, in prior art a Pierce oscillator circuit comprises:

(a) a crystal oscillator element having first and second terminals;

(b) a first varactor having one of its terminals connected directly to the input terminal of the amplifier and another of its terminals connected to a common node;

(c) a second varactor, substantially identical to the first varactor, having one of its terminals connected directly to the output terminal of the amplifier and another of its terminals connected directly to the common node; and

(d) means for applying a control voltage to the common node in order to vary the oscillation frequency of the oscillator element.

During circuit operation, the capacitance of the varactor is varied by varying an external (control) voltage V_C applied to the varactor, whereby the resonant frequency of oscillation of the circuit is pulled ("shifted") by an amount Δf_R that depends upon the magnitude of V_C. However, in many practical applications, the range (interval) of resonant frequencies ("pull range") at which the circuit can oscillate at a frequency that is linearly dependent upon applied voltage is limited to a narrower frequency interval (f_{max}-f_{min}) than is desired. For example, in some practical applications, it is desired to synchronize the clock circuits of two remotely located pieces of equipment by means of a separate VCXO located at each of them, one or both of the VCXOs having unavoidable resonant frequency fluctuations caused by local ambient temperature fluctuations. In such cases, the resonant frequency pull range of one of the VCXOs may not be wide enough to accommodate the unavoidable frequency fluctuations of the other VCXO.

US-A-4 827 226 discloses an oscillator including a crystal oscillator connected in a Pierce oscillator circuit configuration, which is adjustable by means of a tuning network including a pair of digitally adjustable capacitors.

It is desirable to have VCXO circuitry that will increase the pull range.

According to this invention there is provided a voltage controlled oscillator circuit as claimed in claim 1.

In the operation of an embodiment of the invention, the input control voltage V_C is applied through an input network to the two common nodes such that the resulting auxiliary control voltages V_A and V_B, respectively, applied to these nodes differ in a nonlinear manner as a function of V_C. For example, the input network can be arranged so that the auxiliary control voltages V_A and V_B can advantageously differ by the gate-to-source voltage drop of an MOS transistor. Further, in order to achieve (near) linearity over a wider range of input voltages V_C, the aforementioned auxiliary control voltages V_A and V_B may be derived from a non-linear voltage divider network which compensates for other circuit nonlinearities. The flexibility offered by the two common nodes thus enables simultaneously wider pull range and better linearity.

The invention will now be described with reference to the accompanying drawings, in which:

FIG. 1 is a schematic diagram of a known VCXO circuit;

FIG. 2 is a schematic diagram of a VCXO circuit embodying the invention; and

FIG. 3 is a schematic diagram of a nonlinear voltage divider network useful for developing control voltages for the circuit shown in FIG. 2.

As shown in FIG. 1, a VCXO circuit 100 has an input control voltage terminal 70 and a pair of output terminals 26 and 27. The circuit 100 further comprises a crystal oscillator element 11, typically a quartz crystal, to which a pair of electrodes 12 and 13 are attached. Still further, an inverting amplifier 20 in the circuit 100 has an input terminal 22 connected to the electrode 12 and an output terminal 23 connected to the electrode 13. For a Pierce oscillator circuit, as is preferred, the amplifier 20 is connected in a common source configuration (in MOS technology); that is, for example, the input terminal 22 is connected to the gate of a driver MOS transistor whose source terminal is connected to a fixed voltage source V_{SS} and whose drain terminal is connected to the output terminal 23 of the amplifier 20, the output terminal of the amplifier being connected through a load to another fixed voltage source V_{DD}. The electrode 12 is connected through a first varactor 30 to a common node 35, and the electrode 13 is connected to a second varactor 40 to the same common node 35. These first and second varactors 30 and 40 are preferably substantially identical ("matched pair"), in order to balance the circuit. However, for useful operation, they can differ by as

much as about a factor of 2. The common node 35 is connected to ground through a capacitor 50. The common node 35 also connected through a resistor 60 to the input control voltage terminal 70.

During circuit operation, the input control voltage V_C is applied to the control voltage terminal 70 for the purpose of pulling the resonant oscillation frequency f_R. The resistor 60, as known in the art, helps to isolate the circuit 100 from noise at the input terminal 70, as well as to minimize power dissipation at the oscillation frequency.

In addition, a resistor 24 is connected across the amplifier 20, as known in the art, in order to ensure that the average voltage on the input and output terminals 22 and 23 are the same, whereby distortion in the output, caused by otherwise large deviations from the desired 50 percent in the duty cycle of the output waveform are minimized.

A voltage limiter 25 is connected across the amplifier 20, as known in the art, in order to limit the amplitude of oscillations and hence to render the control voltages V_C more effective in pulling the resonant oscillation frequency f_R--i.e., to increase (df_R/dV_C), and hence to increase the pull range.

The purpose of the capacitor 50, as known in the art, is to stabilize the de voltage at the common node 35. Typically, it has a capacitance equal to at least about ten times that of the (equal) varactors 30 and 40.

The output terminals 26 and 27 of the circuit 100 are to be connected to the input and output terminals 22 and 23, respectively, of the amplifier 20. Utilization means 81 or 82 or both are connected respectively to the output terminals 26 and 27 of the circuit 100. The oscillations received by the utilization means 81 will have smaller amplitude than those received by the utilization means 82 but will be more nearly purely sinusoidal. Typically, the utilization means are clock circuits to be synchronized by the VCXO circuit 100.

The addition of the varactor 30, in addition to the varactor 40, or of the varactor 40 in addition to the varactor 30, serves to balance the circuit 100. That is, by making equal the variable impedances of the electrodes 12 and 13 to the input control terminal 70, as well as by making equal the variable impedances of the electrodes 12 and 13 to ground, there is achieved a better circuit balancing, which in turn entails less required semiconductor area on which to build the circuit, less power loss, and greater circuit stability. On the other hand, moderate difference between the varactor parameter--say, one varactor being about twice as large as the other--can be useful in some instances, as for modifying the relationship between signal amplitude at terminal 26 relative to terminal 27.

Capacitors 28 and 29 optionally can be connected to the output terminal 26 and 27, respectively, in order to modify permanently the resonant frequency f_R of the circuit 100, as well as to increase the linearity of Δf_R vs. V_C (at some expense of pull range, however).

Advantageously, the capacitances of both capacitors 28 and 29, though not necessarily equal, are both less than those of varactors 30 and 40 by at least a factor of about five.

Referring now to FIG. 2, elements shown therein which are similar to, or the same as, those shown in FIG. 1 are denoted by the same reference numerals. As shown in FIG. 2, a VCXO circuit 200 is derived from the above-described VCXO circuit 100 (FIG. 1) by the addition of a parallel path supplied by varactors 31 and 41 connected to a second common node 36, together with a capacitor 51 connected between ground and this second common node 36. Advantageously, all the varactors 30, 31, 40, and 41 are matched. In addition, a resistor 61 is added, for the same purpose as resistor 60, and is connected to the second common node 36. A constant current source 71 is connected to the source terminal 73 of a p channel MOS transistor 72, and the gate terminal 74 of this MOS transistor 72 is connected to the input control voltage terminal 70.

During operation the control voltage V_C is applied at this input control voltage terminal 70, and auxiliary control voltages V_A and V_B, respectively, are developed at common nodes 36 and 35. These voltages V_A and V_B differ by the diode gate-to-source voltage drop of the transistor 72. Thus, these voltages V_A and V_B respond in a nonlinear way with respect to the input control voltage V_C. By properly selecting the various parameters of the circuit 200, this nonlinearity in V_A and V_B can serve to compensate for the nonlinearities in the above-described circuit 100, whereby a more nearly linear Δf_R vs. V_C is obtained in the circuit 200 than in the circuit 100. The added varactor paths in the circuit 200 thus give flexibility to achieve more near linearity of Δf_R vs. V_C in the circuit 200 than in the circuit 100.

FIG. 3 shows a nonlinear voltage divider network 300 which can advantageously be used for the purpose of producing the aforementioned voltages V_A and V_B at terminals 36 and 35, respectively, instead of the arrangement shown in FIG. 2 for this purpose. Elements shown in FIG. 3 that are similar to, or the same as, those shown in FIG. 2 , are denoted by the same reference numerals.

As shown in FIG. 3, a voltage divider is formed by the series connection of resistors 62, 63, and the source-to-drain resistance of an auxiliary p channel MOS transistor 64 whose gate is connected to its drain (load configuration). The gate terminal 74 of the transistor 72 is connected to a node 65 between the resistors 62 and 63. As a consequence of the nonlinear characteristics of the source-drain resistance of the MOS transistor 64, the voltage developed at the gate terminal 74 is a nonlinear function of V_C, rather

than being equal to V_C as in the circuit 200 (FIG. 2). Moreover, this nonlinearity can further compensate for the nonlinearities in the circuit 200.

Although the invention has been described in detail with respect to specific embodiments, various modifications can be made.

For example, additional varactors connected to additional control voltages can be added, in order to provide even more nearly linear oscillation frequency response.

Claims

1. A voltage controlled oscillator circuit comprising a crystal oscillator element (11) having first and second terminals, (12,13), an amplifier (20) having an input terminal (22) connected to said first terminal (12) and an output terminal (23) connected to said second terminal (13), a first varactor (30) having one of its terminals connected directly to the input terminal of the amplifier and another of its terminals connected to a common node (35), a second varactor (40) having one of its terminals connected directly to the output terminal of the amplifier and another of its terminals connected directly to the common node, means (70,60) for applying a control voltage (V_A) to the common node in order to pull the oscillation frequency of the oscillator element (11), and CHARACTERISED BY a third varactor (31) having one of its terminals connected to the input terminal of the amplifier and another of its terminals connected to another common node (36), a fourth varactor (41) having one of its terminals connected to the output terminal of the amplifier and another of its terminals connected to said other common node, and means (72, 61) for applying a bias voltage V_B, different from the control voltage (V_A) to said other common node.

2. A circuit as claimed in claim 1 comprising utilization means (82) connected to the output terminal of the amplifier.

3. A circuit as claimed in claim 1 or 2 comprising utilization means (81) connected to the input terminal of the amplifier.

4. A circuit as claimed in claim 1, 2 or 3 wherein the means for applying a bias voltage comprises a first MOS transistor (72), a current source (71) connected to a high-current-carrying terminal of the first MOS transistor for driving a constant current through the source-drain path of the first MOS transistor, resistive means (60) for connecting said common node to the gate terminal (74) of the first MOS transistor, and resistive means (61) for connecting said other common node to the high-current-carrying terminal of the first MOS transistor.

5. A circuit as claimed in claim 4 comprising first and second resistors (62,63) and a second MOS transistor (64) mutually connected in series, the node (65) between the first and second resistors being connected to the gate terminal of the first MOS transistor.

6. A circuit as claimed in any preceding claim wherein the capacitances of the first, second, third and fourth varactors are mutually equal for any applied operating voltage.

Patentansprüche

1. Spannungsgesteuerte Oszillatorschaltung umfassend: einen Kristalloszillator (11) mit einem ersten und zweiten Anschluß (12, 13),
einen Verstärker (20) mit einem an den ersten Anschluß (12) angeschlossenen Eingangsanschluß (22) und einem an den zweiten Anschluß (13) angeschlossenen Ausgangsanschluß (23),
einen ersten Varaktor (30), dessen einer Anschluß unmittelbar mit dem Eingangsanschluß des Verstärkers und dessen anderer Anschluß an einen gemeinsamen Knoten (35) angeschlossen ist, einen zweiten Varaktor (40), dessen einer Anschluß unmittelbar an an den Ausgangsanschluß des Verstärkers und dessen anderer Anschluß unmittelbar an den gemeinsamen Knoten angeschlossen ist,
eine Einrichtung (70, 60) zum Anlegen einer Steuerspannung (V_A) an den gemeinsamen Knoten, um die Schwingungsfrequenz des Oszillators (11) zu ziehen,
gekennzeichnet durch,
einen dritten Varaktor (31), dessen einer Anschluß an den Eingangsanschluß des Verstärkers und dessen anderer Anschluß an einen anderen gemeinsamen Knoten (36) angeschlossen ist,
einen vierten Varaktor (41), dessen einer Anschluß an den Ausgangsanschluß des Verstärkers und dessen anderer Anschluß an den gemeinsamen Knoten angeschlossen ist, und
eine Einrichtung (72, 61) zum Anlegen einer Vorspannung V_B, die die sich von der Steuerspannung (V_A) an dem anderen gemeinsamen Knoten ist.

2. Oszillatorschaltung nach Anspruch 1, gekennzeichnet durch eine Nutzungseinrichtung (82), die an den Ausgangsanschluß des Verstärkers angeschlossen ist.

3. Oszillatorschaltung nach Anspruch 1 oder 2, gekennzeichnet durch eine Nutzungseinrichtung (81), die an den Eingangsanschluß des Verstärkers angeschlossen ist.

4. Oszillatorschaltung nach einem der Ansprüche 1, 2 oder 3, bei der die Einrichtung zum Anlegen einer Vorspannung aufweist:
einen ersten MOS-Transistor (72),
eine Stromquelle (71), die an einen Hoch-Strom führenden Anschluß des ersten MOS-Transistors angeschlossen ist, um einen Konstantstrom durch den Source-Drain-Pfad des ersten MOS-Transistors zu treiben,
ein Widerstandselement (60) zum Verbinden des gemeinsamen Knotens mit dem Gateanschluß (74) des ersten MOS-Transistors, und
ein Widerstandselement (61) zum Verbinden des gemeinsamen Knotens mit dem Hoch-Strom führenden Anschluß des ersten MOS-Transistors.

5. Oszillatorschaltung nach Anspruch 4, gekennzeichnet durch einen ersten und zweiten Widerstand (62,63) sowie durch einen zweiten MOS-Transistors, die zueinander in Reihe geschaltet sind, wobei der Knoten (65) zwischen dem ersten und zweiten Widerstand an den Gateanschluß des ersten MOS-Transistors angeschlossen ist.

6. Oszillatorschaltung nach einem der Ansprüche 1 bis 5, bei der die Kapazitäten des ersten, zweiten, dritten und vierten Varaktors für jede angelegte Betriebsspannung zueinander gleich sind.

Revendications

1. Un circuit oscillateur commandé par tension comprenant un élément oscillateur à cristal (11) ayant des première et seconde bornes (12, 13), un amplificateur (20° ayant une borne d'entrée (22) connectée à la première borne (12) et une borne de sortie (23) connectée à la seconde borne (13), une première diode à capacité variable (30) dont l'une des bornes est connectée directement à la borne d'entrée de l'amplificateur et dont l'autre borne est connectée à un noeud commun (35), une seconde diode à capacité variable (40) dont l'une des bornes est connectée directement à la borne de sortie de l'amplificateur et dont l'autre borne est connectée directement au noeud commun, des moyens (70, 60) pour appliquer une tension de commande (V_A) au noeud commun, dans le but de déplacer la fréquence d'oscillation de l'élément oscillateur (11), et CARACTERISE PAR une troisième diode à capacité variable (31) dont l'une des bornes est connectée à la borne d'entrée de l'amplificateur et dont l'autre borne est connectée à un autre noeud commun (36), une quatrième diode à capacité variable (41) dont l'une des bornes est connectée à la borne de sortie de l'amplificateur et dont l'autre borne est connectée à l'autre noeud commun, et des moyens (72, 61) pour appliquer une tension de polarisation V_B, différente de la tension de commande (V_A) à l'autre noeud commun.

2. Un circuit selon la revendication 1, comprenant des moyens d'utilisation (82) connectés à la borne de sortie de l'amplificateur.

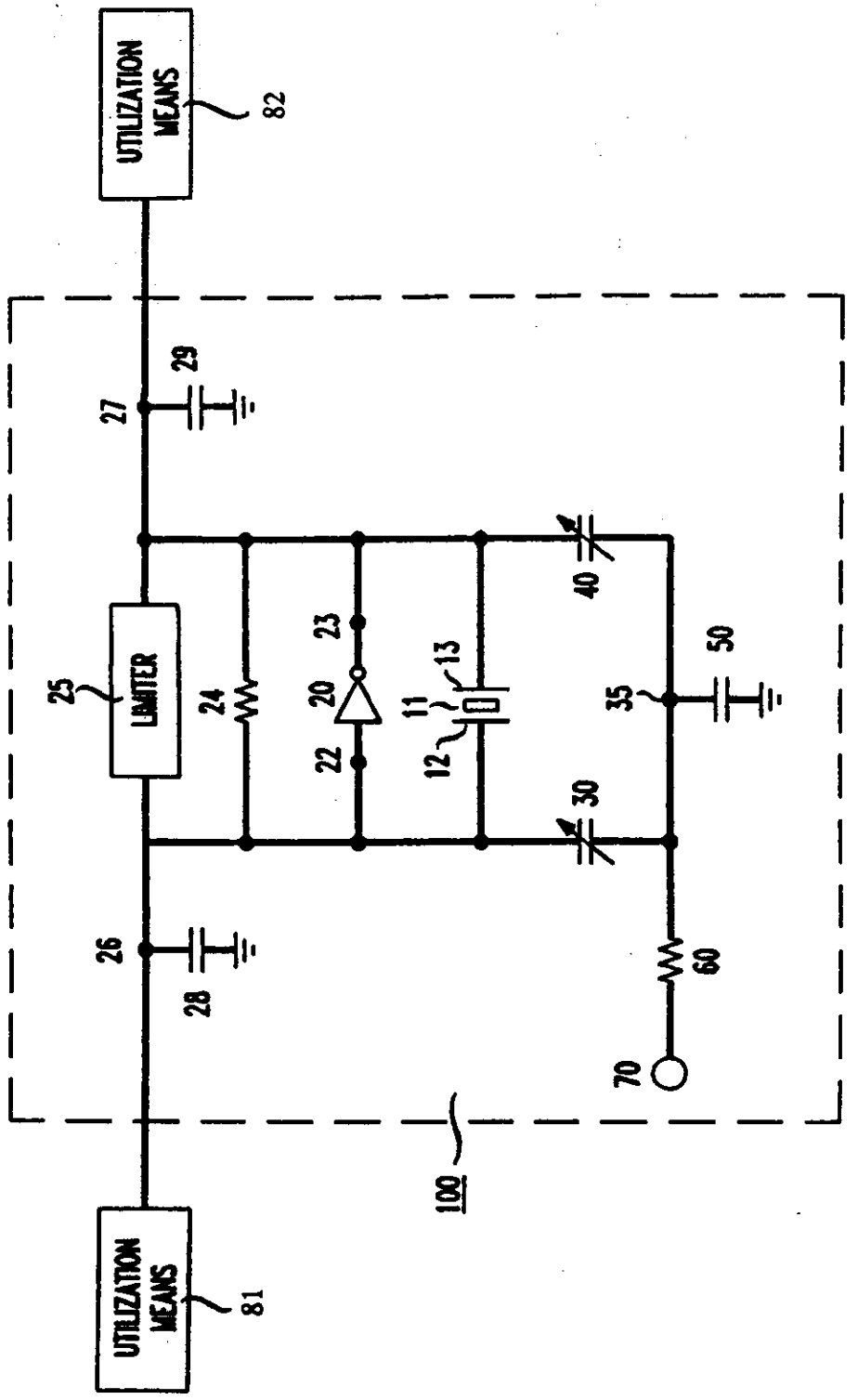
3. Un circuit selon la revendication 1 ou 2, comprenant des moyens d'utilisation (81) connectés à la borne d'entrée de l'amplificateur.

4. Un circuit selon la revendication 1, 2 ou 3, dans lequel les moyens destinés à appliquer une tension de polarisation comprennent un premier transistor MOS (72), une source de courant (71) connectée à une borne du premier transistor MOS qui achemine un courant élevé, pour faire circuler un courant constant dans le chemin source-drain du premier transistor MOS, des moyens résistifs (60) pour connecter le noeud commun à la borne de grille (74) du premier transistor MOS, et des moyens résistifs (61) pour connecter l'autre noeud commun à la borne du premier transistor MOS qui achemine un courant élevé.

5. Un circuit selon la revendication 4, comprenant des première et seconde résistances (62, 63) et un second transistor MOS (64) connectés mutuellement en série, le noeud (65) entre les première et seconde résistances étant connecté à la borne de grille du premier transistor MOS.

6. Un circuit selon l'une quelconque des revendications précédentes, dans lequel les capacités des première, seconde, troisième et quatrième diodes à capacité variable sont égales pour n'importe quelle tension de fonctionnement appliquée.

FIG. 1


UTILIZATION MEANS
82
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29
25
LIMITER
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23
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22
11
12
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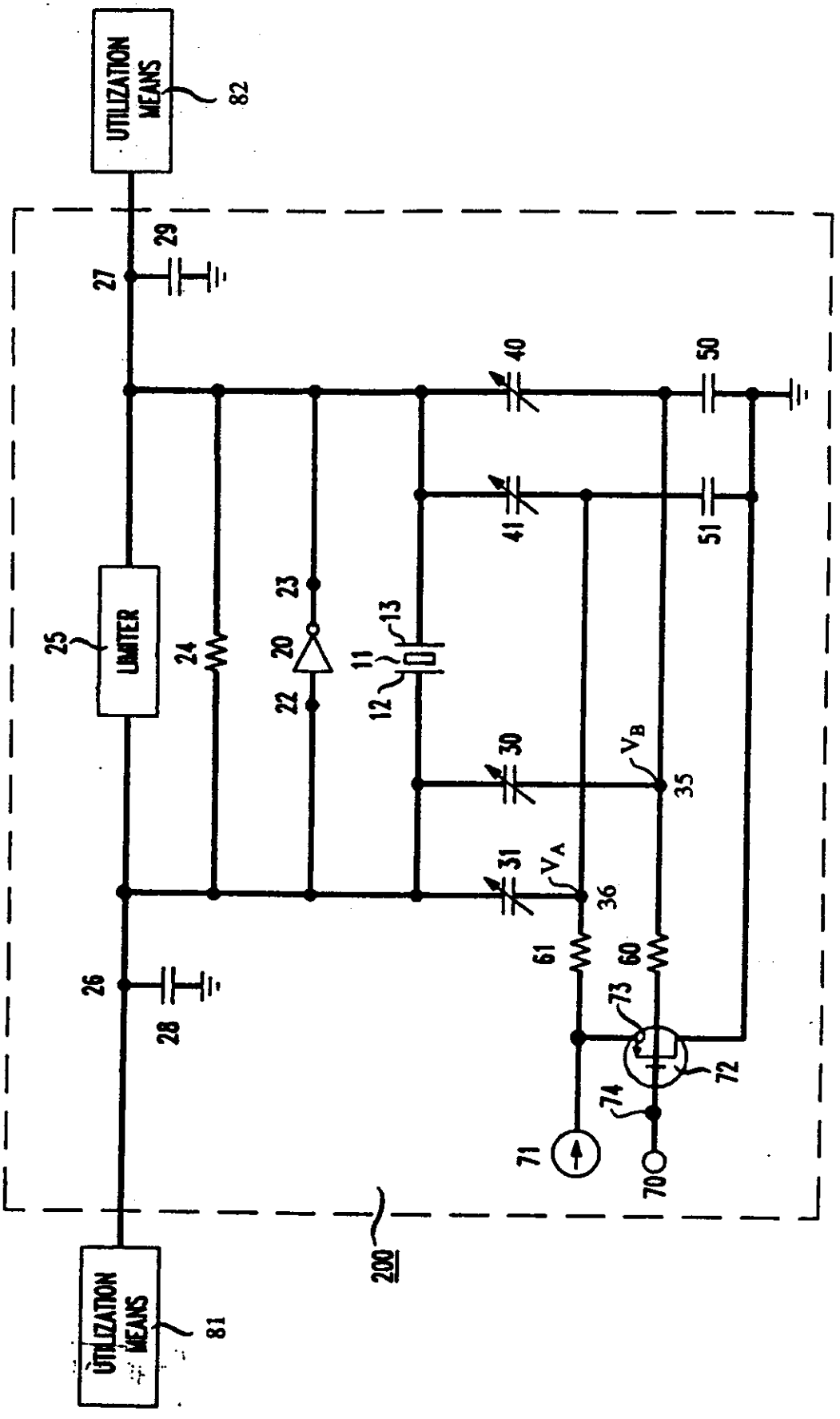
40
35
50
30
26
28
60
70
100
UTILIZATION MEANS
81

FIG. 2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82
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LIMITER
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V_B
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V_A
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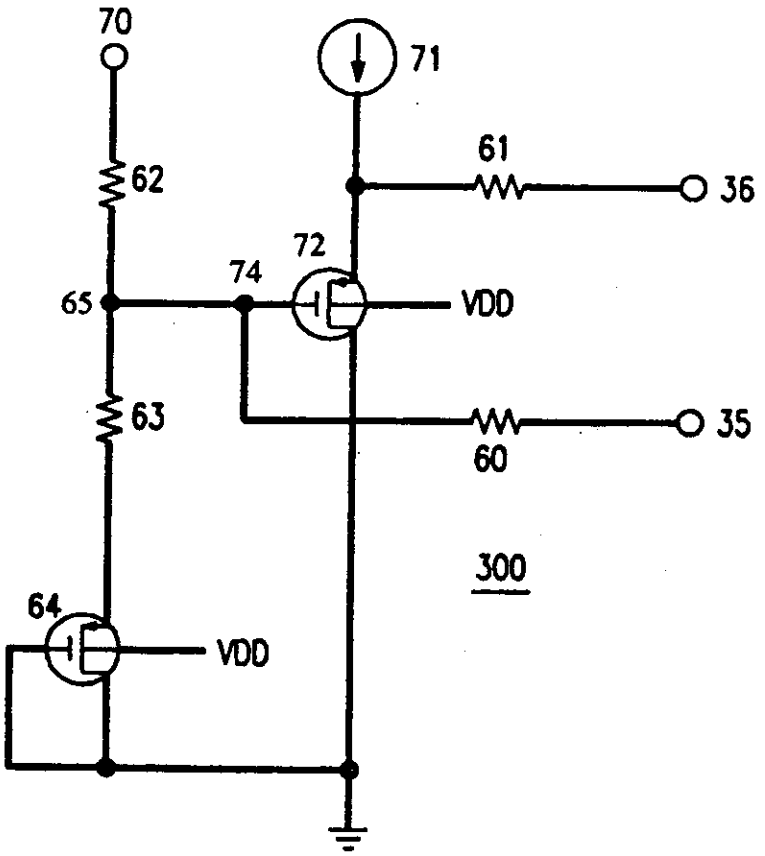
61
60
73
72
74
71
70
26
28
200
UTILIZATION MEANS
81

FIG. 3



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Title VOLTAGE CONTROLLED BALANCED CRYSTAL OSCILLATOR CIRCUIT.

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STATUS	PATENT IN FORCE