

April 6, 1954

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2,674,733

ELECTRONIC SORTING SYSTEM

Filed Dec. 2, 1952

2 Sheets-Sheet 1

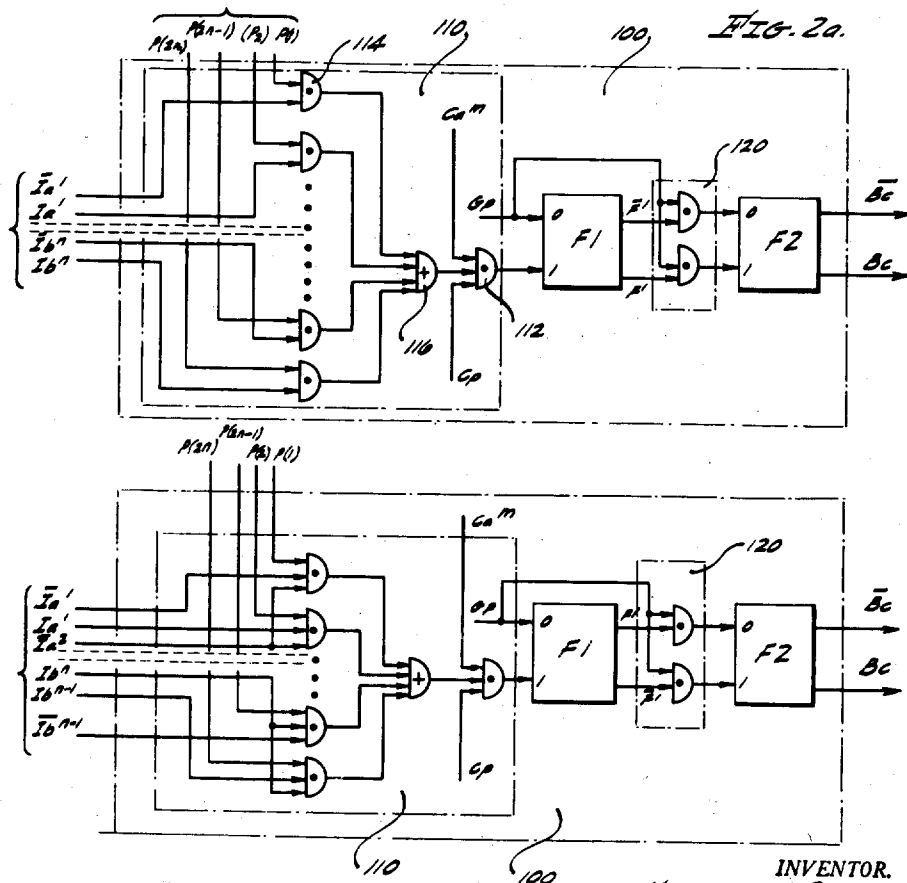
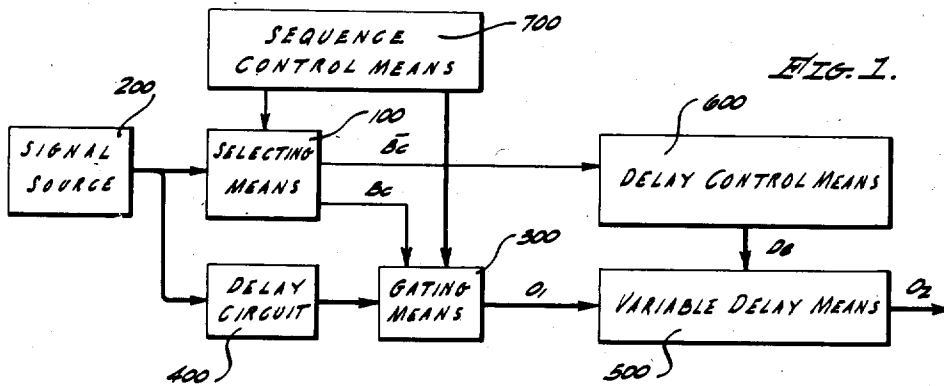


FIG. 2b.

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2 Sheets-Sheet 2

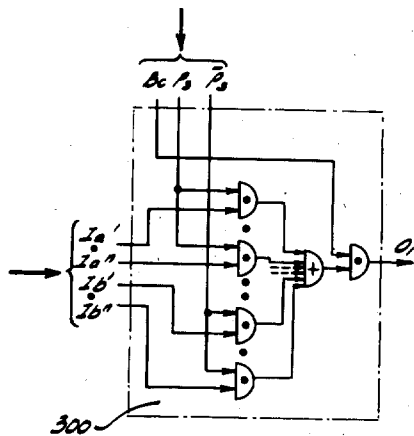


FIG. 3.

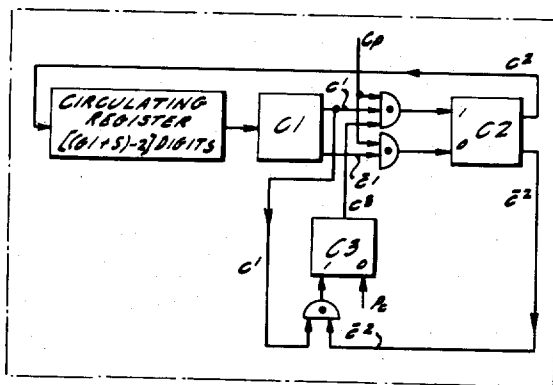


FIG. 4.

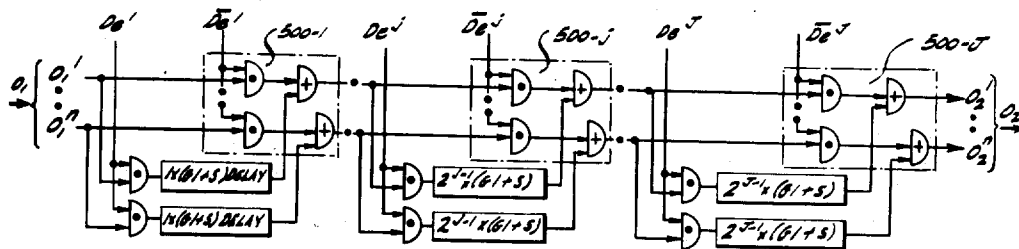


FIG. 5.

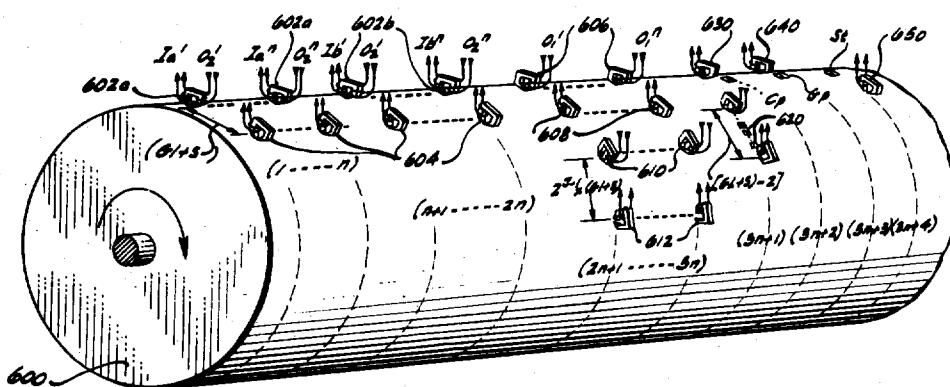


FIG. 6.

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UNITED STATES PATENT OFFICE

2,674,733

ELECTRONIC SORTING SYSTEM

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Application December 2, 1952, Serial No. 323,624

13 Claims. (Cl. 340—347)

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This invention relates to electronic sorting systems, and more particularly to high-speed electronic sorting systems for re-recording randomly-recorded information groups in a predetermined, evenly-spaced sequence.

Although numerous types of sorting systems are known in the art, these systems may be divided into two general classes according to the type of sorting program utilized. In systems of one class, hereinafter referred to as parallel sorting systems, each successive information group is selectively routed to one of a plurality of positions, according to a predetermined sorting function. The punched card sorting system, for example, is a parallel sorting system wherein the selected positions are "bins"; the cards being entered therein according to certain punched identification codes.

Another example of a parallel sorting system is one wherein randomly-recorded magnetic information on an input tape is selectively transferred to one of ten tapes according to a decimal identification character included in each information group. Other examples of parallel sorting systems are described in an article entitled "Sorting and collating," by John W. Mauchly, in vol. III of Theory and Techniques for Design of Electronic Digital Computers, Moore School of Electrical Engineering, University of Pennsylvania, June 30, 1948, on pages 22-25.

Sorting systems of the other class are herein referred to as serial sorting systems, and are distinguished from the parallel systems in that only certain ones of successively appearing information groups are selected; the sorting being performed by passing the information groups through the sorting system a number of times until all of the information groups are arranged into the desired sequence. Thus, in a serial sorting system for transferring randomly-recorded magnetic information from an input tape onto an output tape, in sequence according to decimal identification characters, the input tape must be passed through the system several times before the information groups are all recorded on the output tape according to one decimal digit.

In general, prior art parallel sorting systems have been preferred over serial sorting systems since the former systems readily lend themselves to high-speed operation and present no problem in obtaining a final, evenly-spaced record according to a predetermined sequence.

The high-speed operation of the parallel system is primarily due to the fact that the information to be sorted need only be scanned or passed as many times as there are code characters in the

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identification code number of each information group. For example, information concerning corporate employees, having five-decimal-digit payroll numbers, may be sorted in five passes. Thus, punched cards are passed through the sorting system into the ten "bins" only five times in order to get all cards in order according to a five-decimal-digit number; the final sequence being obtained by integrating the information in the "bins" into serial order.

In the serial sorting systems, a number of sub-sequences are required to arrange the information groups into final sequences according to a code character. Thus, while the parallel system requires only one pass to arrange employee information into "bins" according to one decimal digit, the serial sorting system requires several passes depending upon the particular code utilized. If each decimal digit of the code number is binary coded, at least seven passes are required before a first sequence is formed wherein information groups are arranged in serial order according to the least significant decimal digit. Thus, at least seven times as many passes are required to completely sort information groups containing binary-coded decimal code identification characters in serial fashion as are required to sort the same information in the parallel manner.

Another disadvantage of serial sorting systems is that where tape-recorded information is utilized, it is difficult to integrate the sorted information into an evenly-spaced record which may be recorded on an output tape. As each sequence is formed, the selected information groups appear in a randomly-spaced sequence since only certain groups are read from the input tape according to the sorting program. Consequently, if several sub-sequences are required to form a sequence, a considerable amount of tape is required to allow for the spaces between the selected groups.

Serial sorting systems, however, have a decided advantage over parallel systems with respect to system complexity. In the serial systems, the same structure may be utilized to perform successive steps of the sorting process, whereas in the parallel system, the structure must be duplicated according to the number of positions required. Thus, in the simple case of card sorting, ten "bins" are required to sort decimal information in parallel whereas only one "bin" would be required to sort the same information serially.

Since prior art systems have not been able to overcome the principal disadvantages of the serial sorting systems discussed above, they have not realized the advantage of simplicity. The present

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invention, however, discloses a novel, serial sorting system which obviates the above and other disadvantages of the prior serial sorting systems, may be operated at high speed, and does not require additional tape storage capacity.

According to the basic concept of the present invention, randomly-recorded input information is passed through a selecting device which produces a randomly-spaced sequence corresponding to the selected information groups. The randomly-spaced sequence is then converted to corresponding evenly-spaced sequence by means of a novel variable delay circuit. The variable delay circuit responds to sets of output signals corresponding to the selected, randomly-spaced information groups and produces corresponding evenly-spaced sets of output signals. This is done under the control of a delay control circuit which responds to signals produced by the selecting device, indicating spaces in the selected information, and varies the delay of the delay circuit according to a predetermined function.

Since the variable delay circuit has a multitude of applications, only a brief description thereof is included in the present application, reference for further details being made to co-pending U. S. patent application entitled "Variable Delay Means," by Howard M. Robbins, Serial No. 323,623, filed December 2, 1952.

The high-speed embodiments of the present invention are provided by using a magnetic drum to perform the function of passing the randomly-recorded information under reading heads. Since the magnetic drum may be operated at speeds ranging from ten to twenty times the maximum operating speed permissible with magnetic tape, it is possible to perform serial sorting operations as fast, if not faster, than corresponding parallel sorting operations on magnetic tape.

Accordingly, it is an object of the present invention to provide a serial sorting system requiring a minimum of storage capacity.

Another object of the present invention is to provide a high-speed serial sorter.

A further object of the present invention is to provide a simple, high-speed serial sorter system requiring a minimum of storage capacity.

Yet a further object of the present invention is to provide a high-speed magnetic drum sorting system.

Still another object of the present invention is to provide a novel system for selectively sorting randomly-recorded information groups and recording said groups into a predetermined, evenly-spaced sequence.

The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages thereof, will be better understood from the following description considered in connection with the accompanying drawings, in which several embodiments of the invention are illustrated by way of examples. It is to be expressly understood, however, that the drawings are for the purpose of illustration and description only, and are not intended as a definition of the limits of the invention.

Fig. 1 is a block diagram of an embodiment of the present invention;

Figs. 2a and 2b are schematic diagrams of suitable forms of the selecting means shown in Fig. 1;

Fig. 3 is a schematic diagram of one form of the gating means shown in Fig. 1;

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Fig. 4 is a schematic diagram of one of the circuits forming the sequence control means shown in Fig. 1;

Fig. 5 is a schematic diagram of one form of the variable delay means shown in Fig. 1; and

Fig. 6 shows a magnetic drum and associated circuits utilized in high-speed sorting systems according to the present invention.

Referring now to Fig. 1, there is shown one embodiment of a serial sorting system according to the present invention in which serially-applied, randomly-recorded information groups are sorted and recorded in a predetermined, evenly-spaced sequence. As shown in Fig. 1, the sorting system comprises: selecting means 100, responsive to information signal groups produced by a signal source 200, for producing complementary electrical binary control signals B_c and $\bar{B}_c$ corresponding to each information signal group to control its selection or nonselection; gating means 300, responsive to signals B_c and to the information groups applied after a fixed delay for producing randomly-spaced sets of output signals O_1 , corresponding to the selected signal groups; a delay circuit 400 providing the fixed delay; and variable delay means 500 responsive to randomly-spaced signal sets O_1 for producing evenly-spaced signal sets O_2 .

The delay of signal groups O_1 through variable delay means 500 is controlled by signals D_c produced by delay control means 600 in response to signals $\bar{B}_c$; and the operation of selecting means 100 and gating means 300 is controlled by signals produced by sequence control means 700.

The structure of selecting means 100, gating means 300, variable delay means 500, and delay control means 600 is determined by the particular code which is utilized to identify the information groups, as well as the sorting program which is adopted. Therefore, before proceeding to consider the details of these structures, it is necessary to consider various codes and sorting programs.

As an illustrative problem, consider the sorting of randomly-recorded information groups containing binary-coded decimal identification numbers, where it is desired to arrange the groups into a sequence wherein the identification code numbers of all groups are in serial number order. It is assumed that the least significant binary-coded decimal digits of the respective identification numbers appear in the following random sequence:

Sequence Position	Least Significant Decimal Digit
1.....	0101 (5)
2.....	0901 (1)
3.....	0011 (3)
4.....	0100 (4)
5.....	0010 (2)
6.....	0110 (6)
7.....	1001 (9)
8.....	1000 (8)
9.....	0111 (7)
10.....	0000 (0)

According to one sorting program, a first subsequence is formed by first reading and recording information groups having serial numbers containing a 0 in the least significant binary place of the least significant binary-coded decimal digit, and then reading and recording information groups having a 1 in the corresponding least significant binary place. Thus, the least signi-

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ficant decimal digits appear in the following order in the first sub-sequence:

1st sub-sequence

0100	(4)
0010	(2)
0110	(6)
1000	(8)
0000	(0)

First pass—all first binary digits are 0's

0101	(5)
0001	(1)
0011	(3)
1001	(9)
0111	(7)

Second pass—all first binary digits are 1's

The first sub-sequence is then read and re-recorded as a second sub-sequence after third and fourth passes by recording information groups having 0's and 1's, respectively, in the second binary place of the least significant binary-coded decimal digit. The decimal digits in the second sub-sequence then appear in the following order:

2nd sub-sequence

0100	(4)
1000	(8)
0000	(0)
0101	(5)
0001	(1)
1001	(9)

Third pass—all second binary digits are 0's

0010	(2)
0110	(6)
0011	(3)
0111	(7)

Fourth pass—all second binary digits are 1's

Sorting according to the first decimal digit is then completed by forming third and fourth sub-sequences according to the third and fourth binary digits, respectively. During the first pass of each of these sub-sequences, information groups containing 0's in the corresponding binary place are recorded, and during the second pass of each of these sub-sequences, those information groups having a 1 in the corresponding binary place are recorded. The third and fourth sub-sequences then appear as:

3rd sub-sequence

1000	(8)
0000	(0)
0001	(1)
1001	(9)
0010	(2)
0011	(3)

Fifth pass—all third binary digits are 0's

0100	(4)
0101	(5)
0110	(6)
0111	(7)

Sixth pass—all third binary digits are 1's

4th sub-sequence

0000	(0)
0001	(1)
0010	(2)
0011	(3)
0100	(4)
0101	(5)
0110	(6)
0111	(7)

Seventh pass—all fourth binary digits are 0's

1000	(8)
1001	(9)

Eighth pass—all fourth binary digits are 1's

It will be noted that eight passes are required to complete the above sorting program. It is possible, however, to perform the same sorting problem in only seven passes and two sub-sequences, if the sub-sequences are formed as a function of two binary digits at a time. In this case, four passes are required to form the first sub-sequence, and three passes are required to form the second sub-sequence. The first, second, third, and fourth passes of the first sub-sequence are utilized, respectively, to record decimal digits having 00, 01, 10, and 11 in the first two binary places. Similarly, decimal digits having 00, 01, and 10 in the third and fourth binary places are recorded during the first, second, and third passes of the second sub-sequence, respectively. It will be noted that after the seventh pass, the digits

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are in serial number order. The sub-sequences according to the seven-pass sorting program appear as follows:

5	1st sub-sequence	First pass (00)	2nd sub-sequence	
	0100 (4)		0000 (0)	
	1000 (8)		0001 (1)	
	0000 (0)		0010 (2)	Fifth pass (00)
			0011 (3)	
10	0101 (5)	Second pass (01)	0100 (4)	
	0001 (1)		0101 (5)	
	1001 (9)		0110 (6)	Sixth pass (01)
			0111 (7)	
	0010 (2)	Third pass (10)		
	0110 (6)		1000 (8)	Seventh pass (10)
			1001 (9)	
	0011 (3)	Fourth pass (11)		
	0111 (7)			

In the above analysis, sorting according to one binary-coded decimal digit has been considered. It should be apparent, however, that the process must be repeated for each of the binary-coded decimal digits in a multidigit identification code number. Where binary-coded information is sorted by considering one binary digit at a time, then the number of passes required is equal to $2.n.N$, where n represents the number of binary digits in each character and N represents the number of characters in the identification code. Where the sorting is performed by considering two binary digits during each pass, the total number of passes required is less than $2.n.N$ by a factor which depends upon the code which is utilized. It has been shown that only seven passes are required for sorting the binary-coded decimal digits, as above, and thus the total number of passes required for N digits is $7.N$. Similarly, it can be shown that alphabetical information containing binary-coded letters may be sorted in $9.N$ passes, although each letter is represented by six binary digits.

Binary-coded decimal numbers may be sorted by considering three or four binary digits at a time. However, this sorting program would require ten passes for each decimal digit or a total of $10.N$ passes. The advantage, however, of sorting by all four binary digits is that only one sub-sequence is required, and, therefore, it is not necessary to transfer from one record to another as frequently as would otherwise be necessary. The reason for this is explained more fully below.

While embodiments of the present invention may be utilized to sort information groups identified by other code characters, such as characters in the IBM Hollerith code, binary codes are preferred where it is desired to minimize the storage capacity and the number of passes required.

The discussion which follows concerns sorting structures specifically designed for systems wherein the identification characters are binary coded. It should be understood, however, that the present invention is not so limited and that the principles hereinafter set forth are applicable to a wide variety of codes.

Programs for sorting binary-coded information may be expressed as Boolean algebraic functions, where binary variables are utilized to express the particular pass, the particular identification character, and the particular binary digit which is to be analyzed. Hereinafter, each pass is designated by a binary variable $P(j)$, where j indicates the number of the pass. The variable $P(j)$ has a value of 1 when the particular pass is to be performed; otherwise its value is 0. Similarly, the binary digits in the identification code characters are represented by variables Bd^k , where k indicates the binary place. Thus, Bd^1 represents a first binary digit in a code char-

acter, k being equal to 1. Finally, the particular character which is to be analyzed is represented by Ca^m , where m represents the position of the character in the identification code number; Ca^1 , for example, representing the first character in the identification code number, where m is equal to 1. Corresponding to each of the binary digit variables Bd^k , there is a complementary variable $\bar{Bd}^k$ having values of 1 and 0, respectively, when Bd^k equals 0 and 1, respectively.

With these variables, then it is possible to define a binary control signal Bc and a complementary binary control signal $\bar{Bc}$ having values of 1 and 0 when a particular group is to be selected or recorded into a sub-sequence, and having values of 0 to 1 when a group is not to be selected.

It will be recalled that in sorting by one binary digit at a time, information groups are recorded in a first sub-sequence by recording groups including a 0 first binary digit, during the first pass, and then recording groups including a 1 first binary digit, during the second pass. Thus, the binary control signal Bc has a value of 1 for all identification code characters if the first binary digit is 0 on the first pass or if the first binary digit is 1 on the second pass. Algebraically, this is expressed as follows:

$$Bc = Ca^m \cdot [P(1) \cdot \bar{Bd}^1 + P(2) \cdot Bd^1]$$

where the dot (.) expresses the logical "and" and the plus sign (+) the logical "or." This expression is interpreted as follows. The variable Bc has a value of 1, indicating that an information group is to be recorded into a sub-sequence, whenever the m th identification character is being read, as indicated by variable Ca^m being equal to 1; and either $P(1)$ and $\bar{Bd}^1$ are equal to 1 or $P(2)$ and Bd^1 are equal to 1, indicating a 0 in the first binary digit on the first pass, or a 1 in the first binary digit on the second pass, respectively. This analysis is then completed for all passes and binary digits, the complete function for Bc then becoming:

$$Bc = Ca^m \cdot [P(1) \cdot \bar{Bd}^1 + P(2) \cdot Bd^1 + P(3) \cdot \bar{Bd}^2 + P(4) \cdot Bd^2 + P(5) \cdot \bar{Bd}^3 + P(6) \cdot Bd^3 + \dots P(2n-1) \cdot \bar{Bd}^n + P(2n) \cdot Bd^n]$$

Where the sorting is performed by considering two binary digits at a time, binary control signal Bc has a value of 1 for any identification code character if the first and second binary digits represent the values 00, 01, 10, and 11 on the first, second, third, and fourth passes, respectively. Similarly, binary control signal Bc has a value of 1 on the fifth, sixth and seventh passes where the third and fourth binary digits represent 00, 01, and 10, respectively. In this sorting program the algebraic function for binary control signal Bc is:

$$Bc = Ca^m \cdot [P(1) \cdot \bar{Bd}^2 \cdot \bar{Bd}^1 + P(2) \cdot \bar{Bd}^2 \cdot Bd^1 + P(3) \cdot Bd^2 \cdot \bar{Bd}^1 + P(4) \cdot Bd^2 \cdot Bd^1 + P(5) \cdot \bar{Bd}^4 \cdot \bar{Bd}^3 + P(6) \cdot \bar{Bd}^4 \cdot Bd^3 + P(7) \cdot Bd^4 \cdot \bar{Bd}^3]$$

where it is assumed that each code character is a binary-coded decimal digit.

Where the sorting is performed by considering one binary digit at a time, a new sub-sequence is formed for every two passes. Thus, the second binary digit is read from a different record than the first. Where erasable magnetic recording is utilized, it is possible to alternate between first and second sets of recording channels so that

after each two passes, the signals are read from the same magnetic storage channels. If punched tape is utilized, however, it is apparent that a new tape is required for recording each sub-sequence. For the purpose of illustrating specific structure, it is assumed hereinafter that two sets of magnetic drum channels are used.

The input signals produced by the first and second sets of channels of the magnetic drum are hereinafter referred to as Ia^k and Ib^k , respectively; where k corresponds to the binary digit which is represented. Circuits for deriving complementary input signals Ia^k , $\bar{Ia}^k$ and Ib^k , $\bar{Ib}^k$ from drum signals Ia^k and Ib^k are well-known in the art. For example, the magnetic disk reading circuits shown in U. S. Patent No. 2,609,143, entitled "Electronic Computer for Addition and Subtraction," by G. R. Stibitz, issued September 2, 1952, are suitable for providing the complementary signals.

In considering the actual circuit mechanization then, signals Ia^k and $\bar{Ia}^k$ are substituted for the variables Bd^k and $\bar{Bd}^k$ whenever k is an odd number; and signals Ib^k and $\bar{Ib}^k$ are substituted for the variables Bd^k and $\bar{Bd}^k$ whenever k is an even number. Thus, the algebraic expression for binary control signal Bc for sorting according to one binary digit at a time becomes:

$$Bc = Ca^m \cdot [P(1) \cdot \bar{Ia}^1 + P(2) \cdot Ia^1 + P(3) \cdot \bar{Ib}^2 + P(4) \cdot Ib^2 \dots P(2n-1) \cdot \bar{Ib}^n + P(2n) \cdot Ib^n]$$

where it is assumed that n is an even number.

It will be recalled that when the two binary digits are considered at a time, the same variables Bd^k and $\bar{Bd}^k$ are considered for four passes in succession. Thus, it will be noted in the function for Bc , where two binary digits are considered at a time, that signals Ia^k and $\bar{Ia}^k$ are utilized for four successive passes and then signals Ib^k and $\bar{Ib}^k$ are utilized for four successive passes. The function Bc , considering two binary digits at a time, then is:

$$Bc = Ca^m \cdot [P(1) \cdot \bar{Ia}^2 \cdot \bar{Ia}^1 + P(2) \cdot \bar{Ia}^2 \cdot Ia^1 + P(3) \cdot Ia^2 \cdot \bar{Ia}^1 + P(4) \cdot Ia^2 \cdot Ia^1 + P(5) \cdot \bar{Ib}^4 \cdot \bar{Ib}^3 + P(6) \cdot \bar{Ib}^4 \cdot Ib^3 + P(7) \cdot Ib^4 \cdot \bar{Ib}^3]$$

where it is assumed that n equals 4 and that binary-coded decimal digits are to be sorted.

Before proceeding to consider the details of the mechanizations suitable for selecting means 100 (Fig. 1), it is important to consider the sequence of the sorting operation. Since the information which is to be sorted must be selected before passing through gating means 300, it is necessary that it be delayed so that signals Bc and $\bar{Bc}$, corresponding to the desired selection, are produced just before the corresponding information group is applied through delay circuit 400 to gating means 300. For the present, it is assumed that the delay provided by delay circuit 400 is equal to the length, in time, of an information group, although it will be shown that other delays may be suitable.

Since it has been assumed that delay circuit 400 provides a delay equal to the length of the information groups, each signal Bc must not become effective to actuate gating means 300 until the end of the corresponding group. This operation may be effected by first entering signal Bc , as produced, into a first flip-flop, and then shifting signal Bc into a second flip-flop at the end of the corresponding information group or at the beginning of the next group.

In mechanizing selecting means 100, then, first

and second flip-flops, $F1$ and $F2$, are utilized to provide the operation described above. Flip-flops $F1$ and $F2$ have 1 and 0 setting input circuits referred to, respectively, as $1F1$, $0F1$ and $1F2$, $0F2$ and produce complementary output signals $F1$, $\bar{F1}$ and $F2$, $\bar{F2}$, respectively. When signals are applied separately to the 1 and 0 circuits of a flip-flop, it is set, respectively, to stable states representative of binary 1 and 0; when signals are applied to both input circuits of a flip-flop, it is triggered or complemented.

In order to enter signals Bc into flip-flop $F1$, it is necessary to provide pulse entry signals which will set the flip-flop to the desired stable states. This may be provided by recording a clock pulse signal, herein referred to as signal Cp , adjacent to each character position on the drum. Thus, when the m th code character Ca^m is being read and signal Bc is equal to 1, a clock pulse signal from the drum sets flip-flop $F1$ to 1. On the other hand, if Bc is equal to 0, the clock pulse Cp does not pass to the flip-flop and it will remain set to 0.

At the end of each group, then, signal Bc , stored in flip-flop $F1$, is shifted into flip-flop $F2$ by means of one of group pulse entry signals Gp , recorded on the magnetic drum, one at the end of each information group. Signal Gp is also utilized to set flip-flop $F1$ to 0 at the end of the group so that it is prepared for the entry of the next signal Bc , indicating the selection or non-selection of the next information group.

It will be noted, then, that flip-flop signals $F2$ and $\bar{F2}$ produced by flip-flop $F2$ correspond to signals Bc and $\bar{Bc}$ produced during the preceding information group.

The input circuits for flip-flops $F1$ and $F2$ may be expressed as Boolean algebraic equations, as follows:

$$\begin{aligned} 1F1 &= Bc.Cp \\ 0F1 &= Gp \\ 1F2 &= F1.Gp \\ 0F2 &= \bar{F1}.Gp \end{aligned}$$

These functions are interpreted as follows. Flip-flop $F1$ is set to 1 whenever Bc is 1 and a clock pulse Cp is applied to input circuit $1F1$; and is set to 0 by signal Gp applied to input circuit $0F1$. Each time flip-flop $F1$ is set to 0 by signal Gp , signals $F1$ and $\bar{F1}$ produced by flip-flop $F1$ and corresponding, respectively, to Bc and $\bar{Bc}$, are shifted into flip-flop $F2$, signal $\bar{F1}$ being applied to input circuit $0F2$ and signal $F1$ being applied to input circuit $1F2$.

Two mechanizations of control means 100 are illustrated in Figs. 2a and 2b where the functions for Bc , considering one binary digit at a time and two binary digits at a time, are mechanized, respectively. Since the manner in which these circuits are mechanized should be apparent from one example, only the circuit shown in Fig. 2a is considered in detail.

Referring now to Fig. 2a, it will be noted that the control means therein illustrated comprises two flip-flops $F1$ and $F2$ and logical matrices 110 and 120 mechanized to provide input signals for flip-flops $F1$ and $F2$, respectively. The equations which are utilized to mechanize logical matrices 110 and 120, shown below, are given equation numbers (110) and (120), respectively.

$$(110) \begin{cases} 1F1 = Ca^m.[P(1).\bar{Ia}^1 + P(2).Ia^1 \dots \\ 0F1 = Gp \quad P(2n-1).\bar{Ib}^n + P(2n).Ib^n].Cp \end{cases}$$

$$(120) \begin{cases} 1F2 = F1.Gp \\ 0F2 = \bar{F1}.Gp \end{cases}$$

In mechanizing a logical matrix, according to a mechanization function, each "and" function is provided by an "and" circuit which produces an output signal having a level representing binary 1 only when all applied input signals have a level representing binary 1, and each "or" function, indicated by a plus sign (+), is provided by an "or" circuit which produces an output signal having a level representing binary 1 when any one, or more, of the applied input signals have a level representing binary 1. Thus, the "and" function $Ca^m.[P(1).\bar{Ia}^1 \dots P(2n).Ib^n].Cp$ is provided by "and" circuit 112 having signals $Ca^m.[P(1).\bar{Ia}^1 \dots P(2n).Ib^n]$, and Cp applied to separate input terminals; "and" function $P(1).\bar{Ia}^1$ is provided by "and" circuit 114 having signals $P(1)$ and $\bar{Ia}^1$ applied to separate input terminals; and "or" function

$$[P(1).\bar{Ia}^1 + \dots + \dots + \dots P(2n).Ib^n]$$

is provided by an "or" circuit 116 having signals $P(1).\bar{Ia}^1, \dots$ and $P(2n).Ib^n$ applied to separate input terminals.

In a similar manner, selecting means 100, illustrated in Fig. 2b, is mechanized from the Boolean algebraic functions:

$$(110) \begin{cases} 1F1 = Ca^m.[P(1).\bar{Ia}^2.\bar{Ia}^1 + P(2).\bar{Ia}^2.Ia^1 \dots \\ P(2n-1).Ib^n.\bar{Ib}^{n-1} + P(2n).Ib^n.Ib^{n-1}].Cp \\ 0F1 = Gp \end{cases}$$

$$(120) \begin{cases} 1F2 = F1.Gp \\ 0F2 = \bar{F1}.Gp \end{cases}$$

Circuits which may be utilized to provide the algebraic logic described above are well-known in the art. For example, suitable types of such circuits are shown on pages 37 to 45 of High-Speed Computing Devices by Engineering Research Associates, published in 1950 by McGraw-Hill Company, Inc., New York and London, and in an article entitled "Diode coincidence and mixing circuits in digital computers," by Tung Chang Chen, in vol. 38 of the Proceedings of the Institute of Radio Engineers, May 1950, on pages 511 through 514.

In one form delay means 400 may comprise two sets of magnetic reading heads spaced apart on the magnetic drum a distance equal to the length of one information group, plus any space between groups. Selecting means 100 is then made responsive to signals produced by one of the sets of reading heads and gating means 300 is made responsive to signals produced by the other set, such that signals corresponding to an information group are applied first to selecting means 100 and then, after a one group-time-plus-space delay, to gating means 300.

Other types of delay devices, however, may be utilized. For example, suitable delay devices are shown in an article entitled "Mercury delay line memory using pulse rate of several megacycles," by I. L. Auerback, in vol. 37 of Institute of Radio Engineers Proceedings, August 1949, on pages 855-861; or in U. S. patent application, Serial No. 300,286, entitled "Passive Element Signal Stepping Device," by Daniel L. Curtis, filed July 22, 1952.

In sorting according to one binary digit at a time it will be noted that selecting means 100 responds to signals Ia^k during passes $P(1), P(2),$

... $P(2n-3)$, and $P(2n-2)$; and responds to signals Ib^k during passes $P(3), P(4), \dots, P(2n-1)$, and $P(2n)$. It is convenient, therefore, to introduce the variables P_s and $\bar{P}_s$ having values representing binary 1 during the reading of signals Ia^k and Ib^k , respectively. Thus variable $P_s = P(1) + P(2) + \dots + P(2n-3) + P(2n-2)$ and variables $\bar{P}_s = P(3) + P(4) + \dots + P(2n-1) + P(2n)$. Variables P_s and $\bar{P}_s$ are complements because there are $2n$ pass-indicating variables, and the indication that one of a set of n passes is being performed must mean none of the other set of n passes is being performed. The manner in which corresponding signals P_s and $\bar{P}_s$ are produced by sequence-controlling means 700 is explained in detail below.

It will be recalled that gating means 300 produces sets of signal O_i corresponding to the selected sets of input signals. It should be apparent, then, that when signal Bc is equal to 1, signals O_i correspond to signals Ia^k , if P_s equals 1, and correspond to signals Ib^k , if $\bar{P}_s$ equals 1. Thus, the mechanization of gating means 300 may be defined by the Boolean algebraic expression

$$(300) O_i = Bc.(P_s.Ia^k + \bar{P}_s.Ib^k)$$

where it will be noted that whenever Bc equals 0, gating means 300 produces no output signals, indicating that the particular group has not been selected, and resulting in a space between selected groups of signals.

In a similar analysis, it can be shown that for sorting according to two binary digits at a time, variables P_s and $\bar{P}_s$ may be defined as follows:

$$P_s = P(1) + P(2) + P(3) + P(4) + \dots + P(9) + P(10) + P(11) + P(12) + \dots$$

$$\bar{P}_s = P(5) + P(6) + P(7) + P(8) + \dots + P(13) + P(14) + P(15) + P(16) + \dots$$

where the total number of passes is limited to $2n$.

It can be seen, therefore, that gating means 300 not only functions to produce signals corresponding to selected information groups, but also responds to signals P_s and $\bar{P}_s$ and selects between the first and second sets of drum channels according to the function inherent in signals P_s and $\bar{P}_s$.

A mechanization suitable for gating means 300 is shown in Fig. 3. The manner in which the functions are mechanized should be apparent from the examples already given.

When a magnetic drum is used in the sorting system, each pass is equivalent to one drum revolution. It is possible, then, to count the number of passes by counting the drum revolutions. The pass, indicating signals $P(1), P(2), \dots, P(2n)$, may then be produced by a counter which is pulsed once for each drum revolution, the pulse being provided by a signal which is recorded on the drum, such as signal G_p .

The counter which is utilized must complete one counting cycle for each sorting sequence. Thus, where 12 passes are required to form each sequence, a 12-stable-state counter is utilized. While any of the conventional counters may be utilized, it is convenient to use a binary counter having as many stages as are necessary to provide the desired number of stable states. Where the binary counter produces more stable states than required, it may be converted into the desired counter by means of feed-back connections well-

known in the art. The basic technique, for example, of converting 64-stable-state binary counters into a 60-stable-state counter by means of feed-back connections, is shown and described in U. S. Patent No. 2,410,156, entitled "Electronic Timing Device," by L. E. Flory, issued October 29, 1946.

When a binary counter is utilized, signals P_s and $\bar{P}_s$ for sorting according to one binary digit, may be derived from the second stage of the counter, since this stage produces signals which are on and off alternately, every two counts. Similarly, signals P_s and $\bar{P}_s$ for sorting according to two binary digits at a time, may be derived from the third stage of the binary counter, since this stage produces signals which are alternately on and off every fourth count.

In addition, to producing pass-indicating signals, sequence control means 700 produces signals Ca^m corresponding to the particular character which is to be utilized. A circuit suitable for producing signals Ca^m is shown in Fig. 4. In the circuits shown in Fig. 4 signal Ca^m is produced as a function of two signals C^1 and $\bar{C}^2$ produced by flip-flops $C1$ and $C2$, respectively. This function is: $Ca^m = C^1.\bar{C}^2$. Flip-flops $C1$ and $C2$ are connected in series in a circulating or shifting register having a circulation length equal to the length of the information groups to be sorted plus any space between groups. Thus, if each information group is 80 digits in length and is spaced by one digit from the next group, the circulating register must have an 81 digit capacity.

Where a magnetic drum is utilized, a circulating register may be provided by writing the signals to be circulated on the drum at one point, reading the signals which were written at a second point, and then re-recording these signals at the first point. The reading and writing heads, then, are separated on the drum by a length equal to the circulating-register length desired, less a space corresponding to the two digits provided by flip-flops $C1$ and $C2$.

Other types of circulating registers which are suitable are shown and described in an article entitled "Gate-type shifting register," by J. H. Knapton and L. D. Stevens, in vol. XXII of Electronics, December 1949, on pages 186-192, and in copending U. S. patent application entitled "Passive Element Signal Stepping Device," by Daniel L. Curtis, Ser. No. 300,286, filed July 22, 1952.

When the circulating register is not on the magnetic drum, it is necessary to synchronize its operation with the application of the information groups to selecting means 100, so that the circulating register completes one cycle during the application of each information group.

At the start of the sorting operation, the circulating register is preset with a 1 in each place corresponding to an identification character and a 0 in each of the other places. The 1's are positioned so that when the first code character Ca^1 is to be read during the formation of the first sequence, flip-flop $C1$ stores a 1 and flip-flop $C2$ a 0. Thus, during the forming of the first sequence, the function $C^1.\bar{C}^2$ becomes 1 whenever the first code character Ca^1 is being read.

After the first sequence is formed, the pass counter returns to its starting state, signalling that the next identification character is to be considered or that the second sequence is to be formed. It is necessary, then, that the function $C^1.\bar{C}^2$ become 1 when the second identification character is being read. This operation is pro-

vided by eliminating the first 1 which originally was present in the circulating register, so that signal C^1 does not become 1 until code character Ca^2 is being read. The 1 signals in the circulating register, then are eliminated, one at a time, in succession, at the end of each sequence.

In the circuit shown in Fig. 5 the 1 signals are eliminated under the control of signal C^3 produced by a flip-flop C3. Signal C^3 controls the shifting of signal C^1 , produced by flip-flop C1, into flip-flop C2, so that whenever signal C^3 is equal to 0, a 1 signal in flip-flop C1 cannot enter into flip-flop C2.

Flip-flop C3 is set to 0 at the end of each sequence by a pass counter carry pulse Pc , signalling the end of a counter cycle. Thus, at the end of each counter cycle or each sorting sequence signal C^3 becomes 0, preventing the entry of a 1 into flip-flop C2. In order to prevent the elimination of more than one "1" from the circulating register at a time flip-flop C3 is set again to 1 in response to the function $C^1.C^2$.

The Boolean algebraic expressions defining the input circuits for flip-flops C2 and C3 then are:

$$\begin{cases} 1C2 = C^1.C^3.Cp & 1C3 = C^1.C^2.Cp \\ 0C2 = \bar{C}^1.Cp & 0C3 = Pc \end{cases}$$

where signals Cp are utilized to shift signals C^1 into flip-flop C2, except when C^3 is equal to 0.

It will be noted that during the first pass of each sequence except the first, two code characters are considered since the function $C^1.C^2$ remains 1 during the time that the shift between flip-flops C1 and C2 is prevented by the condition: $C^3=0$. This causes no difficulty since it merely means that selecting means 100 makes two decisions, the latter of which determines the value of signal Bc .

In the above discussion it has been shown how selecting means 100 produces signals Bc and $\bar{Bc}$ corresponding to the desired sorting selection, how gating means 300 operates in response to signals Ia^k and Ib^k to produce corresponding sets of signals O_1 when signal Bc is equal to 1, and that no output signals are produced when $\bar{Bc}$ is equal to 1. It is now necessary to consider the manner in which variable delay means 500 responds to sets of signals O_1 and delay control signals De , produced by delay control means 600, to produce evenly-spaced sets of output signals O_2 .

It will be recalled that whenever an information group is rejected, signal $\bar{Bc}$ is equal to 1. Signal $\bar{Bc}$, then, may be utilized to indicate the spaces between the selected groups in signal sets O_1 , or to control the operation of delay control means 600. At the end of each information group, then, as indicated by signal Gp , a signal is applied to delay control means 600, if $\bar{Bc}$ is equal to 1.

The delay provided by variable delay means 500 must be decreased each time an information group is rejected. In its simplest form, then variable delay means 500 may comprise a plurality of equal delay sections, each section having a length represented by the function

$$F \times (Gl + S)$$

where F is an integer, which is considered in more detail below; Gl is the length of the information group; and S is the space between the groups. The total delay through delay means 500 must be equal to the total circumferential-

digit length of the magnetic drum, less the delay provided by delay circuit 400.

While the equal-delay-section type of delay is simple in concept, it is very complicated in structure, since it requires a great number of delay sections plus a great many gating circuits in order to bypass certain delay sections each time the delay is to be decreased. Consequently, it is preferred to use a variable delay circuit of the type claimed in the above-mentioned copending application to Robbins, Serial No. 323,623, one embodiment of which is shown in Fig. 5 of this specification.

In the variable delay circuit shown in Fig. 5, J delay sections are utilized such that

$$(2^j - 1) \times (Gl + S)$$

is equal to one group-length-plus-space less than the circumferential-digit length of the drum. If, for example, $(Gl + S)$ is equal to 81 digits, and the circumferential-digit length of the drum is 1296 digits, then J is equal to 4.

Each delay section of variable delay means 500 provides a delay equal to $2^{j-1} \times (Gl + S)$ digits, where j indicates the position of the delay section. Thus, the first delay section—where j equals 1—provides a delay of $1 \times (Gl + S)$; the second delay section provides a delay of $2 \times (Gl + S)$; and the third delay section provides a delay of $4 \times (Gl + S)$.

Each delay section is controlled by a delay signal De^j , where j again represents the position of a delay section. When De^j is equal to 1, signals are entered into the delay section. Complementary delay signals $\bar{De}^j$ produced by delay control means 600 are utilized to control the operation of bypass gating circuits 500- j , there being one bypass gating circuit for each delay section. Consequently, when a signal De^j is equal to 0 and $\bar{De}^j$ is equal to 1, the j th delay section is bypassed and signals passed directly through the j th bypass gating circuit 500- j .

Since each delay section is bypassed when the corresponding signal $\bar{De}^j$ is equal to 1 and is passed through when De^j is equal to 1, it is possible to define each of the delays which may be provided by delay means 500 as an "and" function of signals De^j and $\bar{De}^j$. Thus, a delay of $15 \times (Gl + S)$ is expressed as:

$$De^1.De^2.De^3.De^4$$

indicating that delay sections providing delays of 1, 2, 4, and $8 \times (Gl + S)$ are included; and a delay of $10 \times (Gl + S)$ is expressed as:

$$\bar{De}^1.De^2.\bar{De}^3.De^4$$

indicating that signals pass through delay sections providing delays of 2 and 8 times $(Gl + S)$ and bypass delay sections providing delays of 1 and 4 times $(Gl + S)$.

The delay sections of variable delay means 500 may be of the same type described above with regard to delay means 400. Where a magnetic drum is utilized to provide both delay means 400 and the delay sections of variable delay means 500, it may be convenient to utilize the drum as well to provide signal source 200, and the circulating register included in sequence control means 700. The manner in which reading, writing and reading-writing magnetic heads are arranged into a system wherein signal source 200, delay means 400, the delay sections of variable delay means 500, and the circulating register of sequence control means 700 are all provided by a magnetic drum, is shown in Fig. 6.

Referring now to Fig. 6, it will be noted that channels 1 through $2n$ of drum 600 are utilized for the reading of signals Ia^k and Ib^k and for the writing of signals Oz^k . Reading-writing heads 602a are utilized to read signals Ia^k and to write signals Oz^k , produced by the variable delay circuit 500 during the reading of signals Ib^k ; and reading-writing heads 602b are utilized to read signals Ib^k and to write signals Oz^k , during the reading of signals Ia^k . Reading heads 604 are utilized in delay means 400 and are spaced at a distance equal to $(Gl+S)$ digits from the corresponding reading-writing head 602. Thus, each reading head 604 produces output signals Ia^k or Ib^k , corresponding to signals Ia^k or Ib^k read by the reading-writing head 602, on the same channel, after a delay equal to $(Gl+S)$ digits.

The reading and writing heads in channels $(2n+1)$ through $3n$ of drum 600 are utilized in the delay sections of variable delay means 500. Writing heads 606 are utilized to record signals Oz^k and reading heads 608 to read corresponding signals Oz^k , after a delay of $(Gl+S)$ digits, thus providing a first delay section for variable delay means 500. Each writing head 606 is actuated only when signal De^j is equal to 1. Otherwise, as has been explained, signals are caused to bypass the delay section through a corresponding bypass gating circuit. For simplicity, the reading and writing heads for the 2nd through the $(J-1)$ st delay sections are omitted, and writing heads 610 and reading heads 612 shown in Fig. 6 are utilized in the J th delay section of variable means 500. Writing head 610 and reading head 612 are spaced by $2^{J-1} \times (Gl+S)$ digits, as has been explained above.

In specifying the delays which are provided by the magnetic drum, it is assumed that any delay required in reading signals from, or recording signals on the drum is compensated for by a physical positioning of the reading and writing heads. Thus, in providing the delay of

$$2^{J-1} \times (Gl+S)$$

discussed above, the writing head 610 and reading head 612 must be somewhat closer than

$$2^{J-1} \times (Gl+S)$$

digits, since a short time interval is required for reading and writing signals on the drum.

Channel $(3n+1)$ of drum 600 is utilized in the circulating register of sequence control means 700. N magnetic spots, 620, are recorded on channel $(3n+1)$, corresponding to N code characters to be read. Magnetic spots 620 are read by reading head 621 and are then recorded by writing head 622, so that a drum circulation path of $[(Gl+S)-2]$ digits is provided, where two digits are eliminated to provide for the registry of flip-flops C1 and C2, as explained above.

Channel $(3n+2)$ is utilized to provide signals Cp , one for each of the digits in the circumferential length of drum 600; channel $(3n+3)$ provides group-end indicating signals Gp ; and finally, channel $(3n+4)$ provides start signals St , the utilization of which is explained below. Signals Cp , Gp , and St are read by reading heads, 630, 640, and 650, respectively.

At the start of the sorting operation (which may be initiated in a manner described briefly below) signals Ia^k read by reading head 602a, are converted into corresponding complementary signals $Ia^k, \bar{Ia}^k$, as explained above, and are then applied to selecting means 100. At the same

time, that signals Ia^k and Ia^k are entered into selecting means 100, the first "1" signal on channel $(3n+1)$ is entered into flip-flop C1, so that: $Ca^1 = C^1, \bar{C}^2 = 1$. Selecting means 100 then produces a signal Bc corresponding to the desired selection, signal Bc being entered into flip-flop F1 by a clock pulse signal Cp .

At the end of the first group, signal Bc stored in flip-flop F1 is entered into flip-flop F2 by signal Gp on channel $(3n+3)$. As the second group of signals Ia^k are being read by reading heads 602a, reading heads 604 read the corresponding signals of the first group, the signals produced by reading heads 604 being then applied to gating means 300. If signal Bc produced by flip-flop F2, at this time, is 1, gating means 300 produces signals Oz^k corresponding to the selected signal Ia^k . If, however, signal Bc is equal to 0 and signal $\bar{Bc}$ is equal to 1, then, at the end of the first group, a signal Gp is applied to the counter in delay control means 600, changing its delay control representation from

$$De^1, De^2 \dots De^j \text{ to } \bar{De}^1, De^2 \dots De^j.$$

Each time signal Bc is equal to 1, gating means 300 produces signals Oz^k , corresponding to the selected groups of signals Ia^k ; and each time signal $\bar{Bc}$ is equal to 1, the delay control counter counts down one, changing its delay control representation. After (2^j-1) signals $\bar{Bc}$ have occurred, the delay control counter produces a control representation $\bar{De}^1, \bar{De}^2 \dots \bar{De}^j$, indicating that all delay sections are bypassed or that the only delay between the reading of signals Ia^k and the recording of signals Oz^k is a delay of $(Gl+S)$ provided by delay means 400. The next time signal $\bar{Bc}$ is equal to 1, then the delay control representation is changed from

$$\bar{De}^1, \bar{De}^2 \dots \bar{De}^j \text{ to } De^1, De^2 \dots De^j,$$

indicating that the full capacity of the variable delay means is to be utilized. In effect, this requires that the drum slip an entire revolution, no output signals Oz^k being recorded during this time. It is necessary during this slipping period to prevent reading-writing heads 602 from writing "0's" on the drum. For this purpose a biasing flip-flop is included in the writing circuits for heads 602 and is turned on each time the delay control counter changes from a stable state representing $\bar{De}^1, \bar{De}^2 \dots \bar{De}^j$ to a stable state representing $De^1, De^2 \dots De^j$. When the biasing flip-flop is turned on, it is effective to prevent any writing operation through reading-writing heads 602. The biasing flip-flop circuit is not shown since such circuits are well-known to those skilled in the art.

While the drum circuits shown in Fig. 6 are designed to handle only one sorting problem, it is apparent that it may be duplicated as many times as the drum channel capacity will permit. Thus, it may be possible to handle 20 sorting operations simultaneously, the results from the individual sorting operations being collated to provide the desired sequence of information groups.

Circuits for writing signals onto the magnetic drum and for reading signals from the drum are not shown, since such circuits are well-known in the art. For example, suitable reading and writing circuits are shown in three patents: U. S. Patent No. 2,540,654, entitled "Data Storage System," by A. A. Cohen et al., issued February 6, 1951; U. S. Patent No. 2,609,143, entitled

"Electronic Computer for Addition and Subtraction," by G. Stibitz, issued September 2, 1952; and U. S. Patent No. 2,614,169, entitled "Storage and Relay Means," by A. Cohen, issued October 14, 1952.

Circuits which may be utilized for starting the sorting operation are not shown, since such circuits are well-known in the art. In one type of starting circuit known in the art an operate flip-flop and a start flip-flop are utilized. The operate flip-flop is turned on when the operator pushes an operating button. As soon as the operate flip-flop is turned on, signal *St* (recorded on channel $(3n+4)$ of drum 600) is effective to turn the start flip-flop on, which in turn is effective to turn the operate flip-flop off. Signals *S* and $\bar{S}$ produced by the start flip-flop, then, are utilized to control the operation of selecting means 100, gating means 300, delay control means 600, and sequence control means 700. Signal $\bar{S}$ may be utilized to preset the counters and flip-flops prior to operation and signal *S* to prevent the recording of signals until the operation begins, as signalled by: $S=1$.

It is apparent from the foregoing description that the present invention provides a novel, serial sorting system for selectively sorting randomly-recorded information groups and recording said groups into a predetermined, evenly-spaced sequence. A high-speed, magnetic drum embodiment of the present invention has been described in detail, although it is understood that the invention is not so limited.

While only two sorting programs have been considered in detail (sorting according to one and two binary digits at a time) and only one type of coding (binary) it should be apparent to one skilled in the art that other sorting programs may be utilized as well as other codes without departing from the spirit of the invention.

Suitable structure for each of the means utilized in embodiments of the present invention has been illustrated or incorporated by reference to prior art disclosure. It should be apparent, however, that many substitutions may be made without causing substantial change in the embodiments shown.

What is claimed is:

1. A system for selectively sorting randomly-recorded information groups and re-recording said groups into a predetermined, evenly-spaced sequence, each of said information groups being represented by a set of electrical signals, including code identification signals, said system comprising: selecting means responsive to said code identification signals for producing a binary signal when an information group is to be selected, and for producing a complementary binary signal when an information group is not to be selected; gating means responsive to said binary signals and to said sets of electrical signals for producing randomly-spaced sets of output signals corresponding to the selected sets of electrical signals, respectively; variable delay means connected to said gating means for receiving randomly-spaced sets of output signals; and delay control means responsive to said complementary binary signal for applying a delay control signal to said variable delay means to vary the delay of each of said randomly-spaced sets of output signals to produce corresponding evenly-spaced sets of output signals.

2. A serial sorting system for re-recording randomly-recorded information groups, repre-

sented by sets of electrical signals, including code identification signals, into a predetermined, final sequence, the sorting being performed by selectively recording the information groups into a series of sequences, each sequence being formed by passing the information groups through the sorting system a number of times until all groups have been selected; said system comprising: selecting means responsive to said code identification signals for producing complementary binary control signals Bc and $\bar{Bc}$ corresponding to each information signal group to control its selection or nonselection; gating means responsive to signals Bc and to said sets of electrical signals for producing randomly-spaced sets of output signals O_1 , corresponding to said selected groups, respectively; delay control means responsive to signals Bc for producing delay control signals De ; and variable delay means responsive to signals De for delaying signal sets O_1 to compensate for spaces corresponding to non-selected sets of electrical signals and for producing evenly-spaced sets of output signals O_2 .

3. A system for sorting randomly-recorded information groups into a sequence, each of said information groups including data represented by a first set of electrical signals and 1st, . . . , and *N*th identification code characters, each including 1st, . . . , and *N*th binary digits, represented by complementary binary digit signals Bd^1 , $\bar{Bd}^1$, . . . , and Bd^n , $\bar{Bd}^n$, respectively, said sorting being performed by reading and recording said information groups into 1st, . . . , and *N*th sequences, successively, according to the binary digits of said 1st, . . . , and *N*th code characters, respectively, said system comprising: selecting matrix means responsive to said binary digit signals for producing binary signals Bc when said information groups are to be accepted, read, and recorded, and producing complementary binary signals $\bar{Bc}$ when said information groups are not to be accepted; gating means responsive to said binary signals and to said electrical signals for producing randomly-spaced sets of output signals O_1 , corresponding to the accepted sets of electrical signals; variable delay means responsive to a delay control signal De for delaying each of said signals O_1 for a predetermined time interval; and delay control means responsive to said complementary binary signals Bc for producing delay control signals De , said variable delay means being responsive to each of said signals De to vary said predetermined time interval as a function of the nonacceptance of said information groups.

4. The system defined in claim 3 wherein each of said sequences is formed by producing *n* sub-sequences, considering one of said *n* binary digits at a time, said sub-sequences being formed by passing the information groups through the system $2n$ times; wherein said system further includes sequence control means producing signals Ca^m indicating the particular code character to be considered and signals $P(j)$ indicating that *j*th pass is to be performed, where *j* is any of the integers 1 through $2n$; and wherein said selecting means is mechanized according to the Boolean algebraic function:

$$Bc = Ca^m \cdot [P(1) \cdot Bd^1 + P(2) \cdot \bar{Bd}^1 + \dots + P(2n-1) \cdot \bar{Bd}^n + P(2n) \cdot Bd^n]$$

5. The system defined in claim 3 wherein each of said sequences is formed by producing *n/2* sub-sequences, considering two of said *n* binary digits at a time, said sub-sequences being formed

by passing the information groups through the system $2n$ times less a factor determined by the particular binary code utilized; wherein said system further includes sequence control means producing signals Ca^m indicating the particular code character to be considered and signals $P(j)$ indicating that the j th pass is to be performed, where j is any of the integers 1 through $2n$; and wherein said selecting means is mechanized according to the Boolean algebraic function:

$$Bc = Ca^m \cdot [P(1) \cdot \bar{B}d^2 \cdot \bar{B}d^1 + P(2) \cdot \bar{B}d^2 \cdot Bd^1 + P(3) \cdot Bd^2 \cdot \bar{B}d^1 + P(4) \cdot \bar{B}d^2 \cdot Bd^1 + \dots P(2n-3) \cdot \bar{B}d^n \cdot \bar{B}d^{n-1} \dots 1]$$

6. An electrical sorting system for sorting randomly-recorded information signal groups into a final sequence, each of said signal groups including a plurality of information character signal sets and N code character signal sets, each code character signal set including n binary digit signals, said sorting being performed by selectively recording the information signal groups into a series of sequences, each sequence being formed by passing the signal groups through the system a number of times until all signal groups have been selected; said system comprising: signal source means for producing complementary signals Ia^k and $\bar{Ia}^k$ for each character signal set during each odd sequence of said series of sequences and complementary signals Ib^k and $\bar{Ib}^k$ for each character signal set during each even sequence of said series of sequences, said complementary signals corresponding, respectively, to the n binary digit signals of a character signal set, k being any of the integers 1 through n ; sequence control means for producing signals Ca^m indicating the particular one of the N code character signal sets to be considered, and for producing signals $P(j)$ indicating the particular pass to be performed, m being any of the integers 1 through N and j being any of the integers 1 through $2n$; selecting means for producing binary control signals Bc and complementary binary control signals $\bar{Bc}$ when said signal groups are to be selected and not selected, respectively, said selecting means being responsive to signals Ia^k , $\bar{Ia}^k$, and $P(j)$ during each odd sequence and to signals Ib^k , $\bar{Ib}^k$, Ca^m , and $P(j)$ during each even sequence; gating means responsive to signals Bc for producing, during each sequence, randomly-spaced groups of output signals O_1 , corresponding to said selected signal groups, respectively; and variable delay means responsive to signals $\bar{Bc}$ for delaying signals O_1 to produce corresponding evenly-spaced groups of output signals O_2 , signals O_2 constituting signals Ib^k and $\bar{Ib}^k$ and signals Ia^k and $\bar{Ia}^k$ of the next succeeding sequence after each odd and even sequence, respectively.

7. The sorting system defined in claim 6, which also includes a magnetic drum having n channels for receiving said randomly-recorded information signal groups and for receiving signals O_2 during said even sequences, and n channels for receiving signals O_2 during said odd sequences.

8. The sorting system defined in claim 7, wherein said magnetic drum includes a first additional channel for producing signals Cp , one for each digit of a channel, a second additional channel for producing signal group-end-indicating signals Gp , and a third additional channel co-

operating with said sequence control means to produce signals Ca^m .

9. The sorting system defined in claim 8, wherein sorting is performed according to one binary digit signal at a time and wherein said selecting means includes first and second flip-flops F^1 and F^2 having input circuits $\{F^1, 0F^1$ and $\{F^2, 0F^2$, and producing complementary signals F^1 , $\bar{F}^1$ and F^2 , $\bar{F}^2$ respectively; said selecting means being mechanized according to the Boolean algebraic functions:

$$1F^1 = Ca^m \cdot [P(1) \cdot \bar{Ia}^1 + P(2) \cdot Ia^1 \dots P(2n-1) \cdot \bar{Ib}^n + P(2n) \cdot Ib^n] \cdot Cp$$

$$0F^1 = Gp$$

$$1F^2 = F^1 \cdot Gp$$

$$0F^2 = \bar{F}^1 \cdot Gp$$

10. The sorting system defined in claim 9, wherein said sequence control means also produces signals Ps and $\bar{Ps}$ defined by the Boolean algebraic functions:

$$Ps = P(1) + P(2) + \dots P(2n-3) + 2(2n-2)$$

$$\bar{Ps} = P(3) + P(4) + \dots P(2n-1) + P(2n)$$

where n is an even integer; and wherein said gating means is mechanized according to the Boolean algebraic function:

$$O_1 = Bc \cdot (Ps \cdot Ia^k + \bar{Ps} \cdot Ib^k)$$

11. The sorting system defined in claim 6, which includes a magnetic drum having at least $2n$ channels for receiving signals O_2 , an additional channel for producing signal group-end indicating signals Gp , and a further channel for producing signals Cp , one for each digit interval of a channel.

12. The sorting system defined in claim 11, wherein sorting is performed according to two binary digit signals at a time and wherein said selecting means includes first and second flip-flops F^1 and F^2 having input circuits $\{F^1, 0F^1$ and $\{F^2, 0F^2$, and producing complementary signals F^1 , $\bar{F}^1$ and F^2 , $\bar{F}^2$, respectively; said selecting means being mechanized according to the Boolean algebraic functions:

$$1F^1 = Ca^m \cdot [P(1) \cdot \bar{Ia}^2 \cdot \bar{Ia}^1 + P(2) \cdot \bar{Ia}^2 \cdot Ia^1 \dots P(2n-1) \cdot Ib^n \cdot \bar{Ib}^{n-1} + P(2n) \cdot Ib^n \cdot Ib^{n-1}] \cdot Cp$$

$$0F^1 = Gp$$

$$1F^2 = F^1 \cdot Gp$$

$$0F^2 = \bar{F}^1 \cdot Gp$$

13. The sorting system defined in claim 12, wherein said sequence control means also produces signals Ps and $\bar{Ps}$ defined by the Boolean algebraic functions:

$$Ps = P(1) + P(2) + P(3) + P(4) \dots P(9) + P(10) + P(11) + P(12) + \dots$$

$$\bar{Ps} = P(5) + P(6) + P(7) + P(8) \dots P(13) + P(14) + P(15) + P(16) + \dots$$

and wherein said gating means is mechanized according to the Boolean algebraic function:

$$O_1 = Bc \cdot (Ps \cdot Ia^k + \bar{Ps} \cdot Ib^k)$$

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