FIG. 4

C(S\equiv M) + \overline{C(S\not\equiv M)} = \text{SUM}_1

C(S\equiv M) + C(S\not\equiv M) = \text{SUM}_2

\overline{C(S\equiv M)} + C(S\not\equiv M) = \text{SUM}_3

C(S\not\equiv M) + \overline{S.M} = \text{CARRY}_3

C(S\not\equiv M) + S.M = \text{CARRY}_4
This invention relates to logical electric circuits for producing output signals representing desired logical combinations of binary input signals. Such circuits are used in data processing apparatus.

According to the present invention a logical electric circuit comprises a ferromagnetic core having linked with an aperture thereof a primary winding for energization by current pulses from a current source, an inhibit winding for controlling at alternatively a high or a low value the magnetic flux that may be set up by magnetisation provided by the primary winding, and a secondary winding for producing an output E.M.F. in response to changes in such magnetic flux, and controllable impedance means for connection in circuit with the inhibit winding for presenting in response to a predetermined input condition at input terminals of the impedance means a high impedance to the flow of current induced in the inhibit winding, the impedance means otherwise presenting a low impedance to the flow of such induced current, and each output E.M.F. being representative of the negation of an operand or a logical combination of operands of which the said predetermined input condition at the input terminals of the impedance means is representative.

Means may be provided for applying to one end of the secondary winding a determined bias potential representative of a secondary operand or predetermined logical combination of operands and sensed so that on the induction of an output E.M.F. in the secondary winding the potential of the other end of the secondary winding changes temporarily to a value representative of the logical AND combination of the aforesaid operands or predetermined logical combination of operands.

According to a preferred feature of the present invention there is included a second and similar ferromagnetic core having linked therewith a primary winding (hereafter called the second primary winding) connected in series with the first mentioned primary winding (hereafter called the first primary winding) for energisation by the said current pulses, and an inhibit winding (hereafter called the second inhibit winding) for controlling alternatively at a high or a low value the magnetic flux that may be set up by magnetisation provided by the second primary winding, and a second controllable impedance means for connection in circuit with this second inhibit winding for presenting in response to a predetermined input condition at input terminals of this second impedance means a low impedance to the flow of current induced in the second inhibit winding, the second impedance means otherwise presenting a high impedance to the flow of such induced current, and the said predetermined input condition at the terminals of the second impedance means being representative of the negation of the predetermined input condition at the input terminals of the first-mentioned impedance means.

According to another preferred feature of the present invention the two cores may have linking with their respective apertures two similar parts of a tertiary winding for producing a second output signal, the two parts of the tertiary winding contributing equally to the output signal. In such a logical electric circuit, when the predetermined input condition at the input terminals of the first impedance means is representative of a predetermined logical AND combination of first and second operands and the predetermined input condition at the input terminals of the second impedance means is representative of a predetermined logical AND combination of the negations of the first and second operands, the said second output signal is representative of the equivalence of the first and second operands.

According to another preferred feature of the present invention, a logical electric circuit may comprise a plurality of pairs of ferromagnetic cores, each core having linked with an aperture thereof a primary winding for energisation by current pulses from a current source, and an inhibit winding for controlling alternatively at a high or a low value the magnetic flux that may be set up by magnetisation provided by the associated primary winding, and a plurality of controllable impedance means connected in series with the several inhibit windings respectively, each pair of controllable impedance means associated with the two inhibit windings of each pair of cores being arranged to present in response to a predetermined input condition at input terminals of the two impedance means high and low impedances respectively to the flow of currents induced in the respective associated inhibit windings, the two impedance means otherwise presenting low and high impedances respectively to the flow of such induced currents, and a plurality of electric windings each of which is linked with one or with both apertures of an associated pair of cores for producing output signals dependent on desired logical combinations of binary operand signals applied to the input terminals of the various pairs of impedance means.

By way of example several logical electric circuits according to the present invention will now be described with reference to the accompanying drawings in which:

FIG. 1 shows diagrammatically a circuit by which the logical AND function \( A \cdot B \cdot C \) is produced;

FIG. 2 shows diagrammatically a circuit by which the logical AND function \( A \cdot C \) is produced;

FIG. 3 shows diagrammatically a circuit by which the logical equivalence and non-equivalence functions \( A = B \) and \( A \neq B \) are produced; and

FIG. 4 shows diagrammatically a circuit which is suitable for use as one stage of a parallel binary multiplier of a data processing apparatus.

In the drawings an aperture or hole in a pulse transformer ferromagnetic core is symbolically shown as a dotted line. The dot notation is used to indicate the senses in which the windings are wound with respect to one another, the electric polarity induced in a winding with respect to its dot being the same as the electric polarity in the inducing winding with respect to its dot. Another notation adopted for this description is that an input terminal is indicated by a dot and an output terminal by a circle.

In FIG. 1 the logical electric circuit includes a pulse transformer whose ferromagnetic core has an aperture \( H_0 \) with which are linked a primary winding \( P_1 \), a secondary winding \( S_1 \) and an inhibit winding \( I_1 \), the secondary winding \( S_1 \) and the inhibit winding \( I_1 \) being connected in an output circuit between a first input terminal and an output terminal, whilst the inhibit winding \( I_1 \) is connected in an inhibit circuit which includes a controllable impedance means. This controllable impedance means takes the form of a parallel-connected circuits each of which includes a diode and a gate. Each gate has an input terminal, and these will be referred to as the second and third input terminals.

In operation, the primary circuit is energized when desired with "drive" current pulses from a pulse generator (not shown), and input potentials are applied to the input terminals to represent the condition, as shown, of the
3 binary operand C at the first input terminal, and of the negations of the binary operands A and B at the second and third input terminals. If either or both of the gates in the inhibit circuit are "closed" the inhibit winding will be short-circuited, and no output will be induced in the secondary winding. Thus, by controlling the gates in accordance with the input binary signals representing the respective negations A and B an E.M.F. will be induced in the secondary winding only when A and B are both absent; that is to say the secondary E.M.F. pulse will represent the binary AND function \( A \& B \). Also since a bias is applied to the secondary winding \( S_0 \), representing the additional binary operand C, the output voltage will either exceed or not a predetermined level on the occurrence of a drive pulse in the primary circuit, so that the logical AND combination or function \( A \& B \& C \) will be represented by whether or not the voltage at the output terminal exceeds the predetermined level.

It will be readily appreciated from the above that the inhibit winding has the effect of controlling in dependence on its own energisation the magnitude of the magnetic flux due to the primary winding energisation alternatively at a high value or a low value, and that the energisation of the inhibit winding in turn depends on the impedances represented by the controllable impedances means to the flow of current induced in the inhibit winding by the magnetic flux. It will also be appreciated that the impedance presented by the controllable impedance means will be alternatively of a high or a low value, being normally of the low value, but of the high value in response to the unique input condition at the said second and third input terminals which occurs when both \( A \) and \( B \) are represented by the zero state input signal.

Preferably the current pulses supplied to the primary winding \( P_0 \) have a magnitude such that the maximum magnetisation of the core is restricted so as to prevent any appreciable saturation of the core taking place.

The logical electric circuit of FIG. 2 includes two pulse transformers whose ferro-magnetic cores have apertures \( H_1 \) and \( H_2 \). Linked with the aperture \( H_1 \) of the first transformer are a primary winding \( P_1 \), a secondary winding \( S_1 \), and an inhibit winding \( I_1 \). The secondary winding is connected in an output circuit between an output terminal and an input terminal to which is applied as shown an input terminal representative of the operand \( C \) whilst the inhibit winding is connected in an inhibit circuit which includes a controllable impedance means comprising in series a diode and a gate for enabling the anode of the diode to be held at earth potential in the presence of the inhibit winding of the inhibit terminals of the one state of the negation \( \bar{A} \).

Linked with the second aperture \( H_2 \) of the second transformer is a primary winding \( P_2 \) and an inhibit winding \( I_2 \). The primary winding is constructed in series with the primary winding \( P_1 \) for energisation by the same current pulses, whilst the inhibit winding \( I_2 \) is connected in series with the controllable impedance means which comprises a diode connected in series with a gate for enabling the anode of the diode to be held at earth potential in the presence of the inhibit terminal of an input signal representative of the ONE state of the negation \( \bar{A} \).

In operation the circuit functions in a manner analogous to that of the circuit of FIG. 1 to produce an output signal representative of the logical combination \( A \& C \), just as the circuit of FIG. 1 would produce if the gate controlled by the negation \( B \) were maintained permanently open.

It will be observed that since the controllable impedance means connected in circuit with the two inhibit windings respectively are controlled in dependence upon input signals which represent respectively the operand \( A \) and the negation \( \bar{A} \), whatever the state of the operand one of the inhibit windings will be short-circuited and the other open-circuited. Hence the effective impedance of the primary winding circuit to drive current pulses is constant regardless of whether the operand \( A \) has the ZERO or UNIT state. This is a highly advantageous feature in cases where the pulse generator for supplying the primary circuit is a voltage pulse generator, since the impedance of the primary winding circuit can never fall below a predetermined value.

The two pulse transformers may if desired be made with cores which are constituted by a single ferro-magnetic member having approximately apertures and windings so that the action of one transformer is not interfered with magnetically by the action of the other transformer.

The logical electric circuit of FIG. 3 includes four generally similar pulse transformers whose ferro-magnetic cores have apertures \( H_3 \) to \( H_6 \). Linked with each such aperture are a primary winding \( P_3 \) to \( P_6 \), an inhibit winding \( I_3 \) to \( I_6 \), and a secondary winding. The primary windings are all connected in series for energisation by the same drive current pulses, and the secondary windings of the first pair of transformers are connected in series to form a first secondary winding circuit \( S_2 \), whilst the secondary windings of the second pair of transformers are connected in series to form a second secondary winding circuit \( S_3 \).

The inhibit windings are connected in separate inhibit circuits each of which includes a separate controllable impedance means. Each such controllable impedance means comprises two parallel connected circuits each of which comprises in series a diode and a gate having an input terminal. Input signals representative of the states of the operands \( A \) and \( B \) and of their negations \( \bar{A} \) and \( \bar{B} \) are applied to the respective pairs of input terminals of the two controllable impedance means associated with the inhibit windings \( I_3 \) and \( I_4 \), whilst input signals representative of the states of \( A \) and \( \bar{B} \) and of \( \bar{A} \) and \( B \) are applied to the respective pairs of input terminals of the two controllable impedance means associated with the inhibit windings \( I_5 \) and \( I_6 \).

In operation irrespective of the states of the operands \( A \) and \( B \) there will always be one, and only one, of the inhibit windings \( I_3 \) to \( I_6 \) which is not short-circuited, so that on the occurrence of a drive current pulse in the primary winding circuit an E.M.F. will be induced in the secondary winding circuit which is linked with the aperture with which that particular inhibit winding is linked. It can be shown that by varying the impedance of the inhibit circuit in accordance with \( A \) and \( \bar{B} \), of the \( I_4 \) inhibit circuit in accordance with \( \bar{A} \) and \( B \), of the \( I_5 \) inhibit circuit in accordance with \( \bar{A} \) and \( B \), and of the \( I_6 \) circuit in accordance with \( A \) and \( \bar{B} \), an output E.M.F. will be produced by the first secondary winding circuit \( S_2 \) when the operands \( A \) and \( B \) are equivalent, and by the second secondary winding circuit \( S_3 \) when the operands \( A \) and \( B \) are not equivalent. This circuit also provides substantially constant impedance to circuit pulses in the primary circuit.

If desired, the cores of the transformers in this circuit may be composed of two pieces of ferro-magnetic material each having two apertures, or a single piece having four apertures. In such cases the windings \( S_2 \) and \( S_3 \) are wound on the arms separating the apertures \( H_3 \) and \( H_4 \), and \( H_5 \) and \( H_6 \) respectively.

The logical electrical circuit of FIG. 4 includes four pulse transformers having apertures \( H_7 \) to \( H_{10} \). Linked with the apertures \( H_7 \) and \( H_8 \) are primary windings \( P_7 \), \( P_8 \), inhibit windings \( I_7 \) and \( I_8 \), and secondary windings \( S_4 \) and \( S_5 \), whilst linked equally with both such apertures \( H_7 \), \( H_8 \) are secondary windings \( S_6 \) and \( S_7 \). Linked with the apertures \( H_9 \) and \( H_{10} \) are primary windings \( P_9 \) and \( P_{10} \) and inhibit windings \( I_9 \) and \( I_{10} \), whilst, linking equally with both the apertures \( H_9 \) and \( H_{10} \) are secondary winding circuits \( S_8 \) and \( S_9 \).

The primary windings \( P_7 \) to \( P_{10} \) are all connected in series for energisation by the same current pulses, whilst the inhibit windings are connected in separate inhibit cir-
circuits each of which includes a separate controllable impedance means. Each such controllable impedance means comprises two parallel connected circuits each of which includes in series a diode and a gate having an input terminal. Input signals representative of the states of the operands S and M and of their negations $\overline{S}$ and $\overline{M}$ are applied to the respective pairs of input terminals of the two controllable impedance means associated with the inhibit windings $i_7$ and $i_8,$ whilst input signals representative of the states of $S$ and $M$ and of $\overline{S}$ and $\overline{M}$ are applied to the respective pairs of input terminals of the two controllable impedance means associated with the inhibit windings $i_9$ and $i_{10}.$

Input signals representative of the states of the operand C and its negation $\overline{C}$ are applied to the input terminals of the secondary winding circuits $s_6$ and $s_9,$ and $s_7$ and $s_8$ respectively as shown.

Four output terminals $t_1$ to $t_4$ are connected through diodes with the various secondary windings and secondary winding circuits, the terminal $t_1$ being connected to the secondary winding circuits $s_6$ and $s_8,$ terminal $t_2$ being connected with the secondary winding circuits $s_7$ and $s_9,$ terminal $t_3$ being connected with the secondary winding $s_4$ and the secondary winding circuit $s_8,$ and terminal $t_4$ being connected with secondary winding $s_5$ and secondary winding circuit $s_9.$

In operation irrespective of the states of the operands S and M there will always be one, and only one, of the inhibit windings $i_7$ to $i_{10}$ which is not short-circuited, so that on the occurrence of a drive current pulse in the primary winding circuit E.M.F.'s will be induced in the secondary windings and secondary winding circuits which are linked with the aperture with which that particular inhibit winding is linked.

From the foregoing description with reference to FIGS. 1 to 3 it will be appreciated that when the primary winding circuit carries a current pulse output signals dependent on the various states of the following logical combinations of operands and their negations will be produced:

From $s_4$ $S\overline{M}$
From $s_5$ $S\overline{M}$
From $s_6$ $C(S\overline{M})$
From $s_7$ $\overline{U}(S\overline{M})$
From $s_8$ $\overline{U}(S \neq M)$
From $s_9$ $C(S \neq M)$

Thus according to the rules given below for binary multiplication, where S, C and M are respectively the SUM and CARRY operands from a previous multiplication operation and a new multiplicand, the output signals delivered at the terminals $t_1$ to $t_4$ will be respectively representative of the new SUM operand, its negation, the negation of a new CARRY operand, and the new CARRY operand.

$$SUM = C(S\overline{M}) + \overline{U}(S \neq M)$$
$$SUM = C(S\overline{M}) + U(S\overline{M}) + C(S \neq M)$$
$$CARRY = C(S + M) + S.M = C(S \neq M) + S.M$$
$$CARRY = C(S + M) + S.M = U(S\overline{M}) + M$$

It should be noted that $S\overline{M}$ is different from $S \neq M$ only when $S = M = 1$ and in this case $S.M$ will provide the CARRY signal; a similar argument applies to the SUM signal.

As in the circuit described with reference to FIG. 3 the transformer cores may consist of one or more pieces of ferro-magnetic material having a total of four apertures. In a parallel binary multiplier having r stages 4r transformers are required. These may have 4r single cores each having an aperture or a single core piece having 4r apertures or convenient intermediate subdivisions may be made.

As mentioned in connection with the circuit of FIG. 1, it is preferable in the circuits of FIGS. 2–4 that the drive current pulses have a magnitude limited so that the maximum magnetisation of the cores is restricted so as to prevent any appreciable saturation of the cores occurring.

Many other logical electric circuits using the ideas explained above may be devised. However, in order to present a constant impedance to the drive current pulses applied to such circuits there should be for each aperture linked by an inhibit winding another aperture linked by another inhibit winding whose impedance is controlled in accordance with the negation of the operand, or logical combination of operands, in accordance with which the impedance of the first mentioned inhibit winding is controlled.

What we claim as our invention and desire to secure by Letters Patent is:

1. A logic device comprising:
   a magnetizable core;
   a drive winding coupled to the core;
   means for regularly applying drive pulses to the drive winding;
   an inhibit winding coupled to the core;
   a variable impedance means connected across the inhibit winding and controllable in response to an input signal to assume a high or a low impedance state;
   an output winding coupled to the core; and
   a source of logical signals connected to the output winding;
   the core being switched by the drive pulses only if the variable impedance means is in the high impedance state and a true output signal being produced only if the core is switched and the signal produced by said source of logical signals is simultaneously true.

2. A logic device in accordance with claim 1 and further comprising at least one further variable impedance means similar to and connected in parallel with said variable impedance means.

3. A logic device in accordance with claim 1 and further comprising:
   at least one further inhibit winding coupled to the core; and,
   for each further inhibit winding, at least one further variable impedance means similar to said variable impedance means and connected thereacross.

4. A logic system comprising:
   a first logic device comprising:
      a magnetizable core,
      a drive winding coupled to the core,
      an inhibit winding coupled to the core,
      a variable impedance device connected across the inhibit winding and controllable in response to an input signal to assume a high or low impedance state, and
      an output winding coupled to the core;
   a second logic device comprising:
      a magnetizable core,
      a drive winding coupled to the core,
      an inhibit winding coupled to the core,
      a variable impedance device connected across the inhibit winding and controllable in response to the complement of said input signal to assume a high or low impedance state; and
      means for regularly supplying drive pulses at and having the drive windings of the first and second logic devices connected in series thereacross.

5. A logic system comprising:
   a first logic device which comprises:
      a magnetizable core,
      a drive winding coupled to the core,
      an inhibit winding coupled to the core,
      first and second variable impedance devices connected in parallel across the inhibit winding and
controllable in response to first and second input signals respectively to assume high or low impedance states, and

a first output winding coupled to the core;

a second logic device which comprises;

a magnetizable core,
a drive winding coupled to the core,
a second variable impedance device connected in parallel across the inhibit winding and controllable in response to the first input signal and the complement of the second input signal respectively to assume high or low impedance states;

a third logic device which comprises;

a magnetizable core,
an inhibit winding coupled to the core, and
first and second variable impedance devices connected in parallel across the inhibit winding and controllable in response to the complement of the first input signal and the second input signal respectively to assume high or low impedance states;

a fourth logic device which comprises;

a magnetizable core,
a drive winding coupled to the core,
an inhibit winding coupled to the core, and
first and second variable impedance devices connected in parallel across the inhibit winding and controllable in response to the complements of the first and second input signals respectively to assume high or low impedance states;

and drive means for regularly supplying drive pulses and having the drive windings of the first, second, third and fourth logic devices connected in series thereacross.

6. A logic system in accordance with claim 5, wherein each of said second, third, and fourth logic devices has a respective first output winding coupled to its respective core, and the first output windings of the first and second logic devices are connected in series, and

the first output windings of the third and fourth logic devices are connected in series.

7. A logic system in accordance with claim 6, and wherein each of the first and second logic devices is provided with a respective second output winding and a respective third output winding coupled to its respective core; and each of the third and fourth logic devices is provided with a respective second output winding coupled to its respective core;

the second output windings of the first and second logic devices being serially connected together, and the second output windings of the third and fourth logic devices being serially connected together; and further comprising;

means for applying a third input signal to
the serial connection of the first output windings of the first and second logic devices,
and to the serial connection of the second output windings of the third and fourth logic devices;

means for applying the complement of the third input signal to
the serial connection of the second output windings of the first and second logic devices,
and to the serial connection of the first output windings of the third and fourth logic devices;
a first diode OR gate to which the serial connection of the first output windings of the first and second logic devices and the serial connection of the first output windings of the third and fourth logic devices are connected;
a second diode OR gate to which the serial connection of the second output windings of the first and second logic devices and the serial connection of the second output windings of the third and fourth logic devices are connected;
a third diode OR gate to which the third output winding of the first logic device and the serial connection of the first output windings of the third and fourth logic devices are connected; and

a fourth diode OR gate to which the third output winding of the second logic device and the serial connection of the second output windings of the third and fourth logic devices are connected.

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