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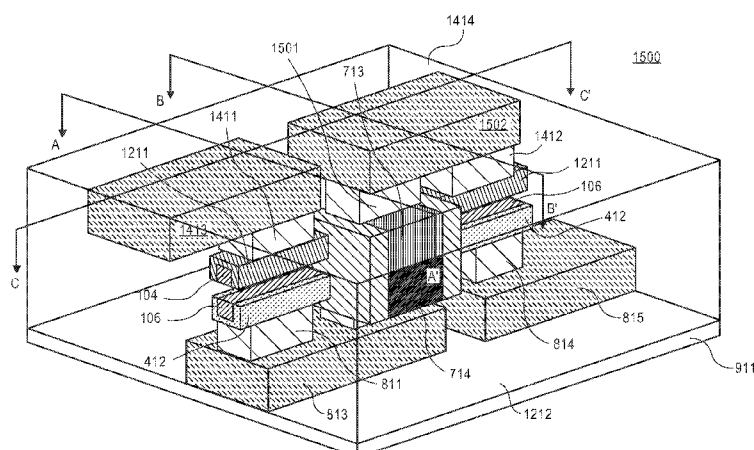


FIG. 15

(57) **Abstract:** A first interconnect layer is bonded to a first substrate. The first interconnect layer is deposited on a first device layer on a second device layer on a second substrate. The second device layer is revealed from the second substrate side. A first insulating layer is deposited on the revealed second device layer. A first opening is formed in the first insulating layer to expose a first portion of the second device layer. A contact region is formed on the exposed first portion of the second device layer.

STACKED TRANSISTORS

FIELD

Embodiments as described herein relate to a field of microelectronic device manufacturing, and in particular, to stacked devices manufacturing.

5 BACKGROUND

Decreasing the dimensions of semiconductor devices and increasing the level of their integration are two major trends in the current device manufacturing. As a result of these trends, the density of elements forming a semiconductor device increases. Scaling of the devices down to submicron dimensions requires the routine fabrication of the device elements at the submicron
10 level that becomes more difficult due to physics challenges at small dimensions.

Generally, semiconductor structures forming semiconductor devices may be stacked on top of one another to increase the level of the device integration and reduce the device footprint. Typically, the stacked devices are interconnected vertically using vias that are a part of an interconnect structure. The interconnect structure includes one or more levels of metal lines to
15 connect the electronic devices to one another and to external connections.

Traditionally, the transistors of the stacked transistor structure are manufactured independently. One of the conventional techniques involves building the transistors independently on two separate wafers and then bonding the wafers to stack the devices on top of one another. Another one of the conventional techniques involves sequentially building the
20 transistors in layers on a single semiconductor wafer. Both conventional techniques require separate sets of the lithographical and other processing operations for each of the transistors that consumes time and is very expensive.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention may be best understood by referring to the following
25 description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

Figure 1 shows a three-dimensional view of a portion of an electronic device according to one embodiment.

Figure 1A shows a side view of the portion of the electronic device shown in Figure 1
30 along a plane YZ according to one embodiment.

Figure 1B shows a cross-sectional view of the portion of the electronic device shown in Figure 1 along an A-A' axis according to one embodiment.

Figure 1C shows a cross-sectional view of the portion of the electronic device shown in Figure 1 along a B-B' axis according to one embodiment.

Figure 2 is a view similar to Figure 1 after a replacement gate and spacers are formed on the fin according to one embodiment.

Figure 2A is a side view of the portion of the electronic device shown in Figure 2 along a plane YZ according to one embodiment.

5 Figure 2B is a cross-sectional view of the portion of the electronic device shown in Figure 2 along A-A' axis according to one embodiment.

Figure 2C is a cross-sectional view of the portion of the electronic device shown in Figure 2 along a B-B' axis according to one embodiment.

10 Figure 3A is a view similar to Figure 2A after portions of the intermediate layers are removed according to one embodiment.

Figure 3B is a view similar to Figure 2B after portions of the intermediate layers are removed according to one embodiment.

Figure 3C is a view similar to Figure 2C after portions of the intermediate layers are removed according to one embodiment.

15 Figure 4A is a view similar to Figure 3A after an insulating layer and a doped layer are deposited according to one embodiment.

Figure 4B is a view similar to Figure 3B after an insulating layer and a doped layer are deposited according to one embodiment.

20 Figure 4C is a view similar to Figure 3C after an insulating layer and a doped layer are deposited according to one embodiment.

Figure 5A is a view similar to Figure 3A after depositing an insulating layer and adding dopants to the exposed portions of the device layer to form source/drain regions according to another embodiment.

25 Figure 5B is a view similar to Figure 3B after depositing an insulating layer and adding dopants to the exposed portions of the device layer to form source/drain regions according to another embodiment.

Figure 5C is a view similar to Figure 3C after depositing an insulating layer and adding dopants to the exposed portions of the device layer to form source/drain regions according to another embodiment.

30 Figure 6A is a view similar to Figure 4A after an insulating layer is deposited on the doped layer according to one embodiment.

Figure 6B is a view similar to Figure 4B after an insulating layer is deposited on a doped layer according to one embodiment.

Figure 6C is a view similar to Figure 4C after an insulating layer is deposited on a doped layer according to one embodiment.

Figure 7A is a cross-sectional view of the portion of the electronic device shown in Figure 6A after removing the replacement gate and depositing a metal gate according to one
5 embodiment.

Figure 7B is a view similar to Figure 6B after removing the replacement gate and depositing a metal gate according to one embodiment.

Figure 7C is a view similar to Figure 7C after removing the replacement gate and depositing a metal gate according to one embodiment.

Figure 8A is a view similar to Figure 7A after an interconnect layer is deposited on the device layer according to one embodiment.

Figure 8B is a view similar to Figure 7B after an interconnect layer is deposited on the device layer according to one embodiment.

Figure 8C is a view similar to Figure 7C after an interconnect layer is deposited on the
15 device layer according to one embodiment.

Figure 9A is a view similar to Figure 8A after an interconnect layer is deposited on the device layer according to one embodiment.

Figure 9B is a view similar to Figure 8B after an interconnect layer is deposited on the device layer according to one embodiment.

Figure 9C is a view similar to Figure 8C after an interconnect layer is deposited on the
20 device layer according to one embodiment.

Figure 10A is a view similar to Figure 9A after the portions of the fin and substrate are removed according to one embodiment.

Figure 10B is a view similar to Figure 9B after the portions of the fin and substrate are
25 removed according to one embodiment.

Figure 10C is a view similar to Figure 9C after the portions of the fin and substrate are removed according to one embodiment.

Figure 11A is a view similar to Figure 10A after an insulating layer filling the backside opening is deposited onto the gate portion according to one embodiment.

Figure 11B is a view similar to Figure 10B after an insulating layer filling the backside opening is deposited onto the gate portion according to one embodiment.

Figure 11C is a view similar to Figure 10C after an insulating layer filling the backside opening is deposited onto the gate portion according to one embodiment.

Figure 12A is a view similar to Figure 11A after a doped layer is deposited through the backside opening according to one embodiment.

Figure 12B is a view similar to Figure 11B after a doped layer is deposited through the backside opening according to one embodiment.

5 Figure 12C is a view similar to Figure 11C after a doped layer is deposited through the backside opening according to one embodiment.

Figure 13A is a view similar to Figure 11A after adding dopants through the backside openings to form source/drain regions according to another embodiment.

10 Figure 13B is a view similar to Figure 11B after adding dopants through the backside openings to form source/drain regions according to another embodiment.

Figure 13C is a view similar to Figure 11C after adding dopants through the backside openings to form source/drain regions according to another embodiment.

Figure 14A is a view similar to Figure 12A after an interconnect layer is deposited on the device layer according to one embodiment.

15 Figure 14B is a view similar to Figure 12B after an interconnect layer is deposited on the device layer according to one embodiment.

Figure 14C is a view similar to Figure 12C after an interconnect layer is deposited on the device layer according to one embodiment.

20 Figure 15 is a three-dimensional view of a portion of an electronic device according to one embodiment.

Figure 16A is a view similar to Figure 12A after a spacer layer is deposited on a sidewall of the opening according to one embodiment.

Figure 16B is a view similar to Figure 12B after a spacer layer is deposited on a sidewall of the opening according to one embodiment.

25 Figure 16C is a view similar to Figure 12C after a spacer layer is deposited on a sidewall of the opening according to one embodiment.

Figure 17A is a view similar to Figure 16A after an opening is formed through the device layers according to one embodiment.

30 Figure 17B is a view similar to Figure 16B after an opening is formed through the device layers according to one embodiment.

Figure 17C is a view similar to Figure 16C after an opening is formed through the device layers according to one embodiment.

Figure 18A is a view similar to Figure 17A after the spacer layer is removed, and a conductive feature is deposited into the opening in the insulating layer according to one embodiment.

Figure 18B is a view similar to Figure 17B after the spacer layer is removed, and a conductive feature is deposited into the opening in the insulating layer according to one embodiment.

Figure 18C is a view similar to Figure 17C after the spacer layer is removed, and a conductive feature is deposited into the opening in the insulating layer according to one embodiment.

Figure 19A is a view similar to Figure 16A after conductive features are deposited according to another embodiment.

Figure 19B is a view similar to Figure 16B after conductive features are deposited according to another embodiment.

Figure 19C is a view similar to Figure 16C after conductive features are deposited according to another embodiment.

Figure 20A is a view similar to Figure 6A after an interconnect layer is deposited on the device layer according to another embodiment.

Figure 20B is a view similar to Figure 6B after an interconnect layer is deposited on the device layer according to another embodiment.

Figure 20C is a view similar to Figure 6C after an interconnect layer is deposited on the device layer according to another embodiment.

Figure 21A is a view similar to Figure 20A after the portion of the electronic device is flipped and bonded to a carrier substrate according to another embodiment.

Figure 21B is a view similar to Figure 20B after the portion of the electronic device is flipped and bonded to a carrier substrate.

Figure 21C is a view similar to Figure 20C after the portion of the electronic device is flipped and bonded to a carrier substrate.

Figure 22A is a view similar to Figure 21A after an insulating layer is deposited onto the exposed gate portion according to another embodiment.

Figure 22B is a view similar to Figure 21B after an insulating layer is deposited onto the exposed gate portion according to another embodiment.

Figure 22C is a view similar to Figure 21C after an insulating layer is deposited onto the exposed gate portion according to another embodiment.

Figure 23A is a view similar to Figure 22A after conductive features are deposited onto source/drain regions according to another embodiment.

Figure 23B is a view similar to Figure 22B after conductive features are deposited onto source/drain regions according to another embodiment.

5 Figure 23C is a view similar to Figure 22C after conductive features are deposited onto source/drain regions according to another embodiment.

Figure 24A is a view similar to Figure 23A after an opening is formed in the insulating layer to expose a portion of the gate according to another embodiment.

10 Figure 24B is a view similar to Figure 23B after an opening is formed in the insulating layer to expose a portion of the gate according to another embodiment.

Figure 24C is a view similar to Figure 23C after an opening is formed in the insulating layer to expose a portion of the gate according to another embodiment.

Figure 25A is a view similar to Figure 24A after a backside opening is formed according to another embodiment.

15 Figure 25B is a view similar to Figure 24B after a backside opening is formed according to another embodiment.

Figure 25C is a view similar to Figure 24C after a backside opening is formed according to another embodiment.

20 Figure 26A is a view similar to Figure 25A after an insulating layer is deposited according to another embodiment.

Figure 26B is a view similar to Figure 25B after an insulating layer is deposited according to another embodiment.

Figure 26C is a view similar to Figure 25C after an insulating layer is deposited according to another embodiment.

25 Figure 27A is a view similar to Figure 26A after a metal gate is deposited according to another embodiment.

Figure 27B is a view similar to Figure 26B after a metal gate is deposited according to another embodiment.

30 Figure 27C is a view similar to Figure 26C after a metal gate is deposited according to another embodiment.

Figure 28A is a view similar to Figure 27A after a conductive feature is deposited according to another embodiment.

Figure 28B is a view similar to Figure 27B after a conductive feature is deposited according to another embodiment.

Figure 28C is a view similar to Figure 27C after a conductive feature is deposited according to another embodiment.

Figure 29 illustrates an interposer that includes one or more embodiments of the invention.

5 Figure 30 illustrates a computing device in accordance with one embodiment of the invention.

DETAILED DESCRIPTION

Methods and apparatuses to provide stacked devices are described. An interconnect layer is deposited on a first device layer on a second device layer on a backside substrate. The
10 interconnect layer is bonded to a carrier substrate. The second device layer is revealed from the second substrate side. An insulating layer is deposited on the revealed second device layer. An opening is formed in the insulating layer to expose a portion of the second device layer. A source/drain region is formed on the exposed portion of the second device layer. In one embodiment, the first device layer on the second device layer are a part of a fin formed on the
15 backside substrate. In one embodiment, an intermediate layer is deposited between the first device layer and the second device layer.

In one embodiment, the stacked device structure comprising an upper device layer on a lower device layer is manufactured by partially forming the lower device contact layers from the backside using a backside reveal process. The backside reveal enables forming a gate and the
20 source/drain regions from the backside of the structure. In one embodiment, forming the contact regions of the device involves epitaxially growing a doped semiconductor layer on the contact region of the device layer from the backside of the structure. In another embodiment, forming the contact regions of the device from the backside involves adding a dopant to the contact region using an implantation technique from the backside of the structure. Backside fabrication of the
25 stacked structure has an advantage over the conventional frontside techniques. The gate and source/drain regions of the lower device of the stacked transistor structure are impossible, or at the very least, difficult to fabricate with the conventional frontside techniques. Fabrication of the contact regions of the lower device layer, from the backside, advantageously simplifies the manufacturing process and reduces cost comparing with the conventional techniques.

30 In one embodiment, manufacturing the stacked device structure involves sharing the fin and gate patterning operations for the stacked devices. Sharing the fin and gate patterning operations for the stacked devices advantageously reduces the manufacturing cost comparing with the conventional techniques.

In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some of the described aspects. For purposes of
5 explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present invention may be practiced without specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

10 Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention; however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

15 While certain exemplary embodiments are described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive, and that the embodiments are not restricted to the specific constructions and arrangements shown and described because modifications may occur to those ordinarily skilled in the art.

Reference throughout the specification to “one embodiment”, “another embodiment”, or “an embodiment” means that a particular feature, structure, or characteristic described in
20 connection with the embodiment is included in at least one embodiment. Thus, the appearance of the phrases, such as “one embodiment” and “an embodiment” in various places throughout the specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

25 Moreover, inventive aspects lie in less than all the features of a single disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment. While the exemplary embodiments have been described herein, those skilled in the art will recognize that these exemplary embodiments can be practiced with modification and
30 alteration as described herein. The description is thus to be regarded as illustrative rather than limiting.

Figure 1 shows a three-dimensional view of a portion of an electronic device 100 according to one embodiment. Figure 1A shows a side view 110 of the portion of the electronic device 100 shown in Figure 1 along a plane YZ according to one embodiment. Figure 1B shows

a cross-sectional view 120 of the portion of the electronic device 100 along an A-A' axis. Figure 1C shows a cross-sectional view 130 of the portion of the electronic device 100 along a B-B' axis. As shown in Figures 1, 1A, 1B, and 1C, electronic device 100 comprises a fin 102 on a substrate 101. In one embodiment, substrate 101 is a backside substrate.

5 In an embodiment, the substrate 101 comprises a semiconductor material, e.g., silicon (Si). In one embodiment, substrate 101 is a monocrystalline Si substrate. In another embodiment, substrate is a polycrystalline Si substrate. In yet another embodiment, substrate 101 is an amorphous Si substrate. In alternative embodiments, substrate 101 includes silicon, germanium ("Ge"), silicon germanium ("SiGe"), a III-V materials based material e.g., gallium arsenide ("GaAs"), or any combination thereof. In one embodiment, the substrate 101 includes
10 metallization interconnect layers for integrated circuits. In at least some embodiments, the substrate 101 includes electronic devices, e.g., transistors, memories, capacitors, resistors, optoelectronic devices, switches, and any other active and passive electronic devices that are separated by an electrically insulating layer, for example, an interlayer dielectric, a trench
15 insulation layer, or any other insulating layer known to one of ordinary skill in the art of the microelectronic device manufacturing. In at least some embodiments, the substrate 101 includes interconnects, for example, vias, configured to connect the metallization layers.

In an embodiment, substrate 101 is a semiconductor-on-insulator (SOI) substrate including a bulk lower substrate, a middle insulation layer, and a top monocrystalline layer. The top
20 monocrystalline layer may comprise any material listed above, e.g., silicon.

In various implementations, the substrate 100 can be, e.g., an organic, a ceramic, a glass, or a semiconductor substrate. In one implementation, the substrate 100 may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which
25 may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which passive and active electronic
30 devices (e.g., transistors, memories, capacitors, inductors, resistors, switches, integrated circuits, amplifiers, optoelectronic devices, or any other electronic devices) may be built falls within the spirit and scope of the present invention.

As shown in Figures 1, 1A, 1B, and 1C, fin 102 comprises a stack of a device layer 106 on an intermediate layer 105 on a device layer 104 on an intermediate layer 103 on a base 201. In

alternative embodiments, fin 102 comprises a stack of more than two device layers on top of each other that are separated by the intermediate layers. In one embodiment, an insulating layer (e.g., an oxide) (not shown) is deposited between intermediate layer 103 and base 201. In one embodiment, base 201 is a part of the substrate 101. In one embodiment, base 201 comprises the same material as that of the substrate 101. In one embodiment, base 201 is silicon. In another embodiment, base 201 comprises the material that is different from that of the substrate 101. As shown in Figures 1, 1A, 1B, and 1C, fin 102 comprises a top portion and opposing sidewalls. The fin 102 has a width along an X axis, a length along an Y axis and a height along a Z axis. In one embodiment, the width of the fin 102 defines the width of the transistor, or other electronic device formed later on in a process. In one embodiment, the width of the fin 102 is from about 1 nanometers (nm) to about 20 nm. In more specific embodiment, the width of the fin 102 is from about 4 nm to about 15 nm. In one embodiment, the height of the fin 102 is at least twice greater than the width and is determined by design. In one embodiment, the length of the fin 102 is greater than the width and is determined by design. In one embodiment, the length of the fin 102 is from about 10 nm to hundreds of microns.

In one embodiment, each of the device layers 104 and 106 is a layer on which a transistor, or other electronic device, is formed later on in a process. In one embodiment, fin 102 comprising a stack of at least two transistors, or other devices is defined using a single lithographical operation. In one embodiment, the material of each of the device layers 104 and 106 is different from the material of each of the intermediate layers 103 and 105. The device layers 104 and 106 can be formed of any semiconductor material, such as but not limited to silicon (Si), germanium (Ge), silicon germanium (Si_xGe_y), a III-V material, e.g., gallium arsenide (GaAs), InSb, GaP, GaSb, carbon nanotubes, other material to fabricate an electronic device, or any combination thereof. In one embodiment, each of the intermediate layers 103 and 105 is a sacrificial layer that is removed later on in a process. In one embodiment, each of the intermediate layers 103 and 105 is a silicon germanium (SiGe) layer. In one embodiment, each of the intermediate layers 103 and 105 is an insulating layer, e.g., a low-k interlayer dielectric (ILD) layer. In alternate embodiments, each of the intermediate layers 103 and 105 is an oxide layer, e.g., a silicon oxide layer, an aluminum oxide, a carbon doped oxide (e.g., a carbon doped silicon oxide), a carbon layer, or any combination thereof. In another embodiment, each of the intermediate layers 103 and 105 is a polymer layer, or other sacrificial layer. In more specific embodiment, each of the device layers 104 and 106 is a silicon layer and each of the intermediate layers 103 and 105 is a silicon germanium layer. In one embodiment, the thickness of each of the

device layers 104 and 106 is from about 5nm to about 100 nm. In one embodiment, the thickness of each of the intermediate layers 103 and 105 is from about 1 nm to about 20 nm.

In one embodiment, each of the device layers 106 and 104 is deposited using one or more deposition techniques, such as but not limited to, a chemical vapour deposition (“CVD”), e.g., a plasma Enhanced chemical vapour deposition (“PECVD”), a physical vapour deposition (“PVD”), molecular beam epitaxy (“MBE”), metalorganic chemical vapor deposition (“MOCVD”), atomic layer deposition (“ALD”), or other deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, each of the intermediate layers 105 and 103 is deposited using one or more deposition techniques, such as but not limited to, a chemical vapour deposition (“CVD”), e.g., a plasma enhanced chemical vapour deposition (“PECVD”), a physical vapour deposition (“PVD”), molecular beam epitaxy (“MBE”), metalorganic chemical vapor deposition (“MOCVD”), atomic layer deposition (“ALD”), or other deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

In one embodiment, the fin 102 is fabricated using one or more patterning and etching techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

As shown in Figures 1, 1A, 1B and 1C, an insulating layer 107 is deposited on substrate 101. In one embodiment, insulating layer 107 is an interlayer dielectric (ILD) layer. In one embodiment, insulating layer 107 is an oxide layer, e.g., a silicon oxide layer. In one embodiment, insulating layer 107 is a low-k dielectric, e.g., silicon dioxide, silicon oxide, carbon doped oxide (“CDO”), or any combination thereof. In one embodiment, insulating layer 107 includes a nitride, oxide, a polymer, phosphosilicate glass, fluorosilicate (“SiOF”) glass, organosilicate glass (“SiOCH”), or any combination thereof. In another embodiment, insulating layer 107 is a nitride layer, e.g., silicon nitride layer. In alternative embodiments, insulating layer 107 is an aluminum oxide, silicon oxide nitride, other oxide/nitride layer, any combination thereof, or other electrically insulating layer determined by an electronic device design.

In one embodiment, the thickness of the insulating layer 107 determines the height of the gate formed later on in a process. In one embodiment, the insulating layer 107 is deposited to the thickness that is similar to the height of the portion 201. In one embodiment, the thickness of the insulating layer 107 is determined by design. In one embodiment, the insulating layer 107 is deposited to the thickness from about 10 nanometers (nm) to about 2 microns (μm). In an embodiment, the insulating layer 107 is deposited on the fin 102 and the exposed portions of the substrate 101 using one of deposition techniques, such as but not limited to a chemical vapour deposition (“CVD”), e.g., a plasma enhanced chemical vapour deposition (“PECVD”), a physical

vapour deposition (“PVD”), molecular beam epitaxy (“MBE”), metalorganic chemical vapor deposition (“MOCVD”), atomic layer deposition (“ALD”), spin-on, or other deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In an embodiment, the insulating layer is recessed to a predetermined thickness to expose device layer 106 on intermediate layer 105 on device layer 104 on intermediate layer 103 using one of etching techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

Figure 2 is a view 200 similar to Figure 1 after a replacement (sacrificial) gate 108 and spacers 109 are formed on the fin 102 according to one embodiment. Figure 2A is a side view 210 of the portion of the electronic device shown in Figure 2 along plane YZ according to one embodiment. Figure 2B is a cross-sectional view 220 of the portion of the electronic device shown in Figure 2 along A-A’ axis. Figure 2C is a cross-sectional view 230 of the portion of the electronic device 100 along B-B’ axis. As shown in Figures 2, 2A, 2B, and 2C, an insulating layer 111 is deposited on the fin 105. An axis C-C’ extends through the gate along the length of the fin 102. Insulating layer 111 is deposited on the top portion and opposing sidewalls of the portion of the fin 102 on which a gate is formed later on in a process. In one embodiment, insulating layer 111 is an oxide layer, e.g., a silicon oxide layer, an aluminum oxide, a carbon doped oxide (e.g., a carbon doped silicon oxide), a carbon layer, or any combination thereof. In one embodiment, the thickness of the insulating layer 111 is from about 2 angstroms (Å) to about 20 Å.

In alternative embodiments, insulating layer 111 is deposited using one of deposition techniques, such as but not limited to, a chemical vapour deposition (“CVD”), e.g., a plasma enhanced chemical vapour deposition (“PECVD”), a physical vapour deposition (“PVD”), molecular beam epitaxy (“MBE”), metalorganic chemical vapor deposition (“MOCVD”), atomic layer deposition (“ALD”), spin-on, or other deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing. Insulating layer 111 is patterned and etched using one or more patterning and etching techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

Replacement gate 108 is formed on the oxide layer 111. In one embodiment, the replacement gate 108 for a stack of at least two transistors or other devices is defined using a single lithographical operation. In one embodiment, replacement gate 108 is a polysilicon gate, or any other replacement gate. In one embodiment, replacement gate 108 is formed by patterning and etching a hard mask 211 on the gate layer (e.g., polysilicon, or other material gate layer) using one or more patterning and etching techniques known to one of ordinary skill in the art of

microelectronic device manufacturing. In alternative embodiments, hard mask 211 is an oxide hard mask, a nitride hard mask, a silicon carbide hard mask, or any other hard mask known to one of ordinary skill in the art of microelectronic device manufacturing. Spacers 109 are formed on the opposite sidewalls of the replacement gate 108 by using one of the spacer deposition techniques known to one of ordinary skill of microelectronic device manufacturing. In one embodiment, spacers 109 are nitride spacers (e.g., silicon nitride), oxide spacers, carbide spacers (e.g., silicon carbide), or other spacers known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, spacers 109 are ultra-low k (k-value less than 2) material spacers.

Figure 3A is a view 310 similar to Figure 2A, Figure 3B is a view 320 similar to Figure 2B, and Figure 3C is a view 330 similar to Figure 2C after portions of the intermediate layers 103 and 105 are removed according to one embodiment. As shown in Figures 3A, 3B, and 3C, the portions of the intermediate layers 103 and 105 outside the replacement gate 108 and spacers 109 are selectively removed to expose portions 311, 312 of the device layer 106 and portions 314 and 313 of device layer 104. In one embodiment, the portions of the intermediate layers 103 and 105 outside the replacement gate 108 and spacers 109 are removed using an isotropic etching technique. In one embodiment, the intermediate layers 103 and 105 of SiGe are wet etched selectively for a predetermined time, in this case, there may be some amount of undercut in the fin region which needs to be controlled. In one embodiment, the intermediate layers 103 and 105 of SiGe are wet etched at an elevated temperature greater than a room temperature. In one embodiment, the portions 311, 312 of the device layer 106 are free standing portions of a nanowire. In one embodiment, the portions 314 and 313 of device layer 104 are free standing portions of a nanowire. In one embodiment, the portions 314 and 313 of device layer 104 represent a nanowire. As shown in Figure 3C, the portions of the intermediate layers 103 and 105 underneath replacement gate 108 and spacers 109 remain substantially intact by etching.

Figure 4A is a view 410 similar to Figure 3A, Figure 4B is a view 420 similar to Figure 3B, and Figure 4C is a view 430 similar to Figure 3C after an insulating layer 411 and a doped layer 412 are deposited according to one embodiment. Insulating layer 411 is deposited on the exposed portions of insulating layer 107 and exposed portions of the base 201. In one embodiment, insulating layer 411 is one of the insulating layers described above with respect to insulating layer 107. In alternative embodiments, the insulating layer 411 is deposited using one or more deposition techniques, such as but not limited to a chemical vapour deposition ("CVD"), e.g., a plasma enhanced chemical vapour deposition ("PECVD"), a physical vapour deposition ("PVD"), molecular beam epitaxy ("MBE"), metalorganic chemical vapor deposition

(“MOCVD”), atomic layer deposition (“ALD”), or other deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the insulating layer 411 is recessed to expose portions 311 and 312 of the device layer 106 outside the gate 108 and spacers 109 to form contact regions. In one embodiment, the portions 311 and 312 are source/drain regions, or other contact regions of the device layer 106. In one embodiment, doped layer 412 is epitaxially grown on the portions 311 and 312. In one embodiment, the concentration of the dopants in the doped layer 412 is greater than in the portions 311 and 312. In one embodiment, the doped layer 412 is an n-type semiconductor layer. In another embodiment, the doped layer 412 is a p-type semiconductor layer. In one embodiment, the doped layer 412 is a silicon layer. In one embodiment, the doped layer 412 is a p-type silicon layer comprising p-type dopants, e.g., boron, aluminum, nitrogen, gallium, indium, or any combination thereof. In one embodiment, the doped layer 412 is an n-type silicon layer comprising n-type dopants, e.g., phosphorous, arsenic, bismuth, lithium, or any combination thereof. In alternative embodiments, the doped layer 412 is a silicon, germanium, silicon germanium, III-V materials based layer, or any combination thereof. In one embodiment, the thickness of the doped layer 412 is from about 10 nm to about 50 nm.

In alternative embodiments, the doped layer 412 is selectively deposited on the exposed portions 311 and 312 using one or more deposition techniques, such as but not limited to a chemical vapour deposition (“CVD”), e.g., a plasma enhanced chemical vapour deposition (“PECVD”), a physical vapour deposition (“PVD”), molecular beam epitaxy (“MBE”), metalorganic chemical vapor deposition (“MOCVD”), atomic layer deposition (“ALD”), or other deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

In one embodiment, the doped layer 412 is annealed at an elevated temperature greater than a room temperature for a predetermined time to drive the dopants into the regions 311 and 312 to form the source/drains. In one embodiment, the doped layer 412 is annealed at the temperature from about 800 degrees C to about 1200 degrees C for about 0.25 seconds or less.

In one embodiment, after the annealing the doped layer 412 is removed using one or more of the doped layer removal techniques such as but not limited to chemical mechanical polishing (CMP), etching, or both.

Figure 5A is a view 510 similar to Figure 3A, Figure 5B is a view 520 similar to Figure 3B, and Figure 5C is a view 530 similar to Figure 3C after depositing insulating layer 411 and adding dopants to the exposed portions 311 and 312 of the device layer 106 to form a source/drain region 511 and a source/drain region 512 according to another embodiment. In one

embodiment, the dopants are added to the exposed portions 311 and 312 using one of implantation techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the dopants added to the exposed portions 311 and 312 are n-type dopants. In another embodiment, the dopants added to the exposed portions 311 and 312 are p-type dopants.

Figure 6A is a view 610 similar to Figure 4A, Figure 6B is a view 620 similar to Figure 4B, and Figure 6C is a view 630 similar to Figure 4C after an insulating layer 611 is deposited on doped layer 412 according to one embodiment. In one embodiment, insulating layer 611 is one of the insulating layers described above with respect to insulating layers 107 and 411. In one embodiment, insulating layer 611 is deposited using one of the techniques described above with respect to insulating layers 107 and 411.

Figure 7A is a cross-sectional view 710 of the portion of the electronic device shown in Figure 6A after removing the replacement gate 108 and depositing a metal gate 721 according to one embodiment. View 710 is the view through the metal gate 721 along the C-C' axis shown in Figure 3. Figure 7B is a view 720 similar to Figure 6B, and Figure 7C is a view 720 similar to Figure 7C after removing the replacement gate 108 and depositing metal gate 721 according to one embodiment. In one embodiment, the hard mask 211 and replacement gate 108 are removed using one of the hard mask and replacement gate removal techniques known to one of ordinary skill in the art of microelectronic device manufacturing. As shown in Figure 7C, the remaining portions of the intermediate layers 103 and 105 are also removed. In one embodiment, the remaining portions of the intermediate layers 103 and 105 are removed using one of the etching techniques, as described above.

As shown in Figures 7A and 7C, metal gate 721 comprises a metal gate 714 on a metal gate 713. Metal gate 714 is deposited on a portion 722 of the device layer 106. Metal gate 713 is deposited on a portion 723 of the device layer 104. As shown in Figure 7C, portion 722 of the device layer 106 has opposing sidewalls 724 and opposing sidewalls 725. Portion 723 of the device layer 104 has opposing sidewalls 726 and opposing sidewalls 727. As shown in Figure 7C, metal gate 714 is deposited on a gate oxide layer 711 on all sidewalls 724 and 725. Metal gate 713 is deposited on a gate oxide layer 712 on all sidewalls 726 and 727. In one embodiment, each of the metal gates 714 and 713 has a work function that corresponds to the transistor body. In one embodiment, the metal of the gate 714 is a p-gate work function metal, e.g., titanium, aluminum, gold, molybdenum, other metal, or other metal alloy having a p-gate work function, and metal of the gate 713 is an n-gate work function metal that includes, e.g., titanium, molybdenum, platinum, other metal, or other metal alloy having a p-gate work function, or vise

versa. In alternative embodiments, metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel, gold, conductive metal oxides, or any combination thereof, are used as n and p gate metals and tungsten is used as a gate fill material. In one embodiment, an actual work function for each of the metal gates is tuned to a p-gate work function or a n-gate work function using a respective combination of metals, metal alloys, or both. In another embodiment, the metal of the gates 714 and 713 is the same. That is, a stack of at least two transistors comprising metal gate 714 on metal gate 713 is formed based on a single fin 102 using a single lithographical operation.

In one embodiment, each of the oxide layers 711 and 712 is a high-k gate oxide layer, e.g., a silicon oxide layer, an aluminum oxide, a carbon doped oxide (e.g., a carbon doped silicon oxide), or any other high-k oxide layer. In one embodiment, the thickness of each of the oxide layers 711 and 712 is from about 2 angstroms (Å) to about 20 Å. In alternative embodiments, each of the oxide layers is deposited using one of the oxide layer deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, metal gate 713 is deposited on the insulating layers 711 and 712. The metal gate 713 is recessed to expose insulating layer 711. In one embodiment, the metal gate 713 is recessed using etching, polishing, or a combination of thereof techniques, e.g., a chemical-mechanical polishing (CMP) technique known to one of ordinary skill in the art of microelectronic device manufacturing. The metal gate 714 is deposited on the recessed metal gate 714 and the exposed insulating layer 711. In one embodiment, each of the metal gates 713 and 714 is deposited using one of the metal gate deposition techniques, e.g., electroplating, electroless plating, or other metal gate forming techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

In one embodiment, the gate oxide includes e.g., titanium (Ti), aluminum (Al), hafnium (Hf), tantalum (Ta), tungsten (W), vanadium (V), molybdenum (Mo), palladium (Pd), gold (Au), silver (Ag), platinum (Pt), copper (Cu), ruthenium (Ru), nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), manganese (Mn), titanium nitride, tantalum nitride, zirconium, tin, lead, metal alloys, metal carbides, e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, aluminum carbide, other metals, or any combination thereof.

Figure 8A is a view 810 similar to Figure 7A, Figure 8B is a view 820 similar to Figure 7B, and Figure 8C is a view 830 similar to Figure 7C after an interconnect layer 821 is deposited on device layer 106 according to one embodiment. Interconnect layer 821 comprises conductive features 811, 812, 813, 815 and 816. A conductive feature 811 connects to a source/drain region 822 of the device layer 106 and a conductive feature 816 connects to a source/drain region 823

of the device layer 106. A conductive feature 812 connects to metal gate 714. In one embodiment, the conductive features 811, 812 and 816 are conductive vias, trenches, or other conductive features to connect the device layer to the features of the interconnect layer 821. Conductive feature 813 connects to conductive feature 811 and conductive feature 812.

- 5 Conductive feature 815 connects to conductive feature 816. In one embodiment, conductive features 813 and 815 are conductive lines. In another embodiment, conductive features 813 and 815 are vias, trenches, or other conductive features. In one embodiment, openings are formed in the insulating layer 611 using the patterning and etching techniques known to one of ordinary skill in the art of microelectronic device manufacturing. One or more conductive layers, e.g., a
- 10 conductive layer on a base layer are deposited to fill the openings in the insulating layer. One of chemical-mechanical polishing (CMP) techniques is used to remove the portions of the one or more conductive layers that extend above the top of the insulating layer 611. The portions of the one or more conductive layers deposited within the openings in the insulating layer 611 are not removed and become the patterned conductive features, such as conductive features 811, 812,
- 15 813, 815 and 816.

In one embodiment, the base layer includes a conductive seed layer deposited on a conductive barrier layer. In alternative embodiments, the seed layer is copper, titanium nitride, ruthenium, nickel, cobalt, tungsten, or any combination thereof. In one embodiment, the conductive barrier layer includes aluminum, titanium, titanium nitride, tantalum, tantalum

20 nitride, tungsten, cobalt, ruthenium, the like metals, or any combination thereof. Generally, the conductive barrier layer is used to prevent diffusion of the conductive material from the seed layer into insulating layer 611 and to provide adhesion for the seed layer. Each of the conductive barrier layer and seed layer may be deposited using any thin film deposition technique known to one of ordinary skill in the art of semiconductor manufacturing, e.g., by sputtering, blanket

25 deposition, and the like. In one embodiment, each of the conductive barrier layer and the seed layer has the thickness in the approximate range of 1 nanometers (nm) to 100 nm. In one embodiment, the barrier layer may be a thin dielectric that has been etched to establish conductivity to the metal layer below. In one embodiment, the barrier layer may be omitted altogether and appropriate doping of the copper line may be used to make a “self-forming

30 barrier”.

In one embodiment, the conductive layer of copper is deposited onto the seed layer of copper by an electroplating process. In another embodiment, the conductive layer is deposited onto the seed layer using one of selective deposition techniques known to one of ordinary skill in the art of semiconductor manufacturing, e.g., electroplating, electroless plating, or the like

techniques. In one embodiment, the choice of a material for the conductive layer determines the choice of a material for the seed layer. For example, if the material for conductive layer includes copper, the material for the seed layer also includes copper. In alternative embodiments, examples of the conductive materials that may be used for the conductive layer to form features 5 811, 812, 813, 815 and 816 include, but are not limited to e.g., copper (Cu), ruthenium (Ru), nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), manganese (Mn), titanium (Ti), aluminum (Al), hafnium (Hf), tantalum (Ta), tungsten (W), vanadium (V), molybdenum (Mo), palladium (Pd), gold (Au), silver (Au), platinum Pt, zirconium, tin, lead, metal alloys, metal carbides, e.g., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, aluminum carbide, other 10 conductive materials, or any combination thereof.

In one embodiment, forming the conductive features 811, 812, 813, 815 and 816 involves removing the portions of the conductive layer and the base layer outside the openings in the insulating layer 611 using etching, polishing, or a combination of thereof techniques, e.g., a chemical-mechanical polishing (CMP) technique known to one of ordinary skill in the art of 15 microelectronic device manufacturing.

Figure 9A is a view 910 similar to Figure 8A, Figure 9B is a view 920 similar to Figure 8B, and Figure 9C is a view 930 similar to Figure 8C after the portion of the electronic device is flipped and bonded to a carrier substrate 911 according to one embodiment. Interconnect layer 821 is attached to carrier substrate 911 to form contact regions on the device layer 104.

20 In various implementations, the substrate 911 can be, e.g., a glass, an organic, a ceramic, or a semiconductor substrate. In one embodiment substrate 911 is one of the substrates described above with respect to substrate 101. In one embodiment, the interconnect layer 821 is attached to carrier substrate using one of substrate bonding techniques, e.g., oxide to oxide bonding, polymer to polymer bonding, metal to metal bonding, nitride to nitride bonding known to one of ordinary 25 skill in the art of microelectronic device manufacturing.

In one embodiment, an adhesion layer (not shown) is deposited on the carrier substrate 911 to bond the carrier substrate to interconnect layer 821. In one embodiment, the adhesive layer comprises organic materials, inorganic materials, or both. In one embodiment, the adhesion layer is an amorphous hydrogenated silicon layer, a carbon doped silicon oxide layer, 30 thermoplastic polymer layer, or any other adhesive material known to one of ordinary skill in the art of microelectronic device manufacturing. In an embodiment, the adhesive layer is blanket deposited on carrier substrate 911 using one of adhesion layer deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

Figure 10A is a view 1010 similar to Figure 9A, Figure 10B is a view 1020 similar to Figure 9B, and Figure 10C is a view 1030 similar to Figure 9C after a gate portion 1012 of device layer 104 is revealed according to one embodiment. In one embodiment, revealing gate portion 1012 involves removing the portions of the fin 102 and substrate 101. In one
5 embodiment, backside substrate 101 is removed using one or more of the substrate removal techniques such as but not limited to CMP, etching, or both. In one embodiment, the portions of the fin 102 are removed using one or more of the substrate removal techniques such as but not limited to grinding, CMP, etching, or any combination thereof. The substrate 101 and portions of the fin 102 are removed to form a backside opening 1011 that exposes a gate portion 1012 of the
10 device layer 104.

Figure 11A is a view 1110 similar to Figure 10A, Figure 11B is a view 1120 similar to Figure 10B, and Figure 11C is a view 1130 similar to Figure 10C after an insulating layer 1113 is deposited onto gate portion 1012 filling the backside opening 1011 according to one embodiment. Backside openings 1111 and 1112 are formed in the insulating layer 1113 to
15 expose portions 1114 and 1115 of the device layer 104 to form contact regions. In one embodiment, insulating layer 1113 is one of the insulating layers described above. In one embodiment, insulating layer 1113 is deposited using one of the insulating layer deposition techniques described above. In one embodiment, openings 1112 and 1112 are formed using one or more of the patterning and etching techniques known to one of ordinary skill in the art of
20 microelectronic device manufacturing.

Figure 12A is a view 1210 similar to Figure 11A, Figure 12B is a view 1220 similar to Figure 11B, and Figure 12C is a view 1230 similar to Figure 11C after a doped layer 1211 is deposited through backside opening 1111 to portion 1114 and through backside opening 1112 to portion 1115 according to one embodiment. In one embodiment, the portions 1114 and 1115 are
25 contact regions of the device layer 104. In one embodiment, the portions 1114 and 1115 are source/drain regions, or other contact regions of the device layer 104. That is, the source/drain portions 1114 and 1115 of the device layer 104 are formed using the backside epitaxial layer processing. As shown in Figures 12A, 12B, and 12C, an insulating layer 1212 comprises insulating layer 107, insulating layer 411 insulating layer 611 and insulating layer 1113.

30 In one embodiment, doped layer 1211 is epitaxially grown on the portions 1114 and 1115. In one embodiment, the concentration of the dopants in the doped layer 1211 is greater than in the portions 1114 and 1115. In one embodiment, the doped layer 1211 is a n-type semiconductor layer. In another embodiment, the doped layer 1211 is a p-type semiconductor layer. In one embodiment, the doped layer 412 is an n-type semiconductor layer, and the doped

layer 1211 is a p-type semiconductor layer, or vice versa. In another embodiment, both the doped layers 412 and 1211 are n-type semiconductor layers, or p-type semiconductor layers. In one embodiment, doped layer 1211 is a silicon layer. In one embodiment, doped layer 1211 is a p-type silicon layer comprising p-type dopants, e.g., boron, aluminum, nitrogen, gallium, indium, other p-type dopants, or any combination thereof. In one embodiment, doped layer 1211 is a n-type silicon layer comprising n-type dopants, e.g., phosphorous, arsenic, bismuth, lithium, other n-type dopants, or any combination thereof. In alternative embodiments, the doped layer 1211 is a silicon, germanium, silicon germanium, III-V materials based layer, or any combination thereof. In one embodiment, the thickness of the doped layer 1211 is from about 10 nm to about 50 nm.

In alternative embodiments, the doped layer 1211 is selectively deposited through the back side openings 1111 and 1112 on the exposed portions 1114 and 1115 of the device layer 104 using one or more deposition techniques, such as but not limited to a chemical vapour deposition (“CVD”), e.g., a plasma enhanced chemical vapour deposition (“PECVD”), a physical vapour deposition (“PVD”), molecular beam epitaxy (“MBE”), metalorganic chemical vapor deposition (“MOCVD”), atomic layer deposition (“ALD”), or other deposition techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

In one embodiment, the doped layer 1211 is annealed at an elevated temperature greater than a room temperature for a predetermined time to drive the dopants into the portions 1114 and 1115 to form the source/drains 1213 and 1214. In one embodiment, the doped layer 1211 is annealed at the temperature from about 800 degrees C to about 1200 degrees C for about 0.25 seconds or less.

In one embodiment, after the annealing the doped layer 1211 is removed using one or more of the doped layer removal techniques such as but not limited to chemical mechanical polishing (CMP), etching, or both. In one embodiment, the annealed doped layer 1211 is removed through the revealed backside.

Figure 13A is a view 1310 similar to Figure 11A, Figure 13B is a view 1320 similar to Figure 11B, and Figure 13C is a view 1330 similar to Figure 11C after adding dopants through backside openings 1111 and 1112 to the exposed portions 1114 and 1115 of the device layer 104 to form a source/drain region 1311 and a source/drain region 1312 according to another embodiment. That is, the source/drain regions 1311 and 1312 are formed through the backside reveal processing.

In one embodiment, the dopants are added to the exposed portions 1114 and 1115 using one of implantation techniques known to one of ordinary skill in the art of microelectronic

device manufacturing. In one embodiment, the dopants added to the exposed portions 1114 and 1115 are n-type dopants, e.g., phosphorous, arsenic, bismuth, lithium, other n-type dopants, or any combination thereof. In another embodiment, the dopants added to the exposed portions 1114 and 1115 are p-type dopants, e.g., boron, aluminum, nitrogen, gallium, indium, other p-type dopants, or any combination thereof.

Figure 14A is a view 1410 similar to Figure 12A, Figure 14B is a view 1420 similar to Figure 12B, and Figure 14C is a view 1430 similar to Figure 12C after an interconnect layer 1414 is deposited on device layer 104 according to one embodiment. Interconnect layer 1414 comprises conductive features 1411, 1412 and 1413. A conductive feature 1411 connects to source/drain 1213 and a conductive feature 1412 connects to source/drain 1214 of the device layer 104. In another embodiment, conductive feature 1411 connects to source/drain 1311 and conductive feature 1412 connects to source/drain 1312 shown in Figures 13A and 13B.

In one embodiment, the conductive features 1411 and 1412 are conductive vias, trenches, or other conductive features to connect the device layer to the features of the interconnect layer 1414. Conductive feature 1413 connects to conductive feature 1411. In one embodiment, conductive feature 1413 is a conductive line. In another embodiment, conductive feature 1413 is a via, trench, or other conductive feature. In one embodiment, each of the conductive features of the interconnect layer 1414 is one of the conductive features described above. In one embodiment, each of the conductive features of the interconnect layer 1414 is formed using one of the conductive features forming techniques described above.

Figure 15 is a three-dimensional view of a portion of an electronic device 1500 according to one embodiment. The embodiment of the device 1500 shown in Figure 15 is different from the Figures 14A, 14B, and 14C in that the interconnect layer 1414 comprises a conductive feature 1501 deposited on metal gate 713 and a conductive feature 1502 deposited on conductive features 1501 and 1412. In one embodiment, the conductive feature 1501 is a conductive via, trench, or other conductive features to connect the gate 713 to the features of the interconnect layer 1414. In one embodiment, conductive feature 1502 is a conductive line. In another embodiment, conductive feature 1502 is a via, trench, or other conductive feature. In one embodiment, each of the conductive features of the interconnect layer 1414 is one of the conductive features described above. In one embodiment, each of the conductive features of the interconnect layer 1414 is formed using one of the conductive features forming techniques described above.

Figure 16A is a view 1610 similar to Figure 12A, Figure 16B is a view 1620 similar to Figure 12B, and Figure 16C is a view 1630 similar to Figure 12C after a spacer layer 1612 is

deposited on a sidewall of the opening 1111 according to one embodiment. Figure 16A is different Figure 12A in that the insulating layer 1113 is deposited on the source/drain 1214. As shown in Figures 16A and 16B, spacer layer 1612 is deposited to narrow the opening 1111, so that an opening 1614 is formed. The opening 1614 is formed down to source/drain 1213. The width of the opening 1614 is smaller than the width of the opening 1111. In one embodiment, spacer layer 1612 is one of the spacer layers described above. In one embodiment, spacer layer 1612 is deposited using one of the spacer deposition techniques described above.

In another embodiment, insulating layer 1113 is deposited on source/drain 1213, gate portion 1012 and source/drain 1214, and opening 1614 is formed by patterning and etching insulating layer 1113. In one embodiment, opening 1614 is formed to connect source/drain regions of the device layer 106 with the source/drain region of the device layer 104.

Figure 17A is a view 1710 similar to Figure 16A, Figure 17B is a view 1720 similar to Figure 16B, and Figure 17C is a view 1730 similar to Figure 16C after an opening 1711 is formed through the device layers 104 and 106 down to conductive feature 811 according to one embodiment. In one embodiment, opening 1711 is formed by etching portions of insulating layer 411 and portions of device layers 104 and 106 using one or more etching techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

Figure 18A is a view 1810 similar to Figure 17A, Figure 18B is a view 1820 similar to Figure 17B, and Figure 18C is a view 1830 similar to Figure 17C after the spacer layer 1612 is removed, and a conductive feature 1811 is deposited into the opening in the insulating layer according to one embodiment. As shown in Figures 18A, 18B, and 18C, a conductive feature 1812 is deposited on metal gate 713. In one embodiment, an opening is formed in insulating layer 1212 to expose metal gate 713 using one of the etching techniques described above. In one embodiment, the conductive layer 1812 is deposited on the exposed metal gate 713 through the opening in the insulating layer 1212.

In one embodiment, the spacer layer 1612 is removed using one of the spacer layer removal techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, each of the conductive features 1811 and 1812 is represented by one of the conductive features described above. In one embodiment, each of the conductive features 1811 and 1812 is deposited using one of the conductive features deposition techniques described above.

Figure 19A is a view 1910 similar to Figure 16A, Figure 19B is a view 1920 similar to Figure 16B, and Figure 19C is a view 1930 similar to Figure 16C after a conductive feature 1912 and a conductive feature 1912 are deposited according to another embodiment. In one

embodiment, the source/drain regions 1311 and 1312 are the source/drain regions formed using the implantation technique, as described with respect to Figures 13A, 13B, and 13C. In one embodiment, the source/drain regions 1311 and 1312 represent source/drain regions 1213 and 1214 respectively. In one embodiment, an opening in the insulating layer 1212 is formed to
5 expose source/drain region 1311 and source/drain region 511. In one embodiment, the opening is formed by etching the insulating layer 1212 selectively to the device layers 106 and 104 to expose source/drain region 1311 and source/drain region 511. In one embodiment, a spacer layer is deposited to narrow the opening in the insulating layer, as described above with respect to Figures 16A, 16B, and 16C. In one embodiment, a portion 1917 of the conductive feature 1911
10 is deposited through the narrowed opening in the insulating layer 1212 onto exposed sidewalls 1913 and 1914 of the source/drain region 1311 and onto the exposed sidewall 1915 of the source/drain region 511. In one embodiment, the spacer layer is removed, and then a portion 1916 of the conductive feature 1911 that fills the opening in the insulating layer 1212 is deposited on the portion 1917. As shown in Figures 19A, 19B, and 19C, conductive feature 1912
15 is deposited on metal gate 713.

In one embodiment, the opening in insulating layer 1212 is formed using one of the etching techniques described above. In one embodiment, the spacer layer is removed using one of the spacer layer removal techniques as described above. In one embodiment, each of the conductive features 1911 and 1912 is one of the conductive layers described above. In one
20 embodiment, each of the conductive features 1911 and 1912 is deposited using one of the conductive feature deposition techniques described above.

Figure 20A is a view 2010 similar to Figure 6A, Figure 20B is a view 2020 similar to Figure 6B, and Figure 20C is a view 2030 similar to Figure 6C after interconnect layer 821 is deposited on device layer 106 according to another embodiment. Figures 20A, 20B, 20C are
25 different from Figures 8A, 8B, and 8C in that the metal gate 713 is deposited on oxide layer 711 on all sidewalls 724 and 725 of the portion 722 of the device layer 106 and is deposited on oxide layer 712 on all sidewalls 726 and 727 of the portion 723 of the device layer 104.

Figure 21A is a view 2110 similar to Figure 20A, Figure 21B is a view 2120 similar to Figure 20B, and Figure 21C is a view 2130 similar to Figure 20C after the portion of the
30 electronic device is flipped and bonded to carrier substrate 911 and the portions of the fin 102 and substrate 101 are removed according to another embodiment. In one embodiment, the portion of the electronic device is flipped and bonded to carrier substrate, as described above with respect to Figures 9A, 9B, and 9C. The substrate 101 and portions of the fin 102 are removed to form a backside opening 2111 that exposes a portion of gate 713. In one

embodiment, the portions of the fin 102 and substrate 101 are removed, as described above with respect to Figures 10A, 10B, and 10C.

Figure 22A is a view 2210 similar to Figure 21A, Figure 22B is a view 2220 similar to Figure 21B, and Figure 22C is a view 2230 similar to Figure 21C after an insulating layer 2211 is deposited onto the exposed gate portion 713 according to another embodiment. In one embodiment, insulating layer 2211 is one of the insulating layers described above. In one embodiment, insulating layer 2211 is a part of the insulating layer 1212. Backside openings 2212 and 2213 are formed in the insulating layer 2211 to expose portions of the device layer 104 to form contact regions, as described above with respect to Figures 11A, 11B, and 11C. A doped layer 1211 is deposited through backside openings 2212 and 2213 to the exposed portions of the device layer 104 to form source/drain regions 1213 and 1214, as described above with respect to Figures 11A, 11B and 11C. In another embodiment, source/drain regions 1213 and 1214 represent source/drain regions 1311 and 1312 described with respect to Figures 13A, 13B, and 13C.

Figure 23A is a view 2310 similar to Figure 22A, Figure 23B is a view 2320 similar to Figure 22B, and Figure 23C is a view 2330 similar to Figure 22C after a conductive feature 2311 and a conductive feature 2312 are deposited onto source/drain regions 1213 and 1214 according to another embodiment. In one embodiment, each of the conductive features 2311 and 2312 is deposited as described above with respect to Figures 14A, 14B, and 14C.

Figure 24A is a view 2410 similar to Figure 23A, Figure 24B is a view 2420 similar to Figure 23B, and Figure 24C is a view 2430 similar to Figure 23C after an opening 2411 is formed in insulating layer 2211 to expose a portion of gate 713 according to another embodiment. In one embodiment, opening 2411 is formed using one of the patterning and etching techniques known to one of ordinary skill in the art of microelectronic device manufacturing.

Figure 25A is a view 2510 similar to Figure 24A, Figure 25B is a view 2520 similar to Figure 24B, and Figure 25C is a view 2530 similar to Figure 24C after a backside opening 2411 in insulating layer 2211 is formed according to another embodiment. A portion of gate 713 is removed through the backside opening 2411 to expose a portion 2511 of metal gate 713. In one embodiment, opening 2411 is formed using one of the patterning and etching techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the portion of the gate 713 is removed to expose the oxide layer 712 on the sidewalls 726 and 727 of the gate portion 723 of the device layer 104. The oxide layer 711 on the gate portion 722 of the device layer 106 is underneath the portion 2511 of the metal gate 713.

Figure 26A is a view 2610 similar to Figure 25A, Figure 26B is a view 2620 similar to Figure 25B, and Figure 26C is a view 2630 similar to Figure 25C after an insulating layer 2611 is deposited on portion 2511 of metal gate 713 according to another embodiment. In one embodiment, the insulating layer 2611 is one of the insulating layers described above. In more specific embodiment, the insulating layer 2611 is one of the oxide layers described above. In one embodiment, the thickness of the insulating layer 2611 is from about 2 angstroms (Å) to about 200 Å. In one embodiment, the insulating layer 2611 is deposited using one of the insulating layer deposition techniques described above, e.g., a spin-coating technique. In one embodiment, the insulating layer 2611 is recessed to form a gap 2612 between the insulating layer 2611 and oxide layer 712 on the bottom of the portion 723 of the device layer 104. In one embodiment, the insulating layer 2611 is recessed using one or more of the CMP and etching techniques, as described above.

Figure 27A is a view 2710 similar to Figure 26A, Figure 27B is a view 2720 similar to Figure 26B, and Figure 27C is a view 2730 similar to Figure 26C after a metal gate 2711 is deposited on insulating layer 2611 according to another embodiment. In another embodiment, the insulating layer 2611 is not deposited, and metal gate 2711 is deposited directly on portion 2511 of metal gate 713. In one embodiment, metal gate 2711 is represented by metal gate 714.

Figure 28A is a view 2810 similar to Figure 27A, Figure 28B is a view 2820 similar to Figure 27B, and Figure 28C is a view 2830 similar to Figure 27C after a conductive feature 2811 is deposited to contact metal gate 2711 according to another embodiment. In one embodiment, conductive feature 2811 is represented by conductive feature 1501.

Figure 29 illustrates an interposer 2900 that includes one or more embodiments of the invention. The interposer 2900 is an intervening substrate used to bridge a first substrate 2902 to a second substrate 2904. The first substrate 2902 may be, for instance, an integrated circuit die. The second substrate 2904 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 2900 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 2900 may couple an integrated circuit die to a ball grid array (BGA) 2906 that can subsequently be coupled to the second substrate 2904. In some embodiments, the first and second substrates 2902/2904 are attached to opposing sides of the interposer 2900. In other embodiments, the first and second substrates 2902/2904 are attached to the same side of the interposer 2900. And in further embodiments, three or more substrates are interconnected by way of the interposer 2900.

The interposer 2900 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer may include metal interconnects 2908, vias 2910, including but not limited to through-silicon vias (TSVs) 2912. The interposer 2900 may further include embedded devices 2914, including passive and active devices. Such devices include, but are not limited to, stacked transistors or other stacked devices as described above, e.g., capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices, radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors and MEMS devices. In accordance with embodiments of the invention, apparatuses or processes disclosed herein may be used in the fabrication of interposer 2900.

Figure 30 illustrates a computing device 3000 in accordance with one embodiment of the invention. The computing device 3000 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in the computing device 3000 include, but are not limited to, an integrated circuit die 3002 and at least one communication chip 3008. In some implementations the communication chip 3008 is fabricated as part of the integrated circuit die 3002. The integrated circuit die 3002 may include a processor 3004 such as a central processing unit (CPU), an on-die memory 3006, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

Computing device 3000 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, a volatile memory 3010 (e.g., DRAM), a non-volatile memory 3012 (e.g., ROM or flash memory), a graphics processing unit 3014 (GPU), a digital signal processor 3016 (DSP), a crypto processor 3042 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 3020, an antenna 3022, a display or a touchscreen display 3024, a touchscreen display controller 3026, a battery 3028 or other power source, a global positioning system (GPS) device 3044, a power amplifier (PA), a compass, a motion coprocessor or sensors 3032 (that may include an accelerometer, a gyroscope, and a compass), a speaker 3034, a camera 3036, user input devices 3038 (such as a keyboard,

mouse, stylus, and touchpad), and a mass storage device 3040 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 3008 enables wireless communications for the transfer of data to and from the computing device 3000. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 3008 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 3000 may include a plurality of communication chips 3008. For instance, a first communication chip 3008 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 3008 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. One or more components e.g., integrated circuit die 3002, communication chip 3008, GPU 3014, cryptoprocessor 3042, DSP 3016, chipset 3020, and other components may include one or more stacked transistors, or other stacked devices formed in accordance with embodiments of the invention. In further embodiments, another component housed within the computing device 3000 may contain one or more stacked transistors, or other stacked devices formed in accordance with embodiments of the invention.

In various embodiments, the computing device 3000 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 3000 may be any other electronic device that processes data.

The above description of illustrated implementations of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise

forms disclosed. While specific implementations of, and examples for the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

These modifications may be made to the invention in light of the above detailed
5 description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

The following examples pertain to further embodiments:

10 In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the
15 second device layer; and forming a contact region on the exposed first portion of the second device layer.

In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device
20 layer from the second substrate side that comprises removing at least a portion of the second substrate; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; and forming a contact region on the exposed first portion of the second device layer.

In one embodiment, a method to manufacture an electronic device comprises bonding a
25 first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; forming a contact region on the exposed first portion of the second device
30 layer; and depositing a conductive layer on the contact region.

In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second

device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; and forming a contact region on the exposed first portion of the second device layer, wherein forming the contact region comprises depositing a doped layer on the exposed first portion.

5 In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the
10 second device layer; and forming a contact region on the exposed first portion of the second device layer, wherein forming the contact region comprises depositing a doped layer on the exposed first portion; and annealing the doped layer.

 In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a
15 first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; and forming a contact region on the exposed first portion of the second device layer, wherein forming the contact region comprises depositing a doped layer on the
20 exposed first portion, and removing the doped layer.

 In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second
25 device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; and forming a contact region on the exposed first portion of the second device layer, wherein forming the contact region comprises adding a dopant to the exposed first portion using an implantation technique.

 In one embodiment, a method to manufacture an electronic device comprises bonding a
30 first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; forming a contact region on the exposed first portion of the second device

layer; depositing a second insulating layer on the contact region; forming an opening in the second insulating layer to expose a portion of the contact region; and depositing a spacer layer onto a sidewall of the opening.

5 In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; forming a contact region on the exposed first portion of the second device layer; depositing a second insulating layer on the contact region; forming an opening in the second insulating layer to expose a portion of the contact region; depositing a spacer layer onto a sidewall of the opening; etching the source/drain region to expose a portion the first interconnect layer; and depositing a conductive layer onto the exposed portion of the first interconnect layer.

10 In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; forming a contact region on the exposed first portion of the second device layer; depositing a second insulating layer on the contact region; forming an opening in the second insulating layer to expose a portion of the contact region; depositing a spacer layer onto a sidewall of the opening; depositing a conductive layer onto the contact region; a second opening in the second insulating layer to expose a gate portion of the second device layer, the gate portion of the second device layer comprising a first metal layer.

25 In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; forming a contact region on the exposed first portion of the second device layer; forming a second opening in the first insulating layer to expose a gate portion of the second device layer, the gate portion of the second device layer comprising a first metal layer; recessing the first metal layer to expose a gate portion of the first device layer; depositing a third

metal layer onto the gate portion of the first device layer, wherein the third metal layer is different from the first metal layer; and depositing a conductive layer onto the third metal layer.

In one embodiment, a method to manufacture an electronic device comprises bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing the second device layer from the second substrate side; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; and forming a contact region on the exposed first portion of the second device layer; forming a second opening in the first insulating layer to expose a gate portion of the second device layer, the gate portion of the second device layer comprising a first metal layer; and depositing a third insulating layer on the exposed gate portion of the first device layer.

In one embodiment, a method to manufacture an electronic device comprises forming a fin on a first substrate, the fin comprising a first device layer on a second device layer, wherein a first intermediate layer is deposited between the first device layer and the second device, and wherein a first interconnect layer is deposited on the first device layer; bonding the first interconnect layer to a second substrate; removing the first substrate; depositing a first insulating layer on the revealed second device layer; forming a first opening in the first insulating layer to expose a first portion of the second device layer; and forming a contact region on the exposed first portion of the second device layer.

In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a backside substrate; forming a first source/drain region on the first transistor layer; forming an interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; and forming a second source/drain region on the second transistor layer.

In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a backside substrate; forming a first gate on the fin; forming a spacer on the first gate; forming a first source/drain region on the first transistor layer; replacing the first gate with a second gate; forming an interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; forming a second source/drain region on the second transistor layer.

In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a

backside substrate; removing the first intermediate layer; forming a first source/drain region on the first transistor layer; forming an interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; and forming a second source/drain region on the second transistor layer.

5 In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a backside substrate; forming a first source/drain region on the first transistor layer; forming an interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; depositing an insulating layer on the second
10 transistor layer; forming an opening in the insulating layer; forming a second source/drain region on the second transistor layer through the opening.

 In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a backside substrate; forming a first source/drain region on the first transistor layer; forming an
15 interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; forming a second source/drain region on the second transistor layer; depositing an insulating layer on the second transistor layer; forming an opening in the insulating layer; and depositing a spacer layer onto a sidewall of the opening

 In one embodiment, a method to manufacture stacked transistors comprises forming a fin
20 comprising a first transistor layer on a first intermediate layer on a second transistor layer on a backside substrate; forming a first source/drain region on the first transistor layer; forming an interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; forming a second source/drain region on the second transistor layer; and depositing a conductive layer on the second source/drain region.

25 In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a backside substrate; forming a first source/drain region on the first transistor layer; forming an interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; and forming a second source/drain region on
30 the second transistor layer, wherein forming the second source/drain region comprises depositing a doped layer.

 In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a backside substrate; forming a first source/drain region on the first transistor layer; forming an

interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; and forming a second source/drain region on the second transistor layer, wherein forming the second source/drain region comprises adding a dopant using an implantation technique.

5 In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a backside substrate; forming a first source/drain region on the first transistor layer; forming an interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; forming a second source/drain region on the
10 second transistor layer; etching the second source /drain region to expose a portion the interconnect layer; and depositing a conductive layer onto the exposed portion of the first interconnect layer.

In one embodiment, a method to manufacture stacked transistors comprises forming a fin comprising a first transistor layer on a first intermediate layer on a second transistor layer on a
15 backside substrate; forming a first source/drain region on the first transistor layer; forming an interconnect layer to connect to the source/drain region; bonding the interconnect layer to a carrier substrate; removing the backside substrate; forming a second source/drain region on the second transistor layer; depositing an insulating layer on the second transistor layer; forming an opening in the insulating layer to expose a gate portion of the second transistor layer; and
20 depositing a conductive layer on the gate portion.

In one embodiment, an electronic device comprises a first transistor layer on a second transistor layer; a first interconnect layer to connect to a first source/drain region on the first transistor layer; a first gate on the first transistor layer; and a second interconnect layer to connect to a second source/drain region on the second transistor layer.

25 In one embodiment, an electronic device comprises a first transistor layer on a second transistor layer; a first interconnect layer to connect to a first source/drain region on the first transistor layer; a first gate on the first transistor layer; a second gate on the second transistor layer; and a second interconnect layer to connect to a second source/drain region on the second transistor layer.

30 In one embodiment, an electronic device comprises a first transistor layer on a second transistor layer; a first interconnect layer to connect to a first source/drain region on the first transistor layer; a first gate on the first transistor layer; and a second interconnect layer to connect to a second source/drain region on the second transistor layer, wherein a portion of the

first interconnect layer is extended through the first source/drain region to connect to the second source/drain region.

In one embodiment, an electronic device comprises a first transistor layer on a second transistor layer; a first interconnect layer to connect to a first source/drain region on the first transistor layer; a first gate on the first transistor layer; and a second interconnect layer to connect to a second source/drain region on the second transistor layer, wherein a portion of the first interconnect layer wraps around the first source/drain region to connect to the second source/drain region.

In one embodiment, an electronic device comprises a first transistor layer on a second transistor layer; a first interconnect layer to connect to a first source/drain region on the first transistor layer; a first gate on the first transistor layer; and a second interconnect layer to connect to a second source/drain region on the second transistor layer, wherein the first gate is on the second transistor layer.

In one embodiment, an electronic device comprises a first transistor layer on a second transistor layer; a first interconnect layer to connect to a first source/drain region on the first transistor layer; a first gate on the first transistor layer; and a second interconnect layer to connect to a second source/drain region on the second transistor layer, wherein the first gate comprises a metal.

In one embodiment, an electronic device comprises a first transistor layer on a second transistor layer; a first interconnect layer to connect to a first source/drain region on the first transistor layer; a first gate on the first transistor layer; a second interconnect layer to connect to a second source/drain region on the second transistor layer; and an insulating layer underneath the first gate.

In one embodiment, an electronic device comprises a first transistor layer on a second transistor layer; a first interconnect layer to connect to a first source/drain region on the first transistor layer; a first gate on the first transistor layer; and a second interconnect layer to connect to a second source/drain region on the second transistor layer, wherein the first transistor layer on the second transistor layer are a part of a fin.

In the foregoing specification, methods and apparatuses have been described with reference to specific exemplary embodiments thereof. It will be evident that various modifications may be made thereto without departing from the broader spirit and scope of embodiments as set forth in the following claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method to manufacture an electronic device, comprising:
 - 5 bonding a first interconnect layer to a first substrate, wherein the first interconnect layer is deposited on a first device layer on a second device layer on a second substrate; revealing at least a portion of the second device layer from the second substrate side;
 - depositing a first insulating layer on the revealed second device layer;
 - 10 forming a first opening in the first insulating layer to expose a first portion of the second device layer; and
 - forming a contact region on the exposed first portion of the second device layer.
2. The method of claim 1, wherein the revealing comprises removing at least a portion of the second substrate.
- 15 3. The method of claim 1, further comprising depositing a conductive layer on the contact region.
4. The method of claim 1, wherein forming the contact region comprises depositing a doped layer on the exposed first portion.
5. The method of claim 1, wherein forming the contact region comprises
 - 20 adding a dopant to the exposed first portion using an implantation technique.
6. The method of claim 1, further comprising
 - depositing a second insulating layer on the contact region;
 - forming an opening in the second insulating layer to expose a portion of the contact region; and
 - 25 depositing a spacer layer onto a sidewall of the opening.
7. The method of claim 1, further comprising
 - forming a second opening in the first insulating layer to expose a gate portion of the second device layer, the gate portion of the second device layer comprising a first metal layer.
- 30 8. The method of claim 1, further comprising
 - forming a fin on the second substrate, the fin comprising the first device layer on the second device layer, wherein a first intermediate layer is deposited between the first device layer and the second device layer;
 - forming a gate on the fin; and

forming a contact region on the first device layer.

9. An electronic device comprising:

a first transistor layer on a second transistor layer;

a first interconnect layer to connect to a first source/drain region on the first transistor layer;

a first gate on the first transistor layer; and

a second interconnect layer to connect to a second source/drain region on the second transistor layer.

10. The electronic device of claim 15, further comprising

a second gate on the second transistor layer.

11. The electronic device of claim 15, wherein a portion of the first interconnect layer is extended through the first source/drain region to connect to the second source/drain region.

12. The electronic device of claim 15, wherein a portion of the first interconnect layer wraps around the first source/drain region to connect to the second source/drain region.

13. The electronic device of claim 15, wherein the first gate is on the second transistor layer.

14. The electronic device of claim 15, further comprising

an insulating layer underneath the first gate.

15. The electronic device of claim 24, wherein the first transistor layer on the second transistor layer are a part of a fin.

16. An electronic device, comprising

a fin including a first transistor layer on a top portion of a second transistor layer;

a first source/drain region on the first transistor layer;

a first interconnect layer to connect to the first source/drain region;

and

a second source/drain region on a bottom portion of the second transistor layer, wherein the bottom portion of the second transistor layer is further away from the first transistor layer than the top portion.

17. The electronic of claim 16, further comprising

a second interconnect layer underneath the second transistor layer to connect to the second source/drain region.

18. The electronic device of claim 16, further comprising

a gate on the fin to connect to at least one of the first transistor layer and the second transistor layer.

19. The electronic device of claim 16, wherein a portion of the first interconnect layer is extended through the first source/drain region to connect to the second source/drain region.

5 20. The electronic device of claim 16, wherein a portion of the first interconnect layer wraps around the first source/drain region to connect to the second source/drain region.

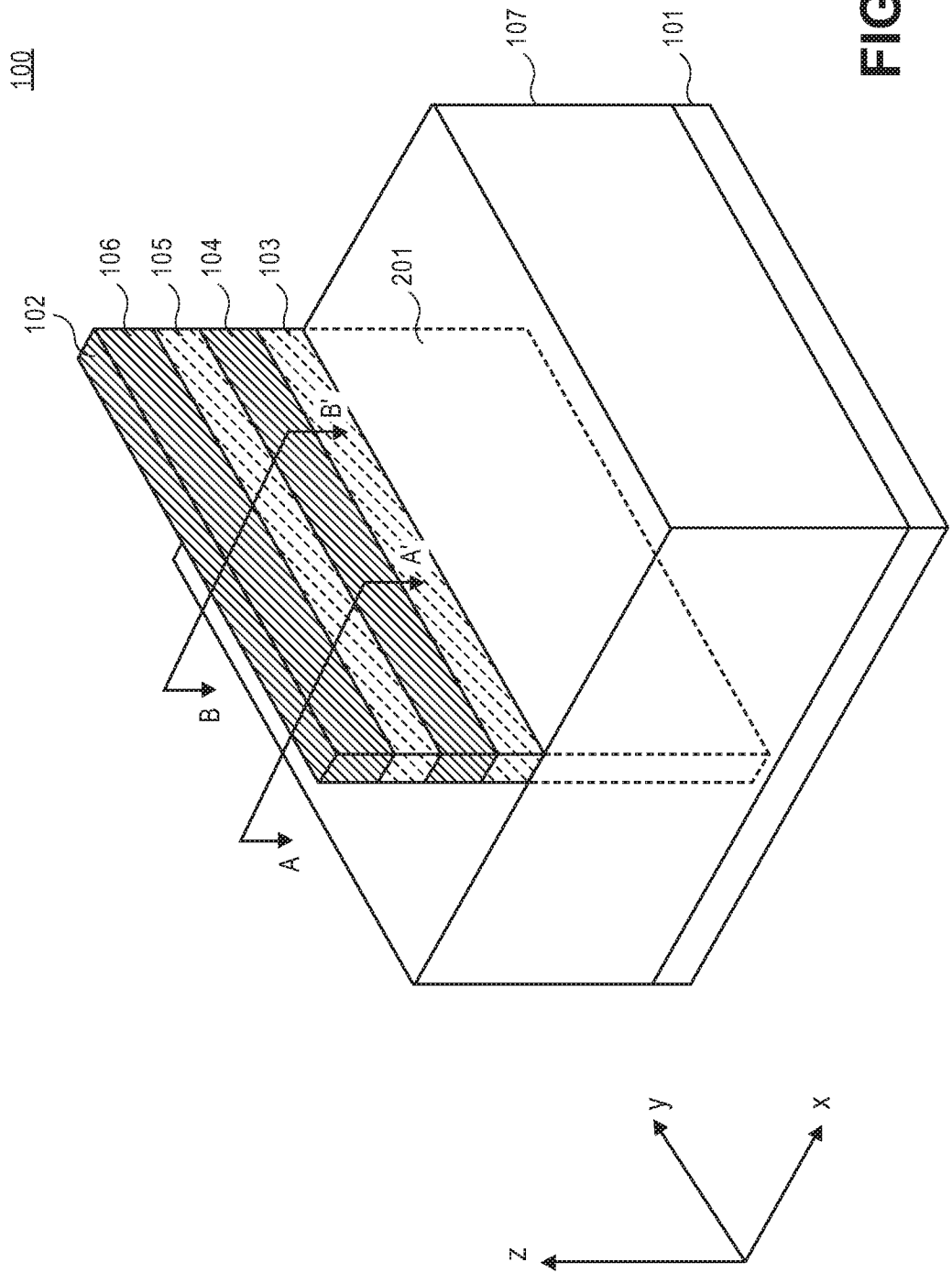


FIG. 1

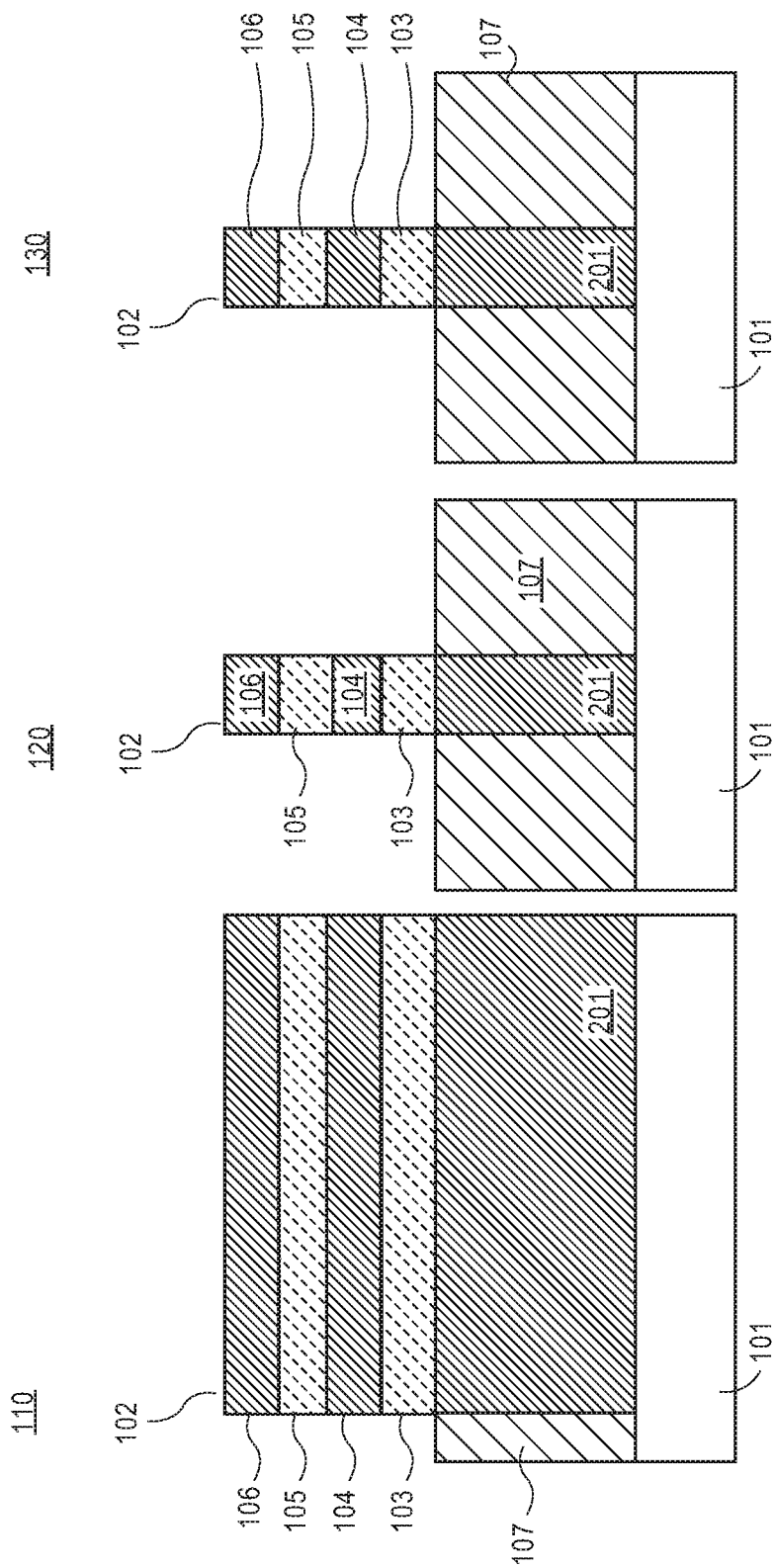


FIG. 1C

FIG. 1B

FIG. 1A

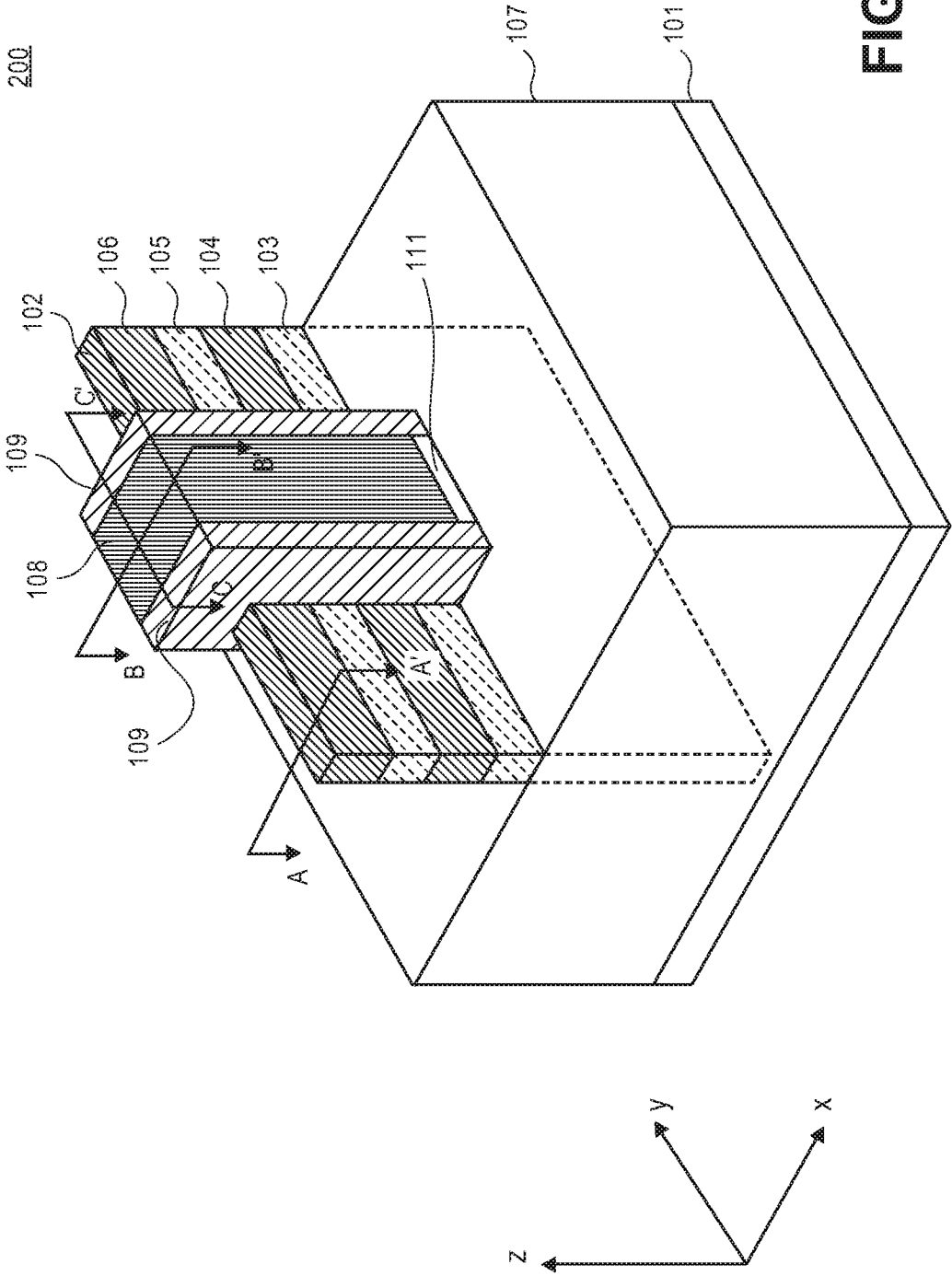


FIG. 2

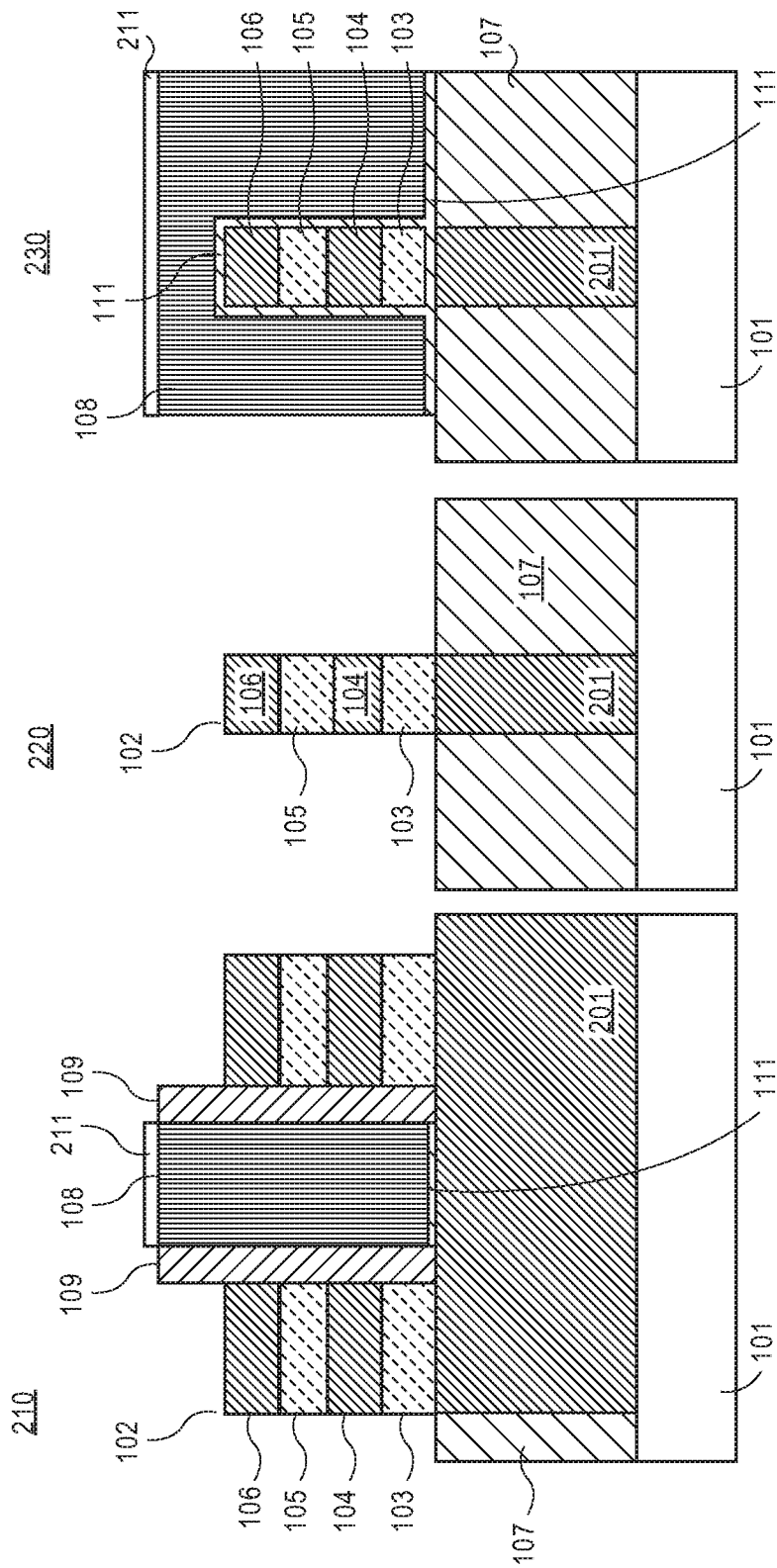
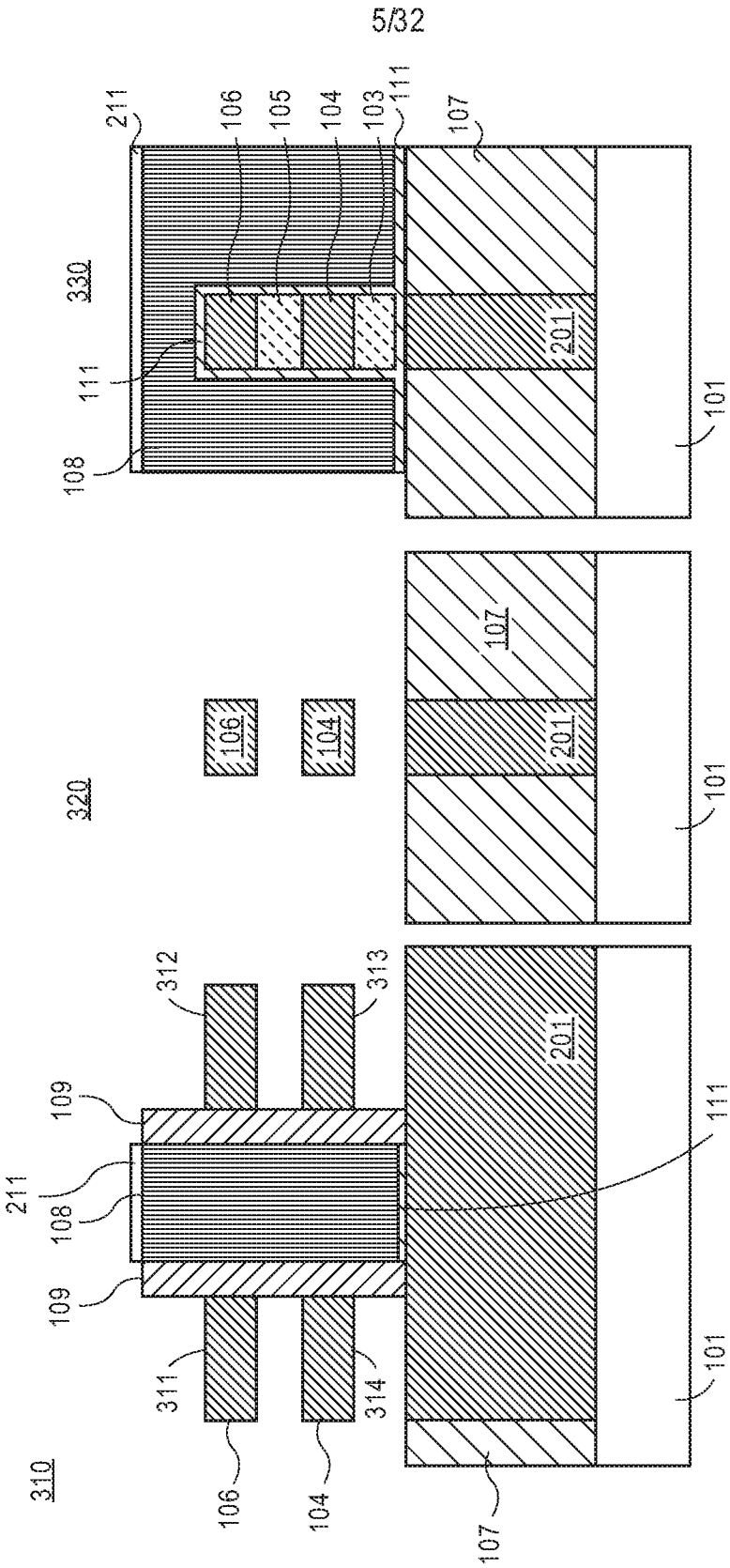


FIG. 2C

FIG. 2B

FIG. 2A



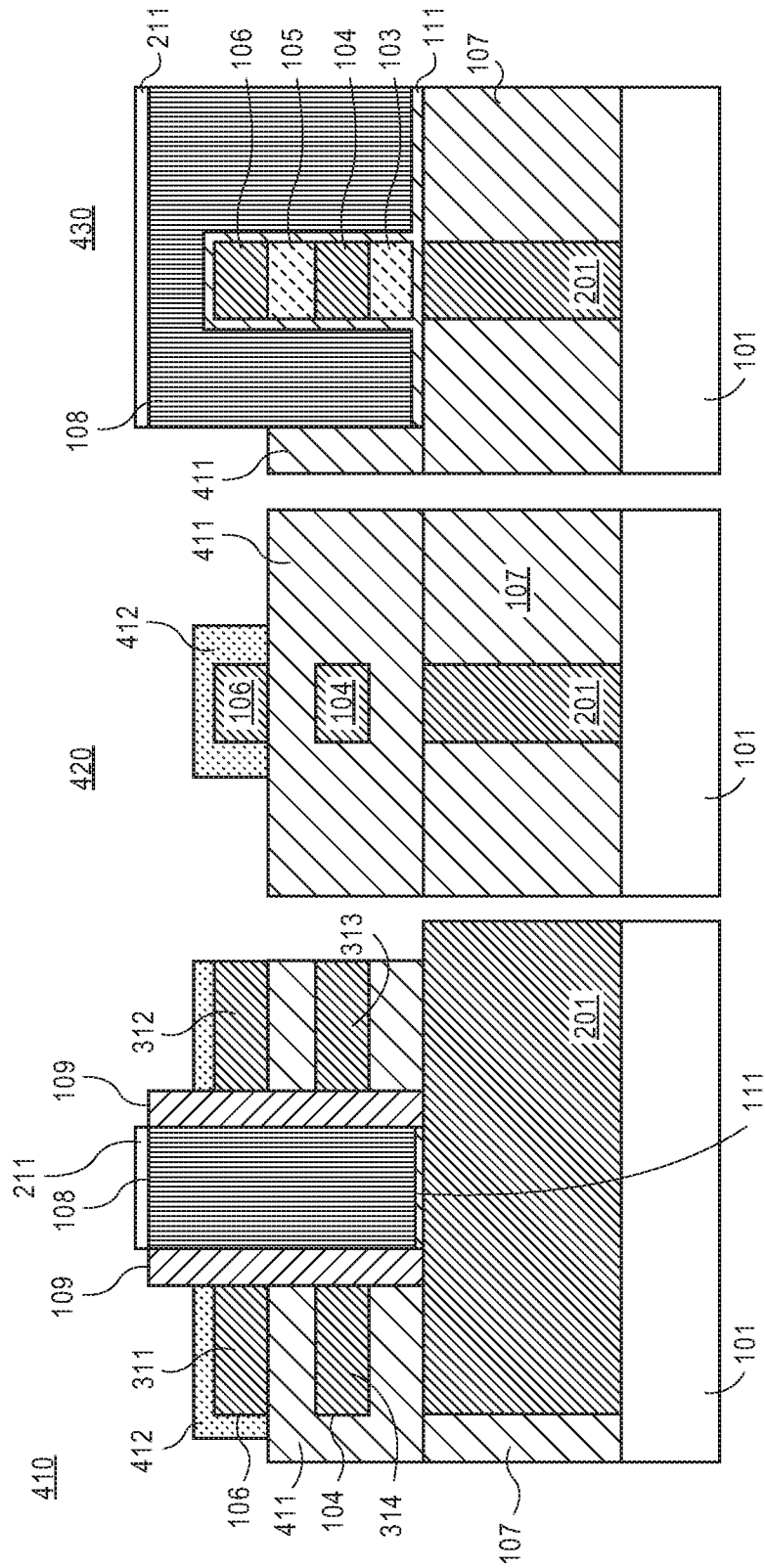


FIG. 4C

FIG. 4B

FIG. 4A

7/32

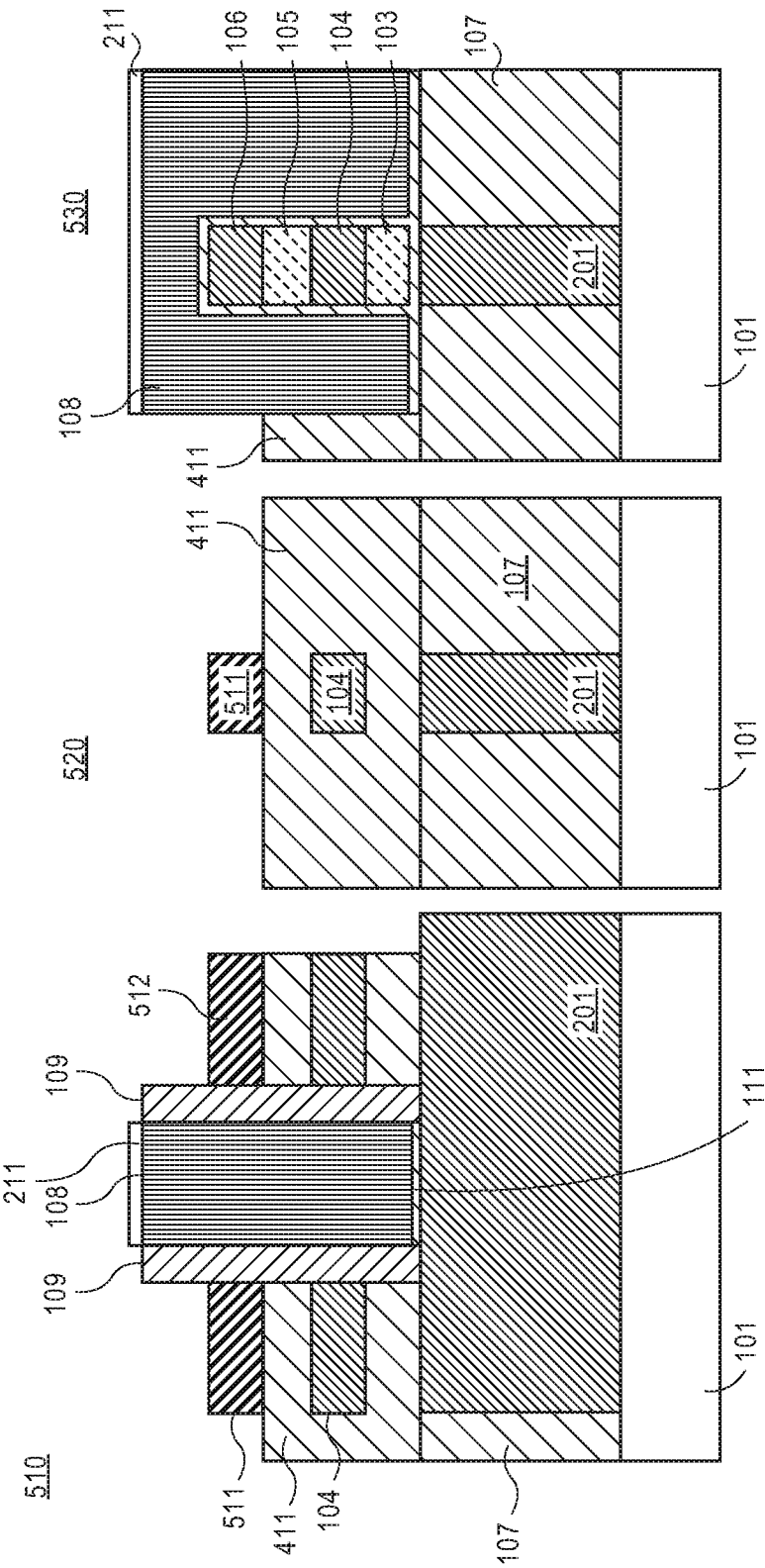


FIG. 5C

FIG. 5B

FIG. 5A

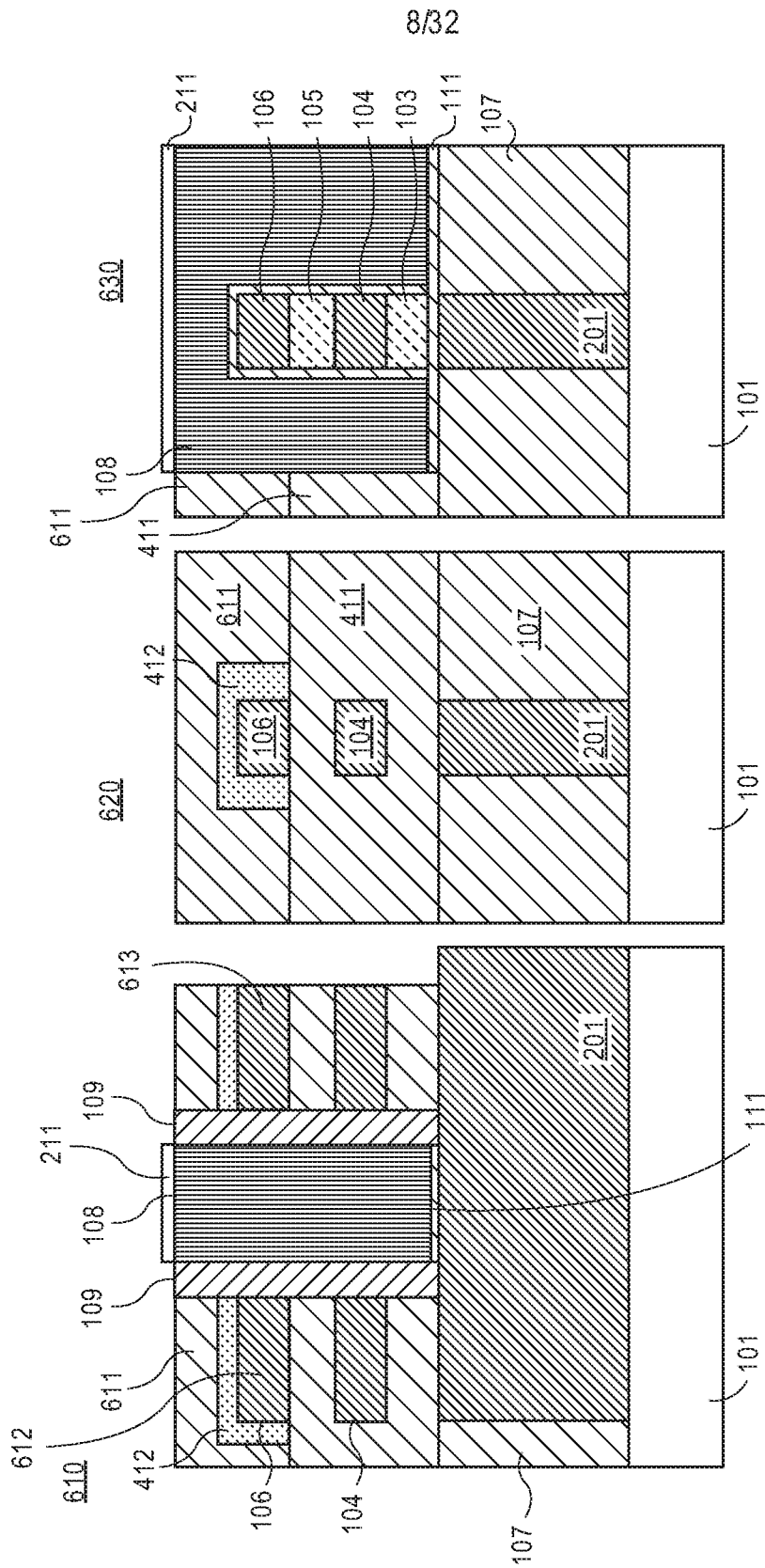


FIG. 6C

FIG. 6B

FIG. 6A

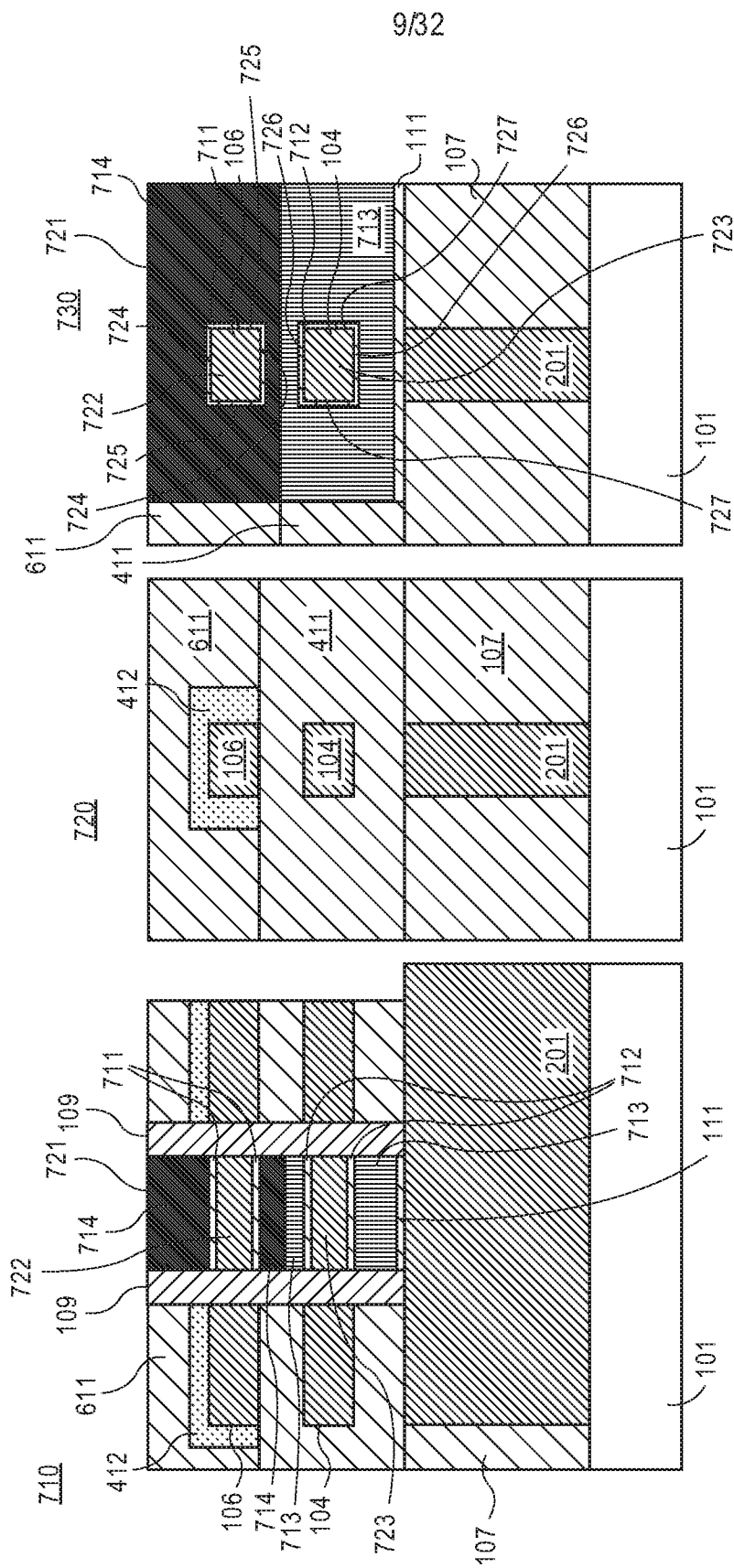


Fig. 7C

FIG. 2

FIG. 7A

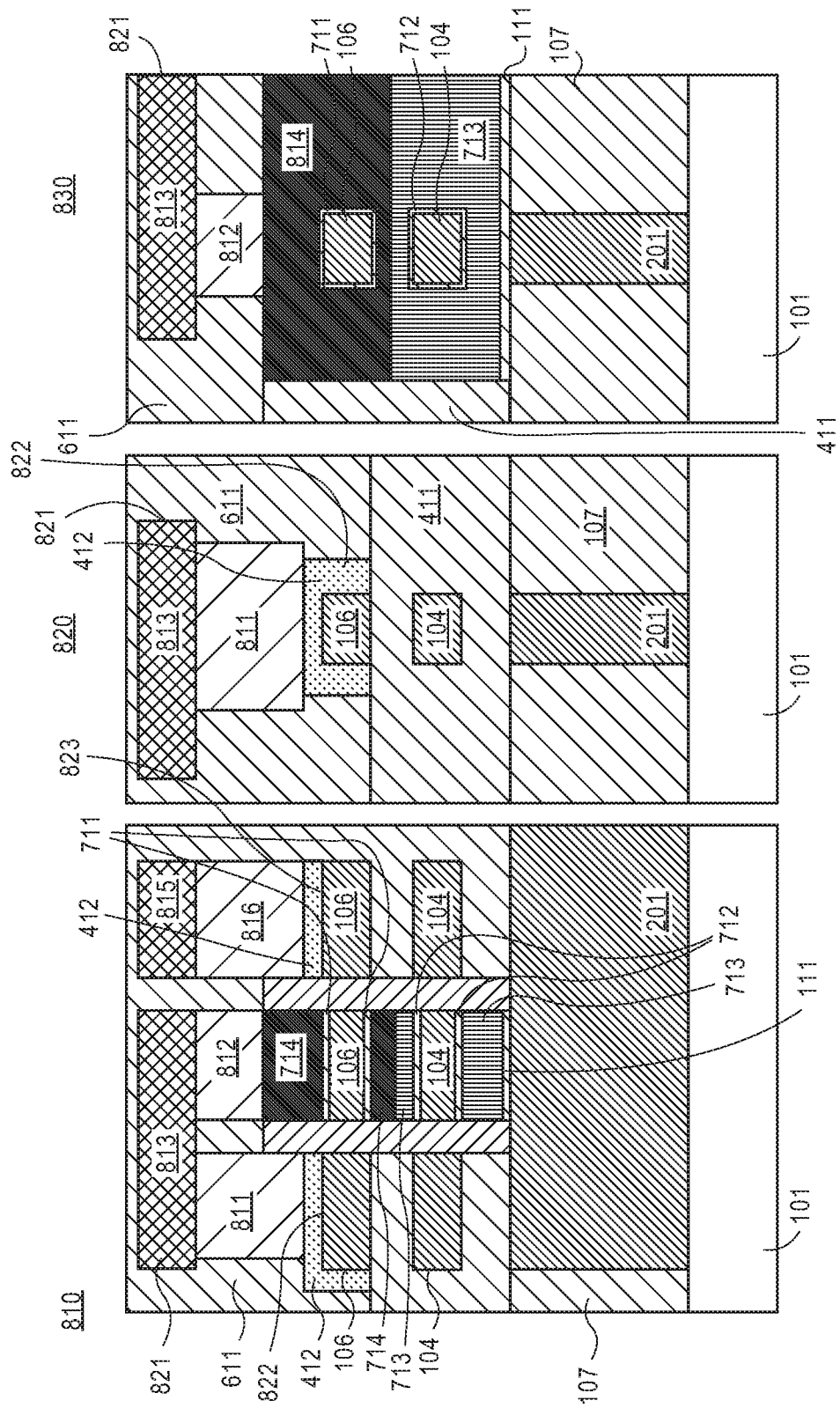
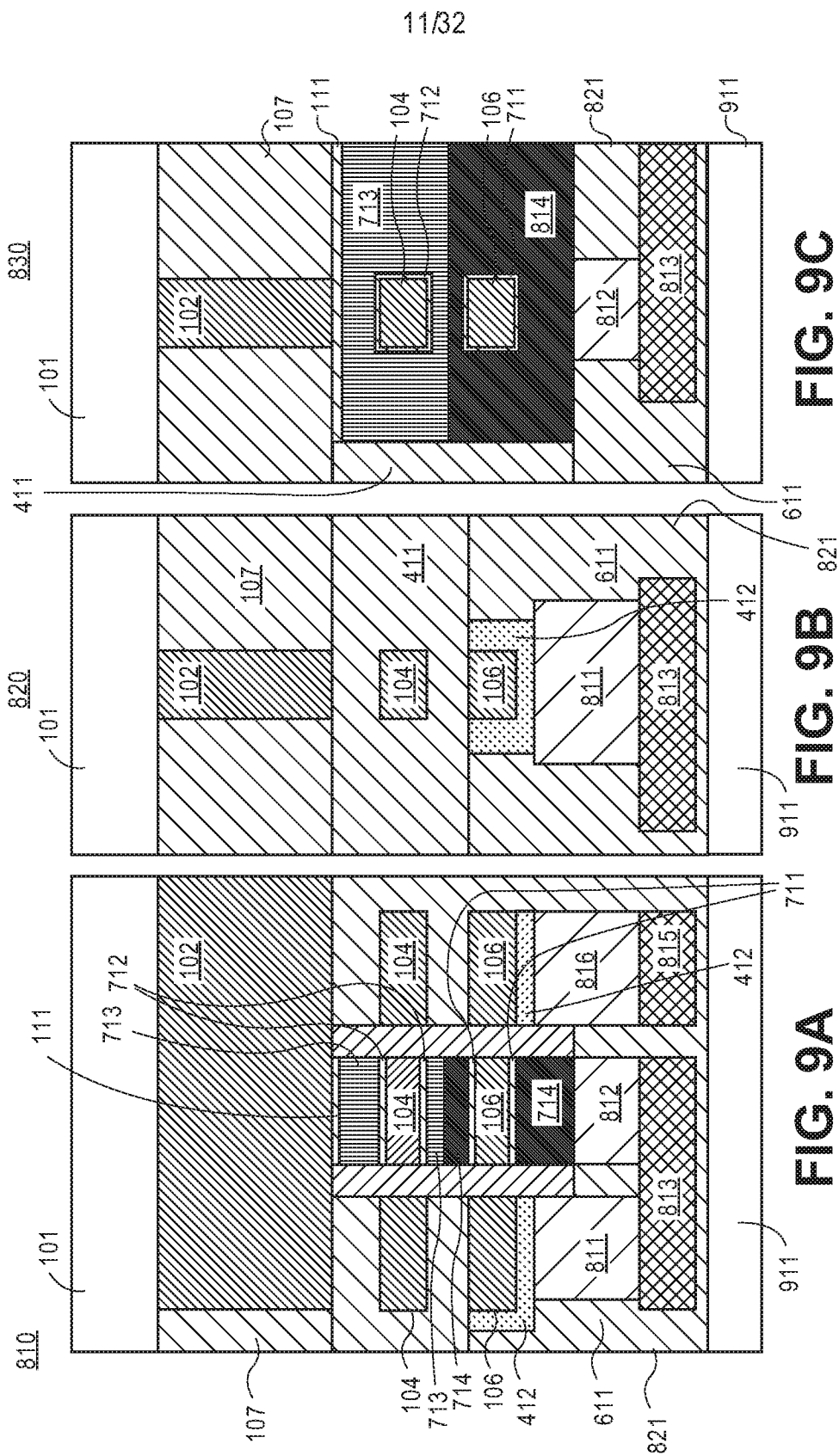


FIG. 8C

FIG. 8B

FIG. 8A



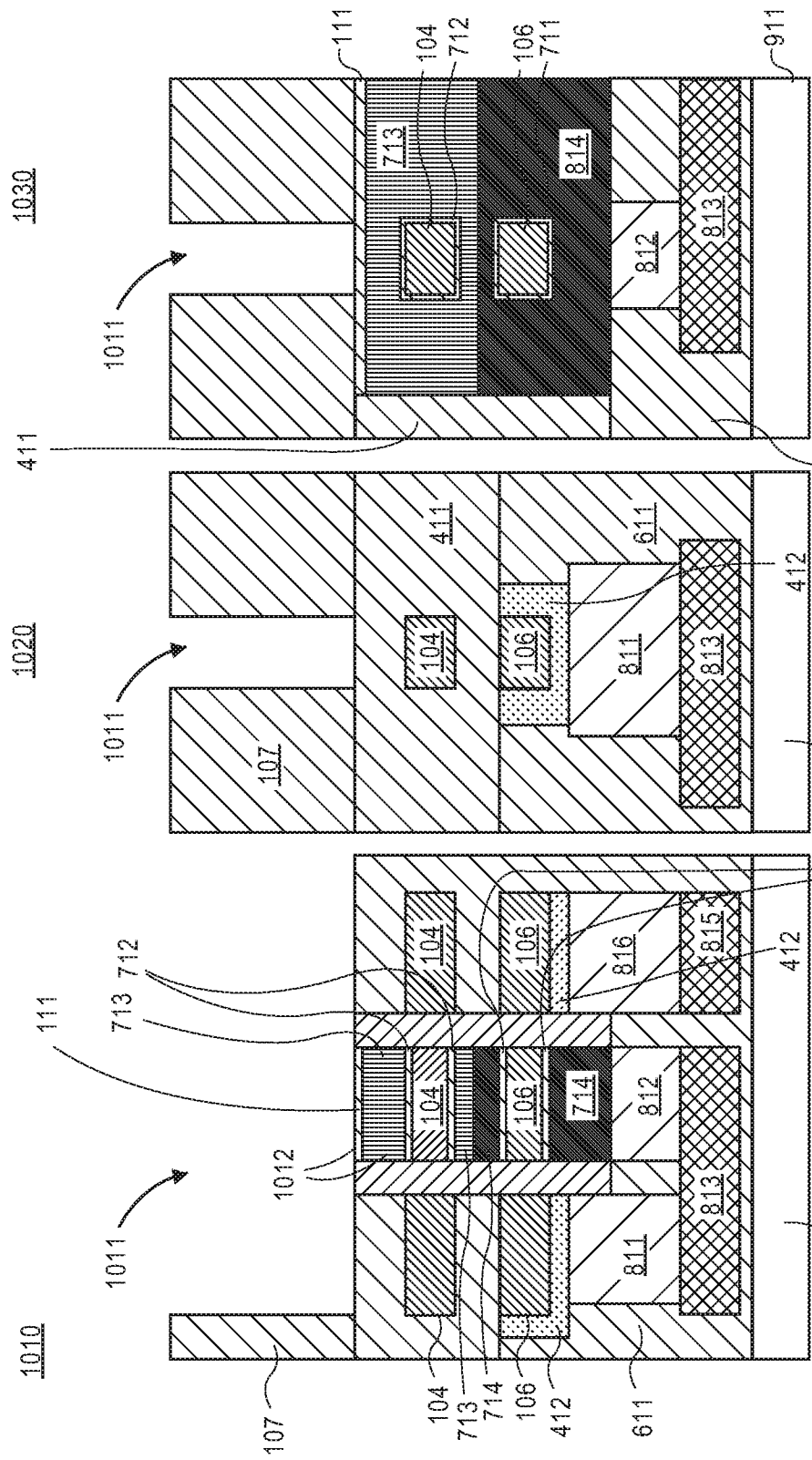
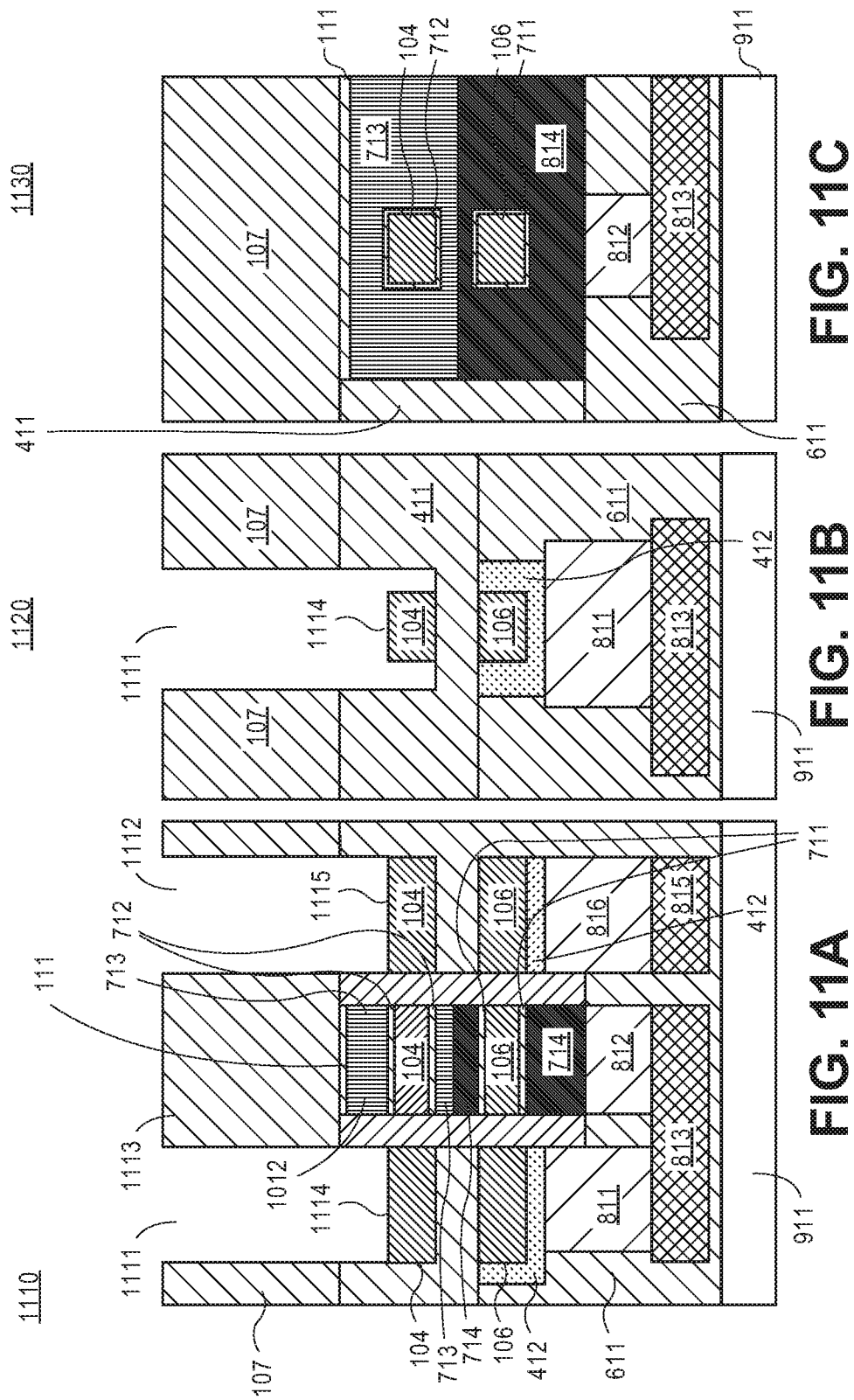


FIG. 10C

FIG. 10B

FIG. 10A

13/32



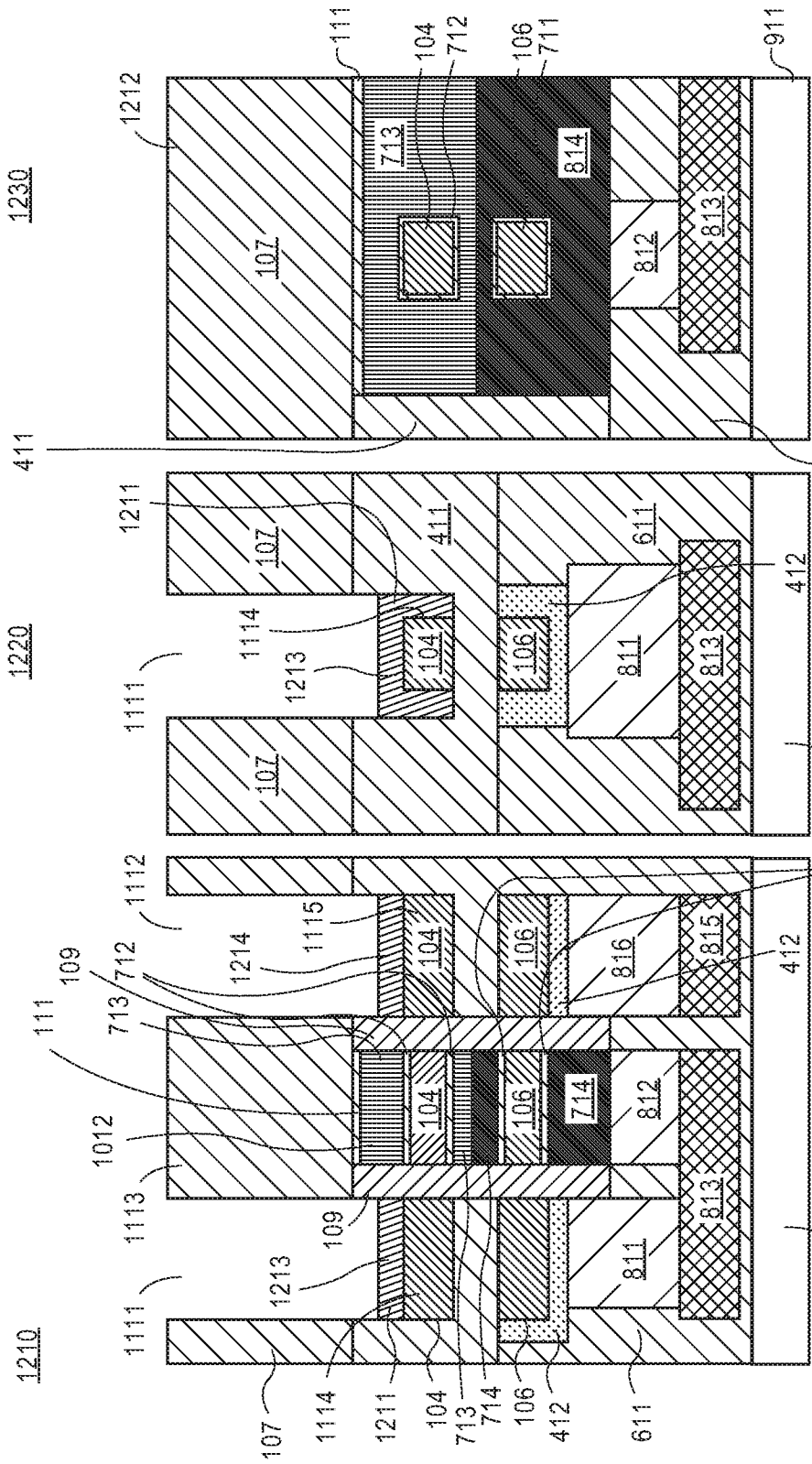
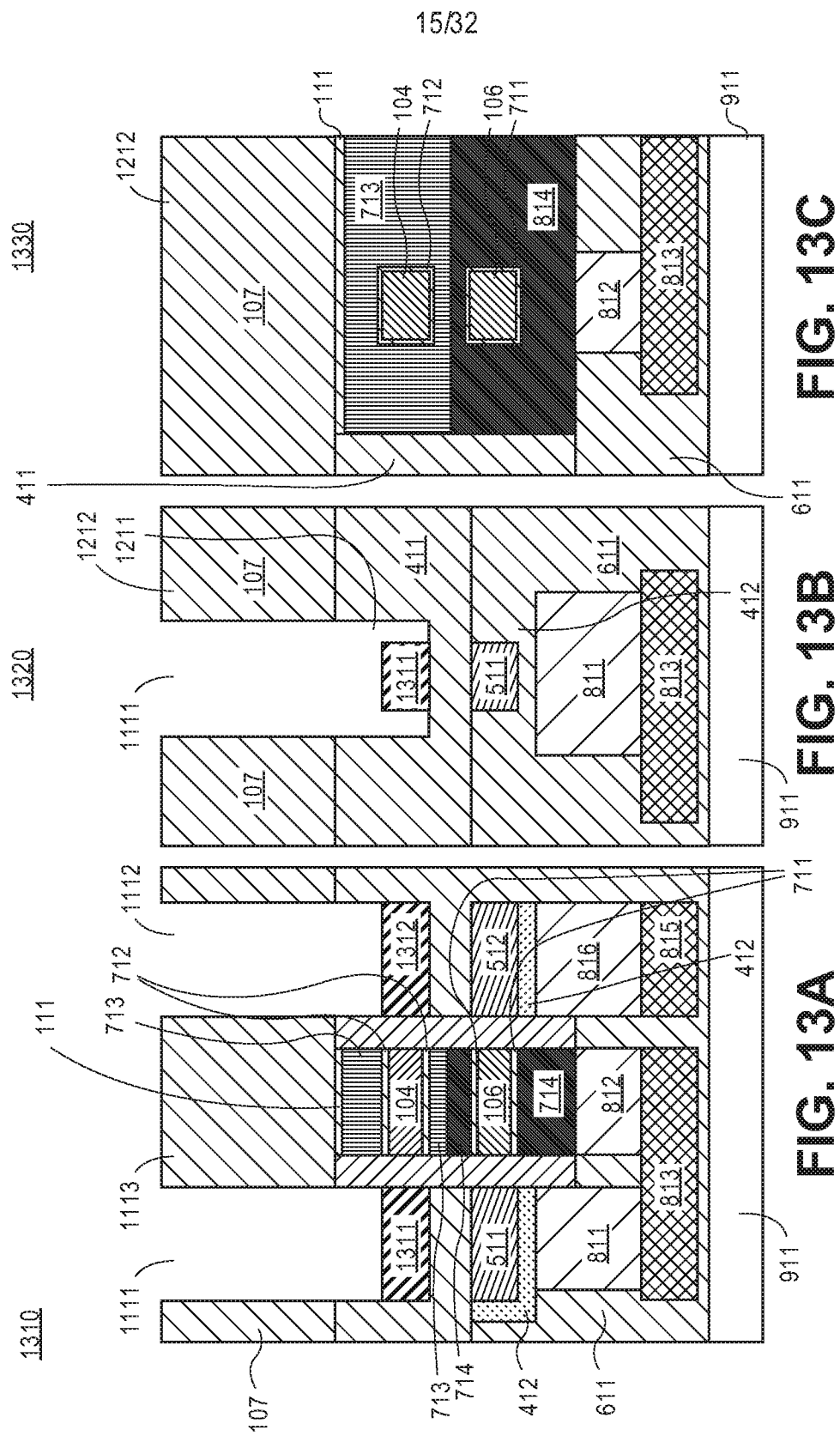
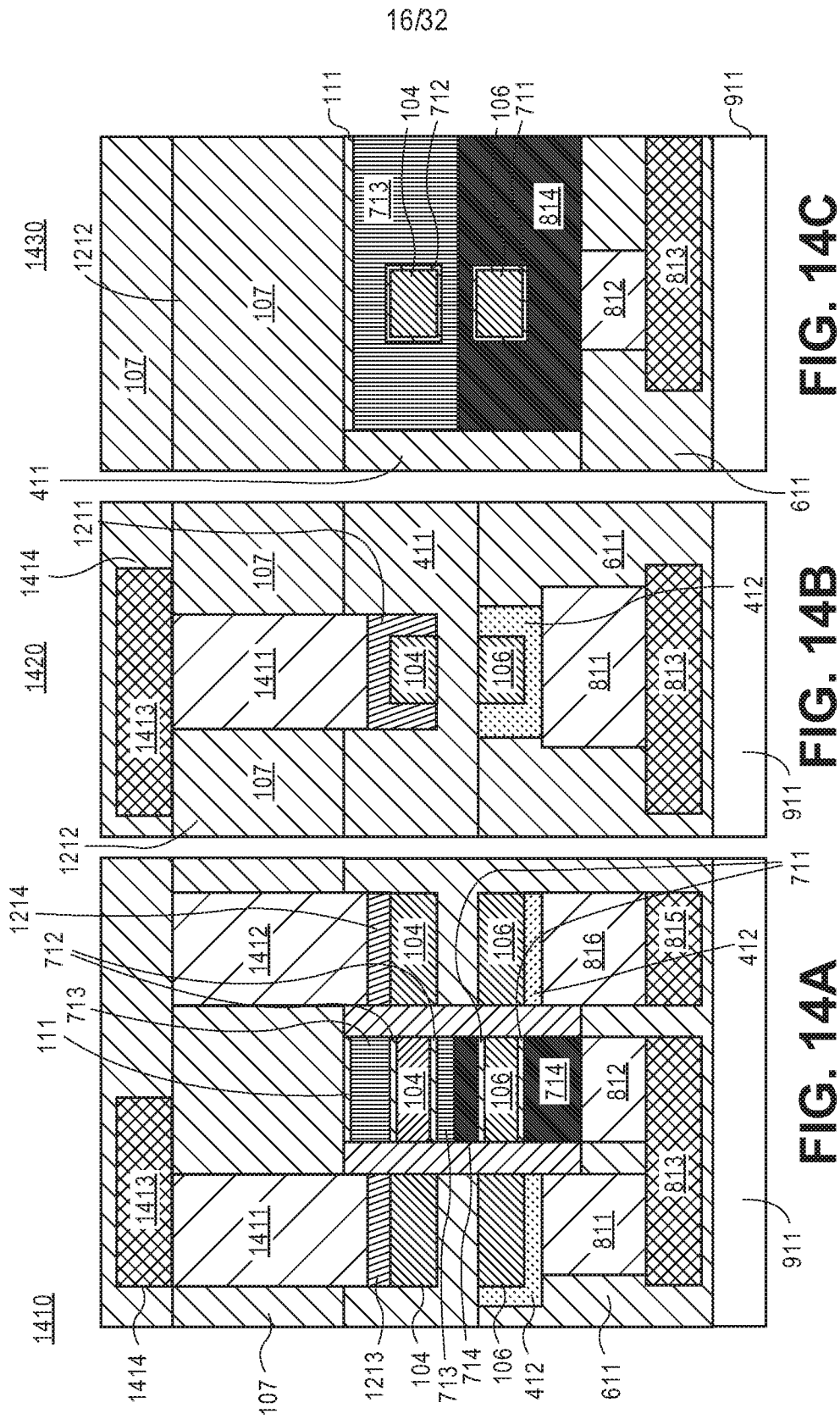


FIG. 12C

FIG. 12B

FIG. 12A





17/32

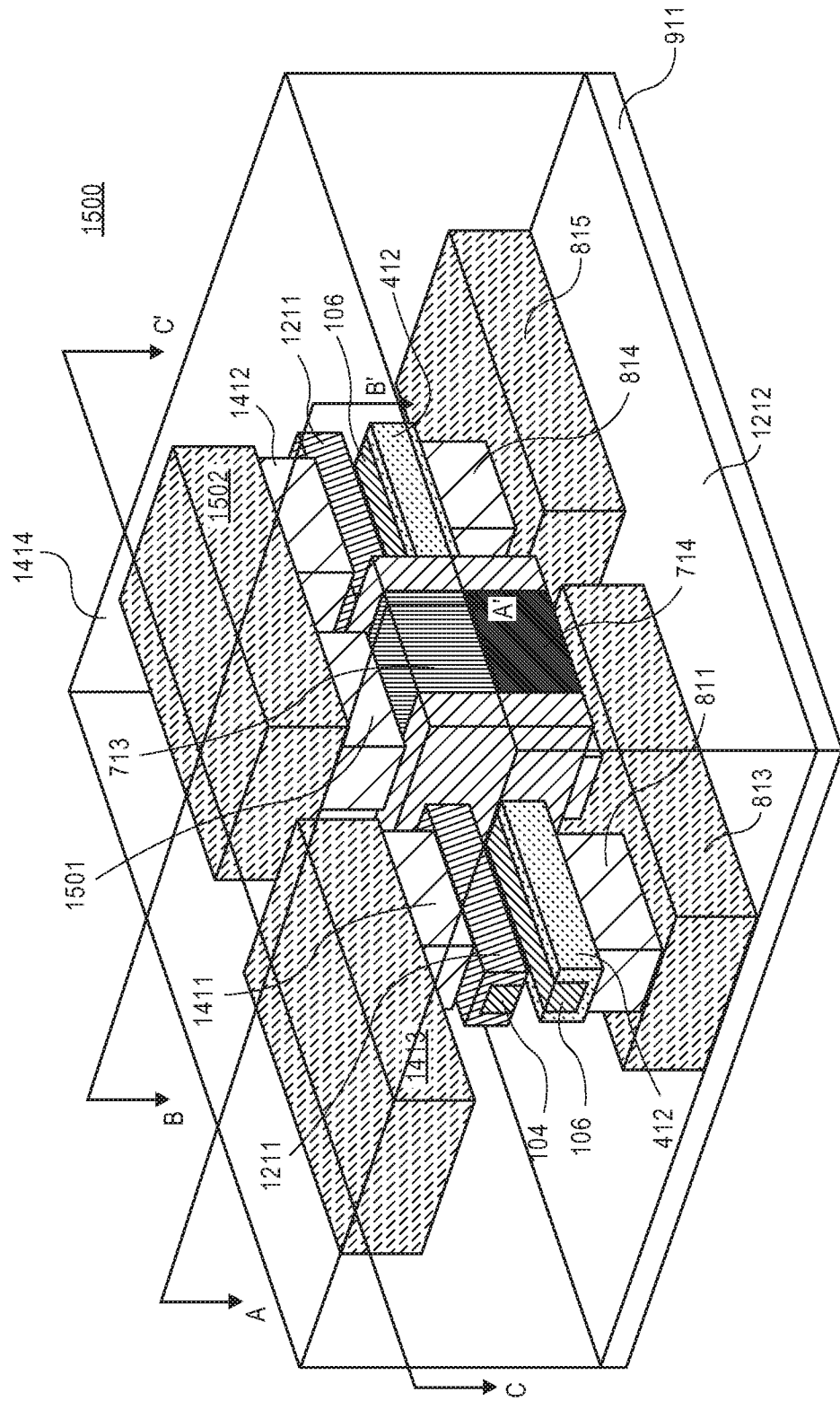


FIG. 15

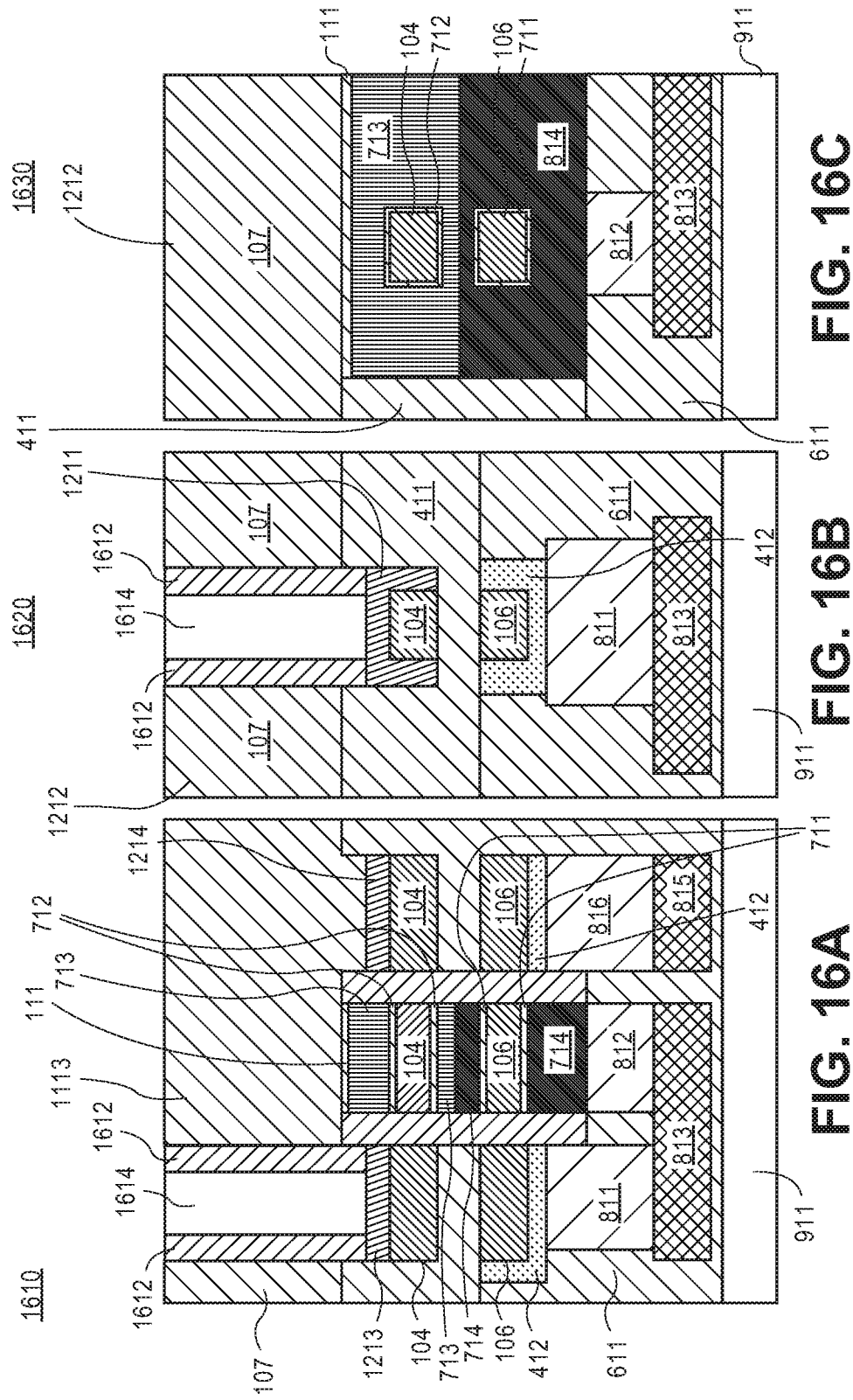
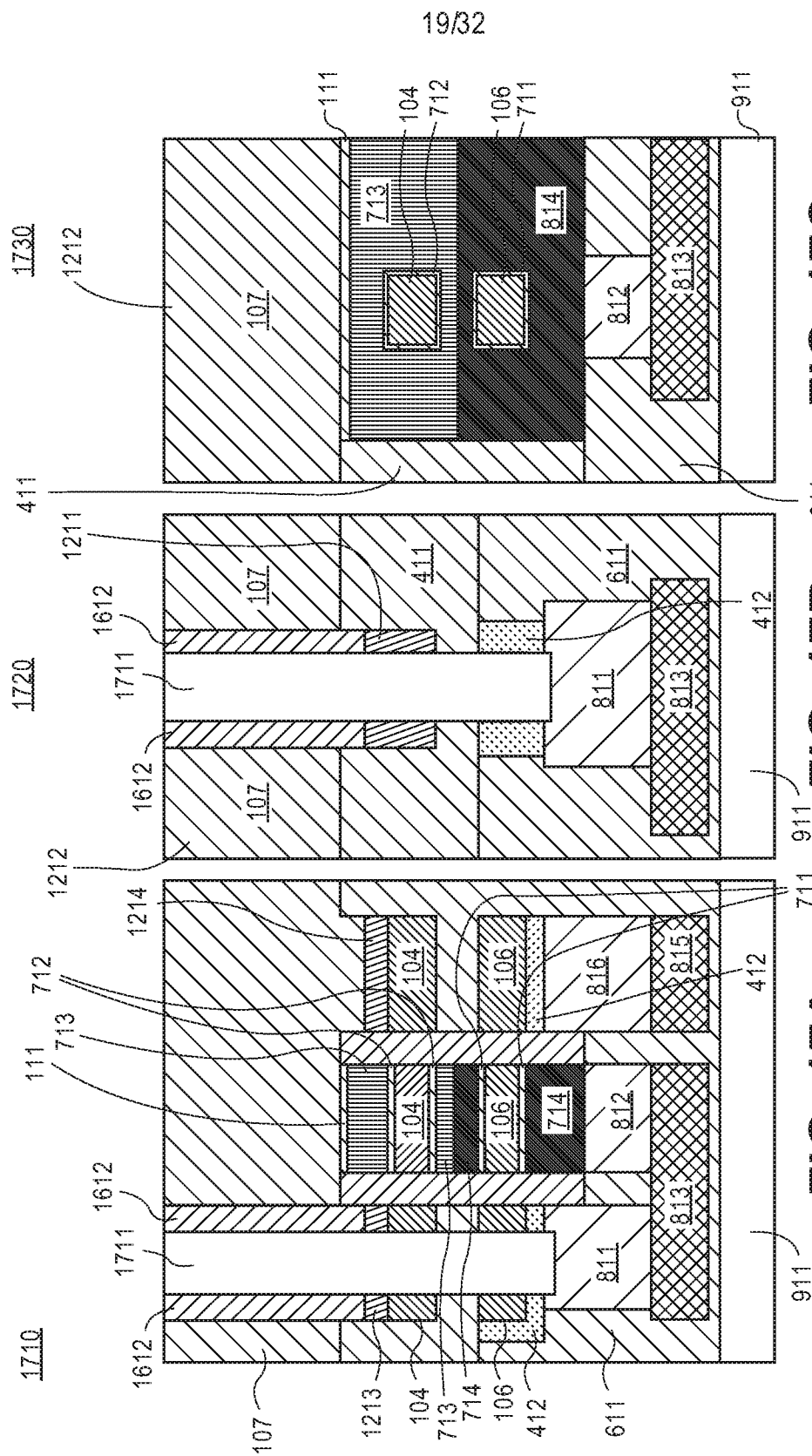


FIG. 16C

FIG. 16B

FIG. 16A



216

FLIGHT 17B

FIG. 17A

20/32

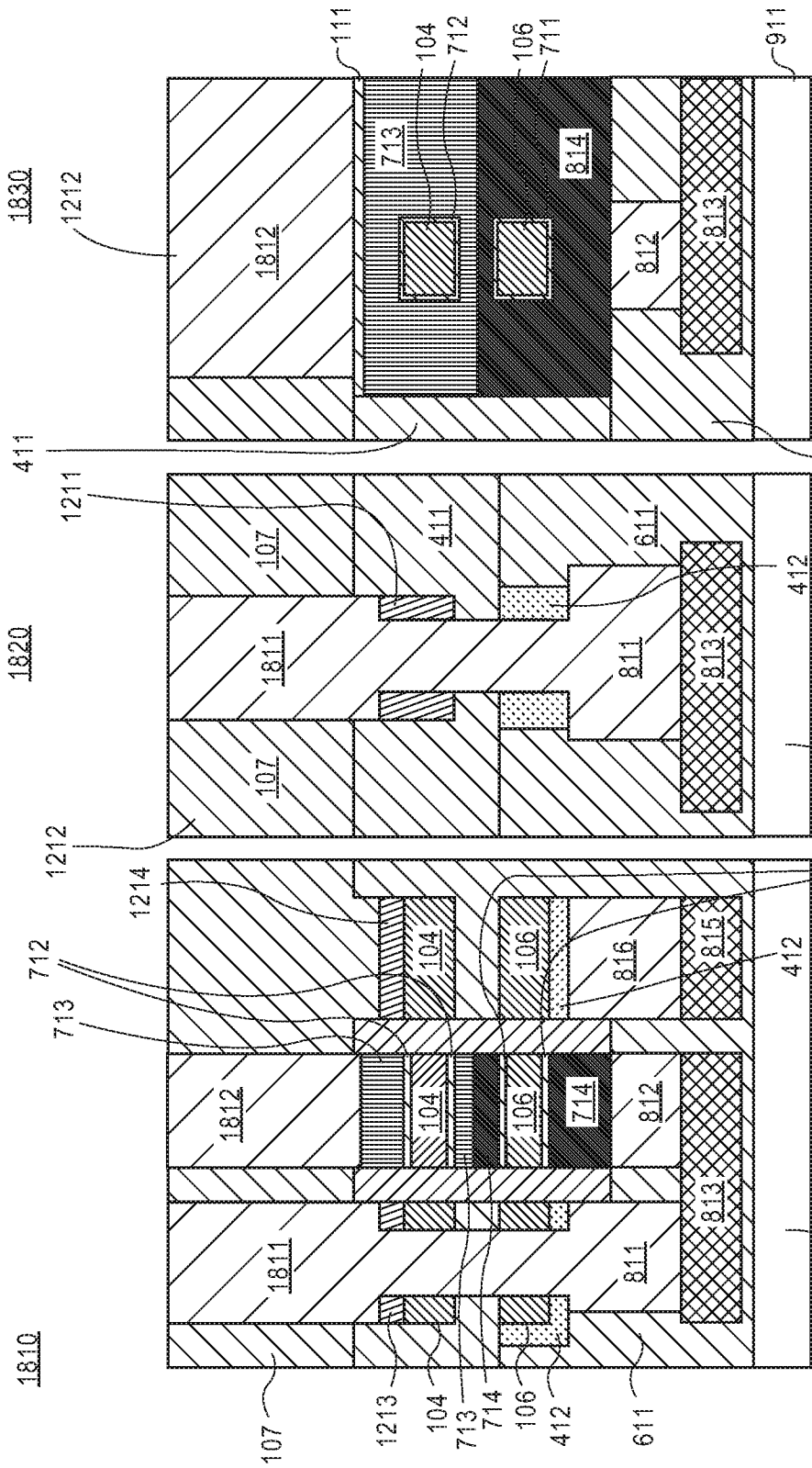


FIG. 18C

FIG. 18B

FIG. 18A

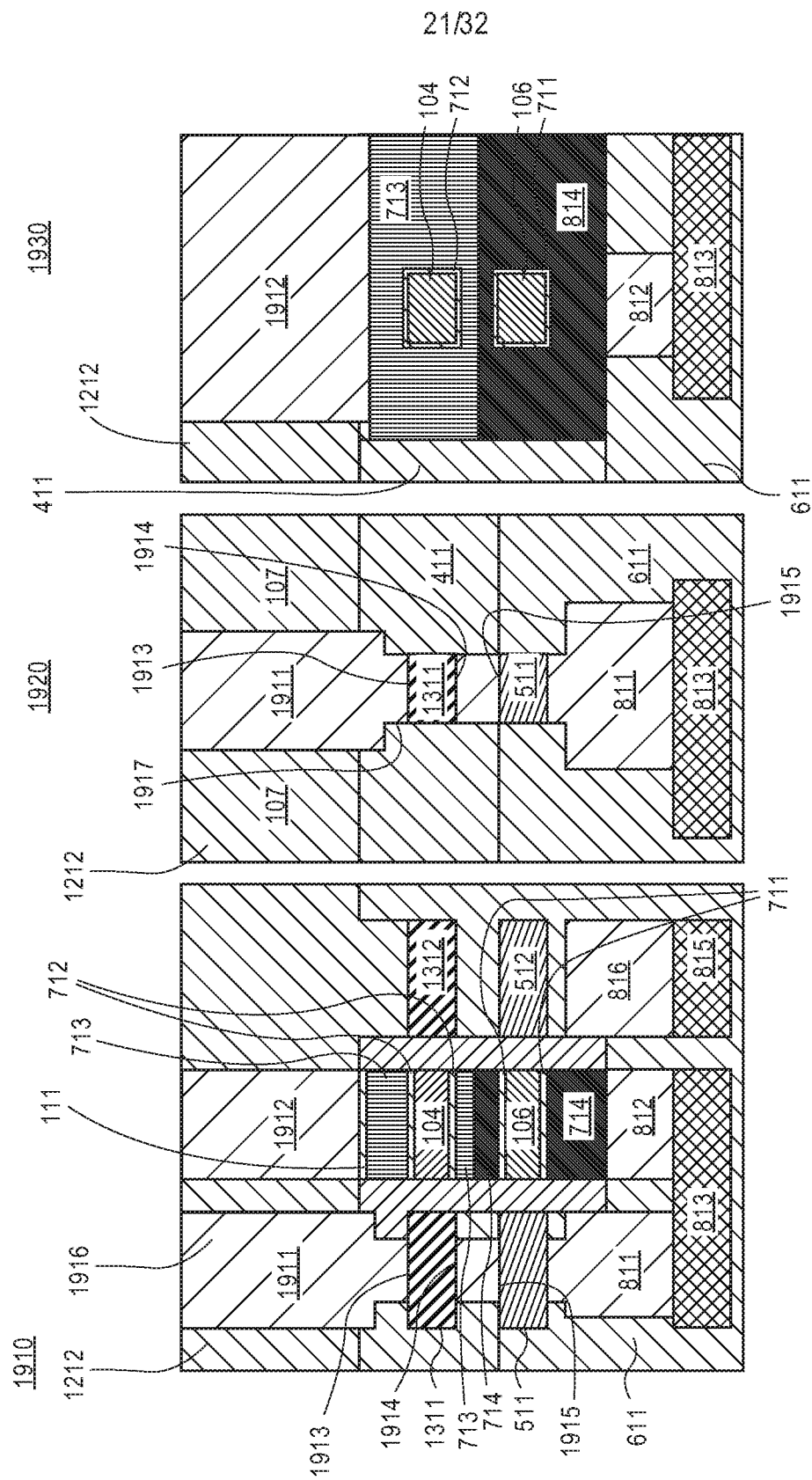
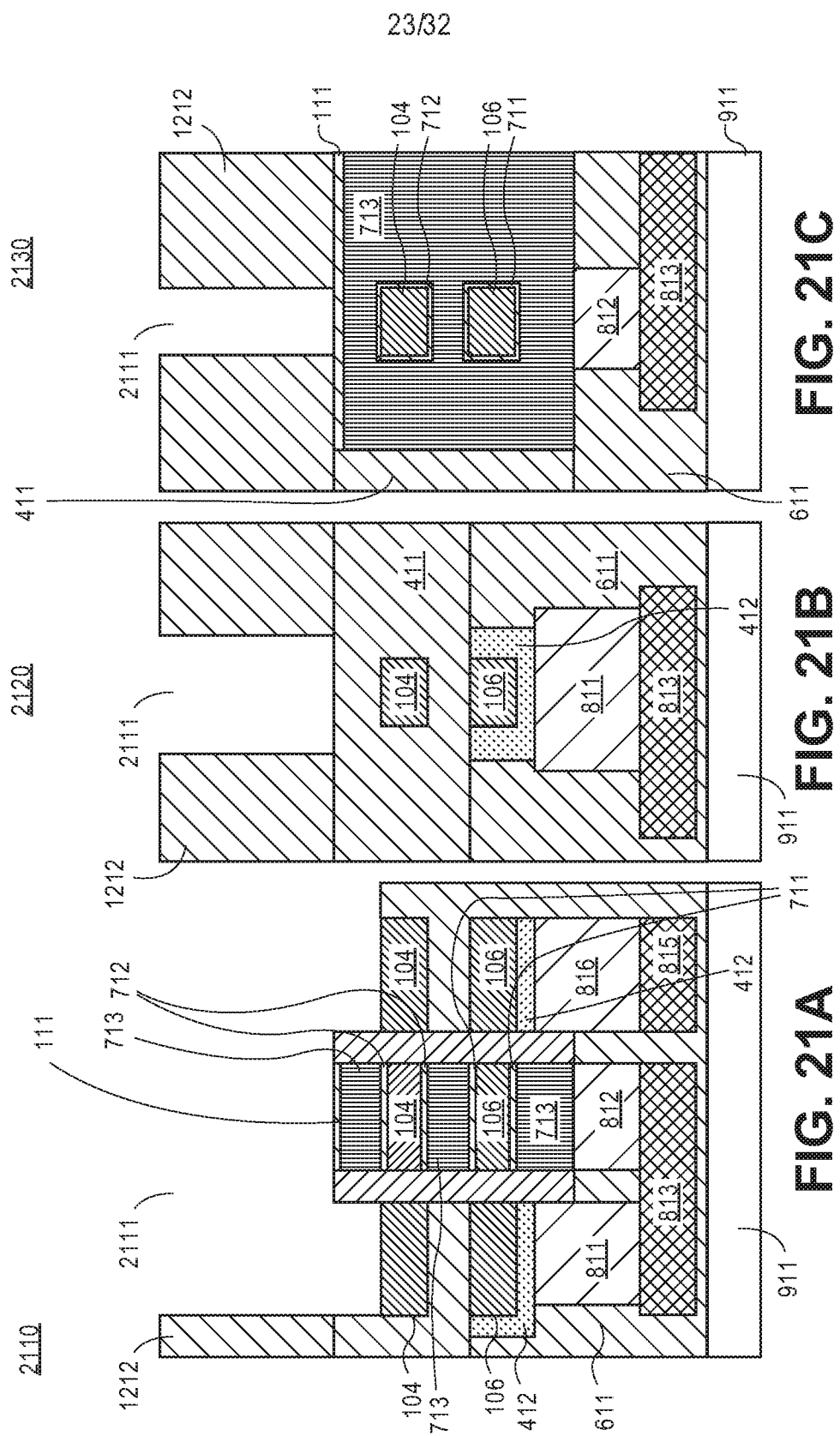


FIG. 19A

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CSLE



25/32

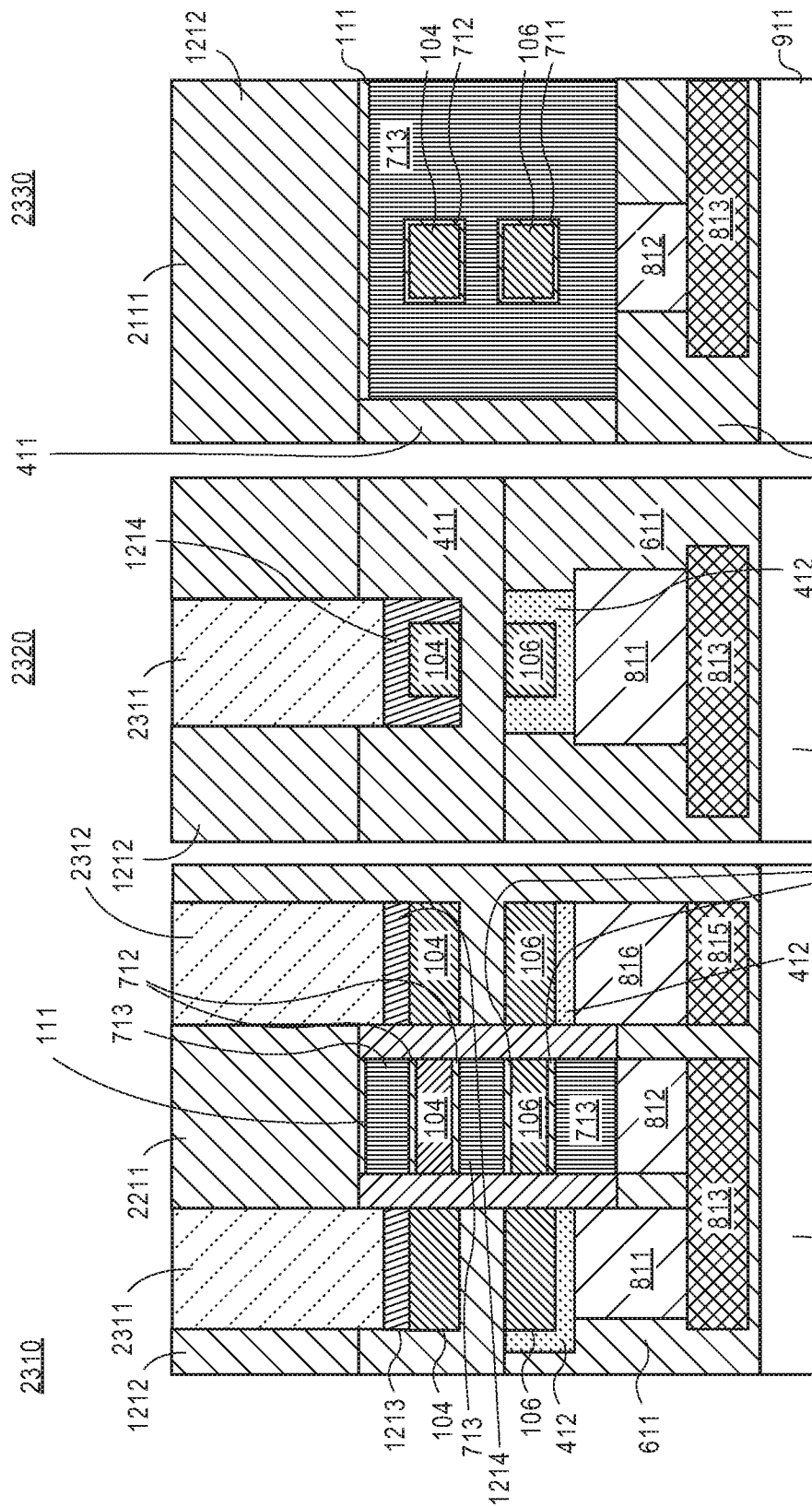
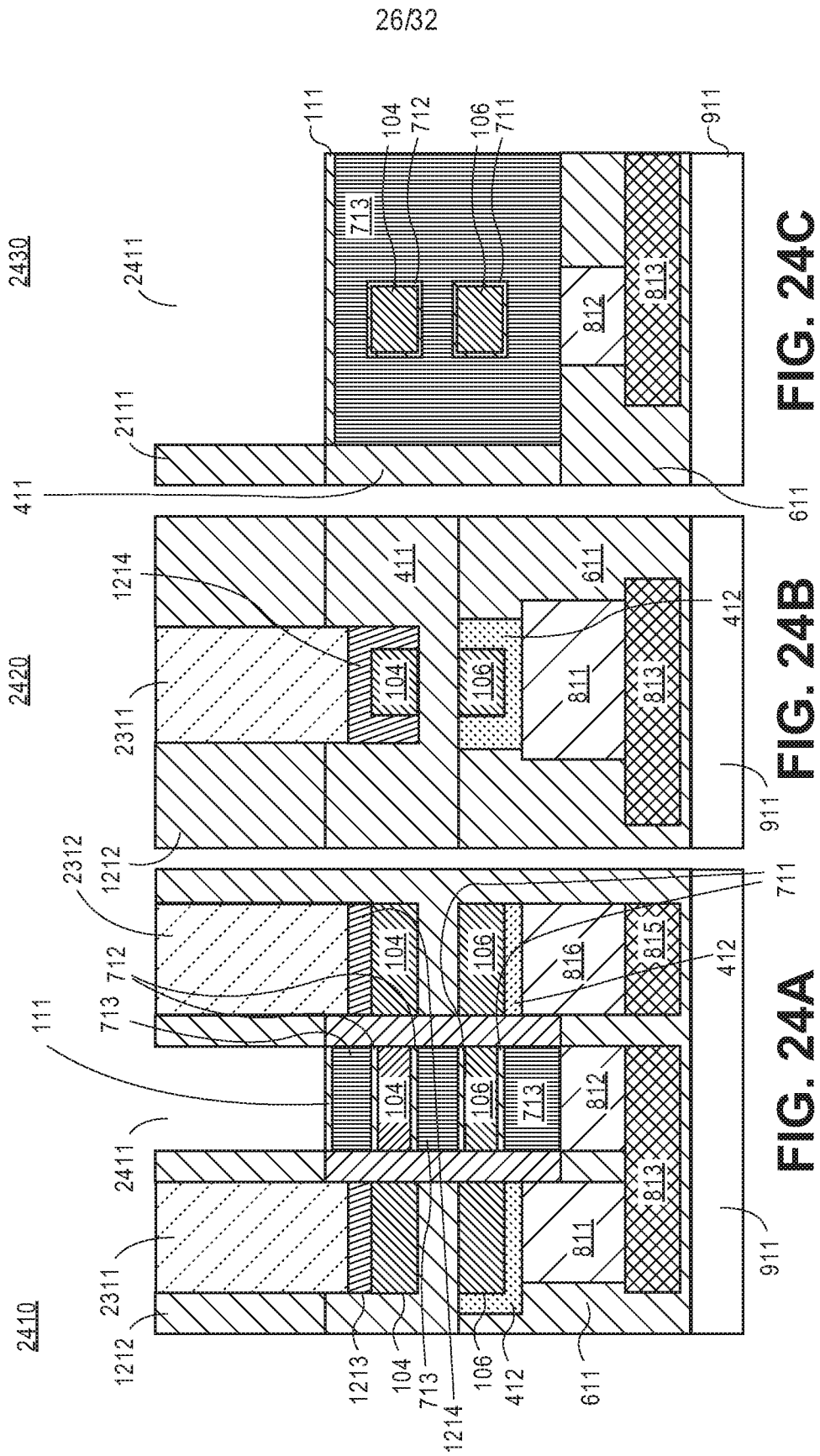
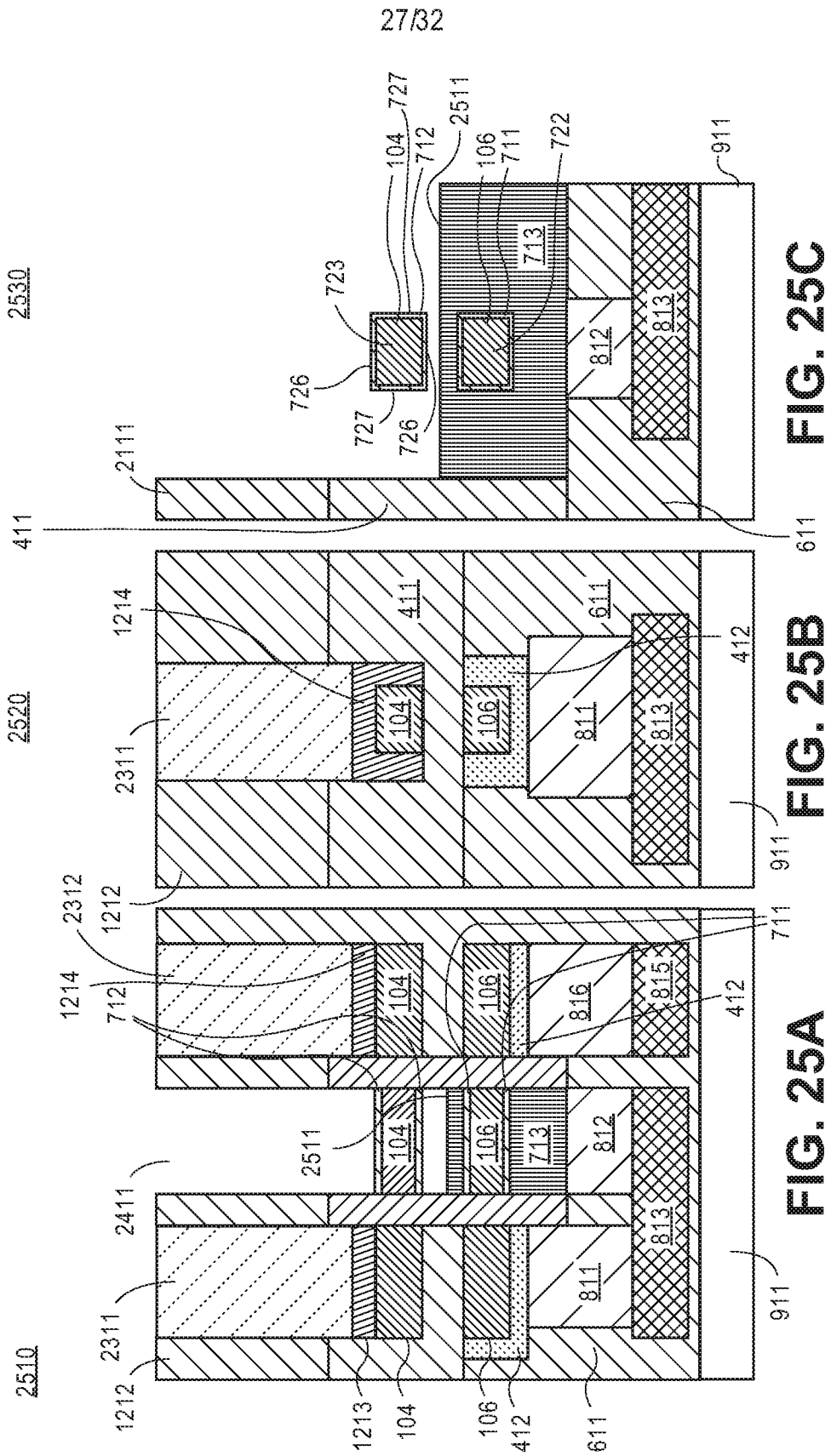


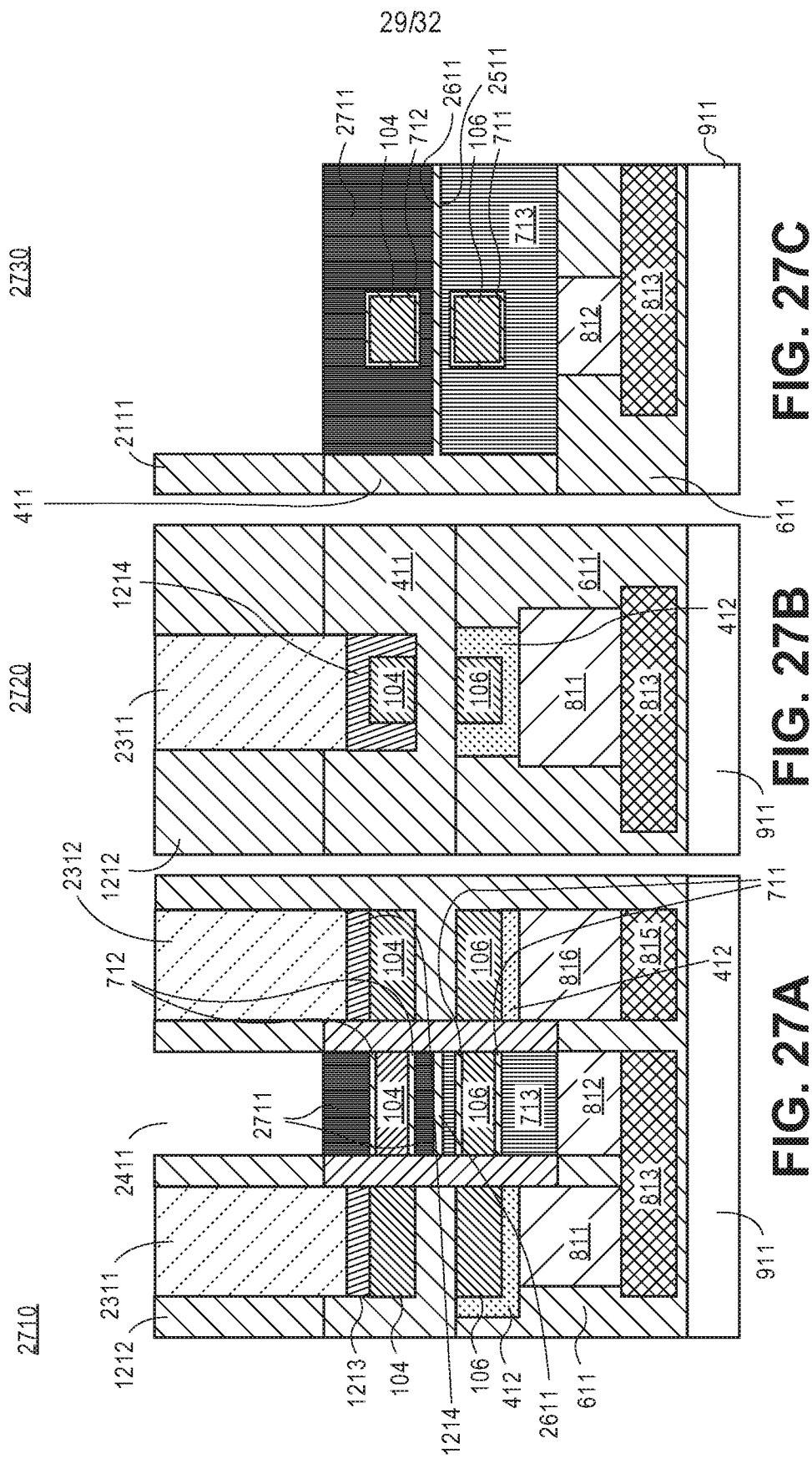
FIG. 23

FIG. 23B

FIG. 23A









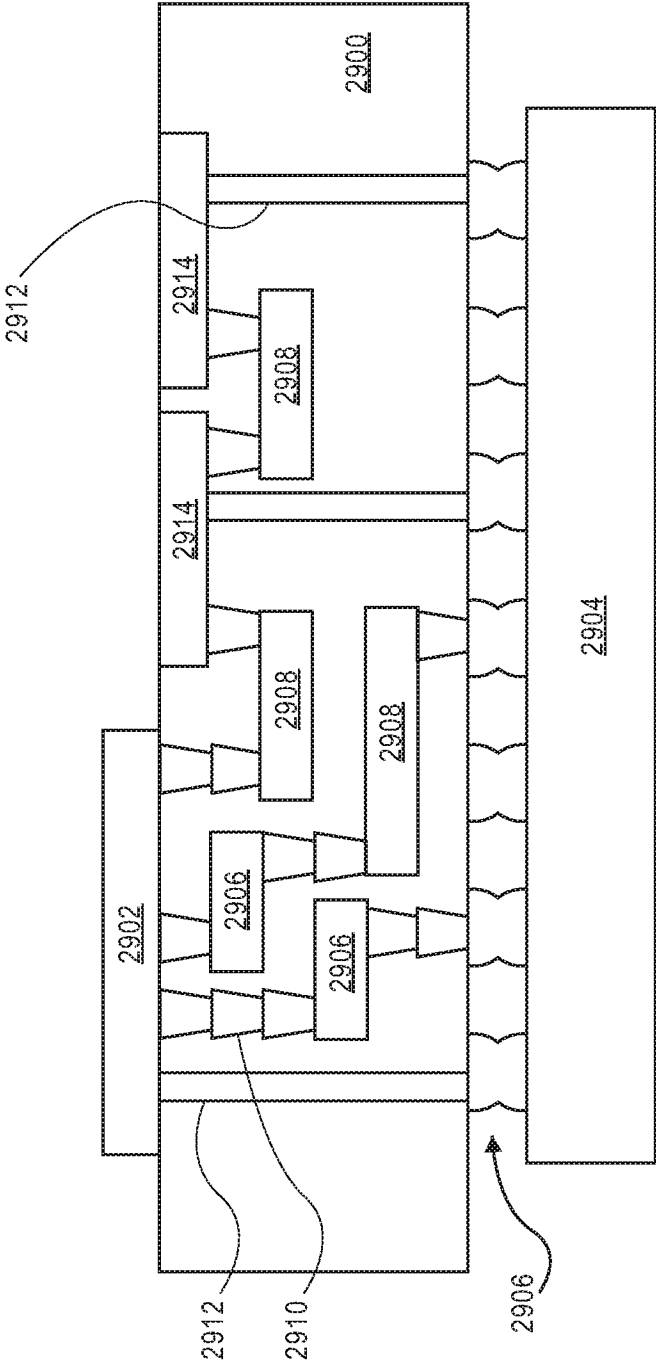
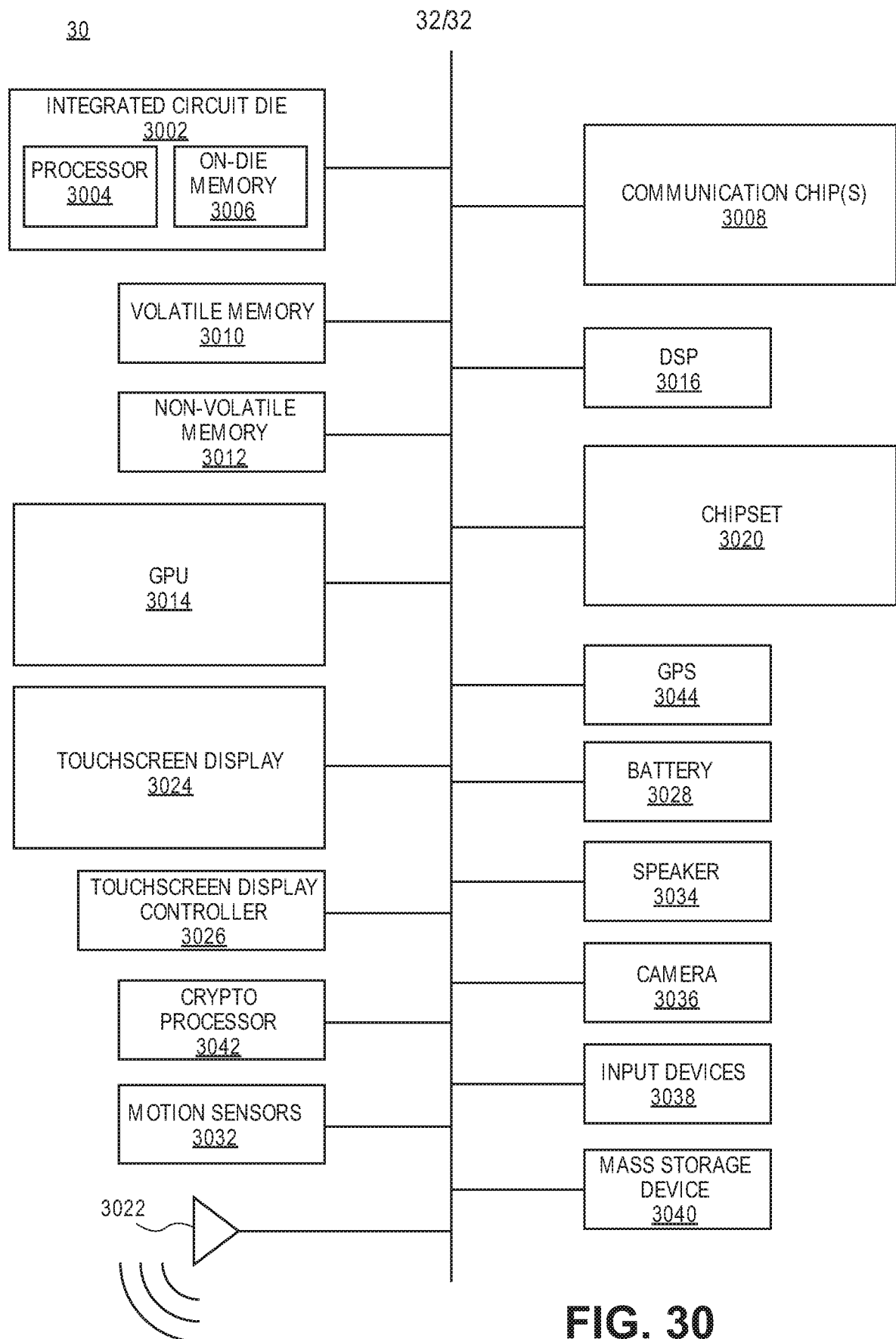


FIG. 29

**FIG. 30**

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/336(2006.01)i, H01L 29/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/336; H01L 21/768; H01L 27/088; H01L 27/105; H01L 29/78; H01L 29/66; H01L 21/78; H01L 21/8239

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: second transistor, fin, interconnect, second substrate, bonding

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2014-209278 A1 (INTEL CORPORATION) 31 December 2014 See abstract, paragraphs [0032]-[0035], [0050], claim 1 and figures 1A, 1B, 2A-2E, 5A-5D.	9, 10, 12-16, 18, 20
Y		11, 19
A		1-8, 17
Y	US 8536023 B2 (ZVI OR-BACH et al.) 17 September 2013 See abstract, column 35, lines 41-51 and figure 29F.	11, 19
A	US 2014-0035041 A1 (RAVI PILLARISETTY et al.) 06 February 2014 See abstract, paragraphs [0063]-[0067] and figure 3.	1-20
A	US 2013-0043531 A1 (MICRON TECHNOLOGY, INC.) 21 February 2013 See abstract, paragraphs [0042]-[0047] and figures 19-23.	1-20
A	KR 10-2011-0004415 A (MICRON TECHNOLOGY, INC.) 13 January 2011 See abstract, paragraphs [0029]-[0031] and figure 20. (* NOTE: As claim 15 refers to non-existing claim 24 and claims 10-14 refer to claim 15, this International Search Report has been established on the assumption that claims 10-15 refer to claim 9.)	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

31 October 2016 (31.10.2016)

Date of mailing of the international search report

31 October 2016 (31.10.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/066889

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