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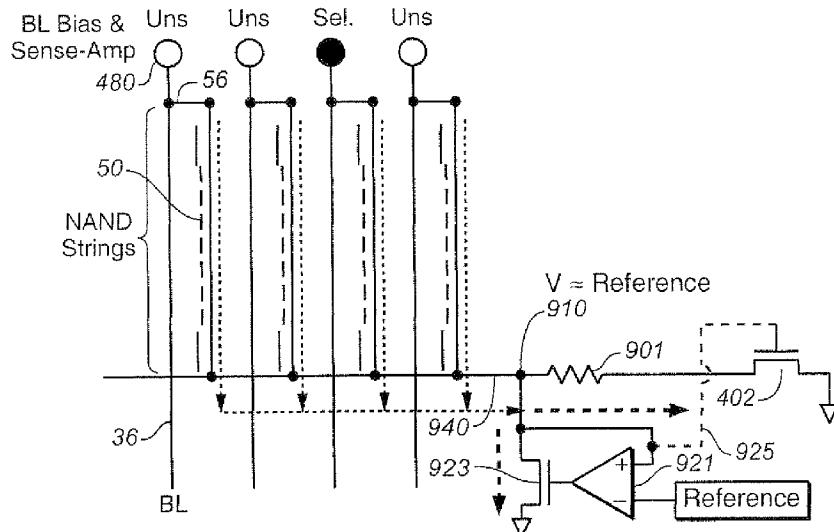


FIG. 15A

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(57) Abstract: Techniques are presented for dealing with possible source line bias is an error introduced by a non-zero resistance in the ground loop of the read/write circuits of a non-volatile memory. The error is caused by a voltage drop across the resistance of the source path to the chip's ground when current flows. For this purpose, the memory device includes a source potential regulation circuit, including an active circuit element having a first input connected to a reference voltage and having a second input connected as a feedback loop that is connectable to the aggregate node from which the memory cells of a structural block have their current run to ground. A variation includes a non-linear resistive element connectable between the aggregate node and ground.

## REGULATION OF SOURCE POTENTIAL TO COMBAT CELL SOURCE IR DROP

### FIELD OF THE INVENTION

**[0001]** This invention relates generally to non-volatile semiconductor memory such as electrically erasable programmable read-only memory (EEPROM) and flash EEPROM, and specifically ones having improved sensing circuits that compensate for source bias errors due to a finite resistance in the ground loop.

### BACKGROUND OF THE INVENTION

**[0002]** Solid-state memory capable of nonvolatile storage of charge, particularly in the form of EEPROM and flash EEPROM packaged as a small form factor card, has recently become the storage of choice in a variety of mobile and handheld devices, notably information appliances and consumer electronics products. Unlike RAM (random access memory) that is also solid-state memory, flash memory is non-volatile, and retaining its stored data even after power is turned off. In spite of the higher cost, flash memory is increasingly being used in mass storage applications. Conventional mass storage, based on rotating magnetic medium such as hard drives and floppy disks, is unsuitable for the mobile and handheld environment. This is because disk drives tend to be bulky, are prone to mechanical failure and have high latency and high power requirements. These undesirable attributes make disk-based storage impractical in most mobile and portable applications. On the other hand, flash memory, both embedded and in the form of a removable card is ideally suited in the mobile and handheld environment because of its small size, low power consumption, high speed and high reliability features.

**[0003]** EEPROM and electrically programmable read-only memory (EPROM) are non-volatile memory that can be erased and have new data written or “programmed” into their memory cells. Both utilize a floating (unconnected) conductive gate, in a field effect transistor structure, positioned over a channel region in a semiconductor substrate, between source and drain regions. A control gate is then provided over the

floating gate. The threshold voltage characteristic of the transistor is controlled by the amount of charge that is retained on the floating gate. That is, for a given level of charge on the floating gate, there is a corresponding voltage (threshold) that must be applied to the control gate before the transistor is turned "on" to permit conduction between its source and drain regions.

**[0004]** The floating gate can hold a range of charges and therefore can be programmed to any threshold voltage level within a threshold voltage window. The size of the threshold voltage window is delimited by the minimum and maximum threshold levels of the device, which in turn correspond to the range of the charges that can be programmed onto the floating gate. The threshold window generally depends on the memory device's characteristics, operating conditions and history. Each distinct, resolvable threshold voltage level range within the window may, in principle, be used to designate a definite memory state of the cell.

**[0005]** The transistor serving as a memory cell is typically programmed to a "programmed" state by one of two mechanisms. In "hot electron injection," a high voltage applied to the drain accelerates electrons across the substrate channel region. At the same time a high voltage applied to the control gate pulls the hot electrons through a thin gate dielectric onto the floating gate. In "tunneling injection," a high voltage is applied to the control gate relative to the substrate. In this way, electrons are pulled from the substrate to the intervening floating gate.

**[0006]** The memory device may be erased by a number of mechanisms. For EPROM, the memory is bulk erasable by removing the charge from the floating gate by ultraviolet radiation. For EEPROM, a memory cell is electrically erasable, by applying a high voltage to the substrate relative to the control gate so as to induce electrons in the floating gate to tunnel through a thin oxide to the substrate channel region (i.e., Fowler-Nordheim tunneling.) Typically, the EEPROM is erasable byte by byte. For flash EEPROM, the memory is electrically erasable either all at once or one or more blocks at a time, where a block may consist of 512 bytes or more of memory.

### EXAMPLES OF NON-VOLATILE MEMORY CELLS

**[0007]** The memory devices typically comprise one or more memory chips that may be mounted on a card. Each memory chip comprises an array of memory cells supported by peripheral circuits such as decoders and erase, write and read circuits. The more sophisticated memory devices also come with a controller that performs intelligent and higher level memory operations and interfacing. There are many commercially successful non-volatile solid-state memory devices being used today. These memory devices may employ different types of memory cells, each type having one or more charge storage element.

**[0008]** FIGs. 1A-1E illustrate schematically different examples of non-volatile memory cells.

**[0009]** FIG. 1A illustrates schematically a non-volatile memory in the form of an EEPROM cell with a floating gate for storing charge. An electrically erasable and programmable read-only memory (EEPROM) has a similar structure to EPROM, but additionally provides a mechanism for loading and removing charge electrically from its floating gate upon application of proper voltages without the need for exposure to UV radiation. Examples of such cells and methods of manufacturing them are given in United States patent no. 5,595,924.

**[0010]** FIG. 1B illustrates schematically a flash EEPROM cell having both a select gate and a control or steering gate. The memory cell 10 has a “split-channel” 12 between source 14 and drain 16 diffusions. A cell is formed effectively with two transistors T1 and T2 in series. T1 serves as a memory transistor having a floating gate 20 and a control gate 30. The floating gate is capable of storing a selectable amount of charge. The amount of current that can flow through the T1’s portion of the channel depends on the voltage on the control gate 30 and the amount of charge residing on the intervening floating gate 20. T2 serves as a select transistor having a select gate 40. When T2 is turned on by a voltage at the select gate 40, it allows the current in the T1’s portion of the channel to pass between the source and drain. The select transistor provides a switch along the source-drain channel independent of the voltage at the control gate. One advantage is that it can be used to turn off those cells

that are still conducting at zero control gate voltage due to their charge depletion (positive) at their floating gates. The other advantage is that it allows source side injection programming to be more easily implemented.

**[0011]** One simple embodiment of the split-channel memory cell is where the select gate and the control gate are connected to the same word line as indicated schematically by a dotted line shown in **FIG. 1B**. This is accomplished by having a charge storage element (floating gate) positioned over one portion of the channel and a control gate structure (which is part of a word line) positioned over the other channel portion as well as over the charge storage element. This effectively forms a cell with two transistors in series, one (the memory transistor) with a combination of the amount of charge on the charge storage element and the voltage on the word line controlling the amount of current that can flow through its portion of the channel, and the other (the select transistor) having the word line alone serving as its gate. Examples of such cells, their uses in memory systems and methods of manufacturing them are given in United States patents nos. 5,070,032, 5,095,344, 5,315,541, 5,343,063, and 5,661,053.

**[0012]** A more refined embodiment of the split-channel cell shown in **FIG. 1B** is when the select gate and the control gate are independent and not connected by the dotted line between them. One implementation has the control gates of one column in an array of cells connected to a control (or steering) line perpendicular to the word line. The effect is to relieve the word line from having to perform two functions at the same time when reading or programming a selected cell. Those two functions are (1) to serve as a gate of a select transistor, thus requiring a proper voltage to turn the select transistor on and off, and (2) to drive the voltage of the charge storage element to a desired level through an electric field (capacitive) coupling between the word line and the charge storage element. It is often difficult to perform both of these functions in an optimum manner with a single voltage. With the separate control of the control gate and the select gate, the word line need only perform function (1), while the added control line performs function (2). This capability allows for design of higher performance programming where the programming voltage is geared to the targeted data. The use of independent control (or steering) gates in a flash EEPROM array is

described, for example, in United States patent nos. 5,313,421 and 6,222,762.

**[0013]** **FIG. 1C** illustrates schematically another flash EEPROM cell having dual floating gates and independent select and control gates. The memory cell 10 is similar to that of **FIG. 1B** except it effectively has three transistors in series. In this type of cell, two storage elements (i.e., that of T1 - left and T1 - right) are included over its channel between source and drain diffusions with a select transistor T1 in between them. The memory transistors have floating gates 20 and 20', and control gates 30 and 30', respectively. The select transistor T2 is controlled by a select gate 40. At any one time, only one of the pair of memory transistors is accessed for read or write. When the storage unit T1 - left is being accessed, both the T2 and T1 - right are turned on to allow the current in the T1 - left's portion of the channel to pass between the source and the drain. Similarly, when the storage unit T1 - right is being accessed, T2 and T1 - left are turned on. Erase is effected by having a portion of the select gate polysilicon in close proximity to the floating gate and applying a substantial positive voltage (e.g. 20V) to the select gate so that the electrons stored within the floating gate can tunnel to the select gate polysilicon.

**[0014]** **FIG. 1D** illustrates schematically a string of memory cells organized into an NAND chain. An NAND chain 50 consists of a series of memory transistors M1, M2, ... Mn (n= 4, 8, 16 or higher) daisy-chained by their sources and drains. A pair of select transistors S1, S2 controls the memory transistors chain's connection to the external via the NAND chain's source terminal 54 and drain terminal 56. In a memory array, when the source select transistor S1 is turned on, the source terminal is coupled to a source line. Similarly, when the drain select transistor S2 is turned on, the drain terminal of the NAND chain is coupled to a bit line of the memory array. Each memory transistor in the chain has a charge storage element to store a given amount of charge so as to represent an intended memory state. A control gate of each memory transistor provides control over read and write operations. A control gate of each of the select transistors S1, S2 provides control access to the NAND chain via its source terminal 54 and drain terminal 56 respectively.

**[0015]** When an addressed memory transistor within an NAND chain is read and verified during programming, its control gate is supplied with an appropriate voltage.

At the same time, the rest of the non-addressed memory transistors in the NAND chain 50 are fully turned on by application of sufficient voltage on their control gates. In this way, a conductive path is effectively created from the source of the individual memory transistor to the source terminal 54 of the NAND chain and likewise for the drain of the individual memory transistor to the drain terminal 56 of the chain. Memory devices with such NAND chain structures are described in United States patent nos. 5,570,315, 5,903,495, 6,046,935.

**[0016]** FIG. 1E illustrates schematically a non-volatile memory with a dielectric layer for storing charge. Instead of the conductive floating gate elements described earlier, a dielectric layer is used. Such memory devices utilizing dielectric storage element have been described by Eitan et al., “NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell,” IEEE Electron Device Letters, vol. 21, no. 11, November 2000, pp. 543-545. An ONO dielectric layer extends across the channel between source and drain diffusions. The charge for one data bit is localized in the dielectric layer adjacent to the drain, and the charge for the other data bit is localized in the dielectric layer adjacent to the source. For example, United States patents nos. 5,768,192 and 6,011,725 disclose a nonvolatile memory cell having a trapping dielectric sandwiched between two silicon dioxide layers. Multi-state data storage is implemented by separately reading the binary states of the spatially separated charge storage regions within the dielectric.

### MEMORY ARRAY

**[0017]** A memory device typically comprises of a two-dimensional array of memory cells arranged in rows and columns and addressable by word lines and bit lines. The array can be formed according to an NOR type or an NAND type architecture.

### NOR Array

**[0018]** FIG. 2 illustrates an example of an NOR array of memory cells. Memory devices with an NOR type architecture have been implemented with cells of the type illustrated in FIGs. 1B or 1C. Each row of memory cells are connected by their sources and drains in a daisy-chain manner. This design is sometimes referred to as a

virtual ground design. Each memory cell 10 has a source 14, a drain 16, a control gate 30 and a select gate 40. The cells in a row have their select gates connected to word line 42. The cells in a column have their sources and drains respectively connected to selected bit lines 34 and 36. In some embodiments where the memory cells have their control gate and select gate controlled independently, a steering line 30 also connects the control gates of the cells in a column.

**[0019]** Many flash EEPROM devices are implemented with memory cells where each is formed with its control gate and select gate connected together. In this case, there is no need for steering lines and a word line simply connects all the control gates and select gates of cells along each row. Examples of these designs are disclosed in United States patent nos. 5,172,338 and 5,418,752. In these designs, the word line essentially performed two functions: row selection and supplying control gate voltage to all cells in the row for reading or programming.

### NAND Array

**[0020]** FIG. 3 illustrates an example of an NAND array of memory cells, such as that shown in **FIG. 1D**. Along each column of NAND chains, a bit line is coupled to the drain terminal 56 of each NAND chain. Along each row of NAND chains, a source line may connect all their source terminals 54. Also the control gates of the NAND chains along a row are connected to a series of corresponding word lines. An entire row of NAND chains can be addressed by turning on the pair of select transistors (see **FIG. 1D**) with appropriate voltages on their control gates via the connected word lines. When a memory transistor representing a memory cell within the NAND chain is being read, the remaining memory transistors in the chain are turned on hard via their associated word lines so that the current flowing through the chain is essentially dependent upon the level of charge stored in the cell being read. An example of an NAND architecture array and its operation as part of a memory system is found in United States patents nos. 5,570,315, 5,774,397 and 6,046,935.

### Block Erase

**[0021]** Programming of charge storage memory devices can only result in adding

more charge to its charge storage elements. Therefore, prior to a program operation, existing charge in a charge storage element must be removed (or erased). Erase circuits (not shown) are provided to erase one or more blocks of memory cells. A non-volatile memory such as EEPROM is referred to as a "Flash" EEPROM when an entire array of cells, or significant groups of cells of the array, is electrically erased together (i.e., in a flash). Once erased, the group of cells can then be reprogrammed. The group of cells erasable together may consist of one or more addressable erase unit. The erase unit or block typically stores one or more pages of data, the page being the unit of programming and reading, although more than one page may be programmed or read in a single operation. Each page typically stores one or more sectors of data, the size of the sector being defined by the host system. An example is a sector of 512 bytes of user data, following a standard established with magnetic disk drives, plus some number of bytes of overhead information about the user data and/or the block in with it is stored.

#### READ/WRITE CIRCUITS

**[0022]** In the usual two-state EEPROM cell, at least one current breakpoint level is established so as to partition the conduction window into two regions. When a cell is read by applying predetermined, fixed voltages, its source/drain current is resolved into a memory state by comparing with the breakpoint level (or reference current  $I_{REF}$ ). If the current read is higher than that of the breakpoint level, the cell is determined to be in one logical state (e.g., a "zero" state). On the other hand, if the current is less than that of the breakpoint level, the cell is determined to be in the other logical state (e.g., a "one" state). Thus, such a two-state cell stores one bit of digital information. A reference current source, which may be externally programmable, is often provided as part of a memory system to generate the breakpoint level current.

**[0023]** In order to increase memory capacity, flash EEPROM devices are being fabricated with higher and higher density as the state of the semiconductor technology advances. Another method for increasing storage capacity is to have each memory cell store more than two states.

**[0024]** For a multi-state or multi-level EEPROM memory cell, the conduction

window is partitioned into more than two regions by more than one breakpoint such that each cell is capable of storing more than one bit of data. The information that a given EEPROM array can store is thus increased with the number of states that each cell can store. EEPROM or flash EEPROM with multi-state or multi-level memory cells have been described in U.S. Patent No. 5,172,338.

**[0025]** In practice, the memory state of a cell is usually read by sensing the conduction current across the source and drain electrodes of the cell when a reference voltage is applied to the control gate. Thus, for each given charge on the floating gate of a cell, a corresponding conduction current with respect to a fixed reference control gate voltage may be detected. Similarly, the range of charge programmable onto the floating gate defines a corresponding threshold voltage window or a corresponding conduction current window.

**[0026]** Alternatively, instead of detecting the conduction current among a partitioned current window, it is possible to set the threshold voltage for a given memory state under test at the control gate and detect if the conduction current is lower or higher than a threshold current. In one implementation the detection of the conduction current relative to a threshold current is accomplished by examining the rate the conduction current is discharging through the capacitance of the bit line.

**[0027]** FIG. 4 illustrates the relation between the source-drain current  $I_D$  and the control gate voltage  $V_{CG}$  for four different charges  $Q1-Q4$  that the floating gate may be selectively storing at any one time. The four solid  $I_D$  versus  $V_{CG}$  curves represent four possible charge levels that can be programmed on a floating gate of a memory cell, respectively corresponding to four possible memory states. As an example, the threshold voltage window of a population of cells may range from 0.5V to 3.5V. Six memory states may be demarcated by partitioning the threshold window into five regions in interval of 0.5V each. For example, if a reference current,  $I_{REF}$  of 2  $\mu$ A is used as shown, then the cell programmed with  $Q1$  may be considered to be in a memory state “1” since its curve intersects with  $I_{REF}$  in the region of the threshold window demarcated by  $V_{CG} = 0.5V$  and 1.0V. Similarly,  $Q4$  is in a memory state “5”.

**[0028]** As can be seen from the description above, the more states a memory cell is

made to store, the more finely divided is its threshold window. This will require higher precision in programming and reading operations in order to be able to achieve the required resolution.

**[0029]** United States Patent No. 4,357,685 discloses a method of programming a 2-state EPROM in which when a cell is programmed to a given state, it is subject to successive programming voltage pulses, each time adding incremental charge to the floating gate. In between pulses, the cell is read back or verified to determine its source-drain current relative to the breakpoint level. Programming stops when the current state has been verified to reach the desired state. The programming pulse train used may have increasing period or amplitude.

**[0030]** Prior art programming circuits simply apply programming pulses to step through the threshold window from the erased or ground state until the target state is reached. Practically, to allow for adequate resolution, each partitioned or demarcated region would require at least about five programming steps to transverse. The performance is acceptable for 2-state memory cells. However, for multi-state cells, the number of steps required increases with the number of partitions and therefore, the programming precision or resolution must be increased. For example, a 16-state cell may require on average at least 40 programming pulses to program to a target state.

**[0031]** **FIG. 5** illustrates schematically a memory device with a typical arrangement of a memory array 100 accessible by read/write circuits 170 via row decoder 130 and column decoder 160. As described in connection with **FIGs. 2 and 3**, a memory transistor of a memory cell in the memory array 100 is addressable via a set of selected word line(s) and bit line(s). The row decoder 130 selects one or more word lines and the column decoder 160 selects one or more bit lines in order to apply appropriate voltages to the respective gates of the addressed memory transistor. Read/write circuits 170 are provided to read or write (program) the memory states of addressed memory transistors. The read/write circuits 170 comprise a number of read/write modules connectable via bit lines to memory elements in the array.

## FACTORS AFFECTING READ/WRITE PERFORMANCE AND ACCURACY

**[0032]** In order to improve read and program performance, multiple charge storage elements or memory transistors in an array are read or programmed in parallel. Thus, a logical “page” of memory elements are read or programmed together. In existing memory architectures, a row typically contains several interleaved pages. All memory elements of a page will be read or programmed together. The column decoder will selectively connect each one of the interleaved pages to a corresponding number of read/write modules. For example, in one implementation, the memory array is designed to have a page size of 532 bytes (512 bytes plus 20 bytes of overheads.) If each column contains a drain bit line and there are two interleaved pages per row, this amounts to 8512 columns with each page being associated with 4256 columns. There will be 4256 sense modules connectable to read or write in parallel either all the even bit lines or the odd bit lines. In this way, a page of 4256 bits (i.e., 532 bytes) of data in parallel are read from or programmed into the page of memory elements. The read/write modules forming the read/write circuits 170 can be arranged into various architectures.

**[0033]** As mentioned before, conventional memory devices improve read/write operations by operating in a massively parallel manner on all even or all odd bit lines at a time. This “alternate-bit-line” architecture of a row consisting of two interleaved pages will help to alleviate the problem of fitting the block of read/write circuits. It is also dictated by consideration of controlling bit-line to bit-line capacitive coupling. A block decoder is used to multiplex the set of read/write modules to either the even page or the odd page. In this way, whenever one set bit lines are being read or programmed, the interleaving set can be grounded to minimize immediate neighbor coupling.

**[0034]** However, the interleaving page architecture is disadvantageous in at least three respects. First, it requires additional multiplexing circuitry. Secondly, it is slow in performance. To finish read or program of memory cells connected by a word line or in a row, two read or two program operations are required. Thirdly, it is also not optimum in addressing other disturb effects such as field coupling between neighboring charge storage elements at the floating gate level when the two neighbors

are programmed at different times, such as separately in odd and even pages.

**[0035]** United States Patent Publication No. 2004-0057318-A1 discloses a memory device and a method thereof that allow sensing a plurality of contiguous memory cells in parallel. For example, all memory cells along a row sharing the same word lines are read or programmed together as a page. This “all-bit-line” architecture doubles the performance of the “alternate-bit-line” architecture while minimizing errors caused by neighboring disturb effects. However, sensing all bit lines does bring up the problem of cross-talk between neighboring bit lines due induced currents from their mutual capacitance. This is addressed by keeping the voltage difference between each adjacent pair of bit lines substantially independent of time while their conduction currents are being sensed. When this condition is imposed, all displacement currents due to the various bit lines' capacitance drop out since they all depend on a time varying voltage difference. The sensing circuit coupled to each bit line has a voltage clamp on the bit line so that the potential difference on any adjacent pair of connected bit lines is time-independent. With the bit line voltage clamped, the conventional method of sensing the discharge due to the bit line capacitance can not be applied. Instead, the sensing circuit and method allow determination of a memory cell's conduction current by noting the rate it discharges or charges a given capacitor independent of the bit line. This will allow a sensing circuit independent of the architecture of the memory array (i.e., independent of the bit line capacitance.) Especially, it allows the bit line voltages to be clamped during sensing in order to avoid bit line crosstalk.

**[0036]** As mentioned before, conventional memory devices improve read/write operations by operating in a massively parallel manner. This approach improves performance but does have repercussions on the accuracy of read and write operations.

**[0037]** One issue is the source line bias error. This is particular acute for memory architecture where a large number memory cells have their sources coupled together in a source line to ground. Parallel sensing of these memory cells with common source results in a substantial current through the source line. Owing to a non-zero resistance in the source line, this in turn results in an appreciable potential difference

between the true ground and the source electrode of each memory cell. During sensing, the threshold voltage supplied to the control gate of each memory cell is relative to its source electrode but the system power supply is relative to the true ground. Thus sensing may become inaccurate due to the existence of the source line bias error.

**[0038]** United States Patent Publication No. 2004-0057287-A1 discloses a memory device and a method thereof that allow sensing a plurality of contiguous memory cells in parallel. The reduction in source line bias is accomplished by read/write circuits with features and techniques for multi-pass sensing. When a page of memory cells are being sensed in parallel, each pass helps to identify and shut down the memory cells with conduction current higher than a given demarcation current value. The identified memory cells are shut down by pulling their associated bit lines to ground. In other words, those cells having higher conduction current and irrelevant to the present sensing are identified and have their current shut down before the actual data of the current sensing is read.

**[0039]** Therefore there is a general need for high performance and high capacity non-volatile memory with reduced power consumption. In particular, there is a need for a compact non-volatile memory with enhanced read and program performance that is power efficient.

## SUMMARY OF INVENTION

**[0040]** These needs for a high capacity and high performance non-volatile memory device are met by having a large page of read/write circuits to read and write a corresponding page of memory cells in parallel. In particular, interactive noises effects inherent in high density chip integration are that may introduce errors into reading and programming are either eliminated or minimized.

**[0041]** Source line bias is an error introduced by a non-zero resistance in the ground loop of the read/write circuits. The error is caused by a voltage drop across the resistance of the source path to the chip's ground when current flows.

**[0042]** A first set of embodiments is for a memory device having individual pages of memory cells to be sensed in parallel, each memory cell having a source, a drain, a charge storage unit and a control gate for controlling a conduction current along said drain and source. The memory includes a page source line connectable to the source of each memory cell in a page, an aggregate node for a structural block connectable to individual page source lines, and a source isolation switch coupled via said aggregate node to a page source line of a selected page in the structural block for a memory operation. The memory device also includes a source potential regulation circuit, including an active circuit element having a first input connected to a first reference voltage and having a second input connected as a feedback loop that is connectable to the aggregate node.

**[0043]** In another set of embodiments, a memory device having individual pages of memory cells to be sensed in parallel, each memory cell having a source, a drain, a charge storage unit and a control gate for controlling a conduction current along said drain and source. The memory includes a page source line connectable to the source of each memory cell in a page, an aggregate node for a structural block connectable to individual page source lines, and a source isolation switch coupled via said aggregate node to a page source line of a selected page in the structural block for a memory operation. The memory device also includes a non-linear resistive element connectable between the aggregate node and ground reference.

**[0044]** Various aspects, advantages, features and embodiments of the present invention are included in the following description of exemplary examples thereof, which description should be taken in conjunction with the accompanying drawings. All patents, patent applications, articles, other publications, documents and things referenced herein are hereby incorporated herein by this reference in their entirety for all purposes. To the extent of any inconsistency or conflict in the definition or use of terms between any of the incorporated publications, documents or things and the present application, those of the present application shall prevail.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0045] FIGs. 1A-1E illustrate schematically different examples of non-volatile memory cells.

[0046] FIG. 2 illustrates an example of an NOR array of memory cells.

[0047] FIG. 3 illustrates an example of an NAND array of memory cells, such as that shown in FIG. 1D.

[0048] FIG. 4 illustrates the relation between the source-drain current and the control gate voltage for four different charges Q1-Q4 that the floating gate may be storing at any one time.

[0049] FIG. 5 illustrates schematically a typical arrangement of a memory array accessible by read/write circuits via row and column decoders.

[0050] FIG. 6A illustrates schematically a compact memory device having a bank of read/write circuits, which provides the context in which the present invention is implemented.

[0051] FIG. 6B illustrates a preferred arrangement of the compact memory device shown in FIG. 6A.

[0052] FIG. 7A illustrates a conventional arrangement in which a bit line voltage control, a word line voltage control and a source voltage control are all referencing from the same ground of the IC memory chip.

[0053] FIG. 7B illustrates the error in both the gate voltage and drain voltage of a memory cell caused by a source line voltage drop.

[0054] FIG. 8 illustrates the effect of source bias errors in an example population distribution of a page of memory cells for a 4-state memory.

[0055] FIG. 9A illustrates an arrangement in which a bit line voltage control and/or a word line voltage control are compensated for source bias by having a reference point at the node where cell source signal accesses the source lines, according to one

preferred embodiment of the invention.

**[0056]** **FIG. 9B** illustrates a bit line voltage control and a word line voltage control are compensated for source bias by referencing with respect to a page source line, according to another preferred embodiment of the invention.

**[0057]** **FIG. 10** is a schematic diagram of a preferred sense module shown in **FIGs. 9A** and **9B** that operates in combination with the tracking bit line voltage control circuit to provide a bit line voltage compensated for source bias.

**[0058]** **FIG. 11** illustrates a preferred embodiment of the tracking bit line voltage control circuit shown in **FIGs. 9A** and **9B**.

**[0059]** **FIG. 12** illustrates a preferred embodiment of the tracking word line voltage control circuit shown in **FIGs. 9A** and **9B**.

**[0060]** **FIG. 13** shows a portion of a NAND array of memory cells simplified for use in illustrating the use of a regulated source potential.

**[0061]** **FIG. 14** illustrates the application of a compensatory bit line bias.

**[0062]** **FIGs. 15A-C** illustrate the use of a regulator to set the source line potential independently of the current in the source line or the resistance in its path to ground.

**[0063]** **FIG. 16** illustrates the use of a clamp to set the source line potential.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

**[0064]** **FIG. 6A** illustrates schematically a compact memory device having a bank of read/write circuits, which provides the context in which the present invention is implemented. The memory device includes a two-dimensional array of memory cells 300, control circuitry 310, and read/write circuits 370. The memory array 300 is addressable by word lines via a row decoder 330 and by bit lines via a column decoder 360. The read/write circuits 370 is implemented as a bank of sense modules 480 and allows a block (also referred to as a “page”) of memory cells to be read or

programmed in parallel. In a preferred embodiment, a page is constituted from a contiguous row of memory cells. In another embodiment, where a row of memory cells are partitioned into multiple blocks or pages, a block multiplexer 350 is provided to multiplex the read/write circuits 370 to the individual blocks.

**[0065]** The control circuitry 310 cooperates with the read/write circuits 370 to perform memory operations on the memory array 300. The control circuitry 310 includes a state machine 312, an on-chip address decoder 314 and a power control module 316. The state machine 312 provides chip level control of memory operations. The on-chip address decoder 314 provides an address interface between that used by the host or a memory controller to the hardware address used by the decoders 330 and 370. The power control module 316 controls the power and voltages supplied to the word lines and bit lines during memory operations.

**[0066]** **FIG. 6B** illustrates a preferred arrangement of the compact memory device shown in **FIG. 6A**. Access to the memory array 300 by the various peripheral circuits is implemented in a symmetric fashion, on opposite sides of the array so that access lines and circuitry on each side are reduced in half. Thus, the row decoder is split into row decoders 330A and 330B and the column decoder into column decoders 360A and 360B. In the embodiment where a row of memory cells are partitioned into multiple blocks, the block multiplexer 350 is split into block multiplexers 350A and 350B. Similarly, the read/write circuits are split into read/write circuits 370A connecting to bit lines from the bottom and read/write circuits 370B connecting to bit lines from the top of the array 300. In this way, the density of the read/write modules, and therefore that of the bank of sense modules 480, is essentially reduced by one half.

**[0067]** The entire bank of  $p$  sense modules 480 operating in parallel allows a block (or page) of  $p$  cells along a row to be read or programmed in parallel. One example memory array may have  $p = 512$  bytes (512x8 bits). In the preferred embodiment, the block is a run of the entire row of cells. In another embodiment, the block is a subset of cells in the row. For example, the subset of cells could be one half of the entire row or one quarter of the entire row. The subset of cells could be a run of contiguous cells or one every other cell, or one every predetermined number of cells. Each sense

module includes a sense amplifier for sensing the conduction current of a memory cell. A preferred sense amplifier is disclosed in United States Patent Publication No. 2004-0109357-A1, the entire disclosure of which is hereby incorporated herein by reference.

### SOURCE LINE ERROR MANAGEMENT

**[0068]** One potential problem with sensing memory cells is source line bias. When a large number memory cells are sensed in parallel, their combine currents can result in significant voltage drop in a ground loop with finite resistance. This results in a source line bias which causes error in a sensing operation employing threshold voltage sensing. Also, if the cell is operating close to the linear region, the conduction current is sensitive to the source-drain voltage once in that region, and the source line bias will cause error in a sensing operation when the drain voltage is offset by the bias.

**[0069]** **FIG. 7A** illustrates a conventional arrangement in which a bit line voltage control, a word line voltage control and a source voltage control are all referencing from the same ground of the IC memory chip. The read/write circuits 370 operate on a page of memory cells simultaneously. Each sense module 480 in the read/write circuits is coupled to a corresponding cell via a bit line, such as a bit line 36. For example, a sense module 480 senses the conduction current  $i_1$  (source-drain current) of a memory cell 10. The conduction current flows from the sense module through the bit line 36 into the drain of the memory cell 10 and out from the source 14 before going through a source line 34 and a consolidated source line 40 and then to the chip's ground 401 via a source control circuit 400. The source line 34 typically joins all the sources of the memory cells in a page along a row in a memory array. In an integrated circuit chip, the source lines 34 of the individual rows in a memory array are all tied together as multiple branches of the consolidated source line 40 connected to the source control circuit 400. The source control circuit 400 has a pull-down transistor 402 controlled to pull the consolidated source line 40 to the chip's ground 401, which is ultimately connected to an external ground pad (e.g. Vss pad) of the memory chip. Even when metal strapping is used to reduce the resistance of the source line, a non-zero resistance  $R$  remains between the source electrode of a

memory cell and the ground pad. Typically, the average ground loop resistance  $R$  can be as high as 50 ohm.

**[0070]** For the entire page of memory being sensed in parallel, the total current flowing through the consolidated source line 40 is the sum of all the conduction currents, i.e.  $i_{TOT} = i_1 + i_2 + \dots + i_p$ . Generally each memory cell has a conduction current dependent on the amount of charge programmed into its charge storage element. For a given control gate voltage of the memory cell, a smaller programmed charge will yield a comparatively higher conduction current (see **FIG. 4.**) When a finite resistance exists in the path between the source electrode of a memory cell and the ground pad, the voltage drop across the resistance is given by  $V_{drop} \sim i_{TOT} R$ .

**[0071]** For example, if 4,256 bit lines discharge at the same time, each with a current of 1  $\mu$ A, then the source line voltage drop will be equal to 4000 lines  $\times$  1  $\mu$ A/line  $\times$  50 ohms  $\sim$  0.2 volts. This means instead of being at ground potential, the effective source is now at 0.2V. Since the bit line voltage and the word line voltage are referenced with respect to the same chip's ground 401, this source line bias of 0.2 volts will have both the effective drain voltage and control gate voltage reduced by 0.2V.

**[0072]** **FIG. 7B** illustrates the error in the threshold voltage level of a memory cell caused by a source line voltage drop. The threshold voltage  $V_T$  supplied to the control gate 30 of the memory cell 10 is relative to the chip's ground 401. However, the effective  $V_T$  seen by the memory cell is the voltage difference between its control gate 30 and source 14. There is a difference of approximately  $V_{drop}$  or  $\Delta V$  between the supplied and effective  $V_T$  (ignoring the smaller contribution of voltage drop from the source 14 to the source line.) This  $\Delta V$  or source line bias will contribute to a sensing error of, for example 0.2 volts when threshold voltages of the memory cells are sensed. This bias cannot be easily removed as it is data-dependent, i.e., dependent on the memory states of the memory cells of the page.

**[0073]** **FIG. 7B** also illustrates the error in the drain voltage level of a memory cell caused by a source line voltage drop. The drain voltage applied to the drain 16 of the memory cell 10 is relative to the chip's ground 401. However, the effective drain

voltage,  $V_{DS}$ , seen by the memory cell is the voltage difference between its drain 16 and source 14. There is a difference of approximately  $\Delta V$  between the supplied and effective  $V_{DS}$ . This  $\Delta V$  or source line bias will contribute to a sensing error when the memory cells are sensed in an operating region sensitive to  $V_{DS}$ . As described above, this bias cannot be easily removed as it is data-dependent, i.e., dependent on the memory states of the memory cells of the page.

[0074] FIG. 8 illustrates the effect of source bias errors in an example population distribution of a page of memory cells for a 4-state memory. Each cluster of memory state is programmed within a range of conduction currents  $I_{SD}$  clearly separated from each other. For example, a breakpoint 381 is a demarcating current value between two clusters, respectively representing the "1" and "2" memory states. A necessary condition for a "2" memory state will be that it has a conduction current less than the breakpoint 381. If there were no source line bias, the population distribution with respect to the supplied threshold voltage  $V_T$  will be given by the curve with the solid line. However, because of the source line bias error, the effective threshold voltage of each of the memory cells at its control gate is reduced from the supplied voltage relative to ground by the source line bias  $\Delta V$ . Similarly, the effective drain voltage is also reduced from the supplied voltage by the source line bias.

[0075] The source line bias results in a shifting of the distribution (broken line) towards a higher supplied  $V_T$  to make up for the shortfall in the effective voltage. The shifting will be more for that of the higher (lower current) memory states. If the breakpoint 381 is designed for the case without source line error, then the existence of a source line error will have some of the tail end of "1" states having conduction currents to appear in a region of no conduction, which means higher than the breakpoint 381. This will result in some of the "1" states (more conducting) being mistakenly demarcated as "2" states (less conducting.)

#### DRAIN COMPENSATION OF SOURCE LINE BIAS

[0076] According to one aspect of the invention, when a page of memory cells are sensed in parallel and their sources are coupled together to receive the cell source signal at an aggregate access node, the operating voltage supplied to the bit line has

the same reference point as the aggregate access node rather than the chip's ground. In this way any source bias differences between the aggregate access node and the chip's ground will be tracked and compensated for in the supplied bit line voltage.

[0077] Generally, the source path from each memory cell to the chip's ground varies over a range since each memory cell will have a different network path to the chip's ground. Also the conduction current of each memory cell depends on the data programmed into it. Even among the memory cells of a page, there will be some variations in the source bias. However, when the reference point is taken as close to the memory cells' sources as possible, the errors will at least be minimized.

[0078] **FIG. 9A** illustrates an arrangement in which a bit line voltage control and/or a word line voltage control are compensated for source bias by having a reference point at the node where cell source signal accesses the source lines, according to one preferred embodiment of the invention. Similar to **FIG. 7A**, the read/write circuits 370 operate on a page of memory cells simultaneously. Each sense module 480 in the read/write circuits is coupled to a corresponding cell via a bit line, such as a bit line 36. A page source line 34 is coupled to the source of each memory cell of the page along a row in the memory array. Multiple rows have their page source lines coupled together and to the source control circuit 400 via an aggregate access node 35. The source control circuit 400 has a pull-down transistor 402 controlled to pull the aggregate access node 35 and therefore the page source line 34 to the chip's ground 401 through a ground path formed by a consolidated source line with resistance  $R_S$ . The ground 401 is ultimately connected to an external ground pad (e.g. Vss pad) of the memory chip. Thus, the source control circuit 400 controls the cell source signal at the aggregate access node 35. Due to the finite resistance ground path, the cell source signal is not at 0V but has a source bias of  $\Delta V_1$ .

[0079] A bit line voltage control embodied as a tracking bit line voltage clamp 700 is implemented to compensate for the data dependent source bias. This is accomplished by generating an output voltage  $V_{BLC}$  in an output 703 that is referencing at the same point as the cell source signal at the aggregate access node 35 instead of the external ground pad. In this way, at least the source bias due to the resistance  $R_S$  of the

consolidated source line is eliminated.

**[0080]** According to another aspect of the invention, when a page of memory cells are sensed in parallel and their sources are coupled to the same page source line, the operating voltage supplied to the bit line is referenced with respect to an access node of the page source line rather than the chip's ground. In this way any source bias differences from the page access node to the chip's ground will be tracked and compensated for in the supplied bit line voltage.

**[0081]** **FIG. 9B** illustrates a bit line voltage control and a word line voltage control are compensated for source bias by referencing with respect to a page source line, according to another preferred embodiment of the invention.

**[0082]** The arrangement is similar to that of **FIG. 9A** except the reference point for the bit line voltage control 700 and word line voltage control 800 is now taken essentially at the selected page source line. A page source line multiplexor 780 is used to selectively couple the selected page source line to a page access node 37, which serves as the reference point.

**[0083]** A bit line voltage control embodied as a tracking bit line voltage clamp 700 is implemented to compensate for the data dependent source bias. This is accomplished by generating an output voltage  $V_{BLC}$  in an output 703 that is referencing with respect to the voltage at the access node 38 of the page source line 34 instead of referencing to the external ground pad. In this way, the source bias is better corrected due the location of the reference point at the access node 37, which is specific to the page.

**[0084]** **FIG. 10** is a schematic diagram of a preferred sense module shown in **FIGs. 9A** and **9B** that operates in combination with the tracking bit line voltage control circuit to provide a bit line voltage compensated for source bias. In the example shown, the sense module 480 senses the conduction current of a memory cell in a NAND chain 50 via a coupled bit line 36. It has a sense node 481 that can be selectively coupled to a bit line, a sense amplifier 600 or a readout bus 499. Initially, an isolation transistor 482, when enabled by a signal BLS connects the bit line 36 to the sense node 481. The sense amplifier 600 senses the sense node 481. The sense

amplifier includes a precharge/clamp circuit 640, a cell current discriminator 650 and a latch 660.

**[0085]** The sense module 480 enables the conduction current of the selected memory cell in the NAND chain to be sensed. The conduction current is a function of the charge programmed into the memory cell and the applied  $V_T(i)$  when there exists a nominal voltage difference between the source and drain of the memory cell. Prior to sensing, the voltages to the gates of the selected memory cell must be set via the appropriate word lines and bit line.

**[0086]** The precharge operation starts with the unselected word line charging to a voltage  $V_{read}$  followed by charging the selected word line to a predetermined threshold voltage  $V_T(i)$  for a given memory state under consideration.

**[0087]** Then the precharged circuit 640 brings the bit line voltage to a predetermined drain voltage appropriate for sensing. This will induce a source-drain conduction current to flow in the selected memory cell in the NAND chain 50, which is detected from the channel of the NAND chain via a coupled bit line 36.

**[0088]** When the  $V_T(i)$  voltage is stable, the conduction current or the programmed threshold voltage of the selected memory cell can be sensed via the coupled bit line 36. The sense amplifier 600 is then coupled to the sense node to sense the conduction current in the memory cell. The cell current discriminator 650 serves as a discriminator or comparator of current levels. It effectively determines whether the conduction current is higher or lower than a given demarcation current value  $I_0(j)$ . If it is higher, the latch 660 is set to a predetermined state with the signal INV = 1.

**[0089]** A pull-down circuit 486 is activated in response to the latch 660 setting the signal INV to HIGH. This will pull down the sense node 481 and therefore the connected bit line 36 to ground voltage. This will inhibit the conduction current flow in the memory cell 10 irrespective of the control gate voltage since there will be no voltage difference between its source and drain.

**[0090]** As shown in **FIGs. 9A and 9B**, there will be a page of memory cells being operated on by a corresponding number of sense modules 480. A page controller 498

supplies control and timing signals to each of the sense modules. The page controller 498 cycles each of the sense module 480 through a predetermined sequence of operations and also supplies a predetermined demarcation current value  $I_0(j)$  during the operations. As is well known in the arts, the demarcation current value can also be implemented as a demarcation threshold voltage, or time period for sensing. After the last pass, the page controller 498 enables a transfer gate 488 with a signal NCO to read the state of the sense node 481 as sensed data to a readout bus 499. In all, a page of sense data will be read out from all the multi-pass modules 480. Similar sense modules have been disclosed in US Patent Application No. 11/015,199 filed December 16, 2004 by Cernea et al., entitled "IMPROVED MEMORY SENSING CIRCUIT AND METHOD FOR LOW VOLTAGE OPERATION". The entire disclosure of US Patent Application No. 11/015,199 is herein incorporated by reference.

**[0091]** The sense module 480 incorporates a constant voltage supply and maintains the bit line at constant voltage during sensing in order to avoid bit line to bit line coupling. This is preferably implemented by the bit line voltage clamp 610. The bit line voltage clamp 610 operates like a diode clamp with a transistor 612 in series with the bit line 36. Its gate is biased to a constant voltage  $V_{BLC}$  equal to the desired bit line voltage  $V_{BL}$  above its threshold voltage  $V_{TN}$ . In this way, it isolates the bit line from the sense node 481 and set a constant voltage level for the bit line, such as the desired  $V_{BL} = 0.4$  to  $0.7$  volts. In general the bit line voltage level is set to a level such that it is sufficiently low to avoid a long precharge time, yet sufficiently high to avoid ground noise and other factors such as operating in the saturated region where  $V_{DC}$  is above  $0.2$  volts.

**[0092]** Thus, when operating at a low  $V_{BL}$ , especially one that approaching the linear region, it is important that  $V_{BL}$  is accurately rendered, as small variations can lead to significant changes in conduction currents. This means  $V_{BLC} = V_{BL} + V_{TN}$  must be accurately set to minimize the source line bias.

**[0093]** **FIG. 11** illustrates a preferred embodiment of the tracking bit line voltage control circuit shown in **FIGs. 9A** and **9B**. The tracking bit line voltage control circuit 700 basically provides an output voltage  $V_{BLC}$  on an output line 703. The

output voltage is essentially generated by a reference current  $I_{REF}$  across an adjustable resistor R 720. A cascode current mirror circuit 730 is employed to maintain  $I_{REF}$  constant over the range of  $V_{BLC}$ . The cascode current mirror circuit 730 has two branches, with a first branch formed by two n-transistors 732, 734 connected as diodes in series and a second, mirrored branch formed by two other n-transistors 736, 738 connected in series. The gates of the transistors 732 and 736 are interconnected, and the gates of the transistors 734 and 738 are interconnected. An  $I_{REF}$  source is connected to the drain of the transistor 732 so that  $I_{REF}$  flows down the first branch and is also mirrored in the second branch. A  $V_{HIGH}$  source is connected to the drain of the transistor 736. The sources of the transistors 734 and 738 are interconnected to form a base rail 701.

**[0094]** The output voltage is taken from a tap between the serially connected transistors 736 and 738. If the voltage of the base rail 701 is at  $V1$ , then  $V_{BLC} = V1 + V_{TN}$ . This is because the voltage on the drain of the transistor 734 is  $V1$  plus a threshold voltage of the n-transistor, and the same  $I_{REF}$  is also mirrored in the second branch, resulting in the same voltage appearing on the drain of the transistor 738.

**[0095]** The voltage  $V1$  at the base rail 701 is set by the voltage drop across the resistor R 720 due to the current  $2I_{REF}$  plus a base voltage at the node 721. The base voltage at node the 721 is selectable by a base voltage selector 740. The base voltage selector 740 selectively connects the node 721 to the aggregate access node 35 (see **FIG. 9A**) or to the page access node 37 of the page source line (see **FIG. 9B**) via a transistor 742 when a control signal ConSL is asserted at its gate. Alternatively, the selector circuit 720 selectively connects the node 721 to ground 401 via a transistor 744 when a control signal ConGND is asserted at its gate. Thus, it will be seen that when the signal ConSL is asserted,  $V1 = \Delta V_1 + 2I_{REF} R$ , and the output of the tracking bit line voltage control circuit,  $V_{BLC} = \Delta V_1 + 2I_{REF} R + V_{TN}$ . In the case of controlling the bit line voltage clamp 610 (see **FIG. 10**), the n-transistor 734 is chosen to have the same  $V_{TN}$  as that of the transistor forming the bit line voltage clamp 610. The resistor R is then adjusted so that the desired bit line voltage  $V_{BL}$  is set by  $2I_{REF} R$ . By referencing with respect to the aggregate access node 35 or the page access node 37, a significant portion of source bias  $\Delta V_1$  that is above ground potential will be

compensated automatically in  $V_{BLC}$ .

#### CONTROL GATE COMPENSATION OF SOURCE LINE BIAS

**[0096]** According to yet another aspect of the invention, when a page of memory cells are sensed in parallel and their sources are coupled together to receive the cell source signal at an aggregate access node, the operating voltage supplied to the word line has the same reference point as the aggregate access node rather than the chip's ground. In this way any source bias differences between the aggregate access node and the chip's ground will be tracked and compensated for in the supplied word line voltage.

**[0097]** As shown in **FIG. 9A**, a word line voltage control embodied as a tracking word line voltage clamp 800 is implemented to compensate for the data dependent source bias. This is accomplished by generating an output voltage  $V_{WL}$  in an output 803 that is referencing at the same point as the cell source signal at the aggregate node 35 instead of the external ground pad. In this way, at least the source bias due to the resistance of the consolidated source line (see **FIG. 7A**) is eliminated.

**[0098]** According to yet another aspect of the invention, when a page of memory cells are sensed in parallel and their sources are coupled to the same page source line, the operating voltage supplied to the word line is referenced with respect to an access node of the page source line rather than the chip's ground. In this way any source bias differences from the page access node to the chip's ground will be tracked and compensated for in the supplied word line voltage.

**[0099]** As shown in **FIG. 9B**, a word line voltage control embodied as a tracking word line voltage clamp 800 is implemented to compensate for the data dependent source bias. This is accomplished by generating an output voltage  $V_{WL}$  in an output 803 that is referencing at the same point as the access node 38 to the selected page source line instead of the external ground pad. In this way, the source bias is better corrected due the location of the reference point at the access node 38, which is specific to the page.

**[0100]** **FIG. 12** illustrates a preferred embodiment of the tracking word line voltage control circuit shown in **FIGs. 9A** and **9B**. The tracking word line voltage

control circuit 800 essentially uses a potential divider on a reference voltage to obtain a desired output voltage  $V_{WL}$  on an output 803. A reference voltage  $V_{REF}$  is provided by a VREF circuit 820.  $V_{REF}$  is driven by a regulated output driver 830. The output level of the driven  $V_{REF}$  is controlled by a DAC-controlled potential divider 840 to produce a programmed  $V_{WL}$  at the output 803.

**[0101]** The regulated output driver 830 includes a p-transistor 832 driving an output from a comparator 834. The drain of the p-transistor 832 is connected to a voltage source,  $V_{HIGH}$  and its gate is controlled by the output of the comparator 834. The comparator 834 receives  $V_{REF}$  at its “-” terminal and compares it with a signal fed back from the source of the p-transistor. Also, a capacitor 836 is used to AC couple the output of the comparator with the “+” terminal. If the voltage at the source of the p-transistor 832 is less than  $V_{REF}$ , the output of the comparator is low, turning on the p-transistor 832, which results in the voltage at the source rising to the level of  $V_{REF}$ . On the other hand, if  $V_{REF}$  is exceeded, the comparator output will turn off the p-transistor 832 to effect regulation, so that a driven, regulated  $V_{REF}$  appears across the potential divider 840. The potential divider 840 is formed by a series of resistors; each tap between any two resistors is switchable to the output 803 by a transistor such as transistor 844 that is turned on by a signal such as DAC1. In this way, by selectively connecting the output 803 to a tap in the potential divider, a desired fraction of  $V_{REF}$  can be obtained; i.e.,  $(n*r/r_{TOT})*V_{REF}$ , where  $n$  is the number of  $r$  DAC setting selected.

**[0102]**  $V_{REF}$  and therefore  $V_{WL}$  are referenced with respect to a node 821. The base voltage at the node 821 is selectable by a base voltage selector 850. The base voltage selector 740 selectively connects the node 721 to the aggregate access node 35 (see **FIG. 9A**) or to the page access node 37 of the page source line (see **FIG. 9B**) via a transistor 742 when a control signal ConSL is asserted at its gate. Alternatively, the selector circuit 850 selectively connects the node 821 to ground 401 via a transistor 854 when a control signal ConGND is asserted at its gate. Thus, it will be seen that when the signal ConSL is asserted,  $\Delta V_1$  will appear at the node 821, which will become the base voltage for the VREF circuit 820 and the voltage divider 840. Therefore the output of the tracking word line voltage control circuit 800 will have

$V_{WL} = (n * r / r_{TOT}) * V_{REF} + \Delta V_1$ . By referencing with respect to the aggregate access node 35 or the page access node 37, a significant portion of source bias  $\Delta V_1$  that is above ground potential will be compensated automatically in  $V_{WL}$ .

**[0103]** The tracking voltage control circuit 800 can alternatively be employed to track the source bias for the  $V_{BLC}$  used in controlling the bit line voltage clamp 610 (see **FIG. 10**). Essentially, the output voltage is set to provide  $V_{BL} + V_{TN} + \Delta V_1$ .

#### REGULATED SOURCE POTENTIAL

**[0104]** The present section a set of alternate embodiments that introduce elements that regulate the source potential. A first set embodiments rely upon using a feedback circuit that senses the source potential and regulates it to be constant at a certain voltage, such as, say 0.5V or 1.0V. An alternate set embodiments use a non-linear resistive element (e.g., a diode) to place the source line at a level above ground. It should be noted that the embodiments of the present section are complementary to those presented in the preceding sections (and developed further in US patents 7,173,854 and 7,170,784), in that they may be utilized alone or in combination.

**[0105]** **FIG. 13** includes many of the elements from earlier figures, but simplified for the present discussion by not explicitly showing a number of circuit elements. Several representative NAND strings 50 are shown connected their corresponding bit lines 36 through drain terminal 56. It should be noted that although a given NAND string, or more generally a given memory cell, is shown directly connected to the source line 940, there will typically be a number of intervening elements (other memory cells in a NAND string, select gates, various switches or multiplexors, etc.) through with the source of the memory cells of a selected page are connected to the source line of the page (34 in **FIG. 7A**) and from then on into the composite source line 940. For this discussion, the various bit line bias and sense amp circuits are schematically represent by the circle 480, one of which is indicated as selected (Sel.). The consolidated source line 940 accepts the current for all of the cells of what will be called a “structural block” and corresponds to element 40 of **FIGs. 7A and 9A**. The current  $I_{CS}$  along this source line 940 will the pass through the source isolation switch 402 to the chip’s ground (401 in earlier figures). Here the various resistances that

cause the source line to become elevated by  $\Delta V$ , as discussed above with respect to **FIG. 7B** are lumped together as  $R_{CS}$  901, so that  $\Delta V = I_{CS} \times R_{CS}$ .

**[0106]** In the preceding sections, the referencing of the bit line or word line voltage to the source voltage was primarily discussed in terms of the page, as it was for the bit line or word line circuits that being used to sense a given page that the compensation was needed. In the embodiments of the present section, rather than reference to word line, bit line, or both to a variable  $\Delta V$  value, circuit elements are introduced to hold the source line to a reference value during sensing operations. Consequently, relevant the source line 940 is that of all the elements a structural block that can contribute to the current through the source isolation switch and corresponds to element 40 of **FIGs. 7A and 9A**. Similarly, node 910 should be compared to nodes 35 and 37 in **FIGs. 9A and 9B**, respectively. In the NAND architecture, the physical block can be taken as the collection of NAND strings that span the width of a word line, so the structural block is word line wide and a NAND string long, such as shown in **FIG. 3**. In NOR and other arrangements, it would be that corresponding structure that is drained by a common source line. It should be noted that the structural block used here is defined differently from the “erase block”, or unit of erase, which the more common usage of “block” in a FLASH memory. It may be, and often is, the case that these two structures coincide, but this need not be so in the more general situation.

**[0107]** Returning to **FIG. 13**, the embodiments of this section treat the problem of the potential being raised by a varying amount at the aggregate node 910 by regulating it to be a constant value. For example, as the bounce on the source line for a structural block can be as high as, say, 0.3V in typical current design, by holding node 910 in the range of 0.5V to 1.0V, there will be sufficient headroom so that this bounce will not affect source voltage. A first set of embodiments achieve this using a feedback circuit to regulate the potential at node 910. A second set of embodiments use a non-linear resistive element to the potential at node 910. Although these techniques keep the source line more or less constant at a reference value, any residual variations at node 910 during sensing operations can be compensated for by the techniques of previous sections if desired.

**[0108]** Further, other complimentary techniques can also be combined, such as employing active circuit elements to regulate the voltage difference between the source line 940 and the word lines, the bit lines, the substrate, or some combination of these. Such an approach for using an active circuit element 799 along line 701 to compensate the bit line bias is shown in **FIG. 14**. Although the detail is not shown in this simplified figure, the element 799 would also the appropriate bit line voltage and include a feedback loop. Such an arrangement to compensate the word line voltage is developed in the US patent application entitled “Read, Verify Word Line Reference Voltage to Track Source Level” by Feng Pan, Trung Pham, and Byungki Woo, filed concurrently with the present application, and which provides more detail on suitable circuits.

**[0109]** **FIG. 15A** presents a first embodiment employing that adjusts the potential drop across between the source line 940 at node 910 and the chip’s ground by using an active circuit. The transistor 923 is connected between node 910 and the chip’s ground, its control gate being driven by the op amp 921. The – input of the op amp 921 is connected to a reference voltage, with the + input connected as a feedback loop to the level of the node 910. The net effect of this circuit is to regulate the voltage at the source line 940 to be fixed at the reference value, independent of current on the line or the resistance drop on the path through the source isolation switch 402, so that the relative biases can accurately determined. As will be understood by those in the art, the op amp 921 can be implemented by the standard design and the circuit may include additional elements commonly incorporated as needed for stability and other operational concerns.

**[0110]** Since the circuit elements added to **FIG. 15A** are added to regulate the source potential during sensing operations (read, verify), switches and control circuit (not shown) would typically be included to couple these elements during sensing operations. Additionally, although the implementation is shown for a regulating a single structural block, in alternate versions, when there are multiple structural blocks in a plane, a single such circuit could be used for the plane as a whole. Similarly, a single such circuit could also be used for multiple planes. In this case, the node being regulated by the feedback loop to the reference value would be on the other side of the

switch 402, as this switch is specific to a single block. Conversely, rather than regulate the whole a structural block together at the aggregate source node 910, the individual pages could also be regulated (i.e., regulate each of the source lines 34 of **FIG. 7A** instead of composite line 40) if closer regulation is wanted; however, this would be at the cost of increased circuitry and complexity. These comments also apply to the embodiments of **FIGs. 15 B, 15C, and 16**.

**[0111]** Optionally, the source isolation switch 402 may also be used as part of the pull down circuit by connecting the gate of switch 402 to feedback loop along line 923. This could lead to an area savings as it may then be possible to use a smaller transistor for 923. If switch 402 were chosen properly, in some cases it may be possible to do without 923; however, as the switch 402 has additional functions and, consequently, may be able to be optimized for this regulation function, it is expected that in most cases the transistor 923 would be used to provide or augment the regulation process.

**[0112]** The value chosen for the reference voltage applied to op amp 921 could be taken as ground, which can be preferable in some applications; however, as regulating a voltage to a given level usually uses a range of voltages on either side of the desired level, regulating at 0V would typically require the availability of negative voltages, a complication which is commonly not desired. In most cases it will be more practical to use a reference value somewhat above the highest expected bounce in the source potential that would otherwise occur. For example, if it is expected that the highest value of  $\Delta V$  would be something on the order of 0.3V, then the reference voltage could be taken as 0.5V or 1.0V. The bias levels during read and verify level would then be adjusted to reflect this elevated, but largely constant source bias.

**[0113]** The arrangement of **FIG. 15A** only regulates downward. If the amount of pull-up in the circuit is insufficient, an embodiment such as in **FIG. 15B** can be used. In **FIG. 15B** an uncompensated current source  $I_{bias}$  930 is added to guarantee a minimum bias to improve stability to keep the source potential from falling too low, although at the cost of increased current usage.

**[0114]** In the embodiment of **FIG. 15C**, the current source is brought into the feedback loop. More specifically, the current source 930 is implemented as a PMOS

transistor whose control gate voltage is set by the output of the op amp 921 along path 931. The use of a regulated pull-up element allows for the amount of pull-up, or down, to be more accurately compensated. The choice between the embodiments of **FIGs. 15A-C** as to which would be preferred in a given application would be a design choice that would balance stability, complexity, power consumption, layout area, and so on, as is familiar in circuit design.

**[0115]** An alternate embodiment for maintaining the source potential at an elevated, constant level is shown in **FIG. 16**. In this embodiment, the active elements of **FIGs. 15A-C** are replaced with a non-linear resistive element, such as the diode 950, which could be implemented by diode connected transistor or other familiar arrangement. The use of such a clamp have the advantage of requiring less layout area relative to **FIGs. 15A-C**. In addition to requiring that the diode 950 be properly selected, the basic arrangement shown here lacks the ability to as accurately control for temperature and voltage variations as the active circuit based implementation.

**[0116]** Although the various aspects of the present invention have been described with respect to certain embodiments, it is understood that the invention is entitled to protection within the full scope of the appended claims.

**WHAT IS CLAIMED IS:**

1. In a non-volatile memory device having individual pages of memory cells to be sensed in parallel, each memory cell having a source, a drain, a charge storage unit and a control gate for controlling a conduction current along said drain and source, the memory device comprising:
  - a page source line connectable to the source of each memory cell in a page;
  - an aggregate node coupled to individual page source lines of a structural block;
  - a source isolation switch coupled via said aggregate node to a page source line of a selected page for a memory operation; and
  - a source potential regulation circuit, including an active circuit element having a first input connected to a first reference voltage and having a second input connected as a feedback loop that is connectable to the aggregate node.
2. The memory device of claim 1, wherein the second input is connected to ground reference through a transistor controlled by the output of the active circuit element.
3. The memory device of claim 1, wherein the source isolation switch includes a transistor through which the aggregate node is connected to ground reference, the transistor controlled by the feedback loop
4. The memory device of claim 1, further including control circuitry whereby the feedback loop is connected to the aggregate node during sensing operations.
5. The memory device of claim 1, further comprising:
  - an associated bit line connectable to the drain of each memory cell of said selected page;
  - a bit line voltage supply for providing a predetermined bit line voltage to the associated bit line of each memory cell of said selected page for a sensing operation;
  - a word line connectable to the control gate of each memory cell of said selected page; and

word line voltage supply circuitry to provide a predetermined word line voltage for the word line of each memory cell of said selected page for said sensing operation,

wherein said first reference voltage is independent of the word line and bit line voltages during the sensing operation.

6. The memory device of claim 1, further comprising:  
a pull-up element connectable to the aggregate node.

7. The memory device of claim 6, wherein the pull-up element is regulated by the active circuit element.

8. The memory device of claim 1, wherein the first reference voltage is in a range of from 0.5V to 1.0V.

9. The memory device of claim 1, wherein the first reference voltage is ground reference.

10. The memory device of claim 1, wherein the memory device has a plurality of planes and wherein said source potential regulation circuit is for a first of said planes, others of said planes having distinct source potential regulation circuits.

11. The memory device of claim 1, wherein the memory cells are organized according to a NAND type architecture.

12. In a non-volatile memory device having individual pages of memory cells to be sensed in parallel, each memory cell having a source, a drain, a charge storage unit and a control gate for controlling a conduction current along said drain and source, a method of sensing a page of memory cells, comprising:

providing a page source line;  
coupling the source of each memory cell of said page to said page line source line;

coupling the page source line to a structural block aggregate node for connection to a source voltage control circuit for sensing operation; coupling the aggregate node to a feedback loop of a source potential regulation circuit including an active circuit element having a first input and having a second input connected to the feedback loop; and applying a first reference voltage to said first input.

13. The method of claim 12, wherein the second input is connected to ground reference through a transistor, the method further comprising: controlling said transistor by the output of the active circuit element.

14. The method of claim 12, wherein the source isolation switch includes a transistor through which the aggregate node is connected to ground reference, the method further comprising:

controlling the transistor by the feedback loop.

15. The method of claim 12, further comprising:

connecting the feedback loop to the aggregate node.

16. The method of claim 12, the memory device further having an associated bit line coupling to the drain of each memory cell of said page and a word line coupling to the control gate of each memory cell of said page, the method further comprising:

providing a predetermined bit line voltage to the associated bit line of each memory cell of said page for the sensing operation; and

providing a predetermined word line voltage for the word line of each memory cell of said page for said sensing operation,

wherein said first reference voltage is independent of the word line and bit line voltages during said sensing operation.

17. The method of claim 12, further comprising:

connecting a pull-up element connectable to the aggregate node.

18. The method of claim 17, further comprising:  
regulating the pull-up element by the active circuit element.

19. In a non-volatile memory device having individual pages of memory cells to be sensed in parallel, each memory cell having a source, a drain, a charge storage unit and a control gate for controlling a conduction current along said drain and source, the memory device comprising:

    a page source line connectable to the source of each memory cell in a page;  
    an aggregate node coupled to individual page source lines of a structural block;  
    a source isolation switch coupled via said aggregate node to a page source line of a selected page for a memory operation; and  
    a non-linear resistive element connectable between the aggregate node and ground reference.

20. The memory device of claim 19, wherein the non-linear resistive element is a diode.

21. The memory device of claim 19, further including control circuitry whereby the non-linear resistor element is connected to the aggregate node during sensing operations.

22. In a non-volatile memory device having individual pages of memory cells to be sensed in parallel, each memory cell having a source, a drain, a charge storage unit and a control gate for controlling a conduction current along said drain and source, a method of sensing a page of memory cells, comprising:

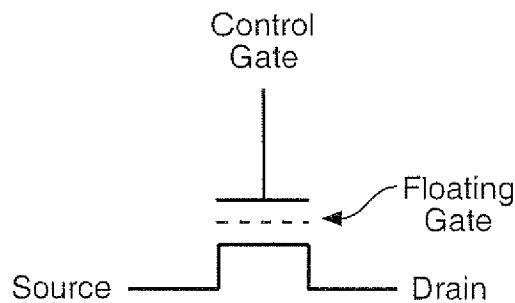
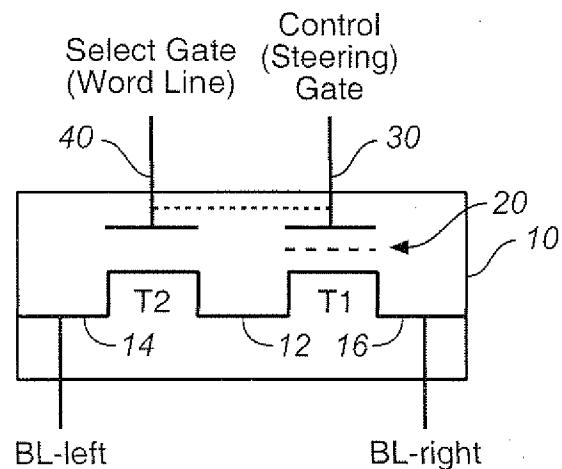
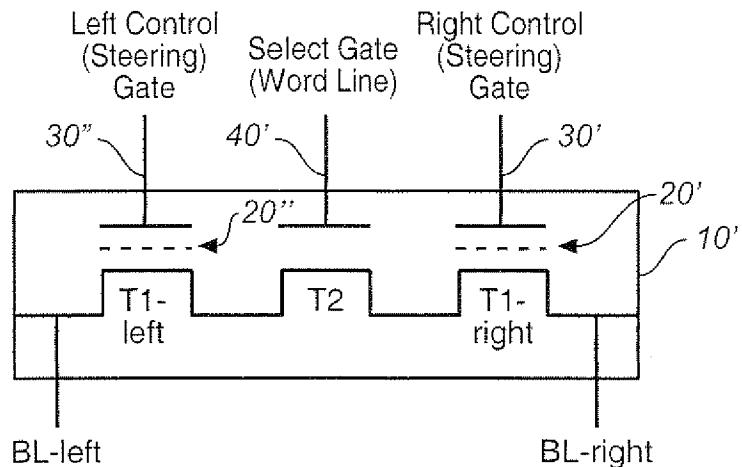
    providing a page source line;  
    coupling the source of each memory cell of said page to said page line source line;  
    coupling the page source line to a structural block aggregate node for connection to a source voltage control circuit for sensing operation; and

coupling the aggregate node to ground reference by a non-linear resistive element connectable.

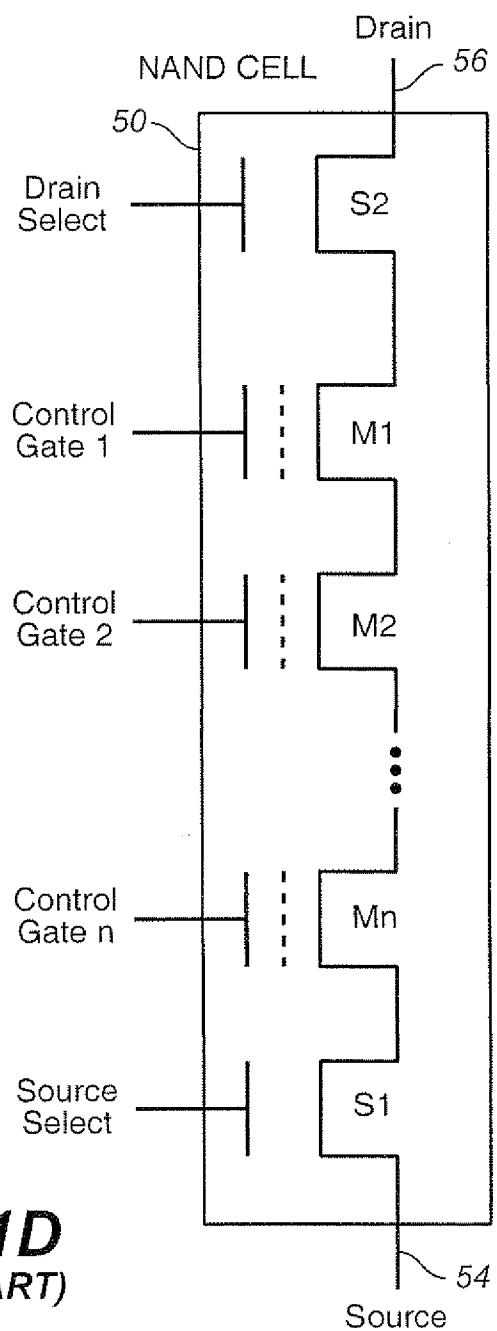
23. The method of claim 22, wherein the non-linear resistive element is a diode.

24. The method of claim 22, further comprising:  
connecting the non-linear resistor element to the aggregate node.

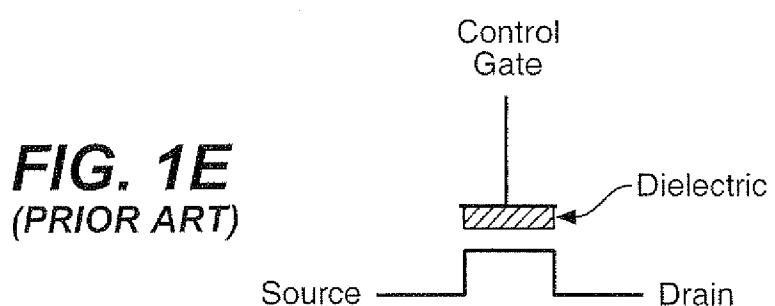
1 / 17

**FIG. 1A (PRIOR ART)****FIG. 1B (PRIOR ART)****FIG. 1C (PRIOR ART)**

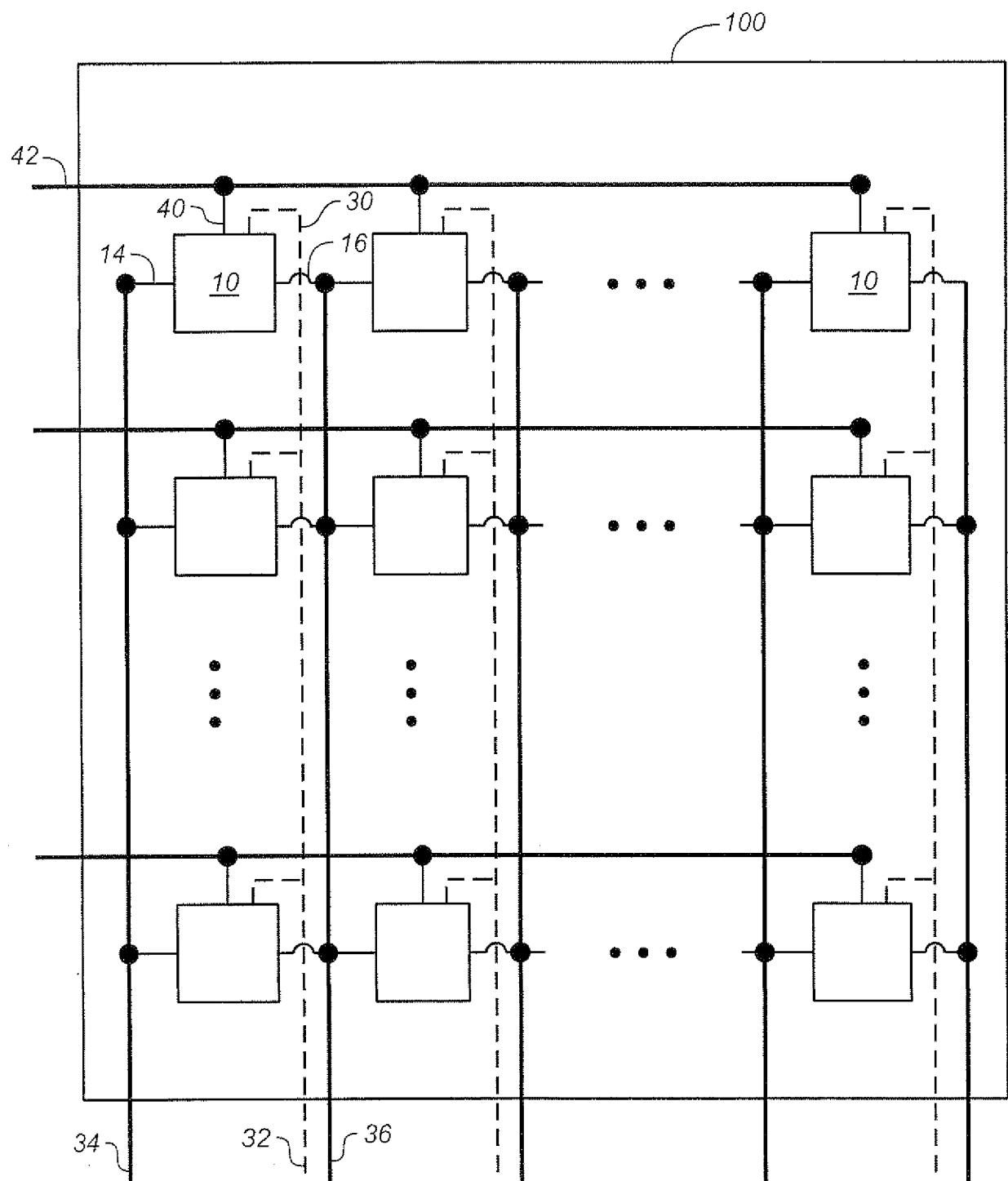
2 / 17



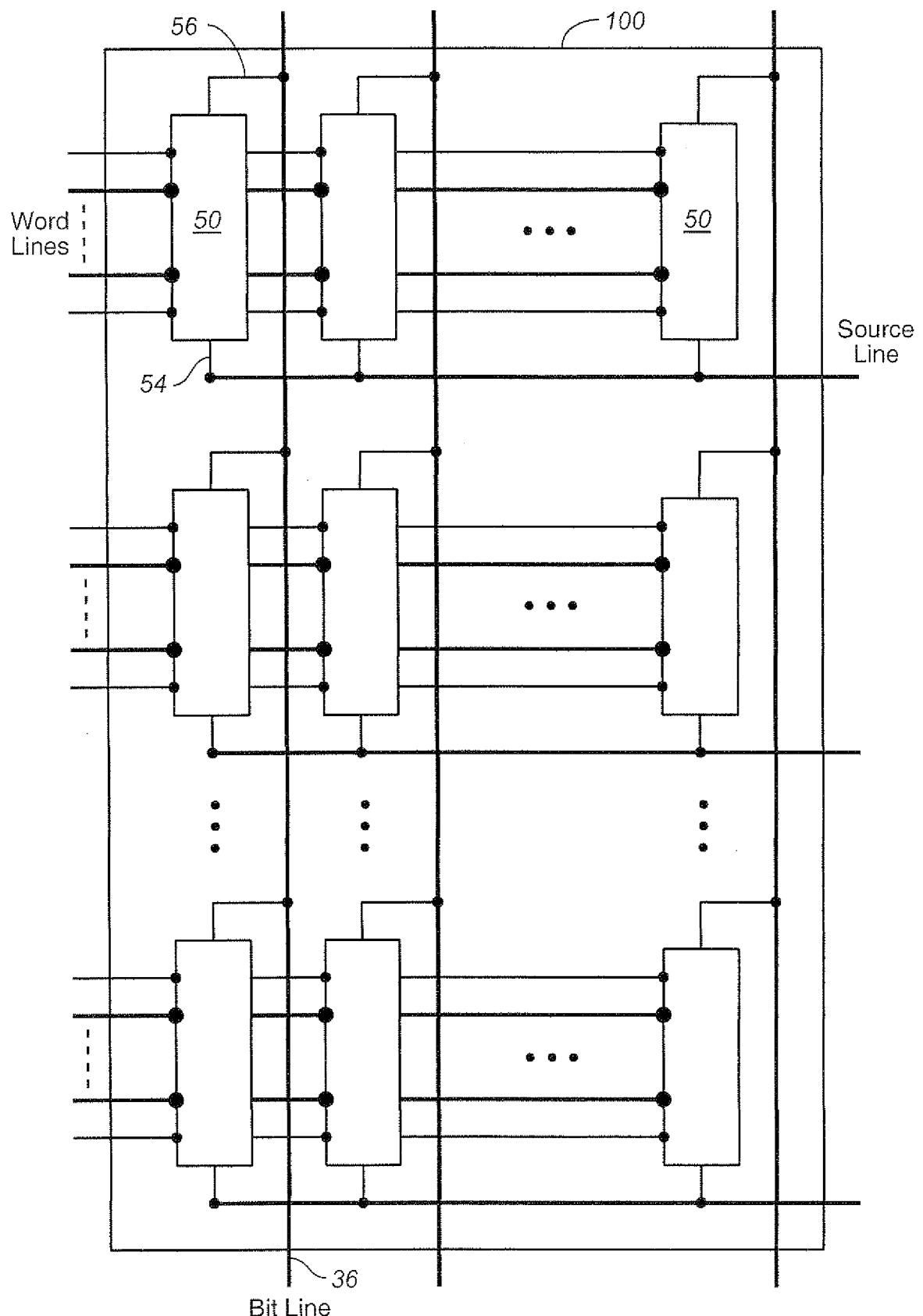
**FIG. 1D**  
(PRIOR ART)



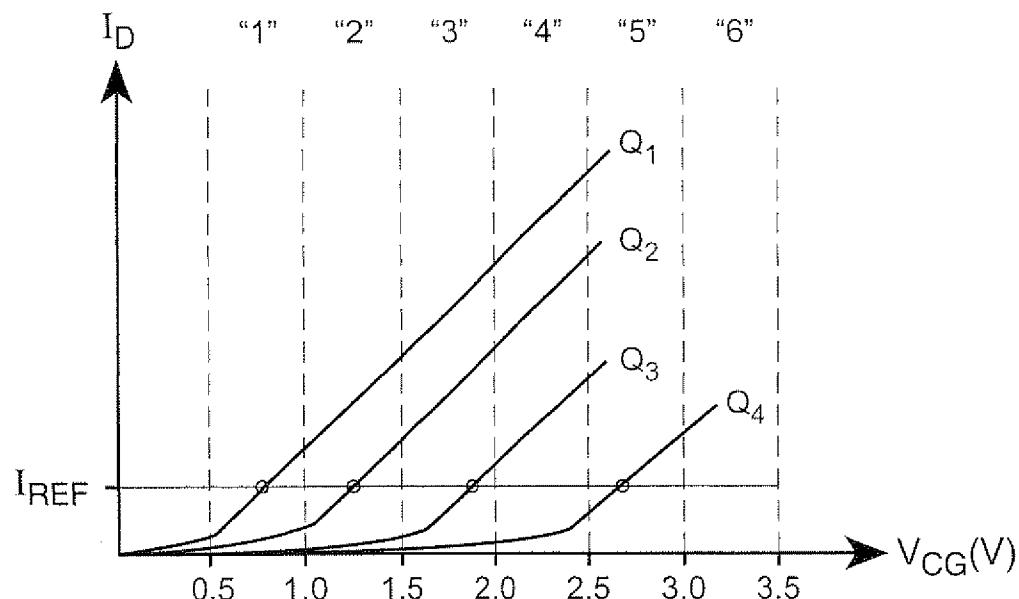
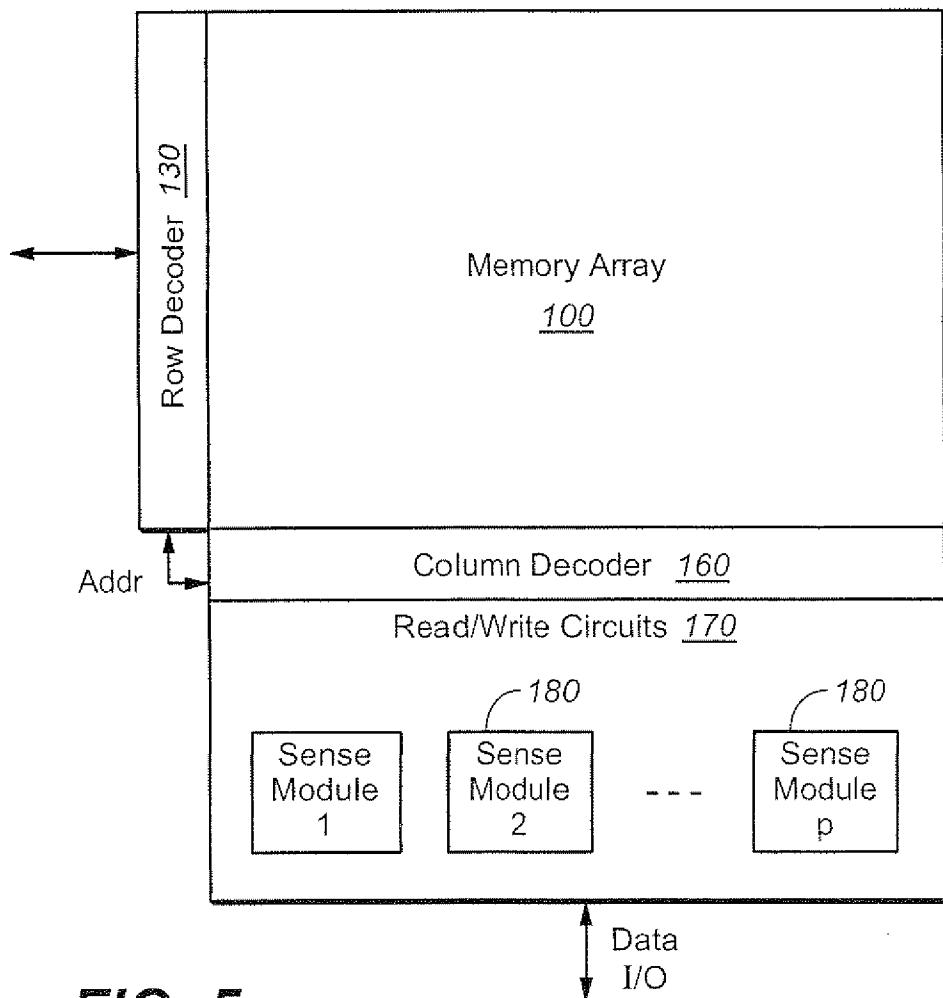
**FIG. 1E**  
(PRIOR ART)

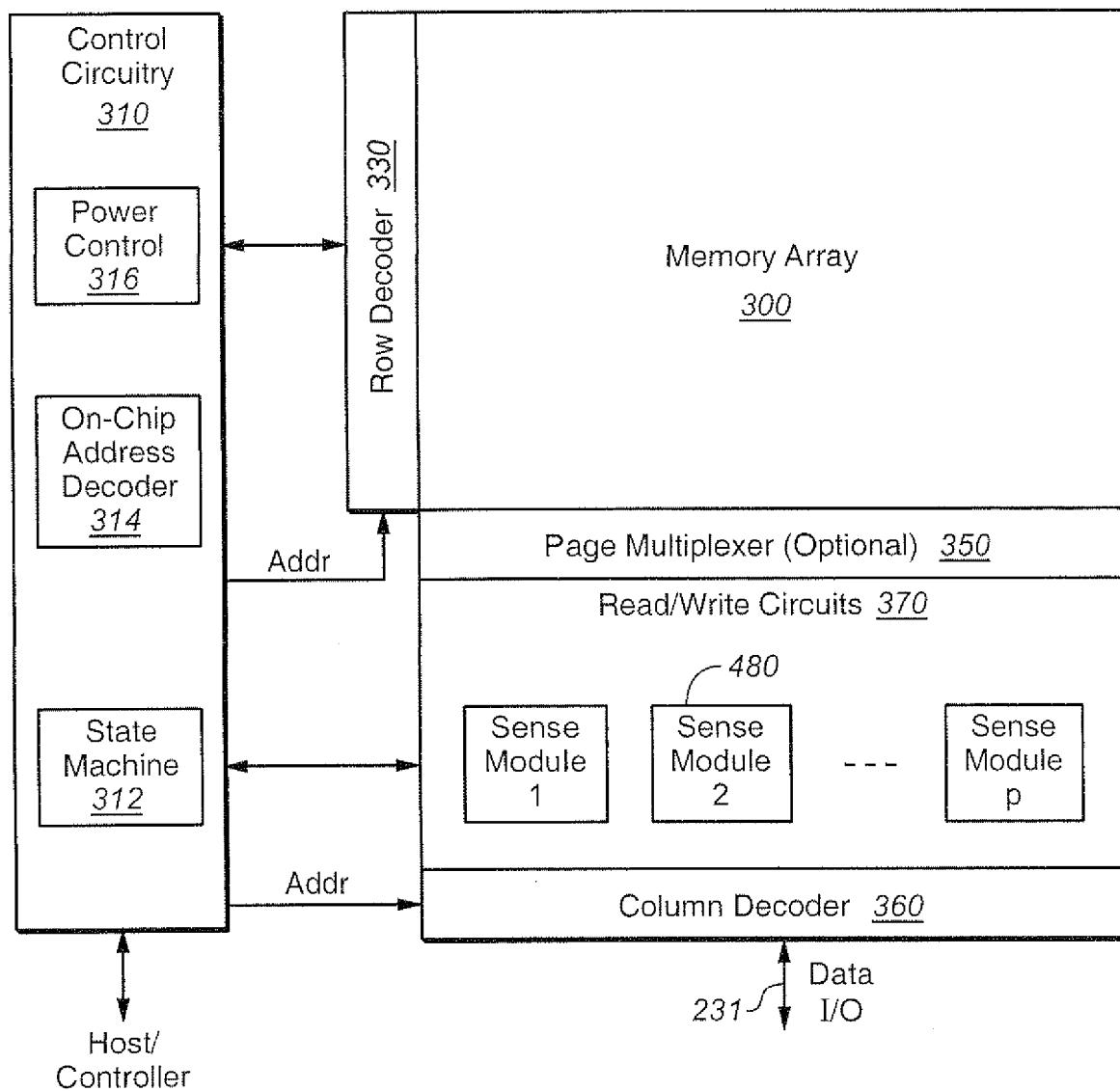


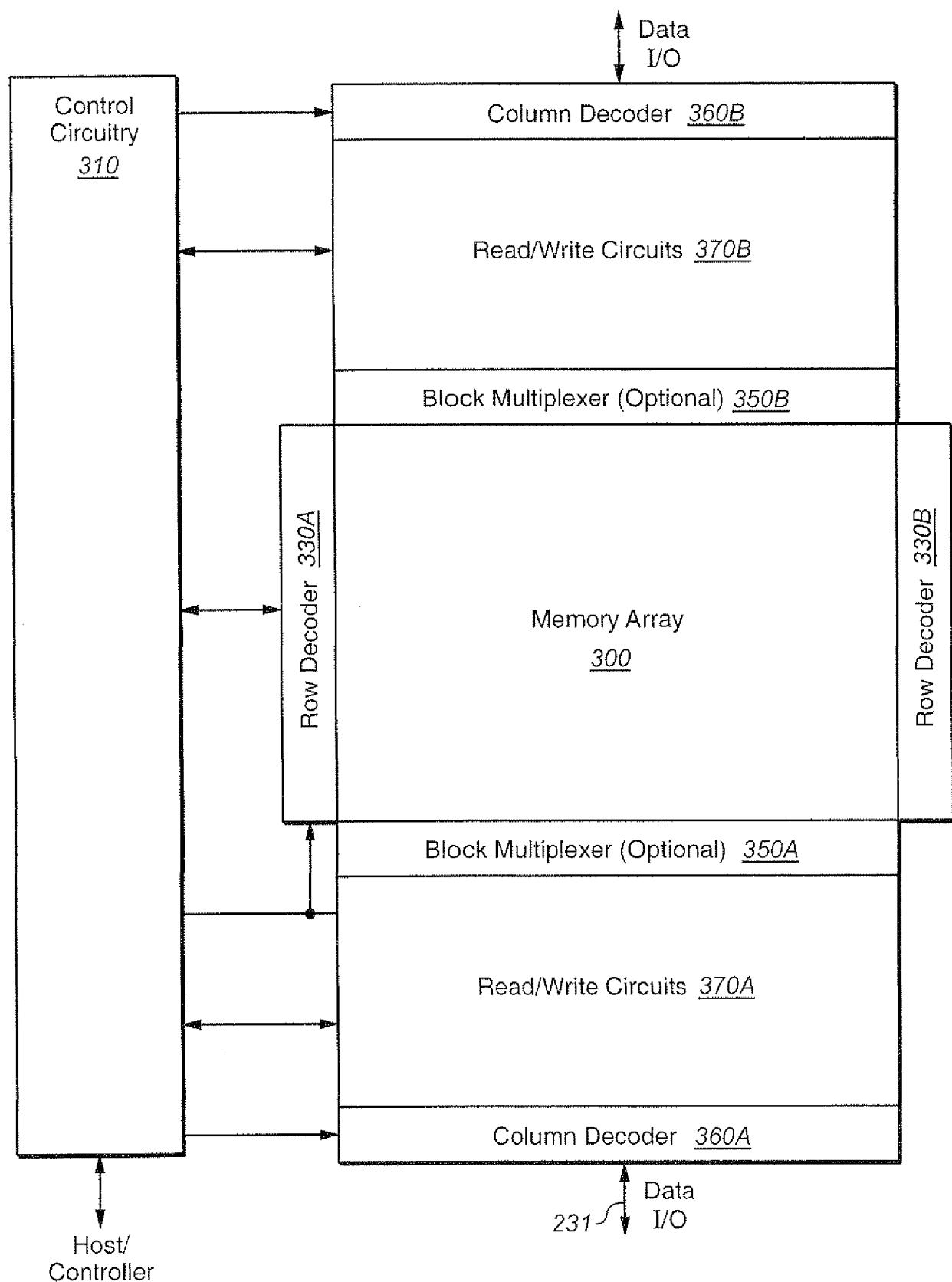
**FIG. 2**  
(PRIOR ART)

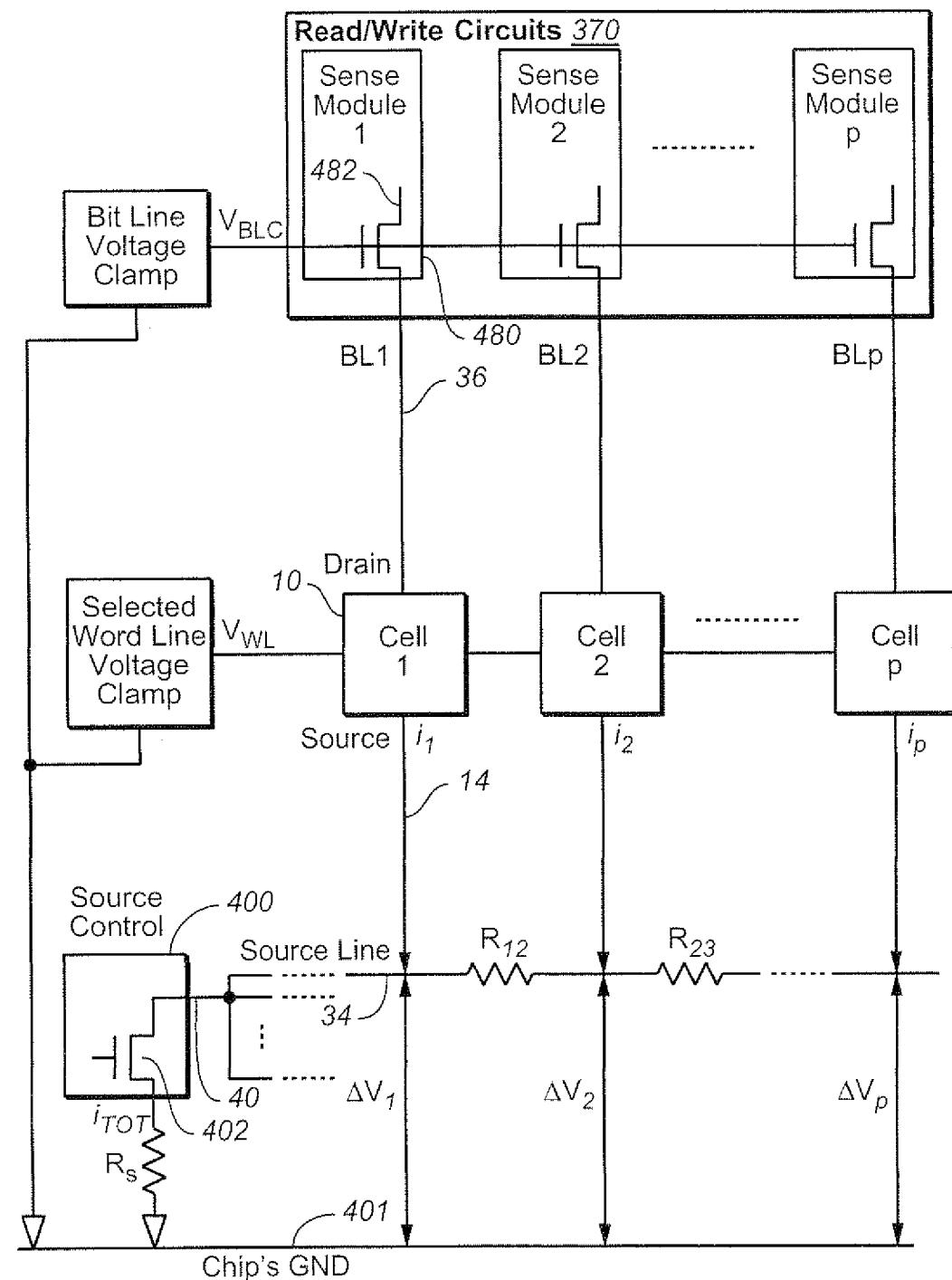


**FIG. 3 (PRIOR ART)**

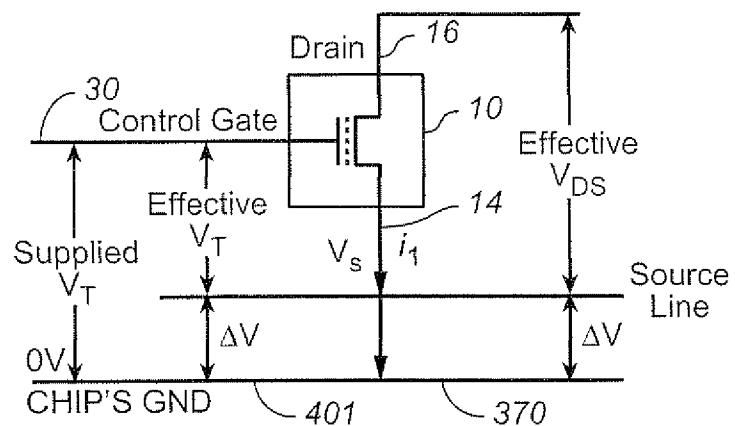
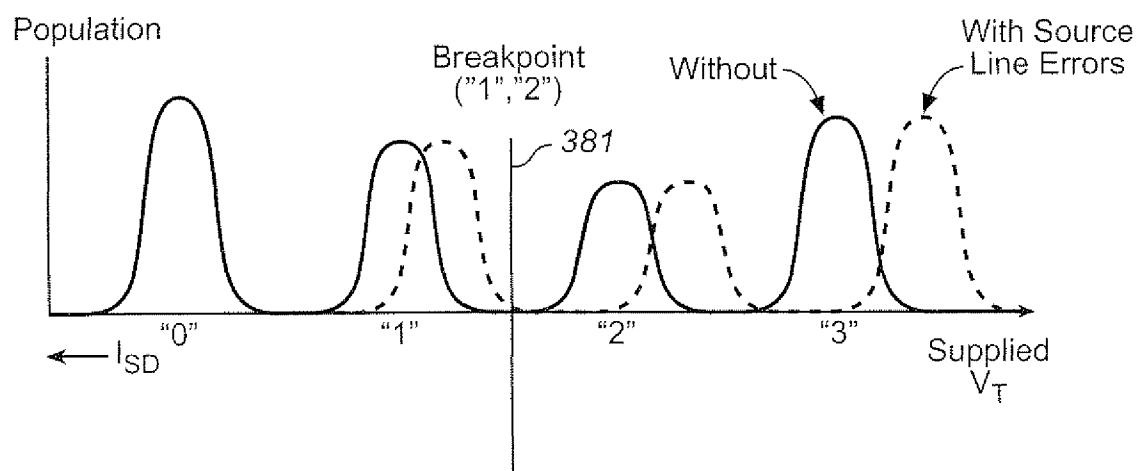
**FIG. 4 (PRIOR ART)****FIG. 5 (PRIOR ART)**

**FIG. 6A**

**FIG. 6B**



**FIG. 7A**  
(PRIOR ART)

**FIG. 7B****FIG. 8**

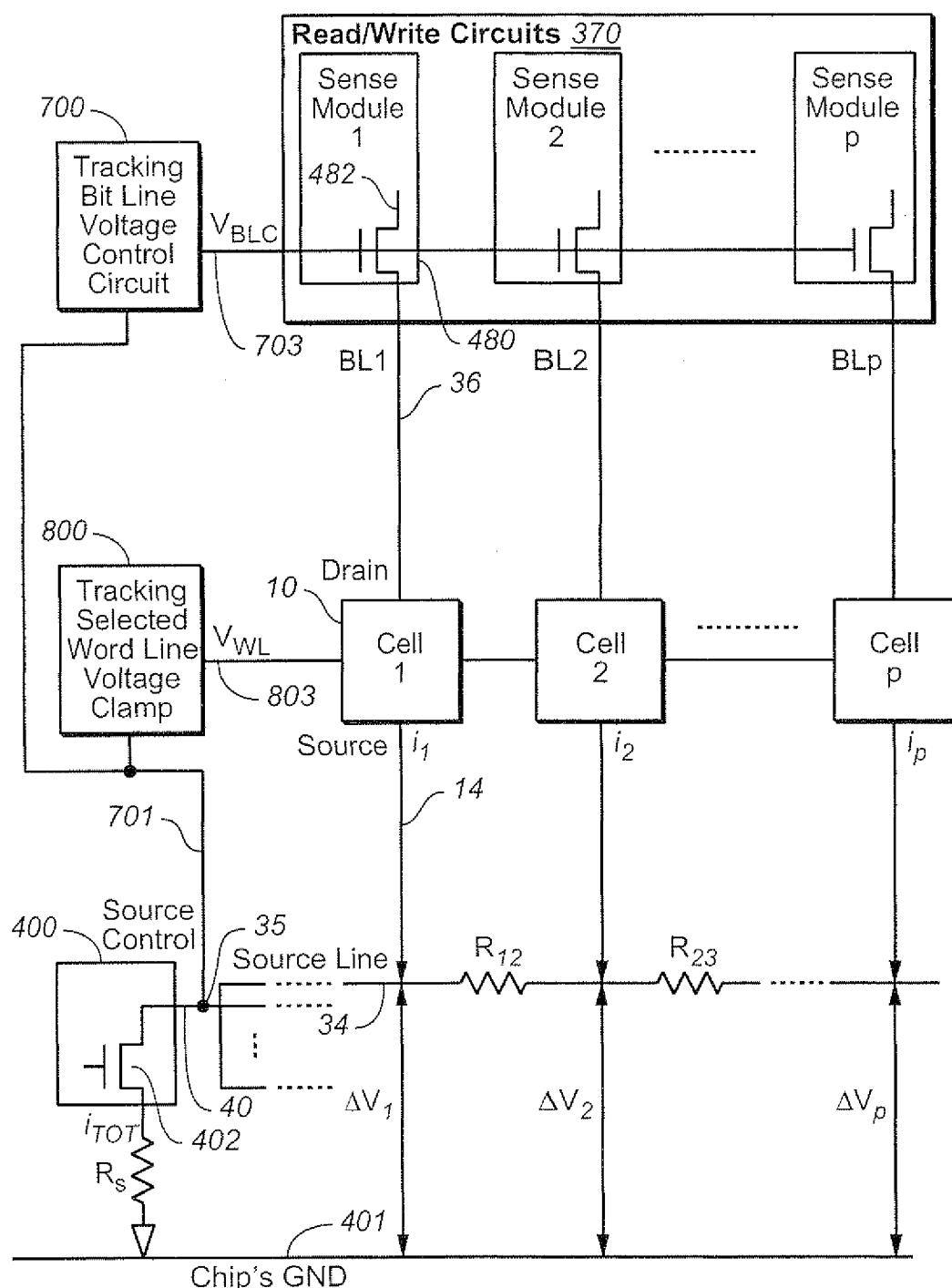
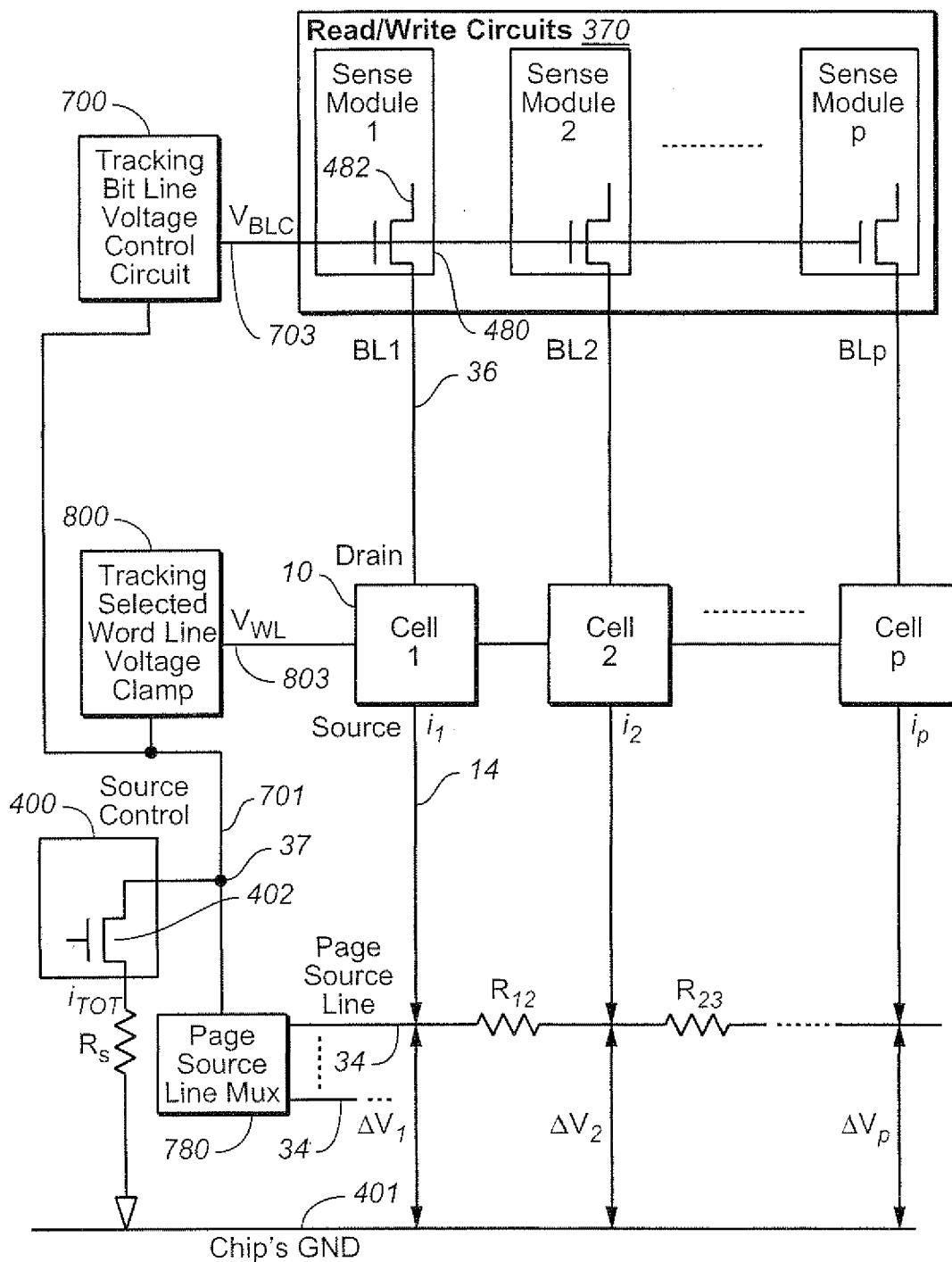
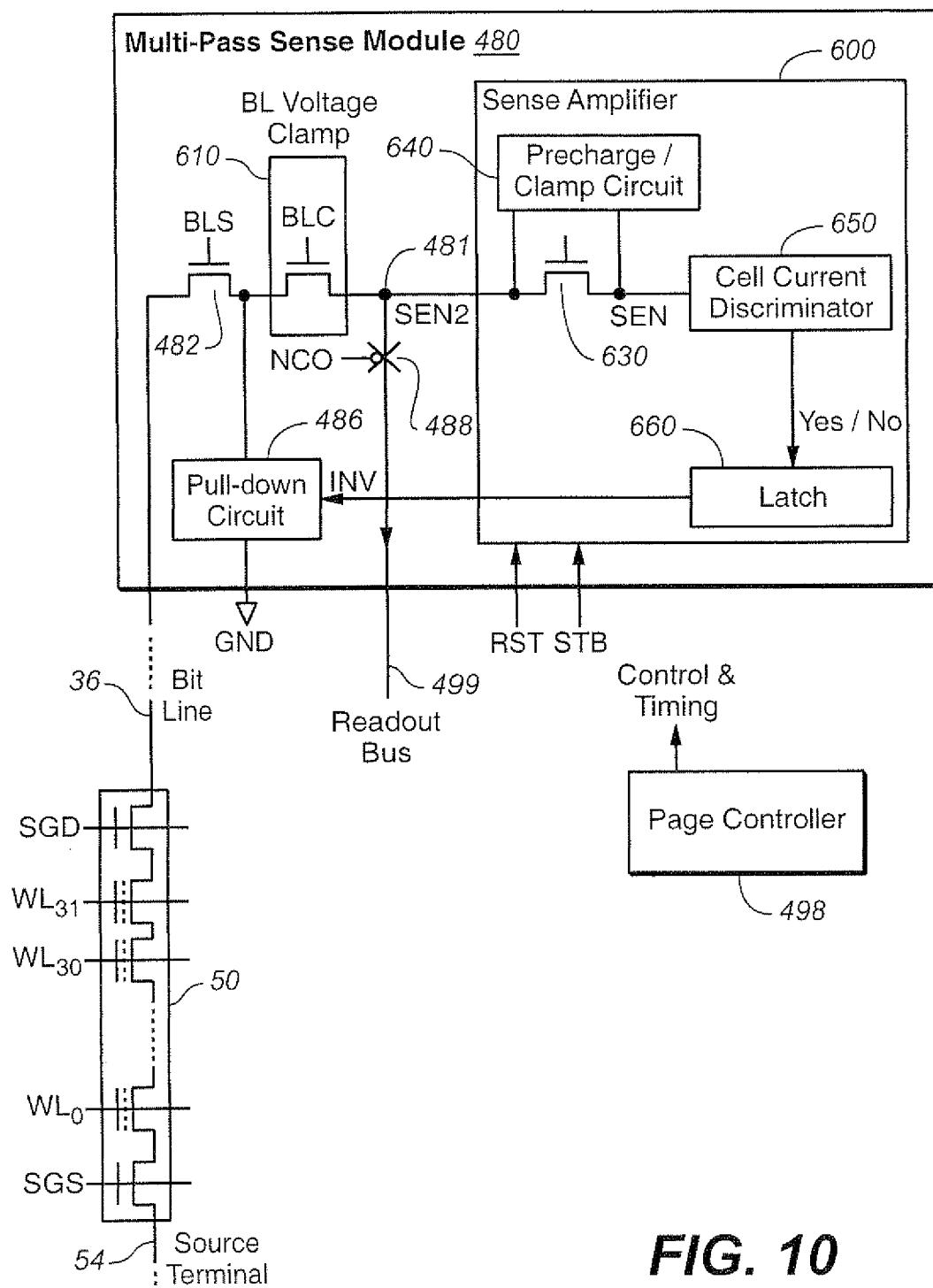
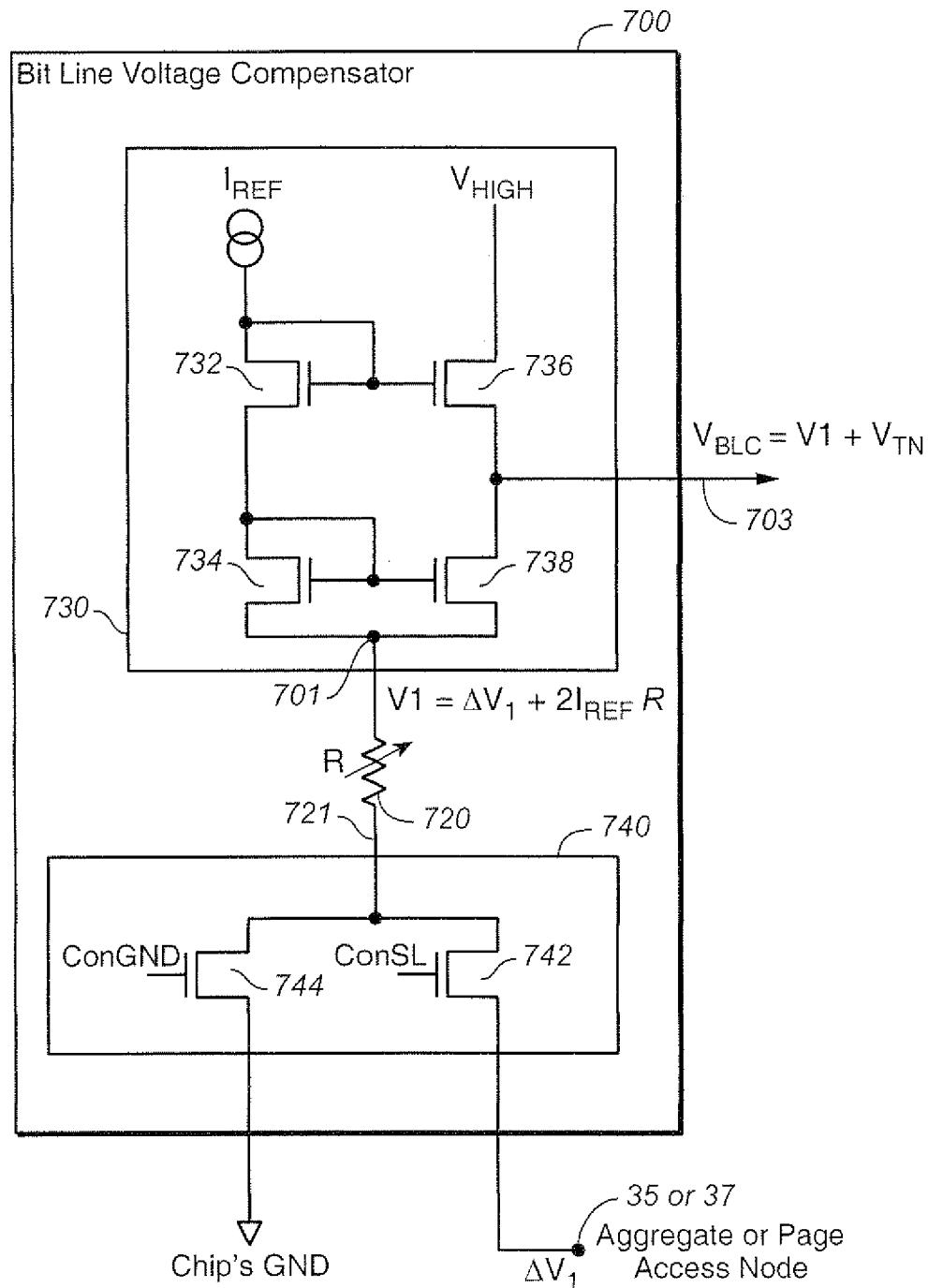


FIG. 9A

**FIG. 9B**



**FIG. 11**

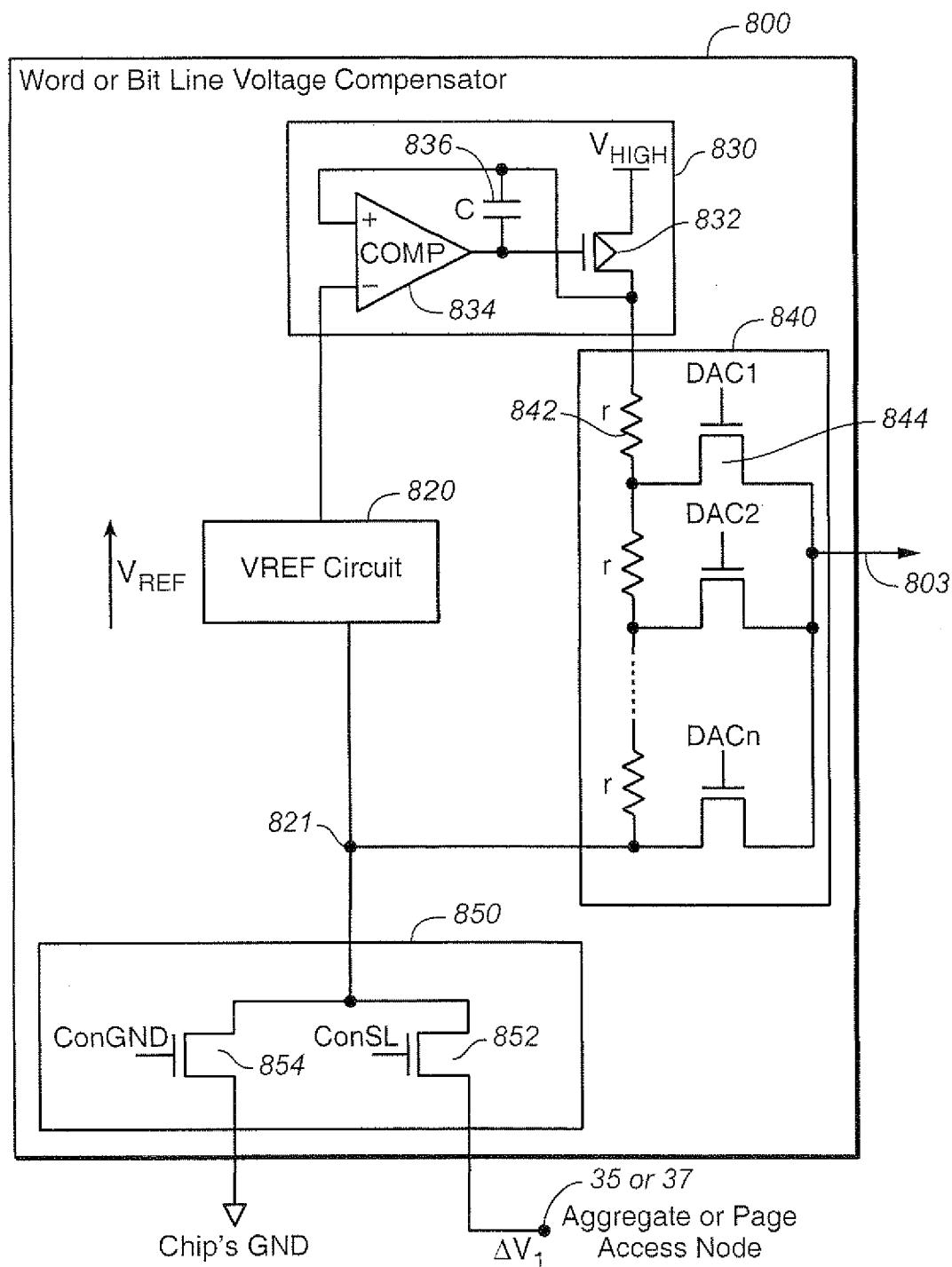
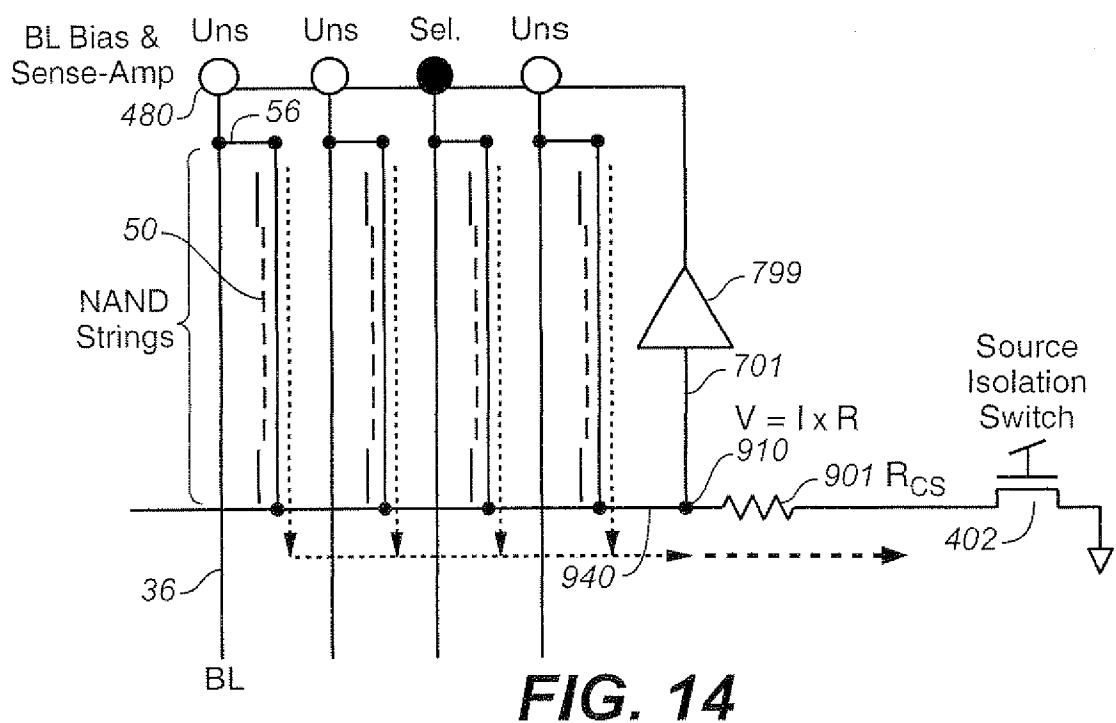
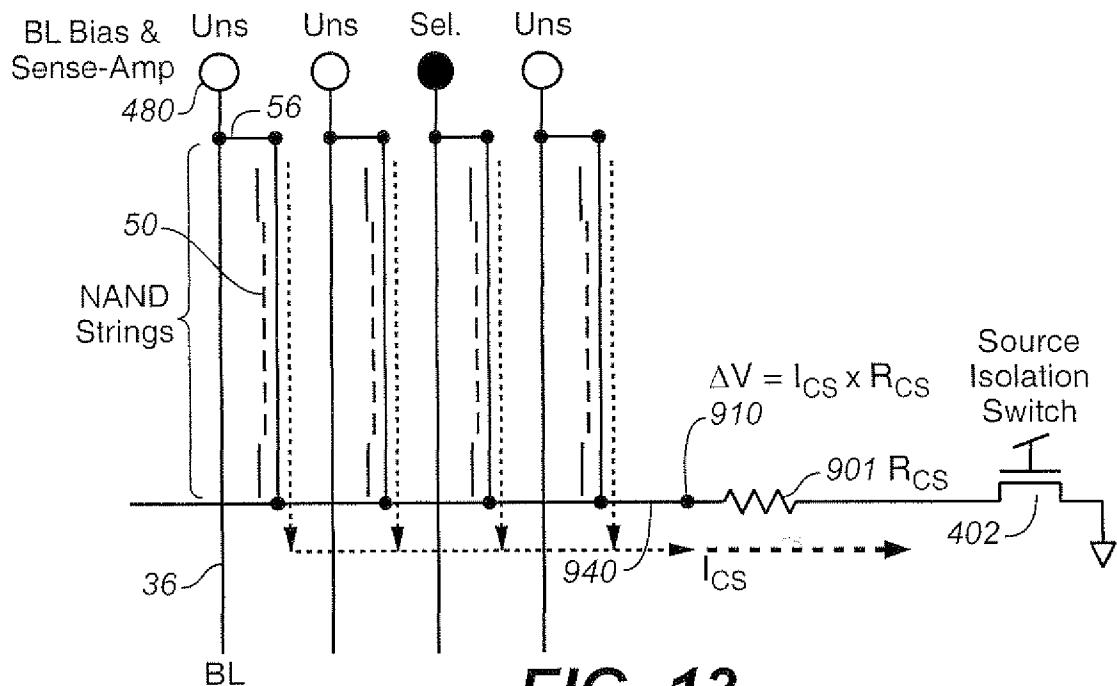


FIG. 12



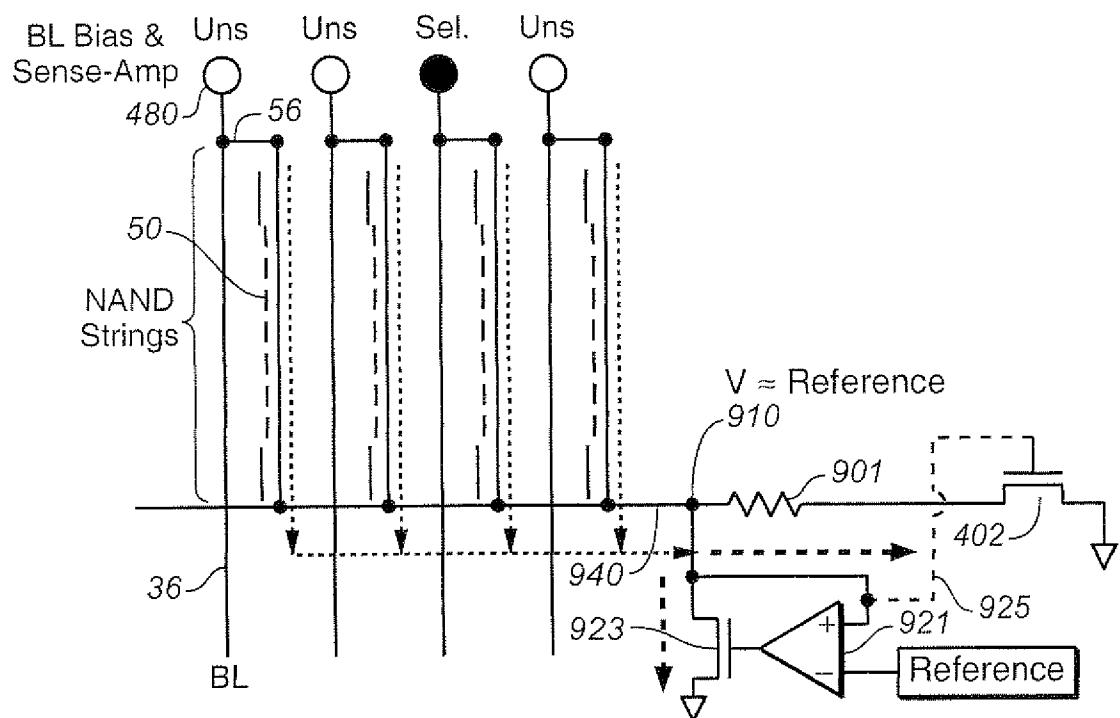


FIG. 15A

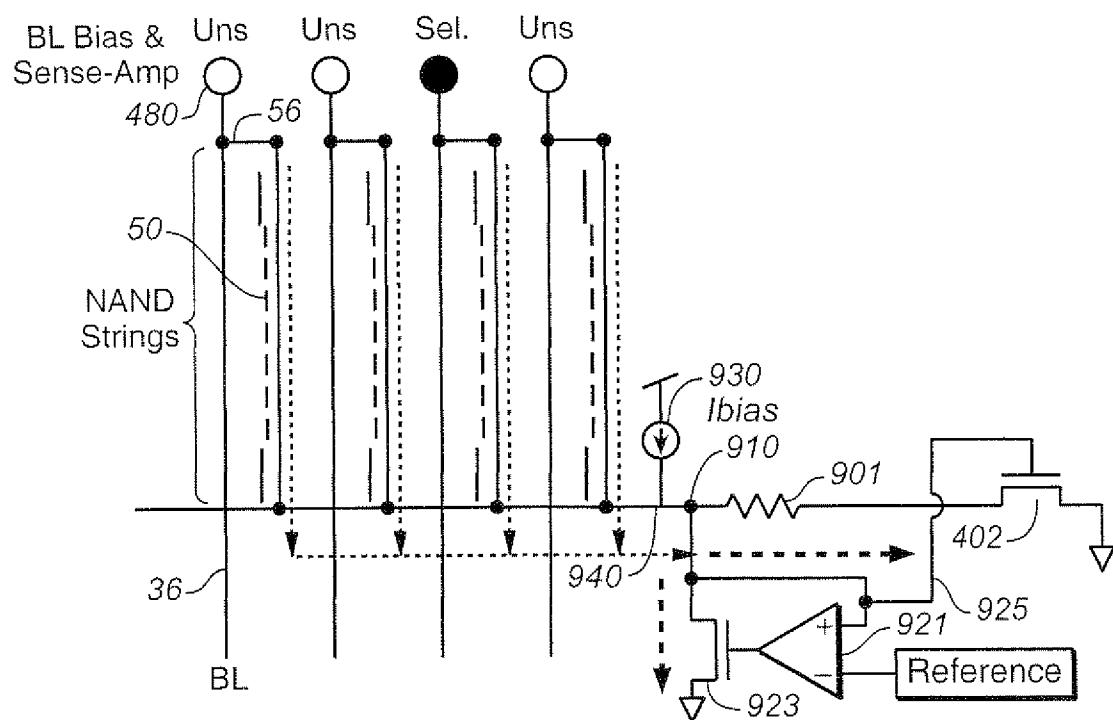


FIG. 15B

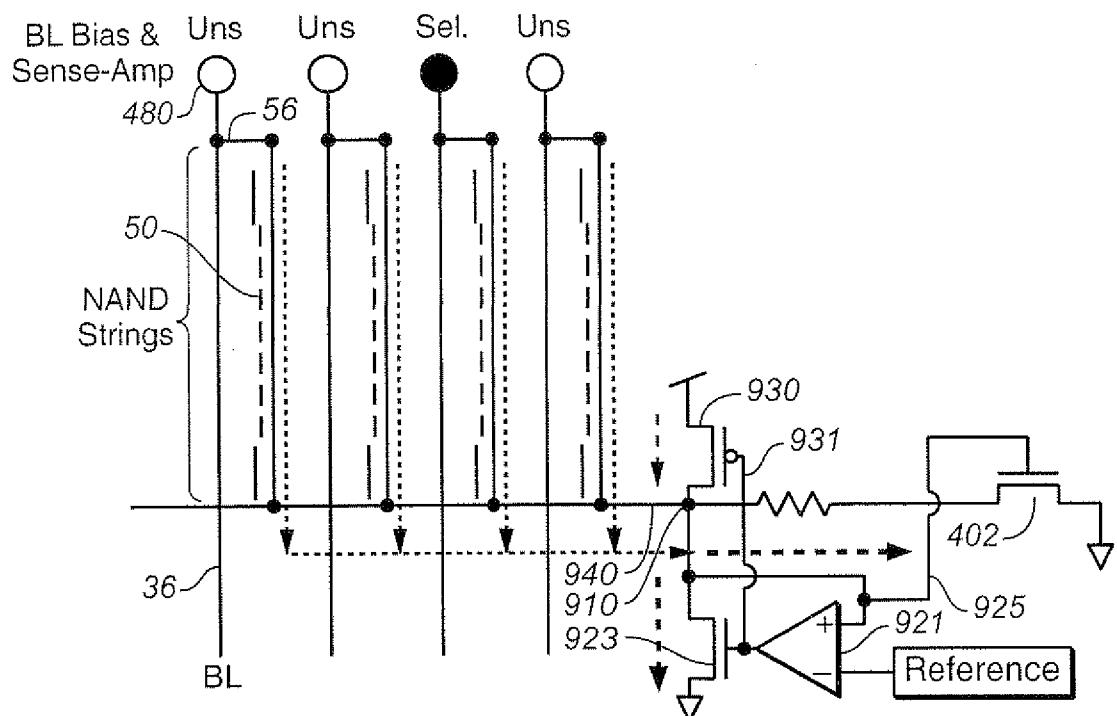


FIG. 15C

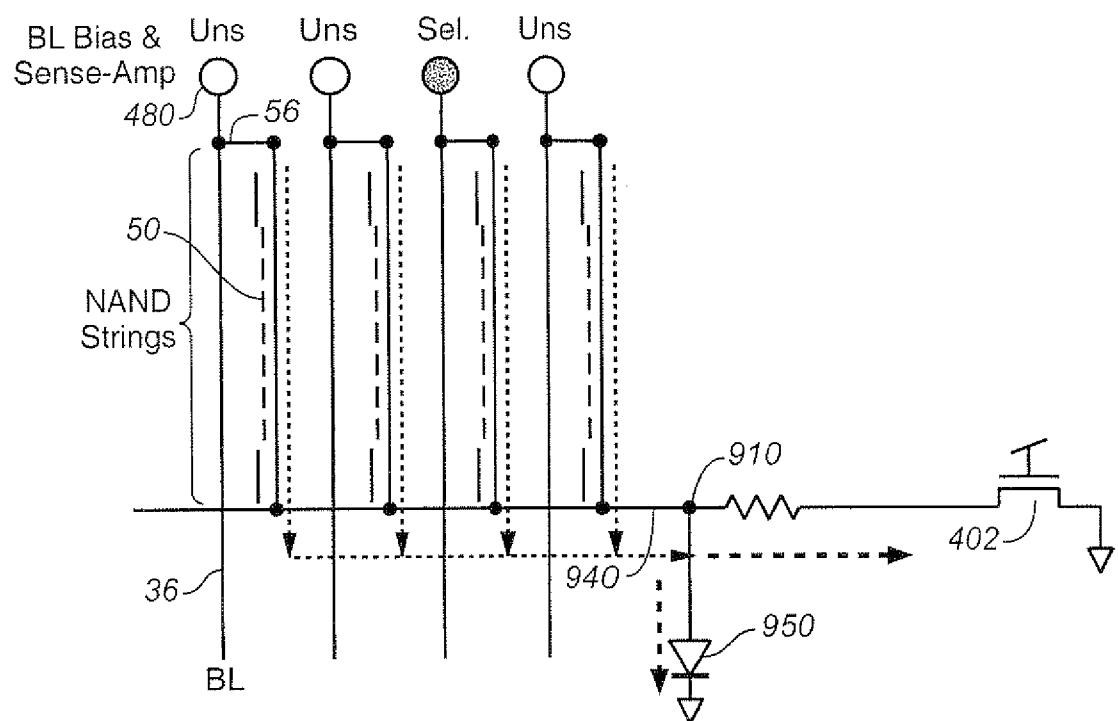


FIG. 16

# INTERNATIONAL SEARCH REPORT

International application No

PCT/US2008/086694

**A. CLASSIFICATION OF SUBJECT MATTER**  
INV. G11C16/30

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal, WPI Data, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2006/105363 A (SANDISK CORP [US]; CERNEA RAUL-ADRIAN [US]; CHAN SIU LUNG [US]) 5 October 2006 (2006-10-05) the whole document	1,2, 4-13, 15-18 3,14
Y	EP 1 331 644 A (ST MICROELECTRONICS SRL [IT]) 30 July 2003 (2003-07-30) paragraph [0026]; figure 7	1,2, 4-13, 15-18
X	US 2007/058429 A1 (UMEZAWA AKIRA [JP]) 15 March 2007 (2007-03-15) figures 1-4	19-24

Further documents are listed in the continuation of Box C.

See patent family annex.

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- \*L\* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- \*O\* document referring to an oral disclosure, use, exhibition or other means
- \*P\* document published prior to the international filing date but later than the priority date claimed

\*T\* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

\*X\* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

\*Y\* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

\*&\* document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
5 March 2009	13/03/2009
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer  Ramcke, Ties

**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No	
PCT/US2008/086694	

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