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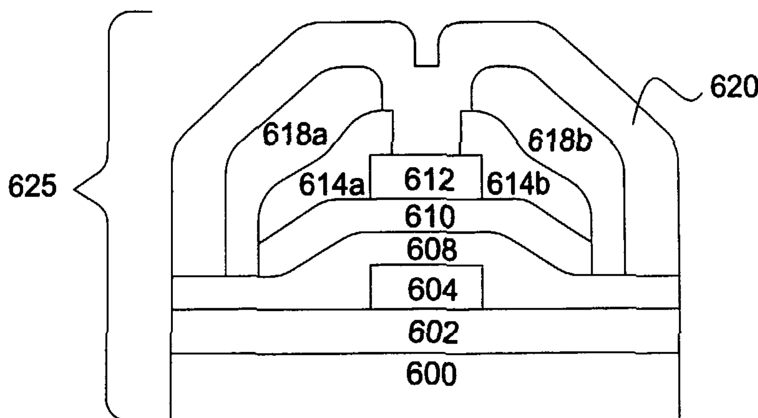
(54) Title: DEPOSITION OF GATE METALLIZATION AND PASSIVATION LAYERS FOR ACTIVE MATRIX LIQUID CRYSTAL DISPLAY (AMLCD) APPLICATIONS



(57) Abstract: A method of gate metal layer deposition and a method of passivation layer deposition using a cyclical deposition process for thin film transistor applications is described. The cyclical deposition process comprises alternately adsorbing a metal-containing precursor and a reducing gas on a substrate. In another aspect, the cyclical deposition process comprises alternately adsorbing a silicon-containing precursor and a reactant gas on a substrate. Thin film transistors, such as a bottom-gate transistor or a top-gate transistor,

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DEPOSITION OF GATE METALLIZATION AND PASSIVATION LAYERS FOR ACTIVE MATRIX LIQUID CRYSTAL DISPLAY (AMLCD) APPLICATIONS

5 ## BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the present invention relate to methods of gate metal layer deposition and passivation layer formation and, more particularly, to methods of gate metal layer formation and passivation layer formation using cyclical deposition 10 techniques for active matrix liquid crystal display (AMLCD) applications.

Description of the Background Art

[0002] Active matrix liquid crystal displays have eliminated many problems associated with passive displays. For example, the fabrication of active matrix liquid 15 crystal displays have enabled display screens to achieve greater brightness, enhanced readability, a greater variety of color shades, and broader viewing angles compared to displays that employ other technologies. Active matrix liquid crystal displays have therefore become the display technology of choice for numerous applications including computer monitors, television screens, camera displays, avionics displays, as well as 20 numerous other applications.

[0003] Active matrix liquid crystal displays generally comprise an array of picture elements called pixels. An electronic switch is associated with each pixel in the display to control the operation thereof. Various electronic switches such as, for example, thin film transistors and organic light emitting diodes (OLED), among others have been 25 investigated to control pixel operation. Thin film transistors, in particular, offer a high degree of design flexibility and device performance.

[0004] Thin film transistors are generally formed on large area substrates having a high degree of optical transparency such as, for example, glass. FIG. 1 depicts a cross-sectional schematic view of a thin film transistor 22 being a type that has a 30 bottom gate structure. The thin film transistor 22 includes a glass substrate 1 having an underlayer 2 formed on the surface thereof. A gate is formed on the underlayer 2. The gate comprises a gate metal layer 4 and a gate dielectric layer 8. The gate controls the movement of charge carriers in the transistor. The gate dielectric layer 8 is formed over the gate metal layer 4 and electrically isolates the gate metal layer 4 from 35 semiconductor layers 10, 14a, 14b, formed thereover, each of which may function to

provide charge carriers to the transistor. A source region 18a of the transistor is formed on semiconductor layer 14a and a drain region 18b of the transistor is formed on semiconductor layer 14b. Finally, a passivation layer 20 encapsulates the thin film transistor 22 to protect it from environmental hazards such as moisture and oxygen.

5 **[0005]** The gate metal layer 4 generally comprises a conductive material (e.g., tungsten (W), aluminum (Al) chromium (Cr)), deposited using conventional techniques, such as, for example, physical vapor deposition (PVD). However, gate material layers deposited using PVD techniques generally tend to have high resistivities. For example, tungsten (W) layers deposited using PVD techniques typically have resistivities of 10 greater than about 150 μΩ/cm. Such high resistivities for the gate metal layer may affect the electrical performance of the transistors, including device reliability and premature failure.

[0006] The passivation layer 20 generally comprises a dielectric material, deposited using conventional techniques, such as, for example, plasma enhanced 15 chemical vapor deposition (PECVD). Unfortunately, it is difficult to deposit passivation layers that are continuous (e.g., without gaps or voids) using PECVD techniques. Furthermore, many conventional PECVD techniques used to form passivation layers tend to be high temperature processes. High deposition temperatures may not be compatible with the glass substrates upon which the thin film transistors are formed, 20 since the glass may soften and become dimensionally unstable.

[0007] Therefore, a need exists to develop a method of forming gate metal layers and passivation layers for use in thin film transistors

SUMMARY OF THE INVENTION

25 **[0008]** A method of gate metal layer deposition for thin film transistor applications for use in active matrix liquid crystal displays (AMLCD) is described. The gate métal layer comprises a metal that is deposited using a cyclical deposition process. The cyclical deposition process comprises alternately adsorbing a metal-containing precursor and a reducing gas on a substrate structure. The adsorbed metal-30 containing precursor reacts with the adsorbed reducing gas to form the gate metal layer on the substrate.

[0009] Thin film transistors, such as for example a bottom-gate transistor or a top-gate transistor, including a gate metal layer may be formed using such cyclical deposition techniques. In one embodiment, a preferred process sequence for

fabricating a bottom-gate transistor includes providing a substrate. A gate metal layer is deposited on the substrate. The gate metal layer is formed by alternately adsorbing a metal-containing precursor and a reducing gas on the substrate. The gate metal layer is than patterned and a gate dielectric layer is formed thereover. Source regions and drain regions are formed on the gate dielectric layer. Thereafter, the bottom-gate transistor may be completed by depositing a passivation layer on the substrate.

[0010] A method of passivation layer deposition for thin film transistor (TFT) applications for use in active matrix liquid crystal displays (AMLCD) is described. The passivation layer may be a silicon-containing passivation layer. The silicon-containing passivation layer may be deposited using a cyclical deposition process. The cyclical deposition process may comprise alternately adsorbing a silicon-containing precursor and a reactant gas on a substrate structure. The adsorbed silicon-containing precursor reacts with the reactant gas to form the silicon-containing passivation layer on the substrate.

[0011] Thin film transistors, such as for example a bottom-gate transistor or a top-gate transistor, including one or more passivation layers may be formed using such cyclical deposition techniques. In one embodiment, a preferred process sequence for fabricating a bottom-gate transistor includes providing a substrate having a gate comprising a gate metal layer and a gate dielectric layer formed thereon. One or more semiconducting layers with adjoining contact regions are formed on the gate dielectric layer. The bottom-gate transistor is completed by depositing a silicon-containing passivation layer over the contact regions and semiconducting layers formed on the substrate. The silicon-containing passivation layer may be formed by alternately adsorbing a silicon-containing precursor and a reactant gas on the substrate. The adsorbed silicon-containing precursor reacts with the adsorbed reactant gas to form the silicon-containing passivation layer on the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] So that the manner in which the above recited features of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings.

[0013] It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0014] FIG. 1 depicts a cross-sectional schematic view of a prior art bottom-gate thin film transistor;

[0015] FIG. 2 depicts a schematic cross-sectional view of a process chamber that can be used to practice embodiments described herein;

[0016] FIG. 3A illustrates a process sequence for gate metal layer formation using cyclical deposition techniques according to one embodiment described herein;

[0017] FIG. 3B illustrates a process sequence for passivation layer formation using cyclical deposition techniques according to one embodiment described herein;

[0018] FIG. 4A illustrates a process sequence for gate metal layer formation using cyclical deposition techniques according to an alternative embodiment described herein;

[0019] FIG. 4B illustrates a process sequence for passivation layer formation using cyclical deposition techniques according to an alternative embodiment described herein;

[0020] FIGS. 5A-5D depict cross-sectional views of a substrate at different stages of a bottom-gate thin film transistor fabrication sequence; and

[0021] FIGS. 6A-6C depict cross-sectional views of a substrate at different stages of a top-gate thin film transistor fabrication sequence.

DETAILED DESCRIPTION OF THE INVENTION

[0022] FIG. 2 depicts a schematic cross-sectional view of a process chamber 310 that can be used to perform integrated circuit fabrication in accordance with embodiments described herein. The process chamber 310 generally houses a substrate support pedestal 348, which is used to support a substrate (not shown). The substrate support pedestal 348 is movable in a vertical direction inside the process chamber 310 using a displacement mechanism 348a.

[0023] Depending on the specific process, the substrate can be heated to some desired temperature prior to or during deposition. For example, the substrate support pedestal 348 may be heated using an embedded heater element 352a. The substrate support pedestal 348 may be resistively heated by applying an electric current from an AC power supply 352 to the heater element 352a. The substrate (not shown) is, in turn,

heated by the pedestal 348. Alternatively, the substrate support pedestal 348 may be heated using radiant heaters such as, for example, lamps (not shown).

[0024] A temperature sensor 350a, such as a thermocouple, is also embedded in the substrate support pedestal 348 to monitor the temperature of the pedestal 348 in
5 a conventional manner. The measured temperature is used in a feedback loop to control the AC power supply 352 for the heating element 352a, such that the substrate temperature can be maintained or controlled at a desired temperature which is suitable for the particular process application.

[0025] A vacuum pump 318 is used to evacuate the process chamber 310 and to
10 maintain the pressure inside the process chamber 310. A gas manifold 334, through which process gases are introduced into the process chamber 310, is located above the substrate support pedestal 348. The gas manifold 334 is connected to a gas panel 311, which controls and supplies various process gases to the process chamber 310.

[0026] Proper control and regulation of the gas flows to the gas manifold 334 are
15 performed by mass flow controllers (not shown) and a microprocessor controller 370. The gas manifold 334 allows process gases to be introduced and uniformly distributed in the process chamber 310. Additionally, the gas manifold 334 may optionally be heated to prevent condensation of the any reactive gases within the manifold.

[0027] The gas manifold 334 includes a plurality of electronic control valves (not
20 shown). The electronic control valves as used herein refer to any control valve capable of providing rapid and precise gas flow to the process chamber 310 with valve open and close cycles of less than about 1-2 seconds, and more preferably less than about 0.1 second.

[0028] The microprocessor controller 370 may be one of any form of general
25 purpose computer processor (CPU) 371 that can be used in an industrial setting for controlling various chambers and sub-processors. The computer may use any suitable memory 372, such as random access memory, read only memory, floppy disk drive, hard disk, or any other form of digital storage, local or remote. Various support circuits 373 may be coupled to the CPU for supporting the processor in a conventional manner.
30 Software routines as required may be stored on the memory or executed by a second CPU that is remotely located.

[0029] The software routines are executed to initiate process recipes or sequences. The software routines, when executed, transform the general purpose computer into a specific process computer that controls the chamber operation so that

a chamber process is performed. For example, software routines may be used to precisely control the activation of the electronic control valves for the execution of process sequences according to the present invention. Alternatively, the software routines may be performed in hardware, as an application specific integrated circuit or
5 other type of hardware implementation, or a combination of software or hardware.

[0030] Alternatively, process chamber 310 may be adapted to generate an electric field therein. The electric field may be applied to one or more of the process gases introduced into the process chamber 310 through the gas manifold 334. For example, a high frequency power supply 312 may be coupled to the substrate support
10 pedestal 348. The high frequency power supply 312 may be a radio frequency (RF) power supply with a frequency of, for example, about 13.56 MHz.

[0031] An electric field may be generated within the process chamber 310 by applying a high frequency power to the substrate support pedestal 348. The electric field may be used to ignite a process gas, such as, for example a reactant gas, forming
15 a plasma 314 within the process chamber 310. The plasma 314 is believed dissociate the gas to enhance the reaction between absorbed process gases on a substrate positioned on the substrate support pedestal 348. The plasma may optionally be generated in a remote plasma chamber (not shown) that may then be introduced into the process chamber 310 through the gas manifold 334.

20

Gate Metal Layer Formation

[0032] A method of forming a gate metal layer for thin film transistor applications is described. The gate metal layer comprises a metal that is deposited using a cyclical deposition process, such as tungsten, aluminum, chromium or molybdenum. The
25 cyclical deposition process comprises alternately adsorbing a metal-containing precursor and a reducing gas on a substrate structure. The metal-containing precursor and the reducing gas react to form a gate metal layer on the substrate.

[0033] FIG. 3A illustrates a process sequence 400 detailing the various steps used for the deposition of the gate metal layer. These steps may be performed in a
30 process chamber similar to that described above with reference to FIG. 2. As shown in step 402, a substrate is provided to the process chamber. The substrate may be for example, a glass or clear plastic material suitable for AMLCD fabrication. The process chamber conditions such as, for example, the temperature and pressure are adjusted to enhance the adsorption of the process gases on the substrate to facilitate the

reaction of the metal-containing precursor and the reducing gas. In general, for gate metal layer deposition, the substrate should be maintained at a temperature between about 20^{0}C and about 450^{0}C at a process chamber pressure of between about 10 mTorr and about 10 Torr.

5 **[0034]** In one embodiment where a constant carrier gas flow is desired, a carrier gas stream is established within the process chamber as indicated in step 404. Carrier gases may be selected so as to also act as a purge gas for removal of volatile reactants and/or by-products from the process chamber. Carrier gases such as, for example, helium (He), argon (Ar), nitrogen (N_2), hydrogen (H_2) and combinations 10 thereof, may be used.

[0035] Referring to step 406, after the carrier gas stream is established within the process chamber, a pulse of a metal-containing precursor is added to the carrier gas stream. The term pulse as used herein refers to a dose of material injected into the process chamber or into the carrier gas stream. The pulse of the metal-containing 15 precursor lasts for a predetermined time interval.

[0036] The metal-containing precursor may comprise a compound of a metal such as, for example, aluminum (Al), tungsten (W), molybdenum (Mo) and chromium (Cr), among others. A suitable aluminum precursor may include, for example, dimethyl aluminum hydride (DMAH) and trimethyl aluminum (TMA). Suitable tungsten 20 precursors may include, for example, tungsten hexafluoride (WF_6) and tungsten hexacarbonyl ($W(CO)_6$). A suitable chromium precursor may include, for example, chromium tetrachloride ($CrCl_4$). A suitable molybdenum precursor may include, for example, molybdenum pentachloride ($MoCl_5$).

[0037] The time interval for the pulse of the metal-containing precursor is 25 variable depending upon a number of factors such as, for example, the volume capacity of the process chamber employed, the vacuum system coupled thereto and the volatility/reactivity of the reactants. For example, (1) a large-volume process chamber may lead to a longer time to stabilize the process conditions such as, for example, carrier/purge gas flow and temperature, requiring a longer pulse time; (2) a 30 lower flow rate for the process gas may also lead to a longer time to stabilize the process conditions requiring a longer pulse time; and (3) a lower chamber pressure means that the process gas is evacuated from the process chamber more quickly requiring a longer pulse time. In general, the process conditions are advantageously selected so that a pulse of the metal-containing precursor provides a sufficient amount

of precursor, such that at least a monolayer of the metal-containing precursor is adsorbed on the substrate. Thereafter, excess metal-containing precursor remaining in the chamber may be removed from the process chamber by the constant carrier gas stream in combination with the vacuum system.

5 **[0038]** In step 408, after the excess metal-containing precursor has been sufficiently removed from the process chamber by the carrier gas stream to prevent co-reaction or particle formation with a subsequently provided process gas, a pulse of a reducing gas is added to the carrier gas stream. Suitable reducing gases may include, for example, silane (SiH_4), disilane (Si_2H_6), dichlorosilane ($SiCl_2H_2$), ammonia (NH_3),
10 hydrazine (N_2H_4), monomethyl hydrazine ($CH_3N_2H_3$), dimethyl hydrazine ($C_2H_6N_2H_2$), t-butyl hydrazine ($C_4H_9N_2H_3$), phenyl hydrazine ($C_6H_5N_2H_3$), 2,2'-azoisobutane ($(CH_3)_6C_2N_2$), ethylazide ($C_2H_5N_3$), triethylborane (Et_3B), borane (BH_3), diborane (B_2H_6), triborane, tetraborane, pentaborane, hexaborane, heptaborane, octaborane, nanoborane and decaborane, among others.

15 **[0039]** The pulse of the reducing gas also lasts for a predetermined time interval. In general, the time interval for the pulse of the reducing gas should be long enough to provide a sufficient amount of the reducing gas for reaction with the metal-containing precursor that is already adsorbed on the substrate. Thereafter, excess reducing gas is flushed from the process chamber by the carrier gas stream.

20 **[0040]** Steps 404 through 408 comprise one embodiment of a deposition cycle for a gate metal layer. For such an embodiment, a constant flow of carrier gas is provided to the process chamber modulated by alternating periods of pulsing and non-pulsing where the periods of pulsing alternate between the metal-containing precursor and the reducing gas along with the carrier gas stream, while the periods of non-
25 pulsing include only the carrier gas stream.

[0041] The time interval for each of the pulses of the metal-containing precursor and the reducing gas may have the same duration. That is the duration of the pulse of the metal-containing precursor may be identical to the duration of the pulse of the reducing gas. For such an embodiment, a time interval (T_1) for the pulse of the metal-
30 containing precursor is equal to a time interval (T_2) for the pulse of the reducing gas.

[0042] Alternatively, the time interval for each of the pulses of the metal-containing precursor and the reducing gas may have different durations. That is the duration of the pulse of the metal-containing precursor may be shorter or longer than the duration of the pulse of the reducing gas. For such an embodiment, a time interval

(T_1) for the pulse of the metal-containing precursor is different than a time interval (T_2) for the pulse of the reducing gas.

[0043] In addition, the periods of non-pulsing between each of the pulses of the metal-containing precursor and the reducing gas may have the same duration. That is the duration of the period of non-pulsing between each pulse of the metal-containing precursor and each pulse of the reducing gas is identical. For such an embodiment, a time interval (T_3) of non-pulsing between the pulse of the metal-containing precursor and the pulse of the reducing gas is equal to a time interval (T_4) of non-pulsing between the pulse of the reducing gas and the pulse of the metal-containing precursor. During the time periods of non-pulsing only the constant carrier gas stream is provided to the process chamber.

[0044] Alternatively, the periods of non-pulsing between each of the pulses of the metal-containing precursor and the reducing gas may have different durations. That is the duration of the period of non-pulsing between each pulse of the metal-containing precursor and each pulse of the reducing gas may be shorter or longer than the duration of the period of non-pulsing between each pulse of the reducing gas and the metal-containing precursor. For such an embodiment, a time interval (T_3) of non-pulsing between the pulse of the metal-containing precursor and the pulse of the reducing gas is different from a time interval (T_4) of non-pulsing between the pulse of the reducing gas and the pulse of the metal-containing precursor. During the time periods of non-pulsing only the constant carrier gas stream is provided to the process chamber.

[0045] Additionally, the time intervals for each pulse of the metal-containing precursor, the reducing gas and the periods of non-pulsing therebetween for each deposition cycle may have the same duration. For such an embodiment, a time interval (T_1) for the metal-containing precursor, a time interval (T_2) for the reducing gas, a time interval (T_3) of non-pulsing between the pulse of the metal-containing precursor and the pulse of the reducing gas and a time interval (T_4) of non-pulsing between the pulse of the reducing gas and the pulse of the metal-containing precursor each have the same value for each subsequent deposition cycle. For example, in a first deposition cycle (C_1), a time interval (T_1) for the pulse of the metal-containing precursor has the same duration as the time interval (T_1) for the pulse of the metal-containing precursor in subsequent deposition cycles ($C_2 \ldots C_N$). Similarly, the duration of each pulse of the reducing gas and the periods of non-pulsing between the pulse of the metal-containing

precursor and the reducing gas in deposition cycle (C_1) is the same as the duration of each pulse of the reducing gas and the periods of non-pulsing between the pulse of the metal-containing precursor and the reducing gas in subsequent deposition cycles ($C_2 \ldots C_N$), respectively.

5 **[0046]** Alternatively, the time intervals for at least one pulse of the metal-containing precursor, the reducing gas and the periods of non-pulsing therebetween for one or more of the deposition cycles of the gate metal layer deposition process may have different durations. For such an embodiment, one or more of the time intervals (T_1) for the pulses of the metal-containing precursor, the time intervals (T_2) for the
10 pulses of the reducing gas, the time intervals (T_3) of non-pulsing between the pulse of the metal-containing precursor and the pulse of the reducing gas and the time intervals (T_4) of non-pulsing between the pulse of the reducing gas and the pulse of the metal-containing precursor may have different values for one or more subsequent deposition cycles of the gate metal layer deposition process. For example, in a first deposition
15 cycle (C_1), the time interval (T_1) for the pulse of the metal-containing precursor may be longer or shorter than the time interval (T_1) for the pulse of the metal-containing precursor in a subsequent deposition cycle ($C_2 \ldots C_N$). Similarly, the duration of each pulse of the reducing gas and the periods of non-pulsing between the pulse of the metal-containing precursor and the reducing gas in deposition cycle (C_1) may be the
20 same or different than the duration of each pulse of the reducing gas and the periods of non-pulsing between the pulse of the metal-containing precursor and the reducing gas in subsequent deposition cycles ($C_2 \ldots C_N$), respectively.

[0047] Referring to step 410, after each deposition cycle (steps 404 through 408) a total thickness of the gate metal layer will be formed on the substrate. Depending on
25 specific device requirements, subsequent deposition cycles may be needed to achieve a desired thickness. As such, steps 404 through 408 are repeated until the desired thickness for the gate metal layer is achieved. Thereafter, when the desired thickness for the gate metal layer is achieved the process is stopped as indicated by step 412.

[0048] In an alternate process sequence described with respect to FIG. 4A, the
30 gate metal layer deposition cycle comprises separate pulses for each of the metal-containing precursor, the reducing gas and the purge gas. For such an embodiment, the gate metal layer deposition sequence 500 includes providing a substrate to the process chamber (step 502), providing a first pulse of a purge gas to the process chamber (step 504), providing a pulse of a metal-containing precursor to the process

chamber (step 506), providing a second pulse of the purge gas to the process chamber (step 508), providing a pulse of a reducing gas to the process chamber (step 510), and then repeating steps 504 through 510 or stopping the deposition process (step 514) depending on whether a desired thickness for the gate metal layer has been achieved (step 512).

[0049] The time intervals for each of the pulses of the metal-containing precursor, the reducing gas and the purge gas may have the same or different durations as discussed above with respect to FIG. 3A. Alternatively, the time intervals for at least one pulse of the metal-containing precursor, the reducing gas and the purge gas for one or more of the deposition cycles of the gate metal layer deposition process may have different durations.

[0050] In FIGS. 3A and 4A, the gate metal layer deposition cycle is depicted as beginning with a pulse of the metal-containing precursor followed by a pulse of the reducing gas. Alternatively, the gate metal layer deposition cycle may start with a pulse of the reducing gas followed by a pulse of the metal-containing precursor.

[0051] One exemplary process of depositing a tungsten gate layer comprises sequentially providing pulses of tungsten hexafluoride (WF_6) and pulses of diborane (B_2H_6). The tungsten hexafluoride (WF_6) may be provided to an appropriate flow control valve, for example, an electronic control valve, at a flow rate of between about 10 sccm (standard cubic centimeters per minute) and about 400 sccm, preferably between about 20 sccm and about 100 sccm, and thereafter pulsed for about 1 second or less, preferably about 0.2 seconds or less. A carrier gas comprising argon (Ar) is provided along with the tungsten hexaflouride (WF_6) at a flow rate between about 250 sccm to about 1,000 sccm, preferably between about 500 sccm to about 750 sccm. The diborane (B_2H_6) may be provided to an appropriate flow control valve, for example, an electronic control valve, at a flow rate of between about 5 sccm and about 150 sccm, preferably between about 5 sccm and about 25 sccm, and thereafter pulsed for about 1 second or less, preferably about 0.2 seconds or less. A carrier gas comprising argon (Ar) is provided along with the diborane (B_2H_6) at a flow rate between about 250 sccm to about 1,000 sccm, preferably between about 500 sccm to about 750 sccm. The substrate may be maintained at a temperature between about 250^{0}C and about 350^{0}C, preferably about 300^{0}C at a chamber pressure between about 1 Torr to about 10 Torr, preferably about 5 Torr.

Passivation Layer Formation

[0052] A method of passivation layer deposition for thin film transistor (TFT) applications is described. A silicon-containing passivation layer is deposited using a cyclical deposition process. The cyclical deposition process may comprise alternately adsorbing a silicon-containing precursor and a reactant gas on a substrate structure. The silicon-containing precursor reacts with the reactant gas to form the silicon-containing passivation layer on the substrate. The silicon-containing passivation layer may comprise, for example, silicon nitride (Si_3N_4), silicon oxide (SiO) and silicon dioxide (SiO_2), among others.

[0053] FIG. 3B illustrates a process sequence 1400 detailing the various steps used for the deposition of the silicon-containing passivation layer. These steps may be performed in a process chamber similar to that described above with reference to FIG. 2. As shown in step 1402, a substrate is provided to the process chamber. The substrate may be for example, a glass or clear plastic material suitable for AMLCD fabrication. The process chamber conditions such as, for example, the temperature and pressure are adjusted to enhance the adsorption of the process gases on the substrate to facilitate the reaction of the silicon-containing precursor and the reactant gas. In general, for silicon-containing passivation layer deposition, the substrate should be maintained at a temperature less than about 500^{0}C at a process chamber pressure of between about 10 mTorr and about 10 Torr.

[0054] In one embodiment where a constant carrier gas flow is desired, a carrier gas stream is established within the process chamber as indicated in step 1404. Carrier gases may be selected so as to also act as a purge gas for removal of volatile reactants and/or by-products from the process chamber. Carrier gases such as, for example, helium (He), argon (Ar), nitrogen (N_2), hydrogen (H_2) and combinations thereof, may be used.

[0055] Referring to step 1406, after the carrier gas stream is established within the process chamber, a pulse of a silicon-containing precursor is added to the carrier gas stream. The term pulse as used herein refers to a dose of material injected into the process chamber or into the carrier gas stream. The pulse of the silicon-containing precursor lasts for a predetermined time interval. The silicon-containing precursor may comprise, for example, silane (SiH_4), disilane (Si_2H_6), hexachlorodisilane (Si_2Cl_6), silicon tetrachloride ($SiCl_4$), dichlorosilane ($SiCl_2H_2$,) and trichlorosilane ($SiCl_3H$), among others.

[0056] The time interval for the pulse of the silicon-containing precursor is variable depending upon a number of factors such as, for example, the volume capacity of the process chamber employed, the vacuum system coupled thereto and the volatility/reactivity of the reactants used. For example, (1) a large-volume process chamber may lead to a longer time to stabilize the process conditions such as, for example, carrier/purge gas flow and temperature, requiring a longer pulse time; (2) a lower flow rate for the process gas may also lead to a longer time to stabilize the process conditions requiring a longer pulse time; and (3) a lower chamber pressure means that the process gas is evacuated from the process chamber more quickly requiring a longer pulse time. In general, the process conditions are advantageously selected so that a pulse of the silicon-containing precursor provides a sufficient amount of precursor so that at least a monolayer of the silicon-containing precursor is adsorbed on the substrate. Thereafter, excess silicon-containing precursor remaining in the chamber may be removed from the process chamber by the constant carrier gas stream in combination with the vacuum system.

[0057] In step 1408, after the excess silicon-containing precursor has been sufficiently removed from the process chamber by the carrier gas stream to prevent co-reaction or particle formation with a subsequently provided process gas, a pulse of a reactant gas is added to the carrier gas stream. Suitable reactant gases may include, for example, ammonia (NH_3), hydrazine (N_2H_4), nitrogen (N_2) and combinations thereof, among others for the deposition of silicon nitride layers. Suitable reactant gases may also include oxygen (O_2), ozone (O_3), hydrogen (H_2), water vapor (H_2O), hydrogen peroxide (H_2O_2) and combinations thereof, among others for the deposition of silicon oxide layers.

[0058] The pulse of the reactant gas also lasts for a predetermined time interval. In general, the time interval for the pulse of the reactant gas should be long enough to provide a sufficient amount of the reactant gas for reaction with the silicon-containing precursor that is already adsorbed on the substrate. Thereafter, excess reactant gas is flushed from the process chamber by the carrier gas stream.

[0059] Alternatively, a high frequency power, such as an RF power, may be applied to the substrate support pedestal 348 (FIG. 2) coincident with the pulse of the reactant gas (step 1408) to generate a plasma comprising the reactant gas within the process chamber. The plasma is believed to enhance the reaction between the adsorbed silicon-containing precursor on the substrate and the reactant gas. The

application of the high frequency power to the substrate support chamber may last for the same predetermined time interval as the time interval for the pulse of the reactant gas. In general, for silicon-containing passivation layer deposition, a high frequency power of about 0.05 W/mm^2 (Watts/square millimeter) to about 2 W/mm^2 may be
5 applied to the substrate support pedestal.

[0060] Steps 1404 through 1408 comprise one embodiment of a deposition cycle for a silicon-containing passivation layer. For such an embodiment, a constant flow of carrier gas is provided to the process chamber modulated by alternating periods of pulsing and non-pulsing where the periods of pulsing alternate between the silicon-
10 containing precursor and the reactant gas along with the carrier gas stream, while the periods of non-pulsing include only the carrier gas stream.

[0061] The time interval for each of the pulses of the silicon-containing precursor and the reactant gas may have the same duration. That is the duration of the pulse of the silicon-containing precursor may be identical to the duration of the pulse of the
15 reactant gas. For such an embodiment, a time interval (T_1) for the pulse of the silicon-containing precursor is equal to a time interval (T_2) for the pulse of the reactant gas.

[0062] Alternatively, the time interval for each of the pulses of the silicon-containing precursor and the reactant gas may have different durations. That is the duration of the pulse of the silicon-containing precursor may be shorter or longer than
20 the duration of the pulse of the reactant gas. For such an embodiment, a time interval (T_1) for the pulse of the silicon-containing precursor is different than a time interval (T_2) for the pulse of the reactant gas.

[0063] In addition, the periods of non-pulsing between each of the pulses of the silicon-containing precursor and the reactant gas may have the same duration. That is
25 the duration of the period of non-pulsing between each pulse of the silicon-containing precursor and each pulse of the reactant gas is identical. For such an embodiment, a time interval (T_3) of non-pulsing between the pulse of the silicon-containing precursor and the pulse of the reactant gas is equal to a time interval (T_4) of non-pulsing between the pulse of the reactant gas and the pulse of the silicon-containing precursor. During
30 the time periods of non-pulsing only the constant carrier gas stream is provided to the process chamber.

[0064] Alternatively, the periods of non-pulsing between each of the pulses of the silicon-containing precursor and the reactant gas may have different durations. That is the duration of the period of non-pulsing between each pulse of the silicon-containing

precursor and each pulse of the reactant gas may be shorter or longer than the duration of the period of non-pulsing between each pulse of the reactant gas and the silicon-containing precursor. For such an embodiment, a time interval (T_3) of non-pulsing between the pulse of the silicon-containing precursor and the pulse of the reactant gas is different from a time interval (T_4) of non-pulsing between the pulse of the reactant gas and the pulse of the silicon-containing precursor. During the time periods of non-pulsing only the constant carrier gas stream is provided to the process chamber.

[0065] Additionally, the time intervals for each pulse of the silicon-containing precursor, the reactant gas and the periods of non-pulsing therebetween for each deposition cycle may have the same duration. For such an embodiment, a time interval (T_1) for the silicon-containing precursor, a time interval (T_2) for the reactant gas, a time interval (T_3) of non-pulsing between the pulse of the silicon-containing precursor and the pulse of the reactant gas and a time interval (T_4) of non-pulsing between the pulse of the reactant gas and the pulse of the silicon-containing precursor each have the same value for each subsequent deposition cycle. For example, in a first deposition cycle (C_1), a time interval (T_1) for the pulse of the silicon-containing precursor has the same duration as the time interval (T_1) for the pulse of the silicon-containing precursor in subsequent deposition cycles ($C_2 \ldots C_N$). Similarly, the duration of each pulse of the reactant gas and the periods of non-pulsing between the pulse of the silicon-containing precursor and the reactant gas in deposition cycle (C_1) is the same as the duration of each pulse of the reactant gas and the periods of non-pulsing between the pulse of the silicon-containing precursor and the reactant gas in subsequent deposition cycles ($C_2 \ldots C_N$), respectively.

[0066] Alternatively, the time intervals for at least one pulse of the silicon-containing precursor, the reactant gas and the periods of non-pulsing therebetween for one or more of the deposition cycles of the passivation layer deposition process may have different durations. For such an embodiment, one or more of the time intervals (T_1) for the pulses of the silicon-containing precursor, the time intervals (T_2) for the pulses of the reactant gas, the time intervals (T_3) of non-pulsing between the pulse of the silicon-containing precursor and the pulse of the reactant gas and the time intervals (T_4) of non-pulsing between the pulse of the reactant gas and the pulse of the silicon-containing precursor may have different values for one or more subsequent deposition cycles of the passivation layer deposition process. For example, in a first deposition

cycle (C_1), the time interval (T_1) for the pulse of the silicon-containing precursor may be longer or shorter than the time interval (T_1) for the pulse of the silicon-containing precursor in a subsequent deposition cycle ($C_2 \ldots C_N$). Similarly, the duration of each pulse of the reactant gas and the periods of non-pulsing between the pulse of the 5 silicon-containing precursor and the reactant gas in deposition cycle (C_1) may be the same or different than the duration of each pulse of the reactant gas and the periods of non-pulsing between the pulse of the silicon-containing precursor and the reactant gas in subsequent deposition cycles ($C_2 \ldots C_N$), respectively.

[0067] Referring to step 1410, after each deposition cycle (steps 1404 through 10 1408) a total thickness of the silicon-containing passivation layer will be formed on the substrate. Depending on specific device requirements, subsequent deposition cycles may be needed to achieve a desired thickness. As such, steps 1404 through 1408 are repeated until the desired thickness for the silicon-containing passivation layer is achieved. Thereafter, when the desired thickness for the silicon-containing passivation 15 layer is achieved the process is stopped as indicated by step 1412.

[0068] In an alternate process sequence described with respect to FIG. 4B, the silicon-containing passivation layer deposition cycle comprises separate pulses for each of the silicon-containing precursor, the reactant gas, and the purge gas. For such an embodiment, the silicon-containing passivation layer deposition sequence 1500 20 includes providing a substrate to the process chamber (step 1502), providing a first pulse of a purge gas to the process chamber (step 1504), providing a pulse of a silicon-containing precursor to the process chamber (step 1506), providing a second pulse of the purge gas to the process chamber (step 1508), providing a pulse of a reactant gas to the process chamber (step 1510), and then repeating steps 1504 through 1510 or 25 stopping the deposition process (step 1514) depending on whether a desired thickness for the silicon-containing passivation layer has been achieved (step 1512).

[0069] Alternatively, a high frequency power, such as an RF power, may be applied to the substrate support pedestal 348 (FIG. 2) coincident with the pulse of the reactant gas (step 1510) to generate a plasma comprising the reactant gas within the 30 process chamber. The plasma is believed to enhance the reaction between the adsorbed silicon-containing precursor on the substrate and the reactant gas. The application of the high frequency power to the substrate support chamber may last for the same predetermined time interval as the time interval for the pulse of the reactant gas. In general, for silicon-containing passivation layer deposition, a high frequency

power of about 0.05 W/mm^2 to about 2 W/mm^2 may be applied to the substrate support pedestal.

[0070] The time intervals for each of the pulses of the silicon-containing precursor, the reactant gas and the purge gas may have the same or different
5 durations as discussed above with respect to FIG. 3B. Alternatively, the time intervals for at least one pulse of the silicon-containing precursor, the reactant gas and the purge gas for one or more of the deposition cycles of the silicon-containing passivation layer deposition process may have different durations.

[0071] In FIGS. 3B and 4B, the silicon-containing passivation layer deposition
10 cycle is depicted as beginning with a pulse of the silicon-containing precursor followed by a pulse of the reactant gas. Alternatively, the silicon-containing passivation layer deposition cycle may start with a pulse of the reactant gas followed by a pulse of the silicon-containing precursor.

[0072] One exemplary process of depositing a silicon oxide passivation layer
15 comprises alternately providing pulses of silicon tetrachloride ($SiCl_4$) and pulses of oxygen (O_2). The silicon tetrachloride ($SiCl_4$) may be provided to an appropriate flow control valve, for example, an electronic flow control valve, at a flow rate of between about 100 sccm (standard cubic centimeters per minute) and about 200 sccm, and thereafter pulsed for about 2 seconds or less. A carrier gas comprising argon (Ar) is
20 provided along with the silane at a flow rate between about 10 sccm to about 1,000 sccm. The oxygen (O_2) may be provided to an appropriate flow control valve, for example, an electronic flow control valve, at a flow rate of between about 100 sccm and about 5,000 sccm, and thereafter pulsed for about 5 seconds or less. The substrate may be maintained at a chamber pressure between about 0.05 Torr to about 10 Torr.
25 The substrate may be maintained at a temperature less than about 350^{0}C. The above mentioned flow rates for the carrier gas, the silicon-containing precursor, and the reactant gas may be varied, depending upon the volume capacity of the process chamber 310.

30 <u>Integrated Circuit Fabrication Processes</u>

1. Bottom-Gate Thin Film Transistor

[0073] FIGS. 5A-5D illustrate cross-sectional schematic views of a substrate structure 650 during different stages of a bottom-gate thin film transistor fabrication sequence incorporating a gate metal layer and a silicon-containing passivation layer

formed using cyclical deposition processes. The transistor fabrication sequence is for a switch in an active matrix liquid crystal display (AMLCD) and this process depicts the formation of one of an array of switches used in an AMLCD. FIG. 5A, for example, illustrates a cross-sectional view of a substrate 600. The substrate 600 may comprise
5 a material that is essentially optically transparent in the visible spectrum, such as, for example, glass or clear plastic, including soda-lime glass, borosilicate glass, or quartz glass. The substrate may be of varying shapes or dimensions. Typically, for thin film transistor applications, the substrate is a glass substrate with dimensions greater than about 500 mm x 500 mm.

10 **[0074]** The substrate 600 may have an underlayer 602 thereon. The underlayer 602 may be an insulating material, for example, such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4). The underlayer 602 may be formed using cyclical deposition techniques or conventional deposition techniques, such as CVD or PECVD.

[0075] Referring to FIG. 5B, a gate metal layer 604 is deposited on the
15 underlayer 602. The gate metal layer 604 is an electrically conductive layer that controls the movement of charge carriers within the thin film transistor. The gate metal layer 604 may comprise a metal such as, for example, aluminum, tungsten, chromium and molybdenum, among others. The gate metal layer 604 may be deposited using an embodiment of the cyclical deposition techniques as described above with reference to
20 FIGS. 3A and 4A. The gate metal layer 604 may be formed to a thickness in the range of about 1,000 Angstroms to about 5,000 Angstroms.

[0076] One or more gates 604 are formed in the gate metal layer 604a as shown in FIG. 5C. The one or more gates 604 may be formed using conventional lithography and etching techniques to form structure 625.

25 **[0077]** A gate dielectric layer 608 is formed on the one or more gates 604. The gate dielectric layer 608 may comprise, for example, silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3) and tantalum oxide (Ta_2O_5), among others. Typically the gate dielectric layer 608 has a thickness in the range of about 20 Angstroms to about 5,000 Angstroms.

30 **[0078]** A bulk semiconductor layer 610 is deposited on the gate dielectric layer 608. Alternatively, a silicon seed layer 609 may be deposited prior to the silicon bulk layer 610 deposition. The silicon seed layer 609 and bulk semiconductor layer 610 may be formed using conventional deposition techniques, such as CVD or PECVD. The bulk semiconductor layer 610 may comprise, for example, amorphous silicon. The

bulk semiconductor layer 610 may be have a thickness within a range of about 20 Angstroms to about 5,000 Angstroms.

[0079] An etch stop layer 612 may be deposited on the bulk semiconductor layer 610. The etch stop layer 612 may comprise an insulating material. The etch stop layer 612 may be formed using, for example, plasma enhanced chemical vapor deposition, chemical vapor deposition, physical vapor deposition, or other conventional methods known to the art. The etch stop layer 612 and the bulk semiconductor layer 610 are lithographically patterned and etched using conventional techniques.

[0080] A doped semiconductor layer 614 is formed on the patterned etch stop layer 612 and the bulk semiconductor layer 610. The doped semiconductor layer 614 may comprise, for example, silicon. The doped semiconductor layer 614 may be deposited to a thickness within a range of about 10 Angstroms to about 100 Angstroms. The doped semiconductor layer 614 contacts portions of the bulk semiconductor layer 610, forming a semiconductor junction.

[0081] A transparent conductor layer 616 is formed on portions of the gate dielectric layer 608 and the doped semiconductor layer 614. The transparent conductor layer 616 comprises a material that is generally optically transparent in the visible spectrum and is electrically conductive. The transparent conductor layer 616 may comprise, for example, indium tin oxide (ITO), zinc oxide, among others. The transparent conductor layer 616 is lithographically patterned and etched using conventional techniques.

[0082] A conductive layer 618 is formed on the doped semiconductor layer 614 and the transparent conductor layer 616. The conductive layer 618 may comprise a metal such as, for example, aluminum, tungsten, molybdenum, chromium, tantalum, and combinations thereof, among others. The conductive layer 618 may be formed using an embodiment of the cyclical deposition techniques as described above with reference to FIGS. 3A and 4A. The conductive layer 618 may be formed to a thickness in the range of about 1,000 Angstroms to about 5,000 Angstroms.

[0083] Both the conductive layer 618 and the doped semiconductor layer 614 may be lithographically patterned to define a source region 614a and a drain region 614b as well as a source contact 618a and a drain contact 618b. The source 614a and drain 614b regions of the thin film transistor are separated from one another by the stop etch layer 612.

[0084] A silicon-containing passivation layer 620 may be deposited on the substrate structure 650. The silicon-containing passivation layer 620 may comprise, for example, silicon nitride (Si_3N_4), silicon oxide (SiO), silicon dioxide (SiO_2) among others, deposited using an embodiment of the cyclical deposition technique described above with reference to FIGS. 3B and 4B. Silicon-containing passivation layer 620 may be deposited to a thickness within a range of about 1,000 Angstroms to about 5,000 Angstroms. The cyclical deposition techniques employed for the passivation bulk layer 620 deposition provide conformal step coverage on exposed surfaces of gate dielectric layer 608, source contact 618a, drain contact 618b, etch stop layer 612 and transparent conductor 616.

2. Top-Gate Thin Film Transistor

[0085] FIGS. 6A-6C illustrate cross-sectional schematic views of substrate structure 750 during different stages of a top-gate thin film transistor fabrication sequence incorporating a gate metal layer and a silicon-containing passivation layer formed using a cyclical deposition process. The top-gate thin film transistor may be, for example, a metal-oxide-semiconductor field effect transistor (MOSFET) or a junction field effect transistor (JFET). This transistor fabrication sequence is for a switch in an active matrix liquid crystal display (AMLCD) and this process depicts the formation of one of an array of switches used in an AMLCD.

[0086] FIG. 6A, for example, illustrates a cross-sectional view of a substrate 700. The substrate may comprise a material that is essentially optically transparent in the visible spectrum, such as, for example, glass or clear plastic, including soda-lime glass, borosilicate glass or quartz. The substrate may have an underlayer 702 thereon. The underlayer 702 may be an insulating material, such as, for example, silicon dioxide (SiO_2) or silicon nitride (Si_3N_4), deposited using an embodiment of the cyclical deposition technique described above with reference to FIGS. 3B and 4B.

[0087] A doped semiconductor layer 704 is deposited on the underlayer 702. The doped semiconductor layer 704 may comprise silicon. The doped semiconductor layer 704 includes n-type doped regions 704n and p-type doped regions 704p. The interfaces between n-type doped regions 704n and p-type doped regions 704p are semiconductor junctions that support the ability of the thin film transistor (TFT) to act as a switching device.

[0088] A gate dielectric layer 708 is deposited on the n-type doped regions 704n and the p-type doped regions 704p. The gate dielectric layer 708 may comprise, for example, silicon oxide, silicon dioxide, aluminum oxide (Al_2O_3), and tantalum oxide (Ta_2O_5), among others. The gate dielectric layer 708 may be formed using 5 conventional deposition processes, such as CVD or PECVD.

[0089] Referring to FIG. 6B, a gate metal layer 710a is deposited on the gate dielectric layer 708. The gate metal layer 710a comprises an electrically conductive layer that controls the movement of charge carriers within the thin film transistor. The gate metal layer 710a may comprise a metal such as, for example, aluminum, 10 tungsten, chromium, molybdenum or combinations thereof, among others.

[0090] The gate metal layer 710a may be formed using an embodiment of the cyclical deposition techniques as described above with reference to FIGS. 3A and 4A. The gate metal layer 710a may be formed to a thickness in the range of about 1,000 Angstroms to about 5,000 Angstroms. After deposition the gate metal layer is 15 patterned to define gates using conventional lithography and etching techniques.

[0091] One or more gates 710 are formed in the gate metal layer 710a as shown in FIG. 6C. The one or more gates 710 may be formed using conventional lithography and etching techniques.

[0092] After the gates 710 are formed, an interlayer dielectric 712 is formed 20 thereon. The interlayer dielectric 712 may comprise, for example, an oxide such as silicon dioxide. The interlayer dielectric 712 may be formed using conventional deposition processes.

[0093] The interlayer dielectric 712 is patterned to expose the n-type doped regions 704n and the p-type doped regions 704p. The patterned regions of the 25 interlayer dielectric 712 are filled with a conductive material to form contacts 720. The contacts 720 may comprise a metal such as, for example, aluminum, tungsten, molybdenum and chromium among others. The contacts 720 may be formed using an embodiment of the cyclical deposition techniques as described above with reference to FIGS. 3A and 4A.

30 [0094] Thereafter, a silicon-containing passivation layer 722 may be formed thereon in order to protect and encapsulate a completed thin film transistor 725. The silicon-containing passivation layer 722 may be formed using an embodiment of the cyclical deposition process described above with reference to FIGS. 3-4. The silicon-containing passivation layer 722 may comprise, for example, silicon nitride (Si_3N_4),

silicon oxide (SiO), and silicon dioxide (SiO_2), among others. The silicon-containing passivation layer 722 may be deposited to a thickness within a range of about 1,000 Angstroms to about 5,000 Angstroms.

[0095] Silicon-containing passivation layers, such as those described with reference to FIGS. 5A-6C, are less likely to form defects that lead to device failure. Thin film transistors incorporating silicon-containing passivation layers deposited using embodiments described herein provide also provide excellent protection of the thin film transistor from environmental hazards such as moisture and oxygen.

[0096] It is within the scope of the invention to form other devices that have configurations of semiconductor layers that are different from those described above with reference to FIGS. 5A-6C. For example, the switch for an AMLCD may be any variety of bipolar or unipolar transistor devices wherein a gate metal layer is deposited using the cyclical deposition process described herein.

[0097] While the foregoing is directed to the preferred embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A method of forming a gate metal layer on a substrate, comprising:

providing a substrate, wherein the substrate is used in an active matrix liquid
5 crystal display; and

depositing a gate metal layer on the substrate using a cyclical deposition process comprising a plurality of cycles, wherein each cycle comprises establishing a flow of an inert gas to a process chamber and modulating the flow of the inert gas with an alternating period of exposure to a metal-containing precursor and a reducing gas.

10

2. The method of claim 1, wherein the period of exposure to the metal-containing precursor, the period of exposure to the reducing gas, a period of flow of the inert gas between the period of exposure to the metal-containing precursor and the period of exposure to the reducing gas, and a period of flow of the inert gas between the period
15 of exposure to the reducing gas and the period of exposure to the metal-containing precursor each have the same duration.

3. The method of claim 1, wherein at least one of the period of exposure to the metal-containing precursor, the period of exposure to the reducing gas, a period of flow
20 of the inert gas between the period of exposure to the metal-containing precursor and the period of exposure to the reducing gas, and a period of flow of the inert gas between the period of exposure to the reducing gas and the period of exposure to the metal-containing precursor has a different duration.

25 4. The method of claim 1, wherein the period of exposure to the metal-containing precursor during each deposition cycle of the cyclical deposition process has the same duration.

5. The method of claim 1, wherein at least one period of exposure to the metal-
30 containing precursor for one or more deposition cycle of the cyclical deposition process has a different duration.

6. The method of claim 1, wherein the period of exposure to the reducing gas during each deposition cycle of the cyclical deposition process has the same duration.

7. The method of claim 1, wherein at least one period of exposure to the reducing gas for one or more deposition cycle of the cyclical deposition process has a different duration.

5

8. The method of claim 1, wherein a period of flow of the inert gas between the period of exposure to the metal-containing precursor and the period of exposure to the reducing gas during each deposition cycle of the cyclical deposition process has the same duration.

10

9. The method of claim 1, wherein at least one period of flow of the inert gas between the period of exposure to the metal-containing precursor and the period of exposure to the reducing gas for one or more deposition cycle of the cyclical deposition process has a different duration.

15

10. The method of claim 1, wherein a period of flow of the inert gas between the period of exposure to the reducing gas and the period of exposure to the metal-containing precursor during each deposition cycle of the cyclical deposition process has the same duration.

20

11. The method of claim 1, wherein at least one period of flow of the inert gas between the period of exposure to the reducing gas and the period of exposure to the metal-containing precursor for one or more deposition cycle of the cyclical deposition process has a different duration.

25

12. The method of claim 1, wherein the gate metal layer comprises a material selected from the group consisting of aluminum, tungsten, chromium and molybdenum.

13. The method of claim 1, wherein the metal-containing precursor comprises a
30 compound selected from the group consisting of dimethyl aluminum hydride, trimethyl aluminum, tungsten hexafluoride, tungsten hexacarbonyl, molybdenum pentachloride and chromium tetrachloride.

14. The method of claim 1, wherein the reducing gas comprises a gas selected from the group consisting of silane, disilane, dichlorosilane, ammonia, hydrazine, monomethyl hydrazine, dimethyl hydrazine, t-butyl hydrazine, phenyl hydrazine, 2,2'-azoisobutane, ethylazide, triethylborane, borane and diborane.

5

15. A method of forming a silicon-containing passivation layer on a substrate, comprising:

providing a substrate, wherein the substrate is used in an active matrix liquid crystal display; and

10 depositing a silicon-containing passivation layer on the substrate using a cyclical deposition process comprising a plurality of cycles, wherein each cycle comprises establishing a flow of an inert gas to a process chamber and modulating the flow of the inert gas with an alternating period of exposure to a silicon-containing precursor and a reactant gas.

15

16. The method of claim 15, wherein the period of exposure to the silicon-containing precursor, the period of exposure to the reactant gas, a period of flow of the inert gas between the period of exposure to the silicon-containing precursor and the period of exposure to the reactant gas, and a period of flow of the inert gas between the period 20 of exposure to the reactant gas and the period of exposure to the silicon-containing precursor each have the same duration.

17. The method of claim 15, wherein at least one of the period of exposure to the silicon-containing precursor, the period of exposure to the reactant gas, a period of flow 25 of the inert gas between the period of exposure to the silicon-containing precursor and the period of exposure to the reactant gas, and a period of flow of the inert gas between the period of exposure to the reactant gas and the period of exposure to the silicon-containing precursor has a different duration.

30 18. The method of claim 15, wherein the period of exposure to the silicon-containing precursor during each deposition cycle of the cyclical deposition process has the same duration.

19. The method of claim 15, wherein at least one period of exposure to the silicon-containing precursor for one or more deposition cycle of the cyclical deposition process has a different duration.

5 20. The method of claim 15, wherein the period of exposure to the reactant gas during each deposition cycle of the cyclical deposition process has the same duration.

21. The method of claim 15, wherein at least one period of exposure to the reactant gas for one or more deposition cycle of the cyclical deposition process has a different
10 duration.

22. The method of claim 15, wherein a period of flow of the inert gas between the period of exposure to the silicon-containing precursor and the period of exposure to the reactant gas during each deposition cycle of the cyclical deposition process has the
15 same duration.

23. The method of claim 15, wherein at least one period of flow of the inert gas between the period of exposure to the silicon-containing precursor and the period of exposure to the reactant gas for one or more deposition cycle of the cyclical deposition
20 process has a different duration.

24. The method of claim 15, wherein a period of flow of the inert gas between the period of exposure to the reactant gas and the period of exposure to the silicon-containing precursor during each deposition cycle of the cyclical deposition process
25 has the same duration.

25. The method of claim 15, wherein at least one period of flow of the inert gas between the period of exposure to the reactant gas and the period of exposure to the silicon-containing precursor for one or more deposition cycle of the cyclical deposition
30 process has a different duration.

26. The method of claim 15, wherein the silicon-containing precursor comprises a compound selected from the group consisting of silane, disilane, hexachlorodisilane, silicon tetrachloride, dichlorosilane and trichlorosilane.

27. The method of claim 15, wherein the reactant gas comprises one or more compound selected from the group consisting of ammonia, hydrazine, nitrogen, oxygen, ozone, hydrogen and water vapor.

5 28. The method of claim 15, wherein the reactant gas is disassociated in a plasma.

29. A transistor for use in an active matrix liquid crystal display, comprising:

a substrate and a gate metal layer formed thereon, the gate metal layer is formed using a cyclical deposition process comprising a plurality of cycles, wherein 10 each cycle comprises establishing a flow of an inert gas to a process chamber and modulating the flow of the inert gas with an alternating period of exposure to a metal-containing precursor and a reducing gas.

30. A transistor for use in an active matrix liquid crystal display, comprising:

15 a substrate and a silicon-containing passivation layer formed thereon, wherein the silicon-containing passivation layer is formed using a cyclical deposition process comprising a plurality of cycles, wherein each cycle comprises establishing a flow of an inert gas to a process chamber and modulating the flow of the inert gas with an alternating period of exposure to a silicon-containing precursor and a reactant gas.

20

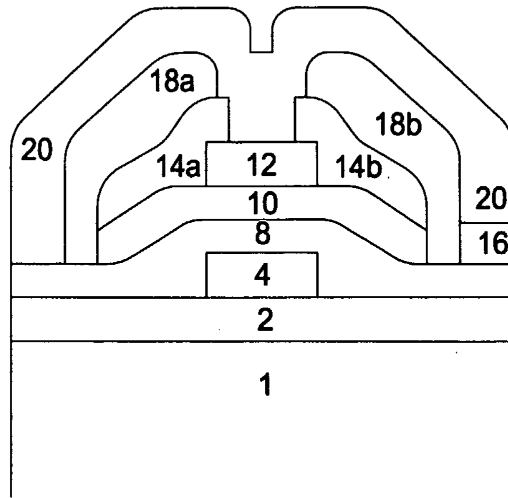

FIG. 1

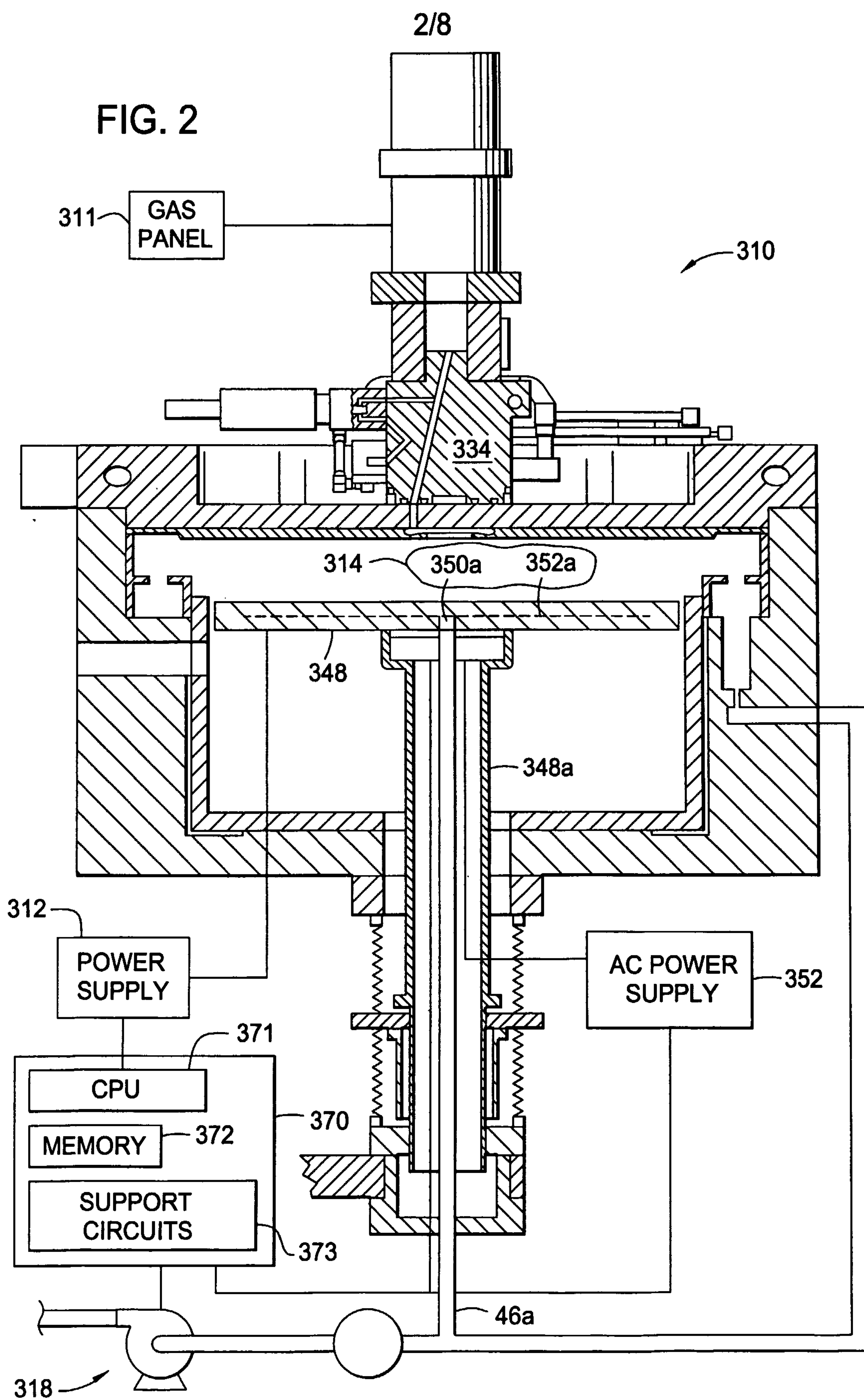
FIG. 2
311
GAS PANEL
310
334
314
350a
352a
348
348a
312
POWER SUPPLY
AC POWER SUPPLY
352
371
CPU
370
MEMORY
372
SUPPORT CIRCUITS
373
46a
318

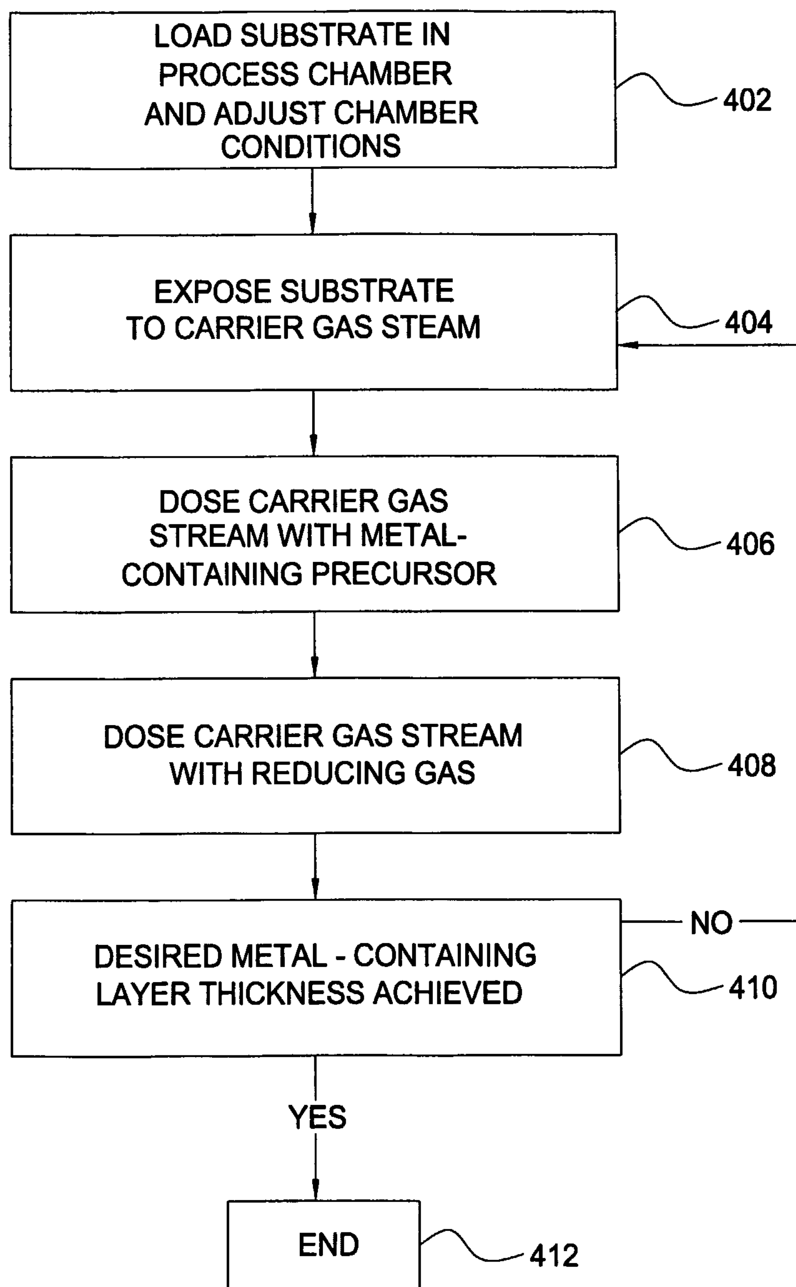

FIG. 3A

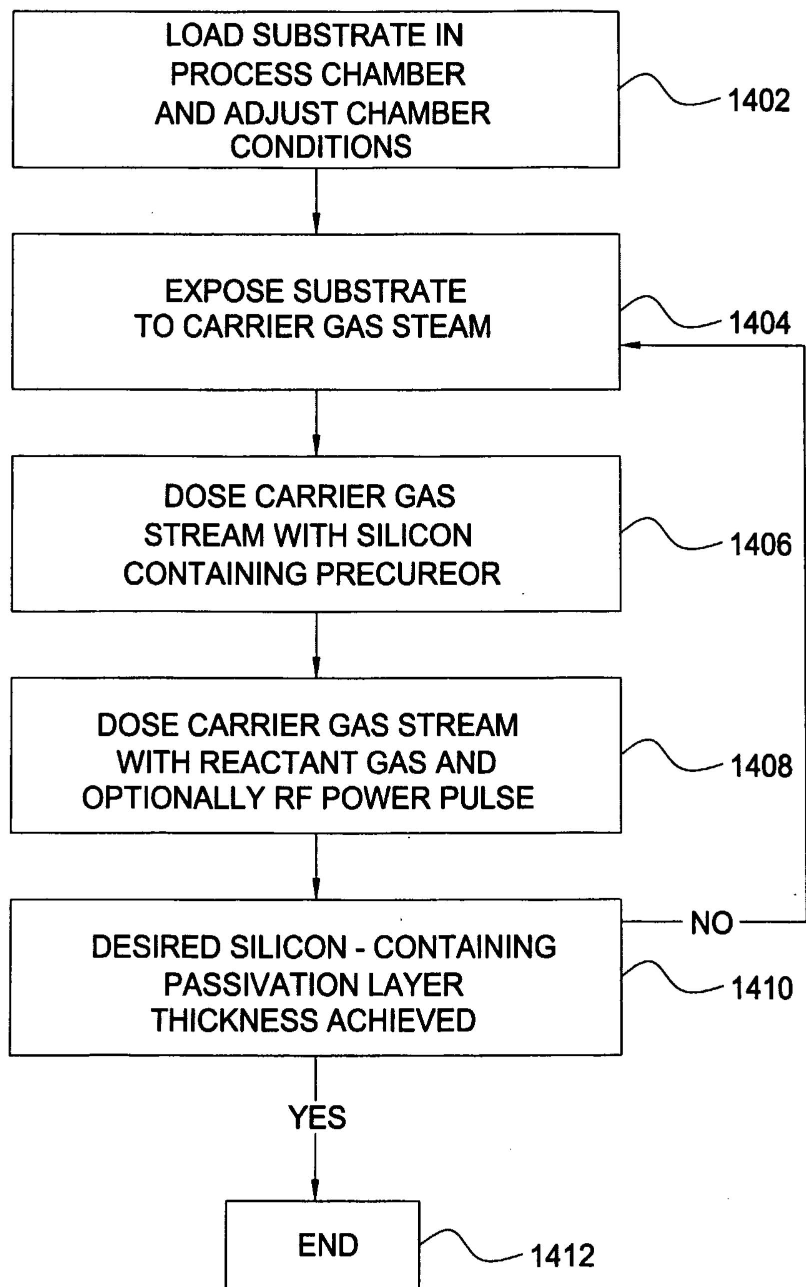

FIG. 3B

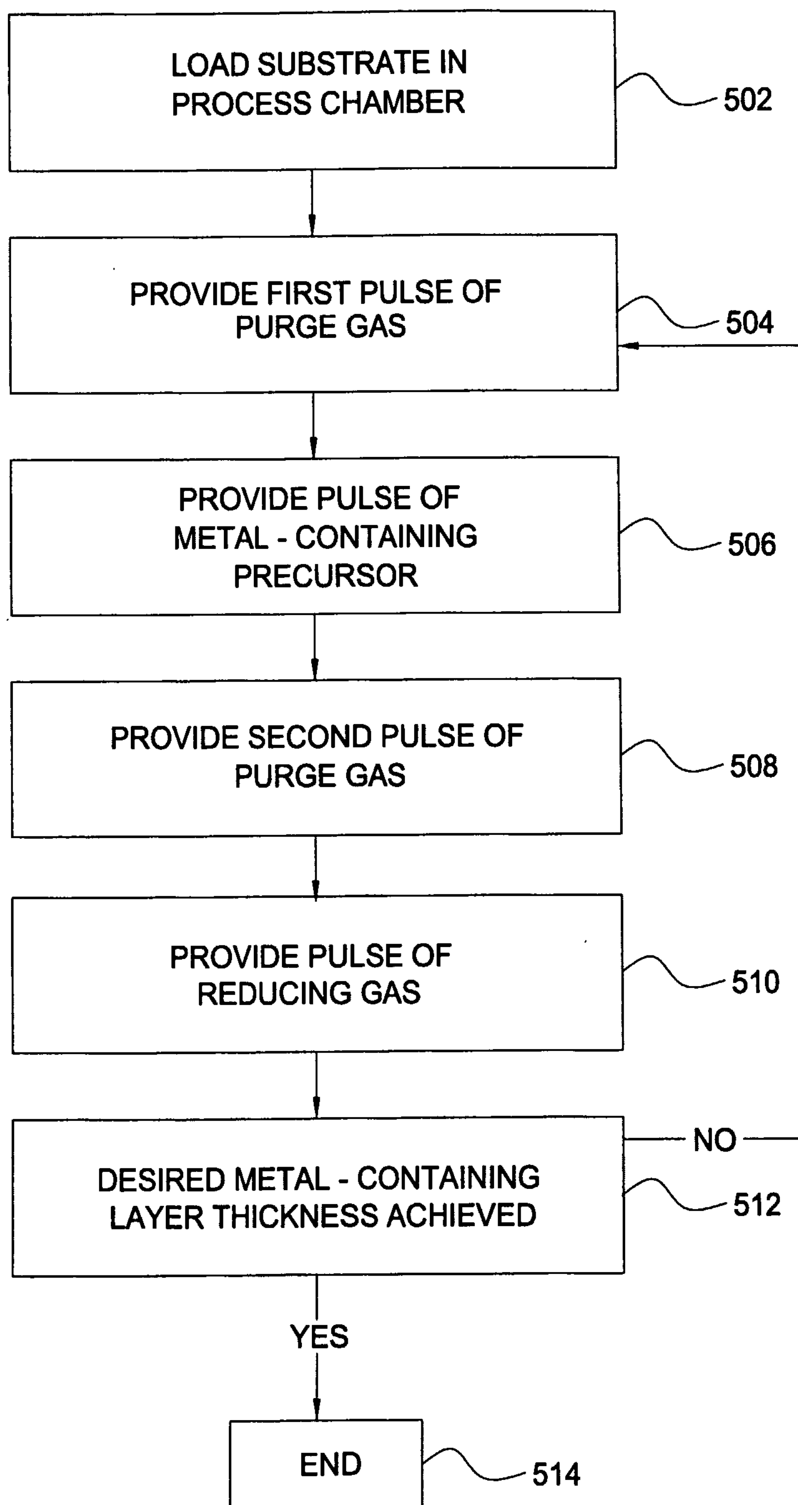

FIG. 4A

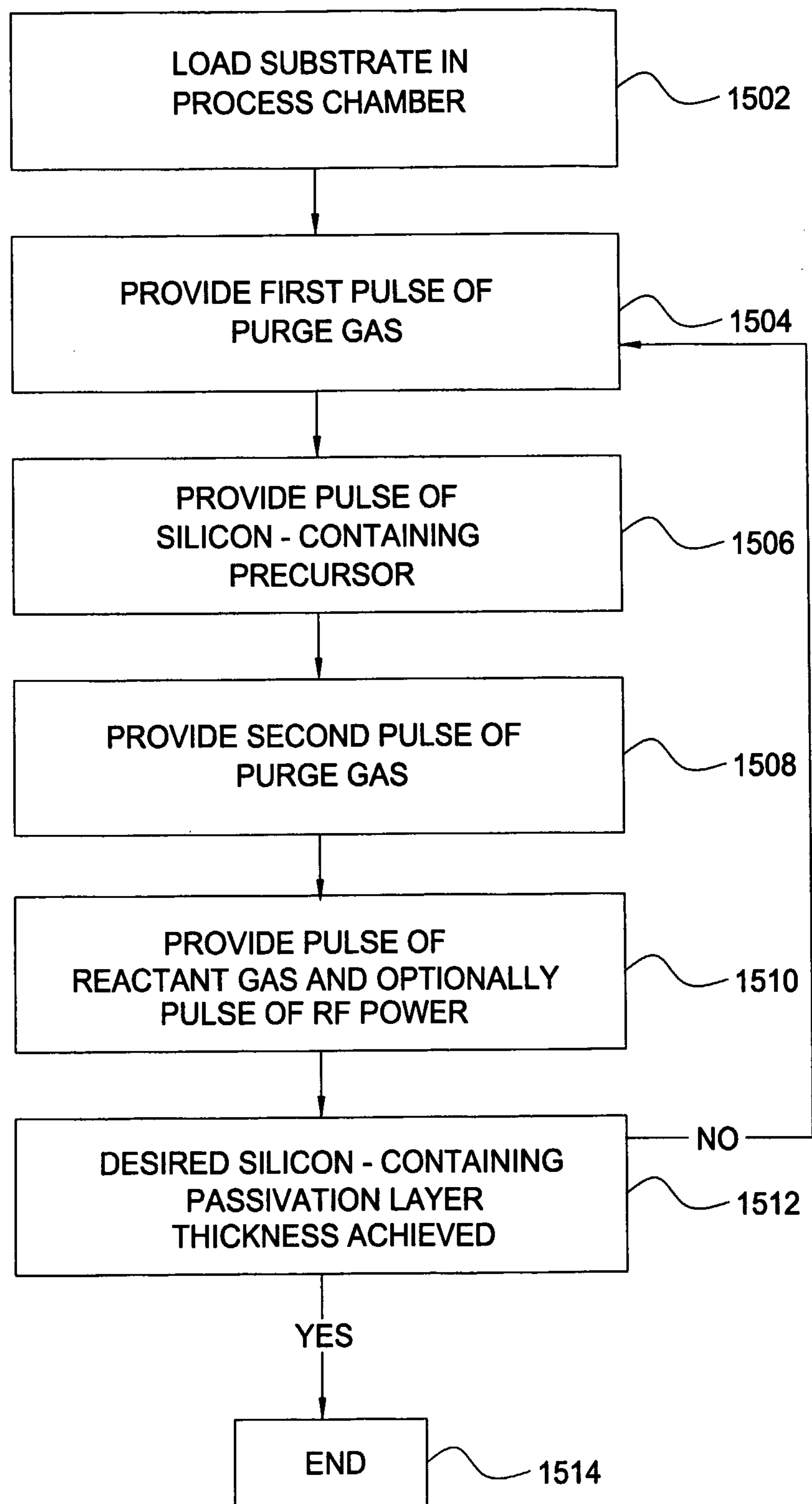

FIG. 4B

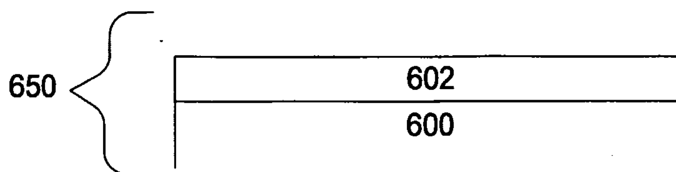

FIG. 5A

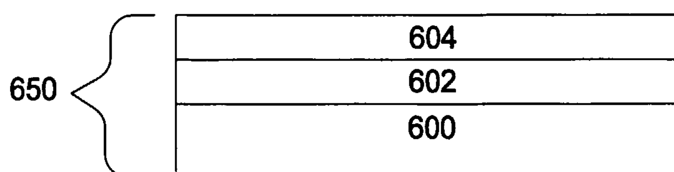

FIG. 5B

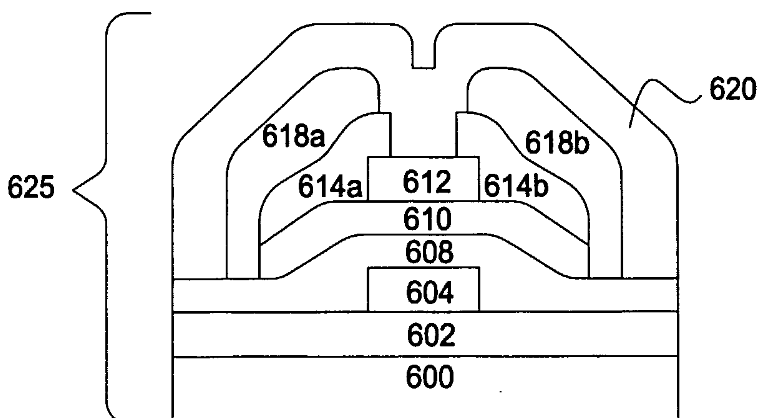

FIG. 5C

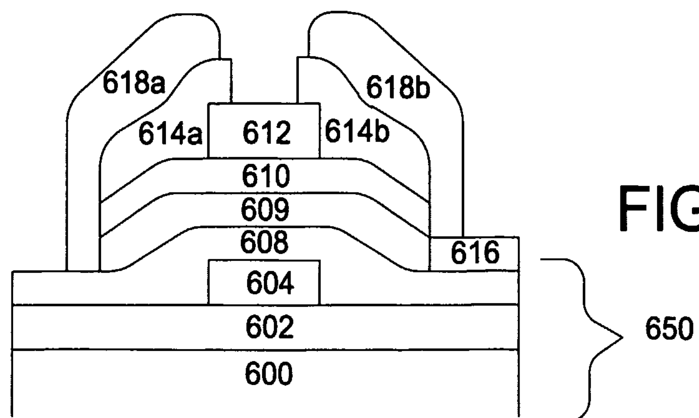

FIG. 5D

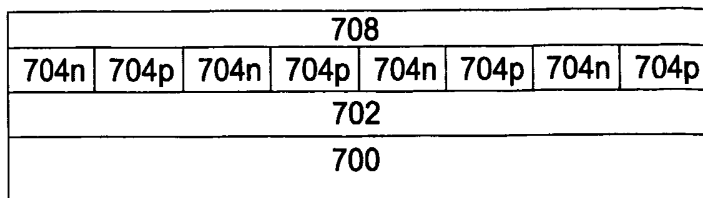

FIG. 6A

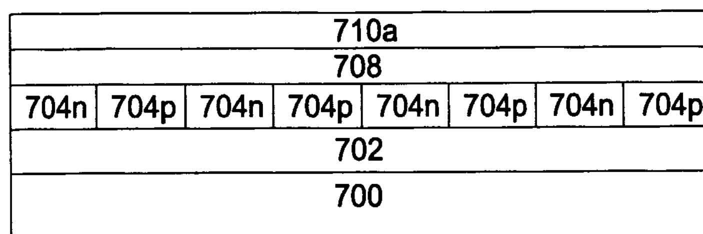

FIG. 6B

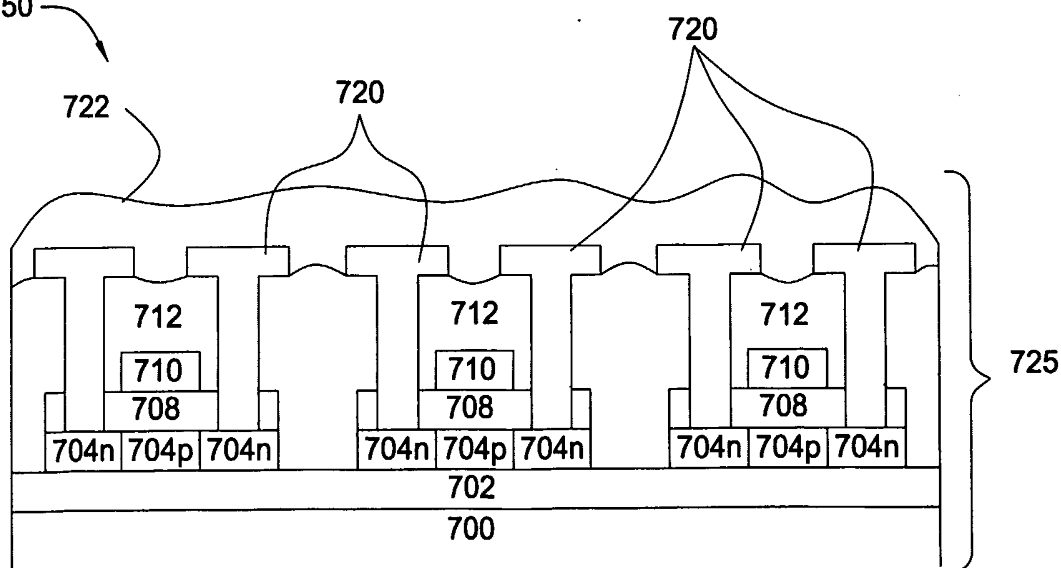

FIG. 6C