

[54] CONTROLLABLE WAVEFORM GENERATOR

[72] Inventor: Lloyd Wayne Hunter, Beaverton, Oreg.

[73] Assignee: Exact Electronics, Inc., Hillsboro, Oreg.

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[58] Field of Search 307/228; 328/127, 128, 151, 328/183, 185

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Primary Examiner—Donald D. Forrer

Assistant Examiner—R. C. Woodbridge

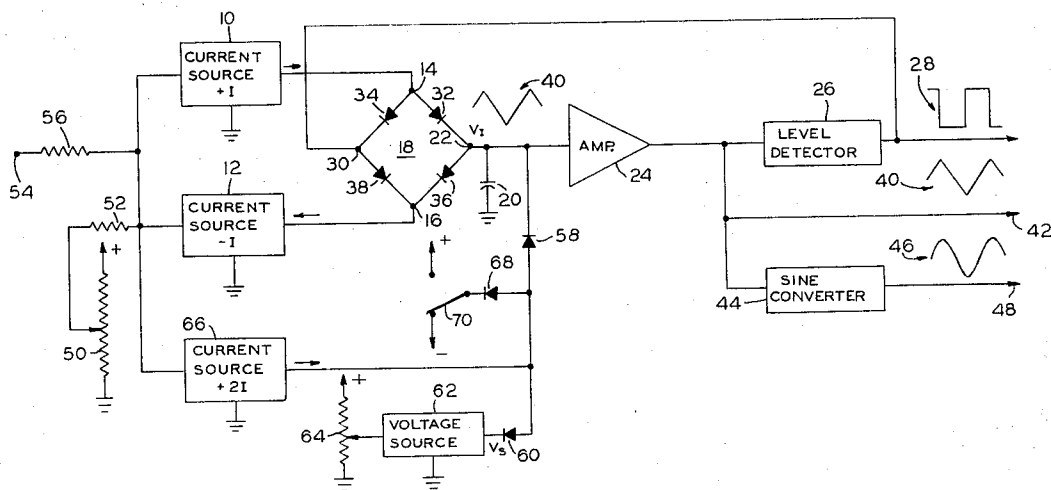
Attorney—Buckhorn, Blore, Klarquist and Sparkman

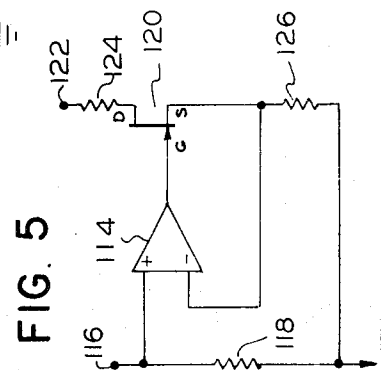
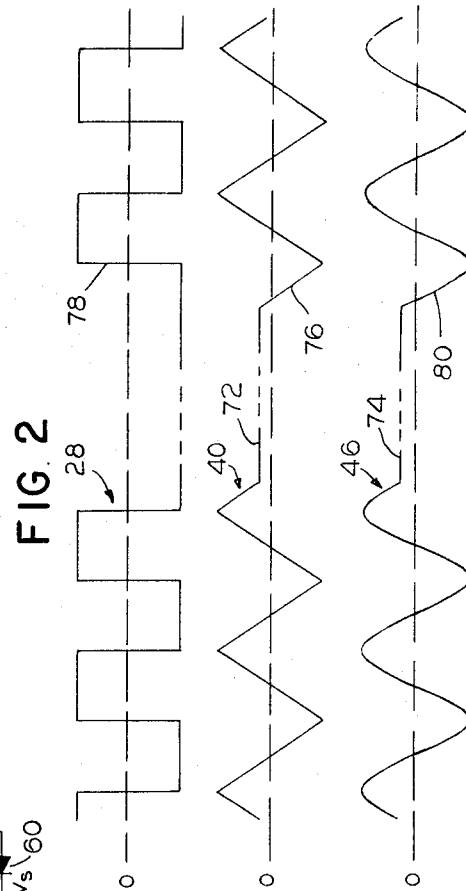
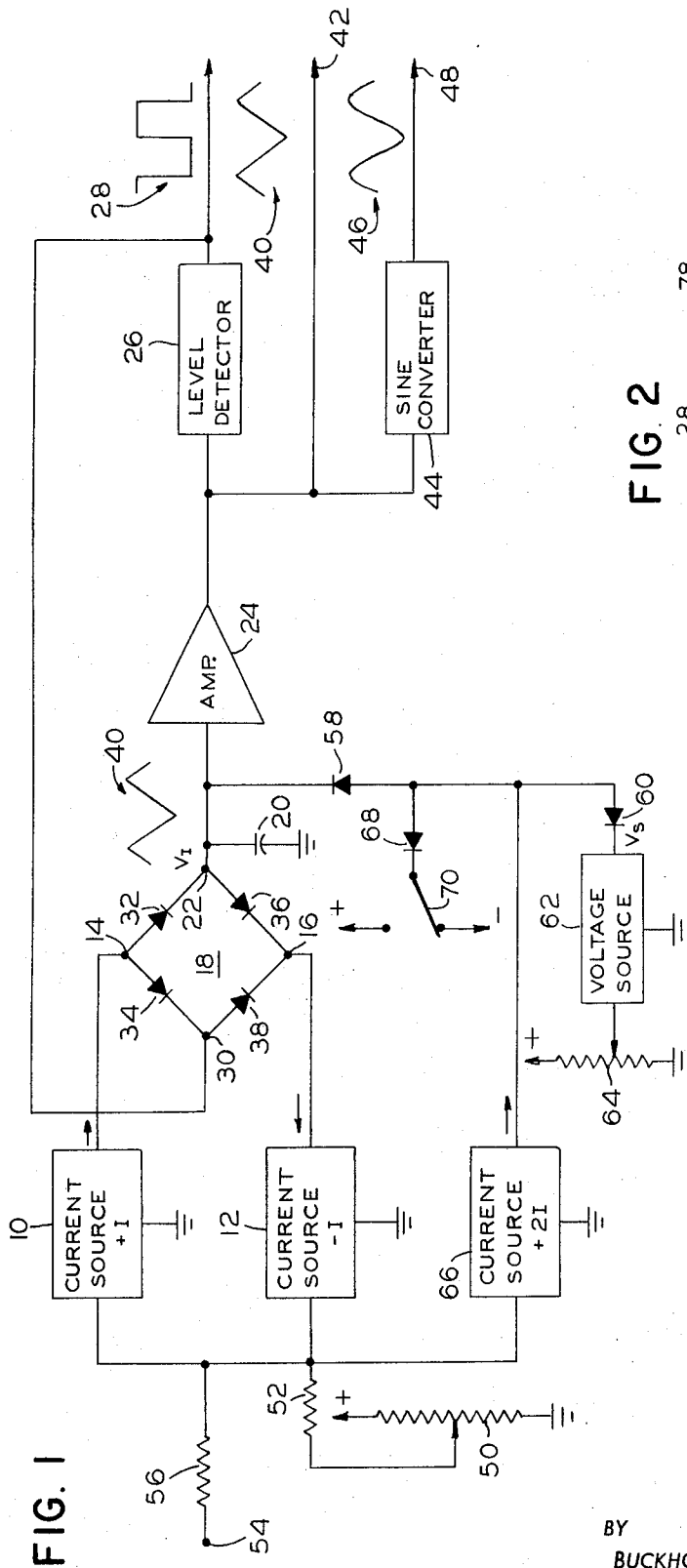
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ABSTRACT

A waveform generator includes an integrating circuit alternately provided with oppositely directed, adjustable input currents, under the control of a level detector responsive to predetermined positive and negative extremes of the integrated output. Adjustment of input current is effective for changing the frequency of operation. The triangular waveform produced may be terminated at a selectable level therealong through operation of a gating means which interrupts an aforementioned input current when the integration reaches a predetermined intermediate voltage level. Waveform generation is subsequently resumed at this same level. When interrupted, the input current returns to a current source providing a current adjustably proportioned relative to the input current.

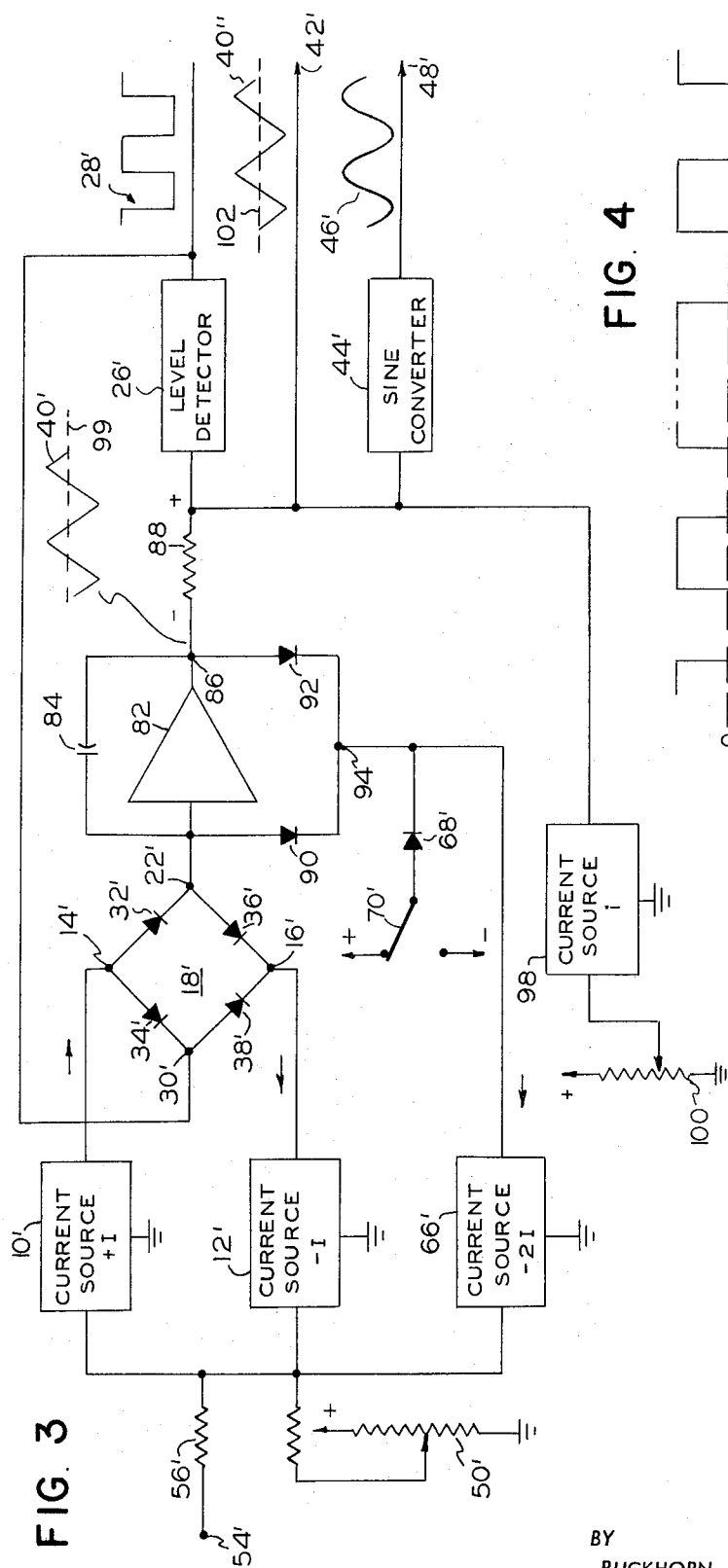
12 Claims, 5 Drawing Figures





LLOYD WAYNE HUNTER
INVENTOR

BY
BUCKHORN, BLORE, KLARQUIST & SPARKMAN
ATTORNEYS



LLOYD WAYNE HUNTER
INVENTOR

BY
BUCKHORN, BLORE, KLARQUIST & SPARKMAN
ATTORNEYS

CONTROLLABLE WAVEFORM GENERATOR

BACKGROUND OF THE INVENTION

Many forms of signal generators are available for producing a selectable waveform having a given configuration, amplitude, repetition rate, or the like, and the generated signal can usually be supplied at some predetermined time. For a variety of test purposes, the generation of an adjustable frequency test signal starting at a more accurately predetermined selectable point relative to its own waveform than signal generators now available would be desirable.

SUMMARY OF THE INVENTION

According to the present invention, a controllable waveform generator produces an output waveform which can be supplied starting at a particular selectable point along the waveform, i.e. in a particular phase relation relative to such waveform. An integrator circuit in the present generator is responsive to an adjustable input current for producing a substantially triangular wave, correspondingly adjustable in frequency, the generator further including a level detector for detecting when the triangular wave reaches predetermined extreme or peak values thereof. The input current provided the integrator is controlled in polarity and responsive to the detection of such extreme values whereby the input current is reversed for generating an oppositely directed ramp of the triangular wave. Gating means are controllably responsive to the integration for detecting when the integration value reaches a predetermined level or value along the triangular wave between peak values, and for thereupon interrupting the flow of input current relative to the integrator. A given output value is maintained at this time by the integrator. A current source return is provided for the input current so that integration thereof is halted, this current source providing a current which changes with changes or adjustments in input current. The aforementioned gating means is also selectively operative for restoring the integrator input current in order to reinitiate generation of the triangular wave beginning at the predetermined value.

According to one embodiment of the present invention, the integrator circuit includes a chargeable capacitor, and the gating means comprises a diode circuit for diverting current from the aforementioned capacitor when the voltage thereacross reaches a predetermined level. A current is supplied through the gating means for providing a return for input current theretofore supplied the capacitor.

In accordance with another embodiment of the present invention, the integrator comprises a Miller integrator circuit, and the gating means comprises diode means for discharging the feedback capacitor of the Miller integrator. A voltage dropping means is included between the Miller integrator and the aforementioned level detector for offsetting the extremes of integrator circuit waveform relative to the input of the level detector. Consequently, the discharge condition of the feedback capacitor can be made to correspond to a selected point along the triangular waveform generated. In either embodiment of the generator circuit according to the present invention, triangular wave generation is resumed by operating the diode gate circuitry for bringing about resumed charging of the integrator capacitor.

It is an object of the present invention to generate an adjustable frequency waveform starting at a selectable point along the waveform configuration.

It is another object of the present invention to provide an improved waveform generator for supplying an adjustable frequency waveform starting at a particular predetermined point along the configuration of said waveform.

It is another object of the present invention to provide an improved waveform generator for supplying an adjustable frequency waveform which is interruptible at a given point therealong and wherein generation of the waveform may be resumed at the same point.

It is a further object of the present invention to provide an improved waveform generator for accurately supplying an adjustable frequency triangular wave output and sine wave output wherein waveform output can be initiated at a particular time and at a particular point relative to the triangular or sine waveform.

It is another object of the present invention to provide an improved waveform generator for supplying an adjustable frequency waveform which can be initiated in selectable phase relation with such waveform.

The subject matter which I regard as my invention is particularly pointed out and distinctly claimed in the concluding portion of this specification. The invention, however, both as to organization and method of operation, together with further advantages and objects thereof, may best be understood by reference to the following description taken in connection with the accompanying drawings wherein like reference characters refer to like elements.

DRAWINGS

FIG. 1 is a schematic diagram of a circuit according to a first embodiment of the generator according to the present invention;

FIG. 2 is a waveform chart depicting operation of the FIG. 1 circuit;

FIG. 3 is a circuit diagram of a second circuit embodiment of the generator of the present invention;

FIG. 4 is a waveform chart illustrating operation of the FIG. 3 circuit; and

FIG. 5 is a schematic diagram of a controlled current source suitably employed with the generator according to the present invention.

DETAILED DESCRIPTION

Referring to the drawings, and particularly to FIG. 1 illustrating a first embodiment of a waveform generator according to the present invention, a positive current source 10 and a negative current source 12 supply input currents of +I and -I, respectively, to terminals 14 and 16 of diode bridge 18. Diode bridge 18 is employed for controllably reversing the current input applied to an integrator circuit, the latter including a capacitor 20 disposed between a conjugate bridge terminal 22 and ground. The junction between capacitor 20 and bridge terminal 22 is also connected to the input buffer amplifier 24, suitably exhibiting a gain of one, this amplifier having a high impedance input and relatively low impedance output for driving a hysteresis switch or level detector 26. Circuits of the level detector type are well known in the art and function to provide an output value switched in accordance with the level reached at the detector input. Thus, for example, if the output of amplifier 24 reaches a given positive level, the output of level detector 26 switches from a predetermined positive value to a predetermined negative value. If the output of amplifier 24 drops below a predetermined negative level, the output of level detector 26 will change from its negative value back to the aforementioned positive value. The output of level detector 26, exemplified by square wave 28 in the drawing, is applied to remaining conjugate bridge terminal 30.

The bridge 18 comprises diodes 32 and 34 having their anodes connected to terminal 14 and their cathodes respectively connected to terminals 22 and 30. The bridge further includes diodes 36 and 38 having their cathodes connected to terminal 16, and their anodes respectively connected to terminals 22 and 30.

The circuit as thus far described generates a triangular waveform 40 at output terminal 42 driven from the output of amplifier 24. Assuming the output of level detector 26 is initially in its lower or negative state, diode 34 will be forward biased by such output, and diode 38 will be reverse biased. Also, diode 32 will be reverse biased by the voltage level at its anode, while diode 36 will conduct. The negative input current, -I, coupled through diode 36, will charge capacitor 20

negatively. Since a current source is involved, the voltage, V_i , on capacitor 20 will increase linearly in a negative direction. Charging will continue until a level of integration equaling the negative switching level of detector 26 is reached, whereupon the output of detector 26 changes from its relatively negative value to its relatively positive value. At this time, diodes 34 and 36 are reverse biased, while diodes 32 and 38 conduct. Therefore, the voltage, V_i , across capacitor 30 will linearly change in a positive direction until the positive switching level of detector 26 is reached. Then the output of detector 26 returns to its negative value completing the cycle. It will be seen that the positive and negative charging excursions of capacitor 20 produce the triangular waveform as illustrated at 40. The currents from sources 10 and 12 are desirably equal in magnitude, whereby the triangular waveform 40 is symmetrical. This triangular waveform is suitably applied to a conventional sine converter 44 which produces a sine wave 46, at terminal 48, this sine wave being generated in phase with triangular wave 40. Although a sine converter is thus employed for providing a highly desirable waveform output, it is understood many other desirable waveforms may be similarly generated in phase synchronism with the triangular wave. In general, analog means may be utilized for generating different portions of a desired wave in response to voltage levels attained by the triangular wave.

The absolute values of current +I and -I are adjustable by means of potentiometer 50 employed for supplying selected input voltage for controlling current sources 10 and 12 via resistor 52. Thus, for example, if the input voltage provided by potentiometer 50 increases, the magnitude of currents +I and -I is proportionately increased such that the capacitor 20 charges more rapidly. Therefore, the time required for the integration value to reach the positive and negative detecting levels of detector 26 will decrease, and the frequency of the triangular wave will increase. Alternatively, if the values of +I and -I are reduced, the frequency will decrease. The outputs of sources 10 and 12 may alternatively be controlled by an external input applied at terminal 54 via coupling resistor 56. Controllable current sources of a desired type are described hereinbelow.

Gating means are selectively operative for reacting to a given integration level of the charge upon capacitor 20, and for concluding the integration cycle at that time. The integration cycle may be later resumed at the same value. Consequently, the triangular or sine wave provided as an output can be controlled to start at a particular level, or phase, according to test requirements.

The gating means in the case of the FIG. 1 embodiment comprises first and second reversely poled diodes 58 and 60 connected in series between the ungrounded terminal of capacitor 20 and an adjustable voltage source 62. Diodes 58 and 60 in the illustrated embodiment have their anodes connected together. Source 62 is provided with an input potentiometer 64 by means of which the output voltage V_s may be adjusted. Also, a current source 66 has its output coupled to the interconnection of diodes 58 and 60, and its control input coupled in common with the control inputs of current sources 10 and 12 so that the current from source 66 charges in proportion to the currents from sources 10 and 12. Current source 66 may be of substantially the same type as current sources 10 and 12, but is designed to provide double the current thereof. Thus, if current source 10 supplies +I and the current from current source 12 is -I, then the current from current source 66 is arranged to be +2I.

An additional diode 68 is interposed between the junctions of diodes 58 and 60 and the movable terminal of a switch 70 adapted for connecting either a predetermined positive or negative voltage to the cathode of diode 68. Switch 70 normally connects the cathode of diode 68 to a negative voltage whereby diode 68 carries the current +2I from current source 66, and diodes 58 and 60 are back biased.

When it is desired to arrest output waveform excursion at a given level, switch 70 is moved to its positive position whereby

diode 68 is reverse biased. The circuit will reach a rest condition wherein a current +I from current source 66 will flow through diode 58, and another +I will flow from source 66 through diode 60 to voltage source 62. The quiescent voltage on capacitor 20, and the corresponding interruption points on the triangular and sine wave output waveforms, are proportionately controlled by the setting of potentiometer 64. The same levels will be maintained until switch 70 is returned to its original position.

Considering operation of this circuit in greater detail, if the output from level detector 26 is positive and the triangular waveform 40 is positive-going at the time switch 70 is thrown to its upper position, integration will continue in a positive direction until level detector 26 switches its output. Then, the voltage across capacitor 20 will decrease until a current, +I, is drawn through diode 58. Current source 66 thus supplies just the correct return current value for current -I from current source 12 flowing through diode 36, and no current will remain for charging capacitor 20 in a negative direction. This will be true whatever the absolute value of current -I may be, since the current sources are designed to "track" one another. Consequently, the voltage across capacitor 20 will change no further. The voltage level reached will be determined by voltage source 62, to which the remaining current, +I, from current source 66 flows via diode 60. Diodes 58 and 60 are desirably matched such that the voltage drops thereacross will be equal when a current, +I, flows through each. Consequently, the voltage reached by waveform 40 before integration stops is accurately determined by voltage source 62 whereby V_i equals V_s .

Of course, if the voltage across capacitor 20 is already negative going when switch 70 is closed, but is above the voltage level selected by voltage source 62, the capacitor will charge down to the voltage selected by source 62, at which time integration will stop. If the voltage across capacitor 20 has charged past the level selected by means of voltage source 62, capacitor 20 will charge up to the selected level.

FIG. 2 depicts, for example, the condition wherein switch 70 is thrown, after the voltage, V_i , across capacitor 20 starts to decrease, but before a level selected by voltage source 62 has been reached. In the particular instance illustrated, a level has been selected by source 62 above the zero axis. Thus, the voltage V_i will decrease until voltage V_s is reached, at which time the charge across capacitor 20 remains constant. This level is indicated at 72 in FIG. 2. Of course, a similar level 74 is dictated for sine wave 46. Subsequently, when it is desired that generation of output waveforms 40 and 46 resume, switch 70 is returned to its original position, connecting the cathode of diode 68 to a negative voltage, whereby diodes 58 and 60 are back biased. Thereupon, the cycle of operation is continued, starting at level 72, with the voltage across capacitor 20 decreasing linearly as indicated at 76 until the level is reached at which level detector 26 switches at 78. Also, the sine wave output resumes at the selected level or phase as illustrated at 80 in the drawing.

Although amplifier 24 is herein described as having a gain of one, it is understood that it may provide amplification if desired, or may even have a controllable amplification. As the gain of amplifier 24 is increased, the frequency achieved with the circuit will increase, assuming the same predetermined switching levels for detector 26.

Another embodiment of a circuit according to the present invention is illustrated in FIG. 3. The FIG. 3 circuit is adaptable for lower frequency operation, while the FIG. 1 circuit is preferred if the desired output waveform is relatively high in frequency. In the FIG. 3 circuit, similar components are referred to by primed reference numerals. The circuit operates in a manner substantially similar to the circuit of the FIG. 1 embodiment for producing a triangular wave output, except the integrator here comprises a Miller integrator circuit including a high gain amplifier 82 provided with a feedback capacitor 84. This type of integrator circuit is well known by those skilled in the art, and will not be described in

detail. Charging currents $+I$ and $-I$ are still delivered from current sources numbered 10' and 12', respectively, through diodes 32' and 36'. The integrated output, 40', is, however, reversed in phase at amplifier output terminal 86, and consequently, level detector 26' is arranged to produce an output 28' which changes from a positive value to a negative value as the integration at terminal 86 reaches a predetermined negative input level of detector 26'. Thereupon, the negative output from detector 26' reverse biases diodes 32' and 38' and the input current is provided from current source 12' via diode 36'. As a consequence, the right-hand side of capacitor 84 will charge positively. Of course, when the value at terminal 86 reaches the predetermined positive input level of detector 26', the output of detector 26' switches to a positive value for completing the cycle. The voltage from terminal 86 as applied to the input of level detector 26' is, however, actually offset by means of a resistor 88 as hereinafter more fully described.

Gating means for discontinuing integration at a predetermined point in the output cycle comprises a pair of similarly poled diodes 90 and 92 coupling the input and output terminals of the Miller integrator circuit to a common point 94. In the illustrated embodiment, the cathode terminals of diodes 90 and 92 are connected in common to terminal 94. Also, diode 68', disposed between the movable contact of switch 70' and point 94, has its cathode connected to terminal 94. Current source 66' in the FIG. 3 embodiment is also connected to terminal 94 and supplies a current $-2I$, and when switch 70' is in its normal, positive position, the current $-2I$ flows through diode 68'.

When switch 70' is thrown to its lower position, current source 66' tends to cause current to flow through diodes 90 and 92 and the result is the discharging of capacitor 84 to zero volts across this capacitor so that the integrator stops at the neutral voltage level 99 of the integrator circuit. If switch 70' is thrown to its negative position while the triangular wave 40' is positive going, the capacitor 84 will however continue charging in the same direction until the output of level detector 26 changes to its positive value for back-biasing diodes 34' and 36'. This will cause the capacitor 84 to discharge until the voltage at terminal 86 equals the voltage at terminal 22'. At this time, a current, I , will flow from source 10' through diode 32' and diode 90 to current source 66'. Diode 92 will also conduct a current I supplied by the amplifier 82. Diodes 90 and 92 are desirably matched whereby the voltage at the input and output terminals of the integrator, i.e. at terminals 22' and 86, will be equal for accurately holding the voltage across the capacitor at zero.

Of course, if switch 70' is thrown to its lower position when triangular waveform 40' is negative-going, above the neutral voltage level of the integrator 99, capacitor 84 will similarly be discharged to zero. If the triangular waveform 40' is negative-going and below such neutral voltage level, the capacitor 84 will also be discharged to zero. Sufficient current will flow through diode 90 to withdraw current from the capacitor and cause the output voltage of the integrator at terminal 86 to increase until it equals the voltage at the input to the amplifier 82 so that the integrator stops at the neutral voltage level 99.

Since the integrator in FIG. 3 always has its output reduced to its neutral voltage level through operation of switch 70', additional means are provided for producing a voltage drop between the output of the Miller integrator circuit and the level detector and changing the quiescent or stopping level of the output waveform at the input to the level detector 26'. This means includes the aforementioned resistor 88 through which a controllable current is passed. The circuit further includes a current source 98 for providing an adjustable current i . Current source 98 is controlled by a potentiometer 100, which is here illustrated as having a grounded end and an end connected to a positive potential. With the movable tap of the potentiometer at ground potential, the source 98 provides no output current. If the movable tap of potentiometer 100 is moved toward the positive end of the potentiometer, current

source 98 suitably provides a positive current. The magnitude of the current i is determined by the distance of the movable tap from the grounded end of the potentiometer. The output of current source 98 is connected to the input of level detector 26', at one end of resistor 88. The current i flows through the resistor 88, since the operational amplifier 82 has a low impedance output and acts as a sink for such current.

The current, i , through resistor 88 produces a voltage drop thereacross, with resistor 88 nonetheless coupling the output of amplifier 82 to the input of the level detector. The level detector can be a voltage actuated circuit so that the output of amplifier 82 is substantially unattenuated by resistor 88. For the direction of current flowing from source 98 to the amplifier 82, the voltage at the right end of resistor 88 will be positive relative to the voltage at terminal 86. The upper and lower limits of the triangular waveform at the input to the level detector 26' and therefore the zero axis 102 of the waveform 40'' at such input are all fixed by the level detector. The result of current flow through the resistor 88 is to offset the waveform 40' at the terminal 86 in the negative direction with respect to the neutral voltage level 99 of the integrator.

If the neutral voltage level 99 of the integrator is initially adjusted so as to be offset from the zero axis 102 of the waveform 40'', as shown in FIG. 4, by a voltage which is equal to one half the peak to peak voltage of the waveforms 40' and 40'', and the contact of the potentiometer 100 is adjusted to a point midway of this potentiometer so that the voltage drop across the resistor 88 is also equal to such offset voltage, then the zero axis of the waveform 40' will be symmetrical about the neutral voltage level 99 of the integrator. Actuation of the switch 70' to the negative position under these conditions will cause the integrator to stop the waveform 40' at the zero axis 99 of this waveform at the terminal 86, and also stop the waveform 40'' at the zero axis 102 of this waveform at the input to the level detector 26'.

If, however, the contact of the potentiometer 100 is moved further in a positive direction to cause more current to flow through the resistor 88, the waveform 40' will be moved further in a negative direction to a position such as shown in FIG. 4, so that stopping of the integrator at the neutral voltage level 99 will stop the waveform 40' at the point 112 and stop the output waveform 40'' at the level 104.

It will be apparent that the stopping point 112 on the waveform 40' and the corresponding level 104 of the waveform 40'' at which this waveform is interrupted may be moved between the lower peaks of the respective waveform 40' and 40'', and their upper peaks along the negative-going portions of these waveforms by adjusting the contact of the potentiometer 100.

Similarly, sine wave 46' will be interrupted at the corresponding level 106, and when triangular wave generation is resumed, the sine wave negative excursion will continue as illustrated at 110. Since the voltage across resistor 88 is controllable through adjustment of the current i , the point along the negative-going ramp of the triangular wave relative to the extremes thereof at which integration stops is readily selectable. Since the output is taken at the input of level detector 26', it is therefore taken relative to the extreme values of the output waveform. The DC level at which waveform generation may be suspended and resumed is thus readily selectable with respect to the unchanging zero or neutral axis of level detector 26'.

In each of the above circuits, the ability to adjust the frequency of circuit operation, e.g. with potentiometer 50 or 50', is of importance. Thus, the generator according to the present invention not only provides an output which can be interrupted or halted at a given phase location, but also an output which is fully adjustable in frequency. The current sources 10, 12, and 66 in FIG. 1 (or corresponding sources indicated by primed numerals in FIG. 3) receive the same input from the variable potentiometer or from an outside adjustable voltage source, and track one another whereby the ratio, $2I/I$, is reserved, current source 66 or 66' always supplying just the

right amount of current for preventing further integration beyond the desired point. A current source which may be advantageously employed is illustrated in FIG. 5.

Referring to FIG. 5, a controllable current source comprises an operational amplifier 114 having its positive or noninverting input connected to input terminal 116 to which a variable or adjustable control voltage is applied, e.g. via resistor 52 or resistor 56 in FIG. 1, or corresponding elements in FIG. 3. The positive input terminal of amplifier 114 is also returned to a negative voltage point via resistor 118. The output of amplifier 114 is coupled to the gate of an N channel field effect transistor 120, the drain of which is coupled to output terminal 122 through resistor 124, and the source terminal of which is connected to the negative or inverting input of amplifier 114. The source terminal is also connected to the negative voltage point which is maintained at a constant negative voltage with respect to ground.

The current source of FIG. 5 is responsive to the input voltage applied at terminal 116 for maintaining the voltage at the source terminal of transistor 120 equal to the voltage applied at terminal 116. If the positive and negative inputs of amplifier 114 are detectably different, the output of amplifier 114 controls the gate of field effect transistor 120 to restore the source voltage to the desired level of terminal 116. Consequently, the voltage from the source terminal of transistor 120 to the aforementioned negative voltage point is constant so long as the input voltage at terminal 116 remains unchanged, whereby the current through resistor 126 will remain constant. It is understood that amplifier 114 provides a very high input impedance, and it is also understood the source current of transistor 120 substantially equals the drain current thereof. Therefore, the current through resistor 124 and terminal 122 will be constant, and determined by the input voltage applied at terminal 116. The field effect transistor is employed in the above circuit in order to reduce or prevent loading of the amplifier, i.e. for isolating the amplifier and the output current circuit.

The current source in FIG. 5 will produce a "negative" current, that is, a flow of current into terminal 122. The provision of a "positive" current source will be obvious to those skilled in the art, and involves the use of a positive rather than a negative voltage reference point at the junction between resistors 118 and 126 and a P channel field effect transistor. It will be appreciated that the various current sources of FIGS. 1 and 3 will have suitable circuits for inverting the input voltages supplied to the "positive" current sources relative to the input voltages supplied to the "negative" current sources such as shown in FIG. 5, and for also suitably offsetting such input voltages to produce the requisite control voltage for such current sources. As will also be appreciated, the current sources 10 and 12 in FIGS. 1 (and corresponding sources 10' and 12' of FIG. 3) will provide the same magnitude of output current. The current source 66 in FIG. 1 (and current sources 66' in FIG. 3) will have a resistor 126 which has one-half the value of the resistor 126 of the current sources 10 and 12 or 10' and 12', for providing an exactly double current magnitude. The circuits will then accurately track for achieving frequency variation, while at the same time providing for accurate termination of integration at a selected waveform point between extremes thereof.

While the circuitry herein illustrated has been described in connection with interrupting a waveform at a selectable point along the negative-going portion thereof with subsequent restarting of waveform generation at the same point, it is understood inverting means may be employed for reversing the polarity of the output signal such that interruption and resumption of the waveform may be accomplished with respect to a positive-going portion thereof. Alternatively, polarity connections may be reversed within the circuit to bring about such a result. For instance, the polarity of connection of diodes 58, 60, and 68 may be reversed in FIG. 1 whereby their cathodes would then be interconnected, with current source 66 supplying a -2I instead +2I. In such instance, the normal

position for switch 70, that is, the position allowing a continuous triangular wave output, would be the position for making a normal positive connection instead of a normal negative connection. In such case, the capacitor 20 would cease charging when the voltage reached V_s at the time of generation of a positive ramp of waveform 40.

A similar change can be made with respect to the circuit of FIG. 3. In the latter instance, the polarity of connection of diodes 90, 92, and 68' would be reversed, while current source 66' would provide a current of +2I instead of -2I. Also, switch 70' would normally reside in its lower or negative position until interruption of the generated waveform was desired.

While I have shown and described several embodiments of my invention, it will be apparent to those skilled in the art that many changes and modifications may be made without departing from my invention in its broader aspects. I therefore intend the appended claims to cover all such changes and modifications as fall within the true spirit and scope of my invention.

I claim:

1. A controllable waveform generator comprising:
 - an input current source which is adjustable to provide a predetermined input current,
 - an integrator circuit including an input current switching means for receiving said input current and producing a ramp waveform in response thereto,
 - gating means coupled to said integrator circuit for bringing the integration in said integrator circuit to a predetermined intermediate level of integration on said ramp waveform and for diverting said input current from said integrator circuit to prevent further integration when the waveform reaches such level, further including a second current source which is adjustable to provide a redetermined current for coupling to said gating means to provide a return for said diverted input current,
 - means for selectively operating said gating means for interrupting said ramp waveform at said intermediate level, and for selectively restoring said waveform starting at said level,
 - and means for concurrently adjusting said current sources for proportionately changing the currents produced thereby for changing the waveform slope.
2. The generator according to claim 1 wherein said integrator circuit includes a capacitor charged by said input current.
3. The generator according to claim 1 wherein said second current source provides a current equaling twice said input current.
4. A controllable waveform generator comprising:
 - an input current source which is adjustable to provide a predetermined input current,
 - an integrator circuit for receiving said input current and producing a ramp waveform in response thereto,
 - gating means coupled to said integrator circuit for bringing the integration in said integrator circuit to a predetermined intermediate level of integration on said ramp waveform and for diverting said input current from said integrator circuit to prevent further integration when the waveform reaches such level, said gating means comprising a pair of balanced, reverse-poled diodes disposed in series between said integrator circuit and a selectable voltage, means for selectively biasing said diodes for conduction and nonconduction, and a second current source providing a current equaling twice said input current for producing an equal flow of current through each of said diodes and establishing equal voltage drop thereacross whereby the voltage at the diode terminal coupled to said integrator circuit equals said selectable voltage, said second current source providing a return for said diverted input current,
 - and means for concurrently adjusting said current sources for proportionately changing the currents produced thereby.

5. The generator according to claim 4 wherein said means for selectively biasing said diodes comprises an additional diode having an electrode thereof coupled to the interconnection between said pair of diodes, said electrode corresponding to the electrodes of said pair of diodes to which it is connected, and switching means for selectively connecting the remaining electrode of said additional diode to a voltage level which selectively reverse biases and forward biases the said pair of diodes.

6. A controllable waveform generator comprising:

an input current source which is adjustable to provide a predetermined input current,

an integrator circuit for receiving said input current and producing a ramp waveform in response thereto, said integrator circuit comprising a Miller integrator including an amplifier and a feedback capacitor,

gating means coupled to said integrator circuit for bringing the integration in said integrator circuit to a predetermined intermediate level of integration on said ramp waveform and for diverting said input current from said integrator circuit to prevent further integration when the waveform reaches such level, said gating means comprising a pair of substantially similarly poled diodes disposed between input and output terminals of said Miller integrator circuit and a common point, a second current source coupled to said common point to provide a return for said diverted input current, said second current source supplying a current equaling twice said input current, and means for selectively reverse biasing said pair of diodes and rendering the same conductive for discharging said feedback capacitor,

and means for concurrently adjusting said current source for proportionately changing the currents produced thereby.

7. The generator according to claim 6 wherein said means for selectively reverse biasing said diodes comprises an additional diode having an electrode thereof coupled to the interconnection between said pair of diodes, said electrode corresponding to the electrodes of said pair of diodes to which it is connected, and switching means for selectively connecting the remaining electrode of said additional diode to voltage level which selectively reverse biases and forward biases the said pair of diodes.

8. The generator according to claim 6 further including means for determining the output of said integrator circuit relative to a discharge condition of said capacitor, said last mentioned means comprising a voltage dropping means connected to the output of said Miller integrator circuit, including a resistor and means for passing a predetermined current through said resistor.

9. A controllable waveform generator comprising:

an input current source which is adjustable to provide a predetermined input current,

an integrator circuit including an input current switching means for receiving said input current and producing a ramp waveform in response thereto,

gating means coupled to said integrator circuit for bringing the integration in said integrator circuit to a predetermined intermediate level of integration on said ramp waveform and for diverting said input current from said integrator circuit to prevent further integration when the waveform reached such level, further including a second current source which is adjustable to provide a predetermined current for coupling to said gating means to provide a return for said diverted input current,

and means for concurrently adjusting said current sources for proportionately changing the currents produced thereby,

wherein said input current source includes positive and negative current source means for alternatively providing said input current, said second current source providing a current in a direction for providing a return for input current in a given polarity direction.

10. A controllable waveform generator comprising:

an input current source which is adjustable to provide a predetermined input current,

an integrator circuit including an input current switching means for receiving said input current and producing a ramp waveform in response thereto,

gating means coupled to said integrator circuit for bringing the integration in said integrator circuit to a predetermined intermediate level of integration on said ramp waveform and for diverting said input current from said integrator circuit to prevent further integration when the waveform reaches such level, further including a second current source which is adjustable to provide a predetermined current for coupling to said gating means to provide a return for said diverted input current,

and means for concurrently adjusting said current sources for proportionately changing the currents produced thereby,

said generator including a level detector for detecting when the output of the integrator reaches each of a pair of output levels representative of the extremes of said triangular wave, and means responsive to such detection for reversing the polarity of input current flow relative to said integrator circuit whereby said generator produces a substantially triangular wave.

11. A controllable waveform generator comprising:

an integrator circuit responsive to an input current for producing a substantially triangular wave, said circuit including a level detector for detecting when the output of the integrator reaches each of a pair of output levels representative of the extremes of said triangular wave, and means responsive to such detection for reversing the polarity of input current flow relative to said integrator circuit,

gating means controllably responsive to the integration in said integrator circuit reaching at least a predetermined value along said triangular wave for interrupting input current flow relative to said integrator circuit and preventing integration beyond said predetermined value, said gating means being selectively operative for restoring said input current to said integrator circuit in order to reinitiate generation of said triangular wave beginning at a predetermined value,

a current source which is adjustable to provide a second predetermined current for coupling to said gating means to provide a return path for said input current when said gating means operates for interrupting said input current flow to said integrator circuit,

and means for proportionately adjusting the values of input current and current from said current source for varying the frequency of said triangular wave.

12. The generator according to claim 1 wherein said gating means includes a pair of substantially similar diodes for establishing equal voltage drop thereacross for maintaining said intermediate level substantially constant relative to said waveform with changes in currents produced by said current sources.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,676,698 Dated July 11, 1972

Inventor(s) LLOYD WAYNE HUNTER

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 2, line 46, after "input" insert --of--

Col. 3, line 58, "charges" should be --changes--

Col. 6, last line, "reserved" should be --preserved--

Col. 8, line 33 (claim 1, line 13) "redetermined" should be
--predetermined--

Col. 9, line 41 (claim 7, line 7) before "voltage"
insert --a--

Col. 9, line 62 (claim 9, line 12) "reached" should be
--reaches--

Col. 10, line 4 (claim 9, line 19) "nd" should be --and--

Col. 10, line 22 (claim 10, line 14) "mans" should be
--means--

Signed and sealed this 23rd day of January 1973.

(SEAL)
Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents