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(54) WAFER CARRIER HAVING IMPROVED PROCESSING CHARACTERISTICS

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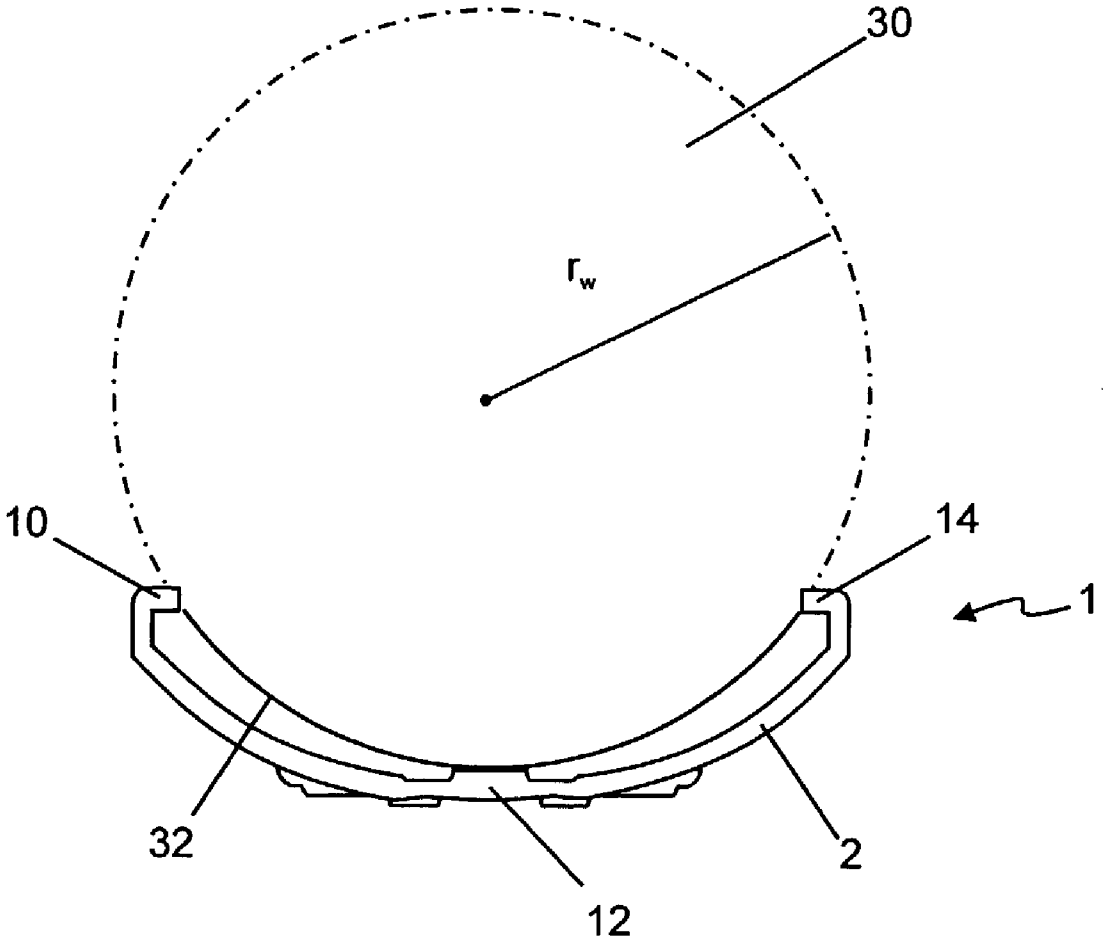
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(57) **ABSTRACT**

A wafer carrier for supporting a plurality of wafers, including a plurality of slots provided in a cradle, the cradle being formed of silicon carbide and having an oxide layer overlying the silicon carbide.



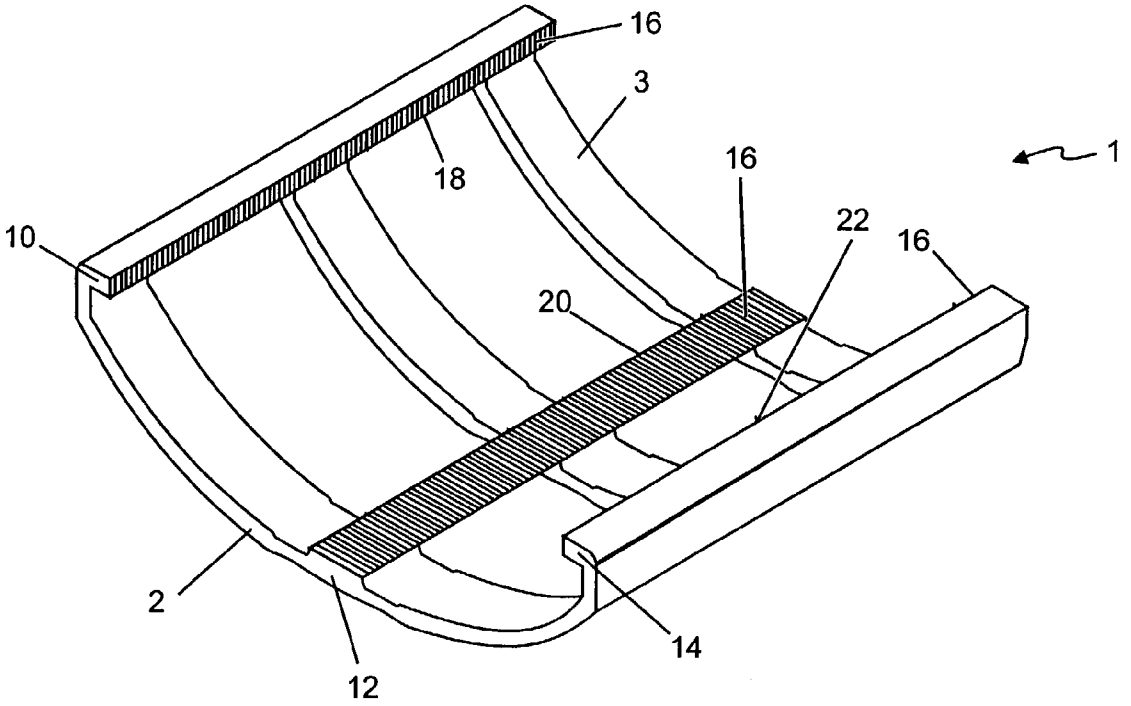


FIGURE 1

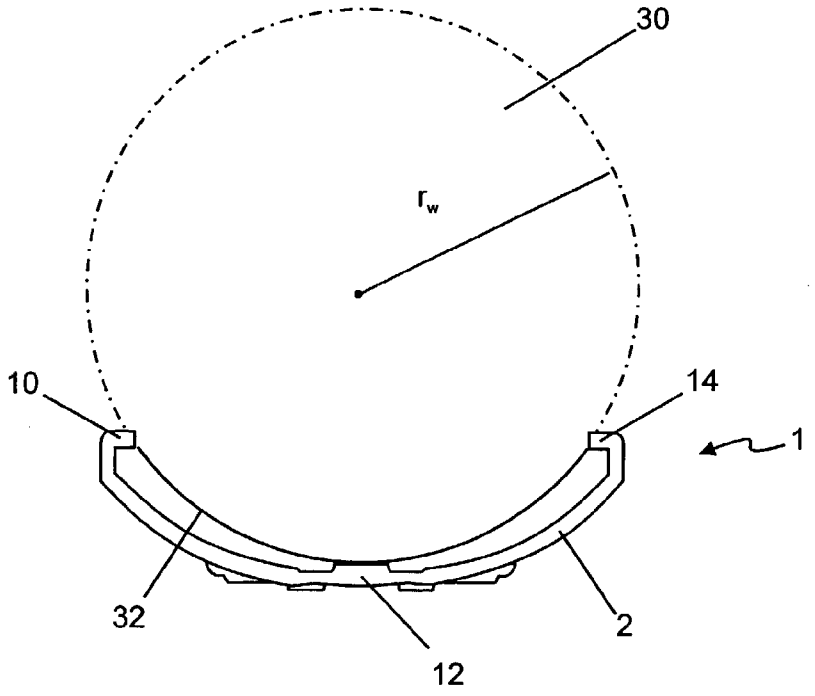


FIGURE 2

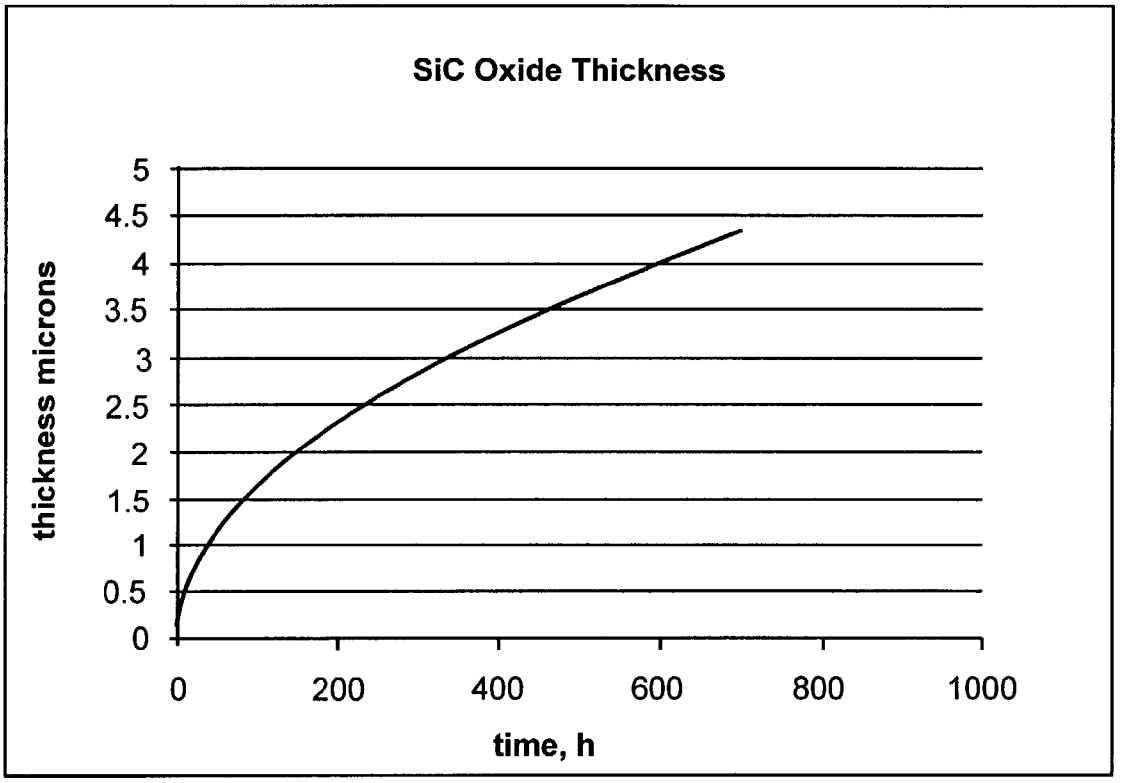

SiC Oxide Thickness
thickness microns
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
0
200
400
600
800
1000
time, h

FIGURE 3

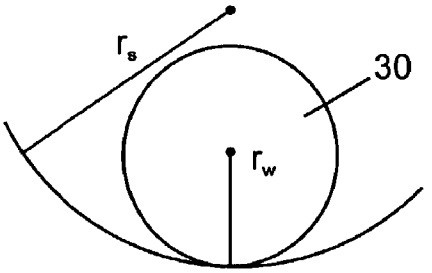


FIGURE 4

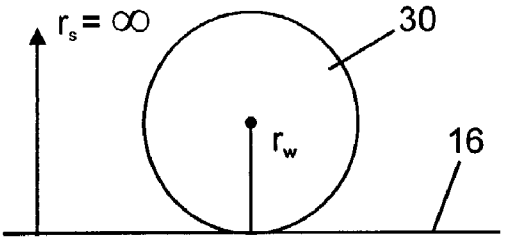


FIGURE 5

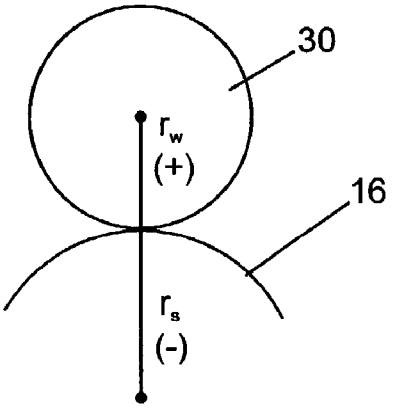


FIGURE 6

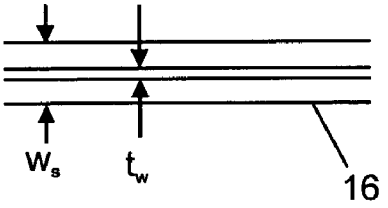


FIGURE 7

WAFER CARRIER HAVING IMPROVED PROCESSING CHARACTERISTICS

BACKGROUND

[0001] 1. Field of the Invention

[0002] The present invention relates generally to kiln furniture, and more specifically, to a wafer carrier for supporting wafers to undergo processing such as exposure to a high temperature processing operation. In addition, the present invention generally relates to processing wafers utilizing such a wafer carrier.

[0003] 2. Description of the Related Art

[0004] As is understood in the art, semiconductor processes typically employ workpieces to support and/or transport semiconductor wafers during various processing steps, including high temperature processes which include annealing, chemical vapor deposition, oxidation, and others. In this regard, horizontal and vertical wafer carriers, also known in the art as wafer boats, are utilized to support a plurality of wafers, typically spaced apart from each other at a constant pitch forming an array of wafers. In this regard, exposure of the wafer to processing operations is generally known as "batch processing," in which a plurality of wafers are processed simultaneously.

[0005] Along with the reduction of transistor critical dimensions, die size, and integrated circuit size, the actual diameter of the wafers being processed continues to increase. For example, the industry has migrated from 4 to 6 inch wafers, and presently 8 inch wafers are commonly used. Further, 12 inch (300 mm) semiconductor fabrication plants (fabs) are coming online. With the introduction of increased wafer size, new engineering problems arise in many phases of the fabrication process.

[0006] Further, semiconductor wafers, principally comprised of silicon, are being used for formation of not only conventional integrated circuit structures including logic and memory devices, but also for opto-electronic devices such as waveguide multiplexers and micro-electro-mechanical systems (MEMS). In this regard, device fabrication sometimes utilizes an extended oxidation step, in which the semiconductor wafers are oxidized, sometimes for extended periods of time beyond what would normally be encountered in conventional semiconductor processing. For example, it is not uncommon to expose a wafer to a processing operation for days at a time, such as on the order of five to ten days. As noted above, oftentimes such a processing operation includes oxidation of the wafers.

[0007] In view of the extended process times, as well as the increased wafer size, technical issues have arisen that impact the robustness and quality of the devices. In this regard, the present inventors have encountered defects in the wafers after being subjected to such processing operations, such as localized or even catastrophic fracture of the wafers. Other defects include deformation and notching of the wafers around the outer periphery, particularly at those points contacting the wafer carrier such as the bottom support portion of the wafer carrier in the case of a horizontal wafer boat.

[0008] Accordingly, a need exists in the art for improved wafer carriers or boats, and in particular horizontal wafer carriers, and for improved processing operations that provide improved device yield and low defectivity.

SUMMARY

[0009] According to one aspect of the invention a wafer carrier is provided for supporting a plurality of wafers, the carrier including a plurality of slots provided in a cradle, the cradle comprising silicon carbide and having an oxide layer overlying the silicon carbide. According to one aspect of the invention a wafer carrier is provided for supporting a plurality of wafers, the carrier including a plurality of slots provided in a cradle, the cradle comprising silicon carbide and having an oxide layer overlying the silicon carbide.

[0010] According to another aspect of the invention, a wafer carrier is provided having a plurality of slots having a particular width. In particular, a portion of each slot has a width (w_s), wherein w, is not less than 1.30 t_w and t_w is a thickness of the wafers.

[0011] According to yet another feature of the present invention, a wafer carrier for supporting a plurality of wafers is provided, the wafers having a radius r_w, and the wafer carrier including a plurality of slots for supporting the wafers, wherein at least a portion of each slot has a radius of curvature r_s, which is not less than about 1.15 r_w. According a variant of this aspect of the present invention, r, may have a negative value while r_w has a positive value.

[0012] According to another aspect of the present invention, methods are provided for processing a plurality of wafers, in which a plurality of wafers are loaded onto a wafer carrier having any one of or all the features described above, and subjecting the wafers to a processing operation as-loaded on the wafer carrier. The processing operation may be one in which the wafers are exposed to an oxidizing environment to oxidize the wafers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0014] **FIG. 1** is a perspective view of a horizontal wafer carrier according to an embodiment of the present invention.

[0015] **FIG. 2** is a sectional view of a horizontal wafer carrier according to an embodiment of the present invention, loaded with a silicon wafer.

[0016] **FIG. 3** is a graph illustrating the growth curve of oxide on a silicon carbide wafer carrier.

[0017] **FIG. 4** represents the radius of curvature of a slot loaded with a semiconductor wafer according to an embodiment of the present invention.

[0018] **FIG. 5** represents the radius of curvature of a slot loaded with a semiconductor wafer according to another embodiment of the present invention.

[0019] **FIG. 6** represents the radius of curvature of a slot loaded with a semiconductor wafer according to yet another embodiment of the present invention.

[0020] **FIG. 7** represents thickness of the wafer in cross-section as loaded in a slot, relative to width of slot, according to an embodiment of the present invention.

[0021] The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[0022] According to an embodiment of the present invention, a particular wafer carrier is provided for supporting a plurality of wafers. In this regard, attention is drawn to **FIG. 1**, illustrating a perspective view of a wafer carrier according to an embodiment of the present invention. As shown, wafer carrier **1** includes a cradle **2** having a generally open structure and including a plurality of cradle arms **3** which take on a generally arcuate shape, and which are integrated with a plurality of support members for supporting the wafers. Particularly, first, second, and third support members, **10**, **12** and **14** are provided, each of which protrudes radially inward, and along which a plurality of slots **16** are provided. Each slot **16** is disposed and oriented so as to be positioned along the same arc of fixed radius, to support a single respective wafer. Each slot is made up of first, second and third slot segments **18**, **20** and **22**, respectively, each of which respectively being positioned along first, second and third support members **10**, **12**, and **14**.

[0023] As shown in **FIG. 2, a** cross-sectional view is provided illustrating the orientation of wafer **30** as engaged and loaded onto the wafer carrier **1**. The general orientation of the wafer carrier illustrated in **FIGS. 1 and 2** is horizontal, and is the orientation of the wafer carrier in use, particularly, in a semiconductor fab environment. As illustrated, the carrier supports the wafers in a generally upright, vertical position.

[0024] As most clearly shown in **FIG. 1**, the slots **16** are arranged in a linear array and spaced apart from each other at a constant pitch. For example, second slot segments **20** are shown to be spaced apart from each other at a constant pitch, and in an array format. As such, the wafers are held by the carrier linearly, forming a horizontal stack of wafers. The pitch of the grooves, and accordingly, the pitch of the wafers may vary depending on the particular application, but generally lies within a range of about 2 to about 4 mm, nominally about 2.38 mm.

[0025] As shown in **FIG. 2**, the first, second and third support members **10**, **12** and **14** are positioned along an arc **32** which has a radius equal to a radius of the wafer r_w, such that the first, second and third support members are positioned sequentially along the arc **32** and the second support member is positioned circumferentially between the first and third support members **10**, **14**. In this regard, the second support member generally supports a larger portion of the weight of the wafer, since it is disposed at a bottom-most position, i.e., at the six o'clock position. The arc **32** sweeps an angle which is not greater than 180 degrees, so as to facilitate loading of the wafers. Typically, the support portions are positioned to define an arc **32** which is not greater than about 150 degrees, or typically not greater than about 130 degrees.

[0026] While three support members are shown in **FIGS. 1 and 2**, the wafer carrier may have a different number of support members. For example, the second support member may be bifurcated so as to form two distinct support members which have distinct slot segments. In such a case, the support members may be equally spaced apart from the bottom-most six o'clock position.

[0027] As noted above, the wafer carrier has a generally open design, which provides several advantages as described in more detail below. Typically, the windows defined between the cradle arms **3** and the support members provide at least 40% open area along an outer partial-cylindrical surface of the cradle. Typically, the open area is not less than about 50%. This open design of the wafer carrier advantageously improves gas flow around the wafer carrier during the pre-oxidation step, to form a conformal, relatively uniform oxide layer.

[0028] Turning to the materials of the wafer carrier, as noted above, the cradle is comprised of silicon carbide. According to one embodiment, the silicon carbide comprises recrystallized silicon carbide, which is a material understood in the art. Typically, a green body containing semiconductor-grade silicon carbide powder is mixed with sintering aids and binders, molded into a desired shaped, dried, heated to burn-out organic binders, and heat treated to densify and recrystallize the body. Following densification, machining steps may be used to arrive at the final dimensions of the wafer carrier.

[0029] Other forms of silicon carbide may be utilized in place of or in combination with recrystallized silicon carbide. For example, the silicon carbide substrate may be formed by a conversion process, in which a carbon preform is converted by gas phase or liquid-phase techniques into silicon carbide. Typically, in this case, the preform is formed of a carbonaceous material, such as semiconductor-grade graphite. Further, in the case of using a porous silicon carbide for the base material of the wafer carrier, the carrier may be impregnated with silicon. Such a compositional feature is known as Si—SiC or siliconized silicon carbide. In this regard, following formation of a relatively porous silicon carbide substrate, the substrate is impregnated with molten silicon, to densify the structure to an extent suitable for use in refractory applications such as in the semiconductor processing environment. The siliconized silicon carbide may be coated with a further layer of silicon carbide, such as chemical vapor deposited (CVD) silicon carbide.

[0030] Still further, the wafer carrier may be formed of free-standing SiC formed by CVD. In this case, an extended CVD process is carried out to form the wafer carrier itself.

[0031] An oxide layer is provided so as to overlie the silicon carbide of the wafer carrier. The oxide layer may be formed by oxidation of the carrier in an oxidizing environment, such as by oxidizing the carrier in an oxygen containing environment at an elevated temperature, such as within a range of 950 to about 1300 degrees C., and more generally in a range of about 1000 to about 1250 degrees C. Oxidation may be carried out in a dry or wet atmosphere, and is typically carried out at atmospheric pressure. A wet ambient can be generated by introducing steam, and functions to increase the rate of oxidation and improve density of the oxide layer. In this regard, wet oxidation at 1150° C. may form a robust, thick (such as about 2-3 microns) oxide layer on the of about 12-48 hours. On the other hand, such a layer may take on the order of 5 days, such as 10-20 days for form according to a dry oxidation treatment. While typically the oxide layer is formed by oxidation, it may also be deposited,

such as by reacting TEOS source gas. However, for durability and robustness, thermally grown layers may be preferred.

[0032] Generally the oxide layer is silicon oxide, generally SiO_2. The silicon oxide layer may be in direct contact with the silicon carbide of the wafer carrier. Alternatively, an intermediate layer, such as silicon may be present between the silicon carbide and the overlying oxide layer, as in the case of silicon-impregnated silicon carbide.

[0033] **FIG. 3** illustrates the growth curve of an oxide layer as a function of time on the silicon carbide wafer carrier. As illustrated, the oxide layer follows a generally parabolic growth curve. For reasons discussed below, according to one embodiment of the invention, the oxide layer has a thickness which is above the relatively rapid growth portion of the curve. For example, the oxide layer may have a thickness greater than about 0.5 microns, or particularly greater than about 0.75 microns, such as greater than about 1.0 microns, and even 1.5 microns. According to particular embodiments of the invention, the oxide has a thickness or at least 2 microns, such as on the order of about 2 to about 3 microns. It is noted that the oxide layer according embodiments of the present invention is a layer which is provided on the wafer carrier, as opposed to any native oxide which may be present on the wafer carrier, but in relatively low thicknesses. Further, while the oxide layer described above is generally formed by thermal oxidation techniques, other techniques may also be utilized, such as direct deposition of an oxide layer.

[0034] The formation of an oxide layer such as by a thermal pre-oxidation step, has been found to improve process control in a semiconductor fab environment. In particular, the present inventors have recognized that during conventional oxidation treatment to form a relatively thick oxide layer on the wafers, the wafers tend to bond with the wafer carrier through the growth of the oxide layer on the wafers and/or an oxide layer which forms on the wafer carrier. It is believed that during subsequent cooling of the wafer/wafer carrier assembly, differences in contraction via differences in thermal expansion coefficients of the wafer and the carrier cause thermally induced stresses in the wafers. Such differences in thermal expansion/contraction properties may be due to compositional and structural differences, and ultimately can cause damage to the wafers. In extreme cases, the wafers may catastrophically fail by a cracking mechanism. By incorporation of a pre-oxidation step to form an oxide layer on the carrier, growth of an oxide layer on the carrier during thermal processing of the wafers is attenuated, and the propensity of bonding between the wafers and the carrier is reduced, thereby enhancing process control and wafer yield.

[0035] According to another feature of the invention, the slots in the wafer carrier have a particular radius of curvature r_s that further enhances process control and wafer yield, particularly during high temperature processing as described above.

[0036] As shown in connection with **FIG. 2**, the wafer has a nominal radius r_w. Current state of the art wafer fabs utilize 8 inch, and increasingly 12 inch (300 mm diameter) wafers. Accordingly, newer fabs may employ wafers having a radius r_w which is on the order of about 150 mm, although older fabs may utilize smaller wafers and newer generation fabs larger. According to a particular feature of one embodiment, the radius of curvature r_s of the slot is not less then about 1.15 r_w. Alternatively stated, the radius curvature of the slot for supporting the wafer is larger than the radius of the wafers by at least 15%. Typically, r_s is not less than about 1.25 r_w, such as 1.35 r_w, and 1.50 r_w. Turning to **FIG. 4, r**$_s$ is shown to be approximately twice that of r_w. Even further, the radius of curvature of the slot may approach a straight line (r_s=infinity). This particular embodiment is illustrated in **FIG. 5**. In this case, a portion of the slot which contacts the wafer extends along a straight line.

[0037] Still further, the radius of curvature of the slot may have the opposite orientation, that is, have a negative radius of curvature as compared with the radius r_w of the wafer. This is shown in **FIG. 6**, in which the slot has a generally convex shape and has a radius which extends in a direction opposite of the radius of the wafer, from the point of contact between the wafer and the slot.

[0038] In the foregoing embodiments, it is not required that each slot segment have the same radius of curvature. However, typically at least a portion of the second slot segment along the second support member has a radius characteristic as described above.

[0039] By providing a slot portion having a radius of curvature r_s as described above, the potential oxidation bond area between the wafer and the carrier is minimized. As such, to the extent that an oxide bond is formed between the wafer and the carrier, the minimized bonding interface is weaker and more likely to break during processing (e.g., during cooling) thereby attenuating thermal stresses in the wafer which can cause fracture as described above.

[0040] According to another embodiment of the present invention, at least a portion of the slots of the wafer carrier has a width w_s which is greater than a thickness t_w of the wafers. Particularly, the width w_s is generally not less than about 1.30 t_w. According to another embodiment, w_s is not less than about 1.35 t_w, and may be within a range of about 1.35 t_w to about 1.50 t_w. In this regard, **FIG. 7** illustrates the width of the slot w_s, with respect to the thickness of the wafer t_w (not shown to scale). It is noted that the actual thickness t_w of the wafers may vary based upon wafer brand, intended use, wafer diameter, composition (e.g., silicon on insulator (SOI)), etc. However, typically, wafers generally have a thickness within a range of about 0.45 mm to about 0.80 mm, more typically between about 0.50 to about 0.765 mm. By providing the slots with the above relative width, as opposed to narrower widths such as on the order of 1.10 t_w to 1.25 t_w, the formation of relatively thick oxide layers is facilitated by the extra room in the slots. In addition, by attenuating the degree to which the wafers are constrained in the slots during oxide growth, wafer creep becomes less problematic. In this regard, utilizing conventional techniques, constraint of the wafer within the slot tends to cause the wafer to creep at high temperatures, causing notching. The formation of notches in the wafer around the outer periphery tends to form a mechanical interlocking structure, which is disadvantageous. In particular, upon cooling, the notch tends to engage the slot and is responsible for placing mechanical stresses in the wafer upon cooling due to differential thermal contraction characteristics of the wafer and the wafer carrier.

[0041] In addition to the particular features of embodiments of the wafer carrier as described above, the present

invention also provides for processing for a plurality of wafers, known as batch processing. In this regard, a wafer carrier is loaded with a plurality of wafers, generally arranged in a linear array at a constant pitch. Thereafter, the wafer/wafer carrier assembly is placed in a furnace, such as a process tube, for high temperature processing. As described above, one desirable processing operation is the formation of a relatively thick oxide layer on the wafers, particularly suitable for MEMS and opto-electronic applications.

[0042] While embodiments of the present invention have been described above with particularity, it is understood that various modifications may be made without departing from the scope of the present claims.

What is claimed is:

1. A wafer carrier for supporting a plurality of wafers, comprising:

a plurality of slots provided in a cradle, the cradle comprising silicon carbide and having an oxide layer overlying the silicon carbide.

2. The wafer carrier of claim 1, wherein the cradle comprises recrystallized silicon carbide.

3. The wafer carrier of claim 1, wherein the cradle comprises silicon impregnated silicon carbide.

4. The wafer carrier of claim 1, wherein the cradle comprises converted silicon carbide.

5. The wafer carrier of claim 1, wherein the cradle comprises free-standing CVD SiC.

6. The wafer carrier of claim 1, wherein the oxide layer comprises silicon oxide.

7. The wafer carrier of claim 6, wherein the silicon oxide has a thickness greater than about 0.5 microns.

8. The wafer carrier of claim 6, wherein the silicon oxide has a thickness greater than about 0.75 microns.

9. The wafer carrier of claim 6, wherein the silicon oxide has a thickness greater than about 1.0 microns.

10. The wafer carrier of claim 6, wherein the silicon oxide has a thickness greater than about 1.5 microns.

11. The wafer carrier of claim 1, wherein the oxide layer is thermally grown.

12. The wafer carrier of claim 1, wherein the oxide layer is deposited.

13. The wafer carrier of claim 1, wherein the wafer carrier is a horizontal wafer carrier, for supporting wafers oriented in a generally upright, vertical position.

14. The wafer carrier of claim 1, wherein slots are arranged in a linear array, and spaced apart from each other at a constant pitch.

15. A wafer carrier for supporting a plurality of wafers, the wafers having a thickness t_w, the wafer carrier comprising a plurality of slots for supporting the array of wafers, at least a portion of each slot having a slot width w_s, wherein w_s is not less than about 1.30 t_w.

16. The wafer carrier of claim 15, wherein wherein w_s is not less than about 1.35 t_w.

17. The wafer carrier of claim 15, wherein w_s is within a range of about 1.35 t_w to about 1.50 t_w.

18. The wafer carrier of claim 1, wherein the cradle includes at least first, second and third support members, each of which is provided to support and contact the wafers, each slot having first, second and third slot segments extending respectively along the first, second and third support members.

19. The wafer carrier of claim 18, wherein the first, second and third slot segments are positioned along an arc having a radius equal to a radius of the wafers, and the first, second, and third support members are positioned sequentially along the arc such that the second support member is positioned circumferentially between the first and third support members.

20. The wafer carrier of claim 19, wherein said portion of each slot having a slot width w_s includes at least a portion of the second slot segment.

21. The wafer carrier of claim 19, wherein the first, second and third slot segments are spaced along said arc which is not greater than 180 degrees.

22. The wafer carrier of claim 19, wherein the first, second and third slot segments are spaced along said arc which is not greater than 150 degrees.

23. A wafer carrier for supporting a plurality of wafers, the wafers having a radius r_w, the wafer carrier comprising a plurality of slots for supporting the plurality of wafers, at least a portion of each slot having a radius of curvature r_s, wherein r_s is not less than about 1.15 r_w.

24. The wafer carrier of claim 23, wherein r_s is not less than about 1.25 r_w.

25. The wafer carrier of claim 23, wherein r_s is not less than about 1.35 r_w.

26. The wafer carrier of claim 23, wherein r_s is not less than about 1.50 r_w.

27. The wafer carrier of claim 23, wherein r_s is infinity, said at least a portion of each slot extending along a straight line.

28. A wafer carrier for supporting a plurality of wafers, the wafers having a radius r_w, the wafer carrier comprising a plurality of slots for supporting the array of wafers, at least a portion of each slot having a radius of curvature r_s, wherein r_s has a negative value and r_w has a positive value.

29. A method for processing a plurality of wafers, comprising:

loading a plurality of wafers in a wafer carrier, the wafer carrier including a plurality of slots provided in a cradle, the cradle comprising silicon carbide and having an oxide layer overlying the silicon carbide; and

subjecting the wafers to a processing operation.

30. The method of claim 29, wherein the processing operation comprises exposing the wafers to an oxidizing environment to oxidize the wafers.

31. The method of claim 29, wherein the oxide layer is formed by oxidation at a temperature higher than a temperature of the processing operation.

32. A method for processing a plurality of wafers, comprising:

loading a plurality of wafers in a wafer carrier, the wafers having a radius r_w, the wafer carrier comprising a plurality of slots for supporting the plurality of wafers, at least a portion of each slot having a radius of curvature r_s, wherein r, is not less than about 1.15 r_w; and

subjecting the wafers to a processing operation.

33. A method for processing a plurality of wafers, comprising:

loading a plurality of wafers in a wafer carrier, the wafers having a thickness t_w, the wafer carrier comprising a plurality of slots for supporting the array of wafers, at

least a portion of each slot having a slot width w_s, wherein w_s is not less than about 1.30 t_w; and

subjecting the wafers to a processing operation.

34. A wafer carrier for supporting a plurality of wafers, the wafers having a thickness t_w and a radius r_w, the wafer carrier comprising a plurality of slots for supporting the plurality of wafers, at least a portion of each slot having a slot width w_s and a radius of curvature r_s, wherein w_s is not less than about 1.30 t_w and r_s is not less than 1.15 r_w, the wafer carrier further comprising silicon carbide and an oxide layer overlying the silicon carbide.

* * * * *