July 21, 1959 F. C. WILLIAMS 2,895,673

TRANSISTOR BINARY ADDER

Filed July 24, 1953 2 Sheets-Sheet 1

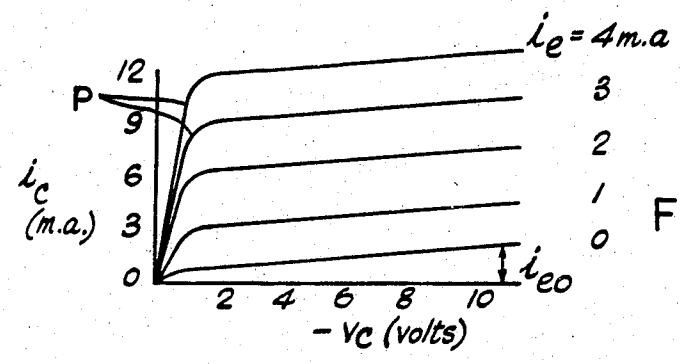


FIG. 1.

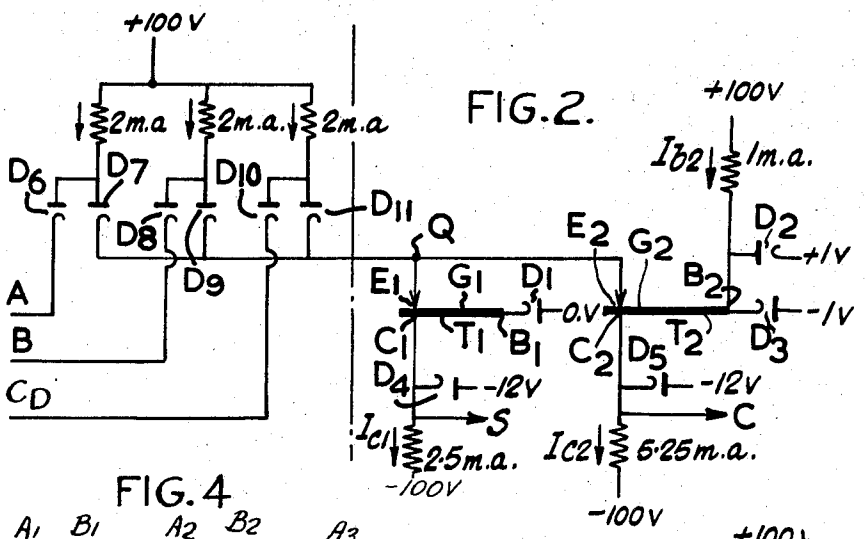
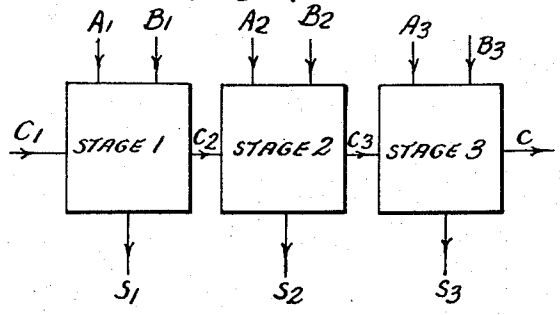


FIG. 4



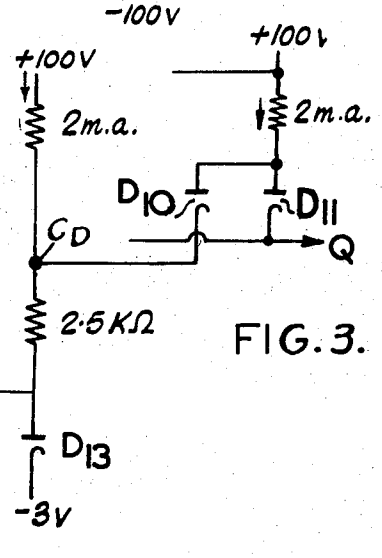
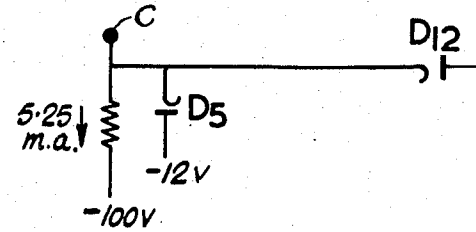


FIG. 3.



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TRANSISTOR BINARY ADDER

Filed July 24, 1953 2 Sheets-Sheet 2

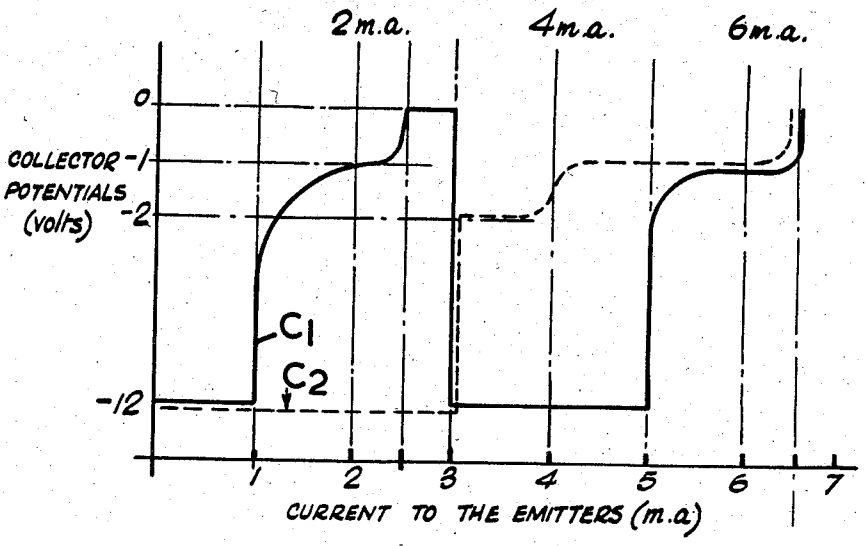

FIG. 2A.

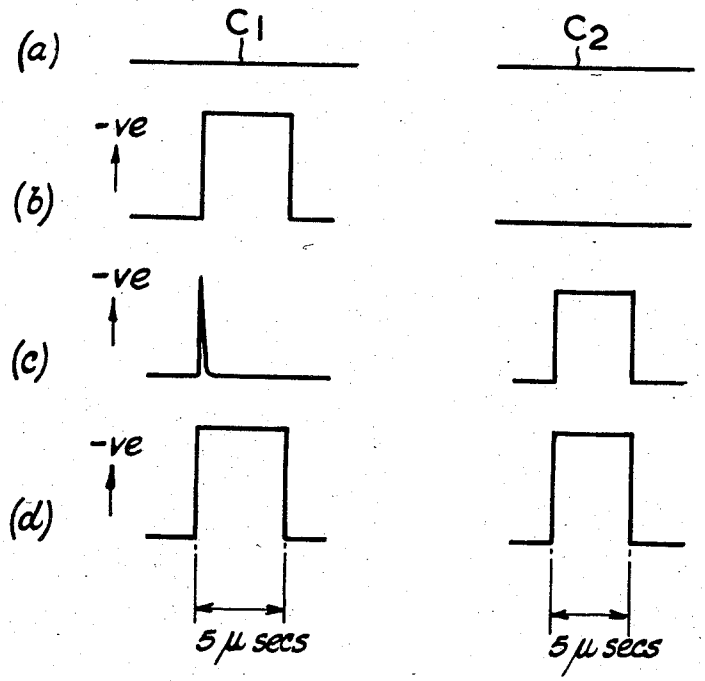

FIG. 2B.

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TRANSISTOR BINARY ADDER

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Claims priority, application Great Britain July 28, 1952

4 Claims. (Cl. 235—164)

This invention relates to electrical circuits employing transistors. When two conductors are contacted at closely adjacent points to the surface of certain semi-conducting materials such as, for example, germanium, which have the property that when suitably contacted a current flows across the contact more readily in one direction than the other, and a back voltage (i.e. a voltage with respect to the material in the sense corresponding with its higher resistance to current flow) is applied to one of these conductors, known as the collector, the amount of current which flows therein increases with increases of the current flowing in the opposite direction relative to the said material in the other conductor, known as the emitter. The combination of semi-conducting material, collector electrode and emitter electrode, together with a base electrode through which a potential can be applied and current supplied to the semiconducting material, is known as a transistor. Where the material is of the type known as n-type, the back voltage is in the sense that the collector is negative with respect to the base, with the result that in order that the collector current may be increased from its back or cut-off value, the emitter must be at a positive potential with respect to the base, so that current can flow from the emitter to the base, giving rise to an increased current from the base to the collector. It will be assumed for the sake of simplicity that all the transistors hereinafter referred to are made of n-type material; any modification of the description necessary to make it applicable to so-called p-type transistors, in which the back voltage is in the opposite sense, will be apparent.

The transistor can be made to function in a manner resembling a thermionic valve, the base of the transistor being analogous to the cathode, the collector to the anode, and the emitter to the control grid. An important difference lies in the fact that it is the emitter current rather than the emitter potential which must be regarded as analogous to the grid voltage of the valve. Figure 1 of the accompanying drawings shows a family of representative characteristic curves of a transistor in which the collector current i_c is plotted against the collector potential v_c relative to the base at different values of the emitter current i_e. Each curve has a steeply sloping portion P and a relatively flat portion Q joined by a "knee." The analogy with the anode current/anode potential characteristics of a pentode valve is apparent, with the difference, however, that the parts P of the transistor curves are separate instead of marging into a single curve as in the case of the valve. This part of the valve characteristics is that in which the type of operation known as "bottoming" occurs, and the corresponding parts P of the transistor curves will, by analogy, be called herein the bottomed region. It will be noted that, as in the valve, the internal resistance of the transistor when bottomed is low. It will further be seen that the curves in Figure 1 exhibit the phenomenon of a current gain of i_c with respect of i_e greater than unity, and it is to be understood that the term "transistor" is used herein is

limited to those transistors which exhibit such a gain of collector current with respect to emitter current. The excess of collector current over emitter current is derived from the current flowing the base electrode i_b and, in general,

$$i_c = i_e + i_b$$

The specification of copending patent application No. 367,482, filed July 14, 1953 by Frederic C. Williams et al., describes a mode of employing transistors in electrical circuits in which the transistor can be triggered from its non-conducting or "off" position to a stable conducting or "on" condition such that the transistor bottoms. The present invention is based on the observation that two transistors can be connected so that each operates in this manner and in combination they perform the functions of a binary adder.

When it is desired in a digital computing machine to add two numbers at least one adder must be provided which is capable of adding two digits (A and B) together with any carry digit (C_D) resulting from the addition of the next less significant pair of digits. The adder must have two outputs, one signifying the sum (S) in the digital place in question and the other the carry digit (C) to be carried to the next more significant place. In the case of a binary adder, there are eight possible combinations of values of A, B and C_D which may be grouped into four categories giving rise respectively to the following values of S and C.

Combinations of A, B and C_D	S	C
0+0+0	0	0
1+0+0 ($\equiv$0+1+0$\equiv$0+0+1)	1	0
1+1+0 ($\equiv$0+1+1$\equiv$1+0+1)	0	1
1+1+1	1	1

Binary adding circuits are known in which separate signals representing A, B and C_D are fed to three separate input terminals and logical operations are performed on them to secure the appropriate values of S and C. Other binary adding circuits are known in which the input signals are first made to produce a single signal having one of four possible magnitudes analogous to the four combinations referred to above. The present invention provides an adder of the latter type, hereinafter called "analogue adders." It will be understood that the input signals in this type of adder are analogous to the digit combinations in the sense that as the sum $A+B+C_D$ increases, the magnitude of the input signal increases.

The circuit according to the invention comprises a first and a second transistor having their emitters connected in parallel to an input terminal, means for feeding to this terminal a current I_0, I_1, I_2 or I_3 in ascending order of magnitude according as $A+B+C_D$ has the value 0, 1, 2 or 3 respectively, means for holding the base of the first transistor at a potential such that this transistor is in the off condition whenever the input current has the value I_0, means for holding the base of the second transistor at a potential below that of the base of the first transistor whenever the input current has the value I_0, and means for extracting substantially constant currents from the collectors of the transistors and for feeding a substantially constant current to the base of the second transistor, the currents being such that the collector current of the first transistor is greater than I_1-I_0, the collector current minus the base current of the second transistor is greater than I_2-I_0, and the sum of the said collector current minus the said base current is greater than I_3-I_0, and that the transistors bottom when in the on condition, whereby when the current fed to the input terminal has the value I_0 both transistors are off,

when it has the value I_1 the first transistor is on and the second off, when it has the value I_2 the first transistor is off and the second on, and when it has the value I_3 both transistors are on. The current I_0 corresponding with zero value of $A+B+C_D$ may conveniently be made zero.

The invention is illustrated by way of example by the accompanying drawings, in which

Figure 1 (already referred to) shows a family of characteristic curves of a transistor,

Figure 2 shows a binary adding circuit according to the invention,

Figures 2A and 2B are diagrams illustrating the action of the circuit of Figure 2, and

Figure 3 shows a circuit whereby the carry digit generated in the circuit of Figure 2 may be fed to the adding circuit associated with the next more significant digit place.

Figure 4 shows a binary adding circuit comprising a plurality of circuits according to the invention.

The convention used to denote the transistors in these drawings is the same as that explained in application No. 367,842, filed July 14, 1953 by Frederic C. Williams et al. The direction of current flow is regarded as conventional throughout. The circuit of Figure 2 comprises two transistors T1 and T2 each consisting of a layer G1 or G2 of semi-conducting material, for example germanium, an emitter electrode E1 or E2, a collector electrode C1 or C2 and a base electrode B1 or B2.

The various electrodes are connected with diodes as shown. These diodes, here and throughout the drawings, are shown as thermionic diodes for convenience, although they may in fact be crystal diodes. Their function is to limit the potentials on the electrodes with which they are connected. The voltage sources are indicated by voltage values such as 100 v., and are of substantially constant potential.

The emitters of the two transistors are connected in parallel to an input terminal Q, which is itself connected in parallel to the cathodes of the right-hand diodes D7, D9 and D11 of three double diode gates. The cathodes of the left-hand diodes D6, D8 and D10 of these diode pairs are connected to input leads to which are applied potentials significant of the digits A, B and C_D respectively, in the sense that a potential of −2 volts or less is significant of the digit value 0 while a potential of +2 volts or more is significant of the digit value 1. The anodes of all the diodes D6–D11 are connected to a potential source of +100 volts through resistors such that a current of 2 ma. flows to any lead or leads to which the potential corresponding with a digit value 0 is applied. If, on the other hand, a potential corresponding with a digit value 1 is applied to any one of the leads, the diode in the corresponding lead is cut off and a current of 2 ma. (I_1) is fed to the input terminal Q; likewise if such a potential is applied to any two or to all three of the leads, a current of 4 ma. (I_2) or 6 ma. (I_3) is fed to terminal Q, while if a potential corresponding with a digit value 0 is applied to all three leads, zero current (I_0) is fed to terminal Q.

As long as zero current is supplied to the emitters of transistors T1 and T2 via terminal Q, both transistors remain in the off condition, with only the small back or cut-off current flowing from the base to the collector. In the case of transistor T1 this current is supplied through diode D1 and holds the base at earth potential. In the case of T2, the cut off current is supplied from I_{b2} (which it will be understood is substantially greater than the cut-off current), the remainder of I_{b2} flowing through D2 and thus holding the base at a potential of +1 volt. The collector potentials are both held at −12 volts by diodes D4 and D5 respectively.

If now a potential corresponding to digit value 1 is applied to one of the input leads, say A, the anode potential of the diode D6 in that lead will tend to rise taking with it the anode of the companion diode D7 connected to point Q so that the emitter E1 will be taken to a potential above the base B1, emitter current will flow and the diode D7 will conduct, the anode voltage of D7 being held down by the voltage drop in its supply lead so that D6 will be cut off and a current of 2 ma. will flow to E1 via point Q. Transistor T1 will thus trigger on in the manner described in copending United States patent application Serial No. 367,842, filed July 14, 1953 by Frederic C. Williams et al. provided the current gain at the knee of the appropriate i_c/v_c curve is greater than 1.25. The potential of C1 will therefore rise from −12 volts to the base potential. This is held at zero by the current flowing in D1, which has the value $I_{c1}-I_1=0.5$ ma. Likewise the potential of E1 and hence of E2 is also held at zero, so that T2 remains off.

If, instead, a potential corresponding to digit value 1 be applied to two leads, say A and B, simultaneously, the same sequence of operations would apply except that both diodes D7 and D9 will conduct so that an increased current will be available through terminal Q. This has the effect that transistor T1, when it switches on, will be unable to absorb this increased current, its emitter will rise to a higher voltage, taking with it the emitter of T2 until such a voltage is reached that E2 is positive with respect to B2 so that transistor T2 switches on. Now when T2 switches on the potential of B2 drops until it is held at −1 volt by D3. Since, in the on condition, the electrodes of the transistor are virtually clamped together, the potential of E2 and hence of E1 also drops to −1 volt, so that T1 is cut off. This occurs in a very short space of time after commencement of the 4 ma. feed to terminal Q. The whole of this current now flows to E2 causing T2 to bottom, the condition being held stable by the current flowing in D3, which will have the value $(I_{c2}-I_{b2})-I_2=0.25$ ma. The potential of C2 has risen from −12 volts to −1 volt, while that of C1 has fallen from +1 volt to −12 volts.

If the current available at terminal Q is made 6 ma. by a 1 digit potential on all three leads the operation is again the same except that there is now an excess of current over $(I_{c2}-I_{b2})$ which causes the potential of transistor T2 to rise, so that D3 cuts off. When the potential of E2 and hence of E1 exceeds zero, transistor T1 is triggered on, and the current of 1.75 ma. available at the emitter E1 is sufficient to cause bottoming. This condition is held stable by the current in D1, which will have the value $(I_{c1}+I_{c2}-I_{b2})-I_3=0.75$ ma. The potentials of C1 and of C2 have now risen again substantially to zero.

Fig. 2A shows the variation of the potentials of C1 (full lines and C2 (broken lines) as a function of the current fed to the emitters. It will be seen that the changes of state occur midway between the current values corresponding with the four possible inputs. The changes are reversible.

Fig. 2B shows the variations of the collector potentials with time when a 5 microsecond current pulse is applied to terminal Q, the current having the value I_0 at (a), I_1 at (b), I_2 at (c) and I_3 at (d). It will be seen from this diagram that the potentials at the leads marked S and C in Fig. 2 correspond with the correct digit values for S and C given above, provided the pulse of short duration occurring at S when a current I_2 is applied can be ignored, as will usually be the case. This spurious pulse can be eliminated altogether by arranging that the emitter potential shall rise to a value adequate to switch on T2 before the potential of C1 can appreciably follow up the emitter voltage, which latter may take about 0.25 microsecond. Although in this example 5 microsecond pulses were used on the input leads, so that the circuit returns to a resting condition with both transistors off, it is obviously possible to feed prolonged control signals or the input leads so that the circuit may "remember" the condition into which it has been set by one combination of inputs until a new combination of signals is ap-

plied. Changes in the available current at point Q due to changes in the signal combination on the input leads will obviously convert the circuit from one state to any other in accordance with the "sum" and "carry" values appropriate to the new combinations of digit signals appearing on the input leads.

The output at C will normally have to be fed to the input lead C_D of an adding circuit associated with the digit place of next higher significance, or through a delay circuit back to lead C_D of Fig. 2. Means for bringing the output at C to the correct voltage levels for effecting this are shown in Fig. 3. This figure shows the collector C of transistor T2 of one stage coupled to the C_D input of the next stage through a diode D12. The C_D input of the next stage is taken from the junction of two resistors forming a potentiometer chain from the 100 volt positive supply to a bias of −3 volts through a further diode D13. When the transistor T2 of the first stage is off, the collector C is at −12 volts so that D5 and D12 are conducting while D13 is cut off. This produces a negative potential of −2 volts at C_D so that D10 will also conduct. When T2 is on, the collector rises to −1 volt or earth so that D5 and D12 are cut off, D13 will conduct and the potential at C_D will rise to +2 volts. Hence the potential at C_D is suitable as an input at the lead C_D of the next stage.

An adding circuit can thus be provided in which a stage such as that illustrated in Figs. 2 and 3 is allotted to each digit of a multi-digit number, so that signals representing all the digits of two multi-digit numbers to be added may be fed in parallel to the respective stages, the inputs to each stage thus being the corresponding digits of the two numbers and a "carry" input from the previous stage.

It will be understood that the current values shown in the drawings are by way of example. Thus, for instance, a transistor having a relatively high value of cut-off current may require a higher value of I_{b2}, say 2 ma., in which case the other currents are scaled up accordingly. Likewise the high tension sources of potential may have different values, and may in some cases be as low as 50 volts.

I claim:

1. An adding circuit for producing "sum" and "carry" binary digit output signals in response to analogue input signals comprising a first transistor having an emitter, a base and a collector, a diode connecting said base to a fixed potential, a high impedance connecting said collector to a low voltage supply, a diode connecting said collector to a small negative bias voltage, a second transistor having an emitter, a base and a collector, a high impedance connecting the latter base to a high voltage supply, diodes connecting said latter base to small positive and small negative bias voltages to restrict the voltage excursions of said latter base between said bias voltages, said small negative bias being lower than said fixed potential, a high impedance connecting the latter collector to a low voltage supply, the latter higher impedance being of smaller value than the high impedance connected to the first transistor collector whereby said second transistor will carry more current than said first transistor, a "sum" output lead connected directly to the first transistor collector, a "carry" output lead connected directly to the second transistor collector, and an input terminal connected directly to the emitters of both said transistors for the application of input current signals of the analogue type representing the sum of three binary digit signals A, B and C_D.

2. A circuit according to claim 1 comprising three diodes, input leads connected directly to the cathodes of said diodes for the application of the binary digit signals A, B, and C_D to different ones of said diodes, three high impedances connecting the respective anodes of said three diodes to a common high voltage supply, three further diodes having their anodes connected directly to the respective anodes of the first-mentioned three diodes to form three diode pairs and having their cathodes connected directly to said input terminal, the different ones of said first-mentioned three diodes being conductive only in response to the appropriate binary digit signal representing a 1, and the different ones of said further three diodes being conductive only when the associated diode of the appropriate diode pair is non-conductive.

3. A circuit according to claim 2 comprising a first diode having its cathode connected directly to said "carry" output lead, a second diode having its cathode connected to a small negative bias voltage, a potentiometer chain connected directly to the anodes of said first and second diodes at one end and to a high voltage supply at the other end, and a further "carry" output lead connected to an intermediate point on said potentiometer chain, said first diode being non-conductive and said second diode being conductive only when the output from said second transistor collector represents a 1 carry digit.

4. An adding circuit comprising a plurality of circuits as claimed in claim 3 wherein the further "carry" output lead of each circuit is connected to the digit signal C_D input lead of the circuit of next highest significance.

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