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(54) Title: IMAGE SENSOR SYNCHRONIZATION WITHOUT INPUT CLOCK AND DATA TRANSMISSION CLOCK

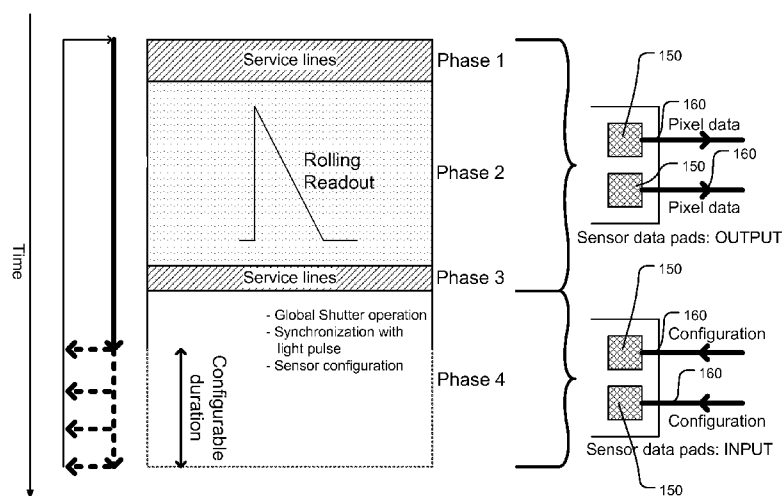


FIG. 1

(57) Abstract: The disclosure extends to systems and methods for reducing the area of an image sensor by reducing the imaging sensor pad count used for data transmission and clock generation.

**IMAGE SENSOR SYNCHRONIZATION WITHOUT INPUT CLOCK
AND DATA TRANSMISSION CLOCK**

BACKGROUND

[0001] Advances in technology have provided improvements in imaging capabilities for medical use. One area that has enjoyed some of the most beneficial advances is that of endoscopic surgical procedures because of the advances in the components that make up an endoscope.

[0002] The disclosure relates generally to electromagnetic sensing and sensors and more particularly related to data transfer. The features and advantages of the disclosure will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by the practice of the disclosure without undue experimentation. The features and advantages of the disclosure may be realized and obtained by means of the instruments and combinations particularly pointed out in the disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Non-limiting and non-exhaustive implementations of the disclosure are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified. Advantages of the disclosure will become better understood with regard to the following description and accompanying drawings where:

[0004] FIG. 1 illustrates a schematic representation of an embodiment of the operation of a pixel array and image sensor in accordance with the principles and teachings of the disclosure;

[0005] FIG. 2 illustrates graphical representation of data transfer with in a sensor service line in accordance with the principles and teachings of the disclosure;

[0006] FIG. 3 illustrates a schematic representation of an embodiment of the operation of a pixel array and image sensor in accordance with the principles and teachings of the disclosure;

[0007] FIG. 4 illustrates graphical representation of a rolling readout output data of a sensor in accordance with the principles and teachings of the disclosure;

[0008] FIG. 5A illustrates a schematic representation of an embodiment of an image sensor having an off-chip oscillator in accordance with the principles and teaching of the disclosure;

[0009] FIG. 5B illustrates a schematic representation of an embodiment of an image sensor having an on-chip oscillator in accordance with the principles and teaching of the disclosure;

[0010] FIG. 6 illustrates a schematic representation of an embodiment of circuitry for clock management and data sequencing in accordance with the principles and teaching of the disclosure;

[0011] FIG. 7 illustrates a schematic representation of an embodiment of circuitry for clock management and data sequencing between a camera unit and a CMOS sensor in accordance with the principles and teaching of the disclosure;

[0012] FIG. 8 illustrates a schematic representation of an embodiment of circuitry for clock management and data sequencing between a camera unit and a CMOS sensor in accordance with the principles and teaching of the disclosure;

[0013] FIG. 9 illustrates a schematic representation of an embodiment of circuitry for clock management and data sequencing between a camera unit and a CMOS sensor in accordance with the principles and teaching of the disclosure;

[0014] FIG. 10 illustrates a schematic representation of an embodiment of circuitry for clock management and data sequencing between a camera unit and a CMOS sensor in accordance with the principles and teachings of the disclosure;

[0015] FIG. 11 illustrates a flow chart of an embodiment of the adjustment of a CMOS sensor operating frequency in accordance with the principles and teachings of the disclosure;

[0016] FIG. 12 illustrates a table of operational parameters in accordance with the principles and teachings of the disclosure;

[0017] FIG. 13 illustrates an embodiment of hardware in accordance with the principles and teachings of the disclosure;

[0018] FIGS. 14A and 14B illustrate an embodiment of a sensor having a plurality of pixel arrays for providing three dimensional functionality in accordance with the principles and teachings of the disclosure;

[0019] FIGS. 15A and 15B illustrate a view of an implementation of an imaging sensor built on a plurality of substrates, wherein a plurality of pixel columns forming the pixel array are located on the first substrate and a plurality of circuit columns may be located on a second substrate and showing an electrical connection and communication between one column of pixels to its associated or corresponding column of circuitry; and

[0020] FIGS. 16A and 16B illustrate a view of an implementation of an imaging sensor having a plurality of pixel arrays for producing a three dimensional image, wherein the plurality of pixel arrays and the image sensor may be built on a plurality of substrates.

DETAILED DESCRIPTION

[0021] The disclosure extends to methods, systems, and computer based products for digital imaging that may be primarily suited to medical applications. In the following description of the disclosure, reference may be made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration specific implementations in which the disclosure may be practiced. It may be understood that other implementations may be utilized and structural changes may be made without departing from the scope of the disclosure.

[0022] The disclosure extends to systems and methods for reducing imaging sensor pad count by negating the need for an output clock (clock-less data transmission) and the need for an input clock. The basic strategy is that the sensor issues a continuous stream of 1s and 0s on its data port(s) upon power-up, in order for the data receiver within the support electronics of the camera to synchronize to it using a CDR (Clock Data Recovery) circuit (clock training). If needed, the continuous stream can be enabled during normal operation by toggling one configuration register bit. Once the receiver has locked onto this training pattern, normal sensor imaging operation may proceed. In order to maintain the lock, long periods without transitions may be avoided by including a single invert bit for the digital value issued for each pixel.

[0023] Traditional rod-lens endoscopes, used for laparoscopy, arthroscopy, urology, gynecology and ENT (ear-nose-throat) procedures are expensive to manufacture owing to their complex optical composition. The incident image information is transported in the optical domain all the way along its length. Typically it is optically coupled to hand-piece unit wherein the image sensing device(s) reside. This type of rigid endoscope is also delicate and prone to damage during handling, use and sterilization. The necessary repair and sterilization processes add further expense to each procedure for which they are utilized.

[0024] Advances in image sensing technology have led to CMOS devices that are cheap to manufacture and are highly customizable. Much of the external circuitry that was necessary to operate CCD-based sensors may be integrated into the same chip as the pixel array and lower operation voltages are needed. Therefore CMOS-based cameras are much cheaper and easier to manufacture and may be much more versatile than their CCD-based counterparts. For similar reasons, CMOS sensors are appearing more and more within endoscope systems.

[0025] Less expensive endoscopes to manufacture may be realized by placing the image sensing device at the distal end of the endoscope, since the optical transport assembly may be effectively replaced by a simple plastic lens stack. They may be so inexpensive that it may make more financial sense to have them be manufactured for single use only, to be subsequently disposed of or recycled, since that negates the repair and sterilization processes.

[0026] The difficulty in creating such an endoscope solution is in maintaining image quality, since the region into which the sensor must fit is highly space constrained in both dimensions. Reducing the sensor area generally implies a reduction in pixel count and/or pixel area, which may impact the resolution, sensitivity and dynamic range. Normally, endoscope systems are geared toward sensing steady broadband illumination and providing color information by virtue of arrays that are segmented into pixels of three or more ranges of wavelength sensitivity. This is done by crafting an individual color filter over each pixel, the Bayer mosaic being the most common solution.

[0027] One way to avoid resolution loss is to eliminate the color filters since with the Bayer mosaic, e.g., there may be up to a factor $1/\sqrt{2}$ loss in luminance resolution (in x or y) as compared with the native array resolution. The color information in such a case can be provided by pulsing a laser or LED-based illuminants with different wavelengths or combinations thereof during separate frame captures. Applicant has developed approaches and solutions to this, which allow for high definition quality at progressive frame rates of 60Hz or higher, by virtue of a special sensor design. Further developments by Applicant have allowed for the peripheral circuitry to be reduced to its minimal area while transmitting image data off chip in the digital domain.

[0028] A significant consumer of chip area is each bond pad, used to provide power or input/output signals to and from the sensor chip. Therefore, in striving for minimal area it is desirable to reduce the number of bond pads as much as possible.

[0029] Synchronization of the sensor data may be performed without an output clock. High speed data transmission may normally be accompanied by a clock for synchronization purposes. This has the inconvenience of one additional pad for CMOS or 2 additional pads if the LVDS standard is in use. An alternative system and method of latching high speed data may be to embed the clock signal within the data stream itself (clock encoding). At the receiving end, the data stream may be decoded in order to extract the clock, which is then used to latch the data. The penalty or disadvantage of this system and method may be that a significant burden is added to the payload and the output frequency has to be significantly increased.

[0030] In this disclosure a method is described, which may prevent the need for output clock pads without the use of clock encoding. Instead, the disclosure may use the CDR (Clock Data Recovery) system on the camera unit to correctly latch the incoming data. In the CDR system, an internal PLL (Phase Locked Loop) is used to lock on the incoming data frequency and to latch the data. The locking process requires data transitions in order for its PLL to converge. Typically, a minimum number of transitions for initial locking (and re-locking) will be specified along with a maximum number of consecutive allowed bits without transition, (which may be required in order for the PLL to stay locked).

[0031] Referring now to the figures, FIG.1 illustrates the internal timing of an embodiment of a minimal area custom CMOS image sensor. Each frame period may comprise 4 distinct phases. During phases 1 and 3, data may be issued from the sensor through sensor data pads 150, which are not signal samples from physical pixels. Rather they are data concerned with the synchronization of the chip to the camera system and for data locking. Phase 2 is concerned with the sensor rolling readout (internal timing, synchronization and readout of physical pixels) while phase 4 is for the purpose of sensor configuration. During the configuration phase, the sensor output data lines 160 may be reversed to accept incoming configuration commands. There is a risk that during phase 4, the CDR circuit in the camera unit will become unlocked, since the sensor will not send any data transitions during a defined period of time. The service lines of phase 1 may be used to send a continuous stream of data transitions, however, to re-lock the camera unit CDR circuit, should they be required.

[0032] FIG. 2 illustrates an example of such a stream where a clock-like signal is inserted into the output data stream, where normally there would be pixel data (clock recovery lines) 210. It should be noted that other clock patterns may be used and fall within the scope of this disclosure. As seen best in FIG. 2, a line header 222 may be defined, in order for the camera system to differentiate between clock recovery lines and pixel data lines. The number of clock recovery lines in phase 1 is adjustable via a register setting.

[0033] It should be noted that the duration of phase 4 may be below about ~5ms-10ms, which allows for a very limited number of clock recovery lines. Therefore, the number of transitions available to re-lock the system may be correspondingly low. This should not normally be an issue, however, because the PLL voltage of the camera unit CDR does not have time to drift very far away from the locking voltage during phase 4. In the event of the PLL voltage being significantly far from the locking voltage (at start-up for example), the receiver needs a significantly greater number of transitions. For that purpose, the sensor can be programmed to be in a full clock training sequence wherein phases 1, 2 and 3 may be merged to become continuous period of clock training. See, for example, FIG. 3. Once the camera unit CDR has locked, the sensor may resume normal operation with phase 1 providing the smaller adjustments needed for re-locking of the camera unit CDR. Therefore, the CDR specification regarding the minimal number of transitions to lock or re-lock is taken care of by the 2 operation modes described.

[0034] In order to address the CDR specification concerned with the maximal number of bits between transitions (to ensure that the CDR does not lose its lock), a method which is based upon a special encoding of the pixel data, may be used.

[0035] In FIG. 4, an example of such a special pixel encoding is shown in which the actual pixel data values are 11 bits, (with the MSB transmitted first and the LSB, last). A 12th bit may be added to each pixel's data, which is always an inverted version of the 11th (least significant) true bit. This results in an encoding with very little overhead. A high transition rate may be obtained during the transmission of pixel data, thereby avoiding any possibility of the camera unit CDR becoming unlocked.

[0036] FIGS. 5A and 5B illustrate two conventional methods to generate a clock signal for an image sensor 505. FIG. 5A relates to an off-chip device that may be a crystal oscillator and a Phase Lock Loop (PLL) circuit. Although very precise, this method adds the burden of one pad 510 and one active component. Moreover the active component may require low speed control programming that further increases the conductor count. This may be a disadvantage at the distal tip of an endoscope where space is very limited. FIG. 5B represents a clock generation using on-chip circuitry. This method provides an advantageous result in terms of pad 510 and conductor counts.

However, such circuits may be inconsistent and exhibit significant variability from chip to chip. Moreover, they are often temperature dependent and can be sensitive to any change in temperature. These drawbacks prevent use in applications like video where the frame rate needs to be ultra-precise.

[0037] This disclosure describes a method and system of generating an on-chip precise clock without adding any external components. It should be further noted that by virtue of re-purposing the sensor data output pads and low speed control programming pads (which may be the same bidirectional pads as described above), no extra pad nor conductor is required.

[0038] FIG. 6 depicts a conventional PLL 600. The VCDL (voltage controlled delay line) clock is compared to the incoming clock with the frequency detector and up-pushes or down-pushes are issued to the external VCO (voltage controlled oscillator) depending on the frequency detector comparison result. This system may dynamically react and adjust to ensure that the VCDL clock always matches the input clock.

[0039] The concept behind the system and method is to create a PLL that overlaps between the sensor and the camera unit, taking advantage of the communication protocol that already exists between the two devices. In an embodiment, the system and method may move the frequency detector from the sensor PLL to the camera unit. Its input can then be attached to the precise clock provided by camera unit oscillator. This local oscillator has the additional benefit of not increasing the sensor pad count because located in the camera unit. In the embodiment, a digital feed-forward and feedback nodes in the PLL may be selected and matched to the feed-forward system node (low speed control programming from camera unit to sensor) and feedback system node (pixel data output from sensor to camera unit).

[0040] In the embodiment of FIG. 7, the feed-forward node may be chosen to be the go-fast go-slow signals and will be updated using the sensor low speed control programming. The feedback node may be chosen to be the multiplied clock prior to the divider by n. This multiplied frequency may be used to serialize the pixel data and is decoded by the CDR in the camera unit, which can then be fed back to the frequency detector. Such an embodiment does not increase the pad 710 count or the conductor count.

[0041] In an implementation, shown in FIG. 8, a DAC 808 instead of charge pump may be used. The low speed control could program a configuration register with a digital word (if using a DAC) instead of a push-up/push-down (if using a charge pump).

[0042] It may be desirable to build such a system without segmenting the on-chip PLL. The embodiment of FIG. 9 depicts an equivalent circuit where the internal PLL remains unchanged, but the clock input pad is removed and the input clock signal is provided by a clock generator distributed circuit equivalent to that of FIG. 7. The version of this last circuit using a DAC 1010 instead of a charge pump 909 is shown in FIG. 10.

[0043] In an embodiment, an algorithm that may reside in the camera unit is depicted in FIG. 11, and may be built for a charge pump based system. The Table in FIG. 12 lists the signals and parameters that may be used by the camera unit for the FIG. 11 algorithm.

[0044] The following is an example of the algorithm implementation. The R_CLK may be compared to the target frequency using REF_CLK as the method or mode of comparison. If R_CLK is too low then PUSH UP may be asserted. If R_CLK is too high then PUSH DOWN may be asserted. The BIG_LITTLE output may be used based on how far R_CLK is from the target frequency. As an example, if a big push represents a 5% change and a little push represents a 1% change in frequency then if R_CLK is lower than target frequency minus 3%, the block

may issue a PUSH UP BIG command. The next time the R_CLK is measured it will be approximately 2% greater than the target and so the block may issue a PUSH DOWN LITTLE command.

[0045] The method of comparing the R_CLK to the target frequency may be as follows. In an example, if the REF_CLK is 27 MHz, the target is 40 MHz and the R_CLK is 38 MHz, then the block may count the number of R_CLK transitions over 1 ms (or 27,000 transitions of REF_CLK). It may compare its counter value, now 38,000 to the desired target of 40,000 and issue a PUSH UP BIG command assuming the BIG and LITTLE thresholds are 5% and 1%.

[0046] It will be appreciated that implementations of the disclosure may comprise or utilize a special purpose or general-purpose computer including computer hardware, such as, for example, one or more processors and system memory, as discussed in greater detail below. Implementations within the scope of the disclosure may also include physical and other computer-readable media for carrying or storing computer-executable instructions and/or data structures. Such computer-readable media can be any available media that can be accessed by a general purpose or special purpose computer system. Computer-readable media that store computer-executable instructions may be computer storage media (devices). Computer-readable media that carry computer-executable instructions may be transmission media. Thus, by way of example, and not limitation, implementations of the disclosure can comprise at least two distinctly different kinds of computer-readable media: computer storage media (devices) and transmission media.

[0047] Computer storage media (devices) includes RAM, ROM, EEPROM, CD-ROM, solid state drives (“SSDs”) (e.g., based on RAM), Flash memory, phase-change memory (“PCM”), other types of memory, other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium which can be used to store desired program code means in the form of computer-executable instructions or data structures and which can be accessed by a general purpose or special purpose computer.

[0048] A “network” may be defined as one or more data links that enable the transport of electronic data between computer systems and/or modules and/or other electronic devices. In an implementation, a sensor and camera control unit may be networked in order to communicate with each other, and other components, connected over the network to which they may be connected. When information is transferred or provided over a network or another communications connection (either hardwired, wireless, or a combination of hardwired or wireless) to a computer, the computer properly views the connection as a transmission medium. Transmissions media can include a network and/or data links which can be used to carry desired program code means in the form of computer-executable instructions or data structures and which can be accessed by a general purpose or special purpose computer. Combinations of the above should also be included within the scope of computer-readable media.

[0049] Further, upon reaching various computer system components, program code means in the form of computer-executable instructions or data structures that can be transferred automatically from transmission media to computer storage media (devices) (or vice versa). For example, computer-executable instructions or data structures received over a network or data link can be buffered in RAM within a network interface module (e.g., a “NIC”), and then eventually transferred to computer system RAM and/or to less volatile computer storage media (devices) at a computer system. RAM can also include solid state drives (SSDs or PCIx based real time memory tiered Storage, such as FusionIO). Thus, it should be understood that computer storage media (devices) can be included in computer system components that also (or even primarily) utilize transmission media.

[0050] Computer-executable instructions comprise, for example, instructions and data which, when executed at a processor, cause a general purpose computer, special purpose computer, or special purpose processing device to perform a certain function or group of functions. The computer executable instructions may be, for example, binaries, intermediate format instructions such as assembly language, or even source code. Although the subject matter has been described in language specific to structural features and/or methodological acts, it is to be understood that the subject matter defined in the appended disclosure is not necessarily limited to the described features or acts described above. Rather, the described features and acts may be disclosed as example forms of implementing the disclosure.

[0051] Those skilled in the art will appreciate that the disclosure may be practiced in network computing environments with many types of computer system configurations, including, personal computers, desktop computers, laptop computers, message processors, control units, camera control units, hand-held devices, hand pieces, multi-processor systems, microprocessor-based or programmable consumer electronics, network PCs, minicomputers, mainframe computers, mobile telephones, PDAs, tablets, pagers, routers, switches, various storage devices, and the like. It should be noted that any of the above mentioned computing devices may be provided by or located within a brick and mortar location. The disclosure may also be practiced in distributed system environments where local and remote computer systems, which may be linked (either by hardwired data links, wireless data links, or by a combination of hardwired and wireless data links) through a network, both perform tasks. In a distributed system environment, program modules may be located in both local and remote memory storage devices.

[0052] Further, where appropriate, functions described herein can be performed in one or more of: hardware, software, firmware, digital components, or analog components. For example, one or more application specific integrated circuits (ASICs) or field programmable gate arrays can be programmed to carry out one or more of the systems and procedures described herein. Certain terms may be used throughout the following description and Disclosure to refer to particular system components. As one skilled in the art will appreciate, components may be referred to by different names. This document does not intend to distinguish between components that differ in name, but not function.

[0053] FIG. 13 is a block diagram illustrating an example computing device 1300. Computing device 1300 may be used to perform various procedures, such as those discussed herein. Computing device 1300 can function as a server, a client, or any other computing entity. Computing device can perform various monitoring functions as discussed herein, and can execute one or more application programs, such as the application programs described herein. Computing device 1300 can be any of a wide variety of computing devices, such as a desktop computer, a notebook computer, a server computer, a handheld computer, camera control unit, tablet computer and the like.

[0054] Computing device 1300 includes one or more processor(s) 1302, one or more memory device(s) 1304, one or more interface(s) 1306, one or more mass storage device(s) 1308, one or more Input/Output (I/O) device(s) 1310, and a display device 1330 all of which may be coupled to a bus 1312. Processor(s) 1302 include one or more processors or controllers that execute instructions stored in memory device(s) 1304 and/or mass storage device(s) 1308. Processor(s) 1302 may also include various types of computer-readable media, such as cache memory.

[0055] Memory device(s) 1304 include various computer-readable media, such as volatile memory (e.g., random access memory (RAM) 1314) and/or nonvolatile memory (e.g., read-only memory (ROM) 1316). Memory device(s) 1304 may also include rewritable ROM, such as Flash memory.

[0056] Mass storage device(s) 1308 include various computer readable media, such as magnetic tapes, magnetic disks, optical disks, solid-state memory (e.g., Flash memory), and so forth. As shown in FIG. 13, a particular mass storage device is a hard disk drive 1324. Various drives may also be included in mass storage device(s) 1308 to enable reading from and/or writing to the various computer readable media. Mass storage device(s) 1308 include removable media 1326 and/or non-removable media.

[0057] I/O device(s) 1310 include various devices that allow data and/or other information to be input to or retrieved from computing device 1300. Example I/O device(s) 1310 include digital imaging devices, electromagnetic sensors and emitters, cursor control devices, keyboards, keypads, microphones, monitors or other display devices, speakers, printers, network interface cards, modems, lenses, CCDs or other image capture devices, and the like.

[0058] Display device 1330 includes any type of device capable of displaying information to one or more users of computing device 1300. Examples of display device 1330 include a monitor, display terminal, video projection device, and the like.

[0059] Interface(s) 1306 include various interfaces that allow computing device 1300 to interact with other systems, devices, or computing environments. Example interface(s) 1306 may include any number of different network interfaces 1320, such as interfaces to local area networks (LANs), wide area networks (WANs), wireless networks, and the Internet. Other interface(s) include user interface 1318 and peripheral device interface 1322. The interface(s) 1306 may also include one or more user interface elements 1318. The interface(s) 1306 may also include one or more peripheral interfaces such as interfaces for printers, pointing devices (mice, track pad, etc.), keyboards, and the like.

[0060] Bus 1312 allows processor(s) 1302, memory device(s) 1304, interface(s) 1306, mass storage device(s) 1308, and I/O device(s) 1310 to communicate with one another, as well as other devices or components coupled to bus 1312. Bus 1312 represents one or more of several types of bus structures, such as a system bus, PCI bus, IEEE 1394 bus, USB bus, and so forth.

[0061] For purposes of illustration, programs and other executable program components may be shown herein as discrete blocks, although it is understood that such programs and components may reside at various times in different storage components of computing device 1300, and may be executed by processor(s) 1302. Alternatively, the systems and procedures described herein can be implemented in hardware, or a combination of hardware, software, and/or firmware. For example, one or more application specific integrated circuits (ASICs) can be programmed to carry out one or more of the systems and procedures described herein.

[0062] It will be appreciated that the disclosure may be used with any image sensor, whether a CMOS image sensor or CCD image sensor, without departing from the scope of the disclosure. Further, the image sensor may be located in any location within the overall system, including, but not limited to, the tip of the endoscope, the hand piece of the imaging device or camera, the control unit, or any other location within the system without departing from the scope of the disclosure.

[0063] Implementations of an image sensor that may be utilized by the disclosure include, but are not limited to, the following, which are merely examples of various types of sensors that may be utilized by the disclosure.

[0064] FIGS. 14A and 14B illustrate an implementation of a monolithic sensor 1405 having a plurality of pixel arrays 1410 for producing a three dimensional image in accordance with the teachings and principles of the

disclosure. Such an implementation may be desirable for three dimensional image capture, wherein the two pixel arrays 1410 may be offset during use. In another implementation, a first pixel array 1410 and a second pixel array 1410 may be dedicated to receiving a predetermined range of wave lengths of electromagnetic radiation, wherein the first pixel array 1410 is dedicated to a different range of wave length electromagnetic radiation than the second pixel array 1410.

[0065] FIGS. 15A and 15B illustrate a view of an implementation of an imaging sensor built on a plurality of substrates 1510, 1511. As illustrated, a plurality of pixel columns forming the pixel array 1515 are located on the first substrate 1511 and a plurality of circuit columns 1520 are located on a second substrate 1510. Also illustrated in the figure are the electrical connection and communication between one column of pixels to its associated or corresponding column of circuitry.

[0066] In one implementation, an image sensor, which might otherwise be manufactured with its pixel array and supporting circuitry on a single, monolithic substrate/chip, may have the pixel array separated from all or a majority of the supporting circuitry. The disclosure may use at least two substrates/chips, which will be stacked together using three-dimensional stacking technology. The first of the two substrates/chips may be processed using an image CMOS process. The first substrate/chip may be comprised either of a pixel array exclusively or a pixel array surrounded by limited circuitry. The second or subsequent substrate/chip may be processed using any process, and does not have to be from an image CMOS process. The second substrate/chip may be, but is not limited to, a highly dense digital process in order to integrate a variety and number of functions in a very limited space or area on the substrate/chip, or a mixed-mode or analog process in order to integrate for example precise analog functions, or a RF process in order to implement wireless capability, or MEMS (Micro-Electro-Mechanical Systems) in order to integrate MEMS devices. The image CMOS substrate/chip may be stacked with the second or subsequent substrate/chip using any three-dimensional technique. The second substrate/chip may support most, or a majority, of the circuitry that would have otherwise been implemented in the first image CMOS chip (if implemented on a monolithic substrate/chip) as peripheral circuits and therefore have increased the overall system area while keeping the pixel array size constant and optimized to the fullest extent possible. The electrical connection between the two substrates/chips may be done through interconnects, which may be wirebonds, bump and/or TSV (Through Silicon Via).

[0067] FIGS. 16A and 16B illustrate a view of an implementation of an imaging sensor having a plurality of pixel arrays for producing a three dimensional image. The three dimensional image sensor may be built on a plurality of substrates 1611a, 1611b, 1611c, and may comprise the plurality of pixel arrays 1615a, 1615b and other associated circuitry 1630a, 1630b, wherein a plurality of pixel columns forming the first pixel array and a plurality of pixel columns forming a second pixel array are located on respective substrates and a plurality of circuit columns are located on a separate substrate. Also illustrated are the electrical connections and communications between columns of pixels to associated or corresponding column of circuitry.

[0068] It will be appreciated that the teachings and principles of the disclosure may be used in a reusable device platform, a limited use device platform, a re-posable use device platform, or a single-use/disposable device platform without departing from the scope of the disclosure. It will be appreciated that in a re-usable device platform an end-user is responsible for cleaning and sterilization of the device. In a limited use device platform the device can be used for some specified amount of times before becoming inoperable. Typical new device is delivered sterile with

additional uses requiring the end-user to clean and sterilize before additional uses. In a re-posable use device platform a third-party may reprocess the device (e.g., cleans, packages and sterilizes) a single-use device for additional uses at a lower cost than a new unit. In a single-use/disposable device platform a device is provided sterile to the operating room and used only once before being disposed of.

[0069] Additionally, the teachings and principles of the disclosure may include any and all wavelengths of electromagnetic energy, including the visible and non-visible spectrums, such as infrared (IR), ultraviolet (UV), and X-ray.

[0070] It will be appreciated that various features disclosed herein provide significant advantages and advancements in the art. The following embodiments may be exemplary of some of those features.

[0071] An embodiment of a reduced area image sensor may comprise: input and output pads wherein the pad count is reduced by no having a no synchronization clock pad; wherein signal transitions are encoded within the output data; service lines within the frame; wherein a camera unit clock and/or data recovery circuit may be used to lock on the incoming sensor data to keep it synchronized. An embodiment may further comprise a minimal area CMOS image sensor disposed within the distal end of endoscopes. An embodiment may further comprise at least one transition within each pixel serial data created within the pixel array. An embodiment may further comprise at least one transition during a series of a plurality pixel data sets created by the pixel array. An embodiment may further comprise a plurality of transitions within each pixel serial data created by the pixel array. An embodiment may further comprise replaced pixel data with clock signal data. An embodiment may further comprise replaced pixel data with clock signal data within at least one service line phase of one frame period. An embodiment may further comprise replaced pixel data with clock signal data within the service line phase just prior to the true pixel data output phase. An embodiment may further comprise replaced pixel data with clock signal data within and at all output frame phases except during pixel data output phase.

[0072] An embodiment of a reduced image sensor may operate, be designed by, and may comprise: replacing pixel data with clock signal data within, and at all output frame phases including during pixel data output phase; removing clock pads; building a Phase Lock Loop (PLL) with blocks of the sensor and other blocks of the camera unit; using data lines and configuration lines for connecting together sensor PLL blocks and camera unit PLL blocks; and using the camera unit clock and data recovery circuit to lock on the incoming sensor data. An embodiment may further comprise minimal area CMOS image sensor for use in the distal end of endoscopes. An embodiment may further comprise bidirectional data pads to issue image data during a defined portion of the frame timing. An embodiment may further issue other types of data during another portions of the frame data output. An embodiment may switch direction and receive commands from the external camera system during a third defined time period during the frame while in receive mode. An embodiment may be PLL based on a charge pump for driving the Voltage Controlled Oscillator (VCO). An embodiment may be PLL based on a Digital to Analog Convertor (DAC) for driving the VCO. An embodiment may further comprise programming a sensor configuration register to store increase of decrease of the resultant operating frequency. An embodiment may further comprise local oscillator as a PLL reference clock. An embodiment may further comprise the use differing strength pushes.

[0073] In the foregoing Detailed Description of the Disclosure, various features of the disclosure may be grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the disclosure requires more features than may be expressly

recited in the disclosure. Rather, inventive aspects lie in less than all features of a single foregoing disclosed embodiment.

[0074] It is to be understood that the above-described arrangements may be only illustrative of the application of the principles of the disclosure. Numerous modifications and alternative arrangements may be devised by those skilled in the art without departing from the spirit and scope of the disclosure and the appended disclosure may be intended to cover such modifications and arrangements.

[0075] Thus, while the disclosure has been shown in the drawings and described above with particularity and detail, it will be apparent to those of ordinary skill in the art that numerous modifications, including, but not limited to, variations in size, materials, shape, form, function and manner of operation, assembly and use may be made without departing from the principles and concepts set forth herein.

[0076] Further, where appropriate, functions described herein can be performed in one or more of: hardware, software, firmware, digital components, or analog components. For example, one or more application specific integrated circuits (ASICs) can be programmed to carry out one or more of the systems and procedures described herein. Certain terms may be used throughout the following description and Disclosure to refer to particular system components. As one skilled in the art will appreciate, components may be referred to by different names. This document does not intend to distinguish between components that differ in name, but not function.

[0077] The foregoing description has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the disclosure to the precise form disclosed. Many modifications and variations may be possible in light of the above teaching. Further, it should be noted that any or all of the aforementioned alternate implementations may be used in any combination desired to form additional hybrid implementations of the disclosure.

[0078] Further, although specific implementations of the disclosure have been described and illustrated, the disclosure is not to be limited to the specific forms or arrangements of parts so described and illustrated. The scope of the disclosure is to be defined by the disclosure appended hereto, any future disclosure submitted here and in different applications, and their equivalents.

CLAIMS

What is claimed is:

1. An endoscopic system for use a controlled light environment comprising:
an endoscope comprising a lumen and an image sensor;
an emitter;
a fiber optic cable;
a control circuit in electronic communication with the image sensor and the emitter;
wherein the control circuit will control a duty cycle of the emitter in response to signals that correspond to the duty cycle of the emitter;
wherein the image sensor comprises:
input and output pads wherein the pad count is reduced by not having a dedicated synchronization clock pad;
a frame period that is divided into three defined states:
a rolling-readout state during which image data is output through the pads,
a service-line state during which non-image data is output through the pads, and
a configuration state during which the instruction data is received by the image sensor through the pads,
wherein signal transitions are encoded within the output data from the image sensor in correspondence to the frame period states.
2. The endoscopic system of claim 1, wherein the output data comprise signal transitions as service lines within frame data.
3. The endoscopic system of claim 1, wherein a camera unit clock is used to synchronize the incoming sensor data.
4. The endoscopic system of claim 1, wherein a data recovery circuit may be used to lock on the incoming sensor data to keep it synchronized.
5. The endoscopic system of claim 1, further comprising at least one transition within each pixel serial data created within a pixel array of the image sensor.
6. The endoscopic system of claim 5, further comprising at least one transition during a series of a plurality pixel data sets created by the pixel array.
7. The endoscopic system of claim 5, further comprising a plurality of transitions within each pixel serial data created by the pixel array.
8. The endoscopic system of claim 1, wherein pixel data is replaced created with clock signal data for synchronization.
9. The endoscopic system of claim 1, wherein pixel data is replaced with clock signal data within at least one service line phase of one frame period.
10. The endoscopic system of claim 1, wherein pixel data is replaced with clock signal data within the service line phase just prior to the true pixel data output phase.

11. The endoscopic system of claim 1, wherein clock signal data is transmitted during all frame period phases except during pixel data output phase.
12. The endoscopic system of claim 1, further comprising a Phase Lock Loop built with blocks of the sensor and blocks of the camera unit.
13. The endoscopic system of claim 12, further comprising data lines and configuration lines electrically connecting together sensor Phase Lock Loop blocks and camera unit Phase Lock Loop blocks.
14. The endoscopic system of claim 13, wherein a camera unit clock and a data recovery circuit are used to lock on to the incoming sensor data.
15. The endoscopic system of claim 1, further comprising bidirectional data pads to issue image data during a defined portion of the frame timing.
16. The endoscopic system of claim 15, wherein the data pads issue a plurality of types of data during and corresponding to a plurality of portions of frame data output.
17. The endoscopic system of claim 16, wherein the data pads are configured to switch direction and receive commands from external system components during a third defined time period of the frame period while in receive mode.
18. The endoscopic system of claim 1, further comprising a Phase Loop Lock based on a charge pump for driving the Voltage Controlled Oscillator.
19. The endoscopic system of claim 18, further comprising Phase Loop Lock based on a Digital to Analog Converter for driving the Voltage Controlled Oscillator.
20. The endoscopic system of claim 1, further comprising a sensor configuration register to store changes in resultant operating frequency.
21. The endoscopic system of claim 1, further comprising a local oscillator as a Phase Lock Loop reference clock.
22. The endoscopic system of claim 1, further comprising a Phase Lock Loop based on differing voltage strength pushes.

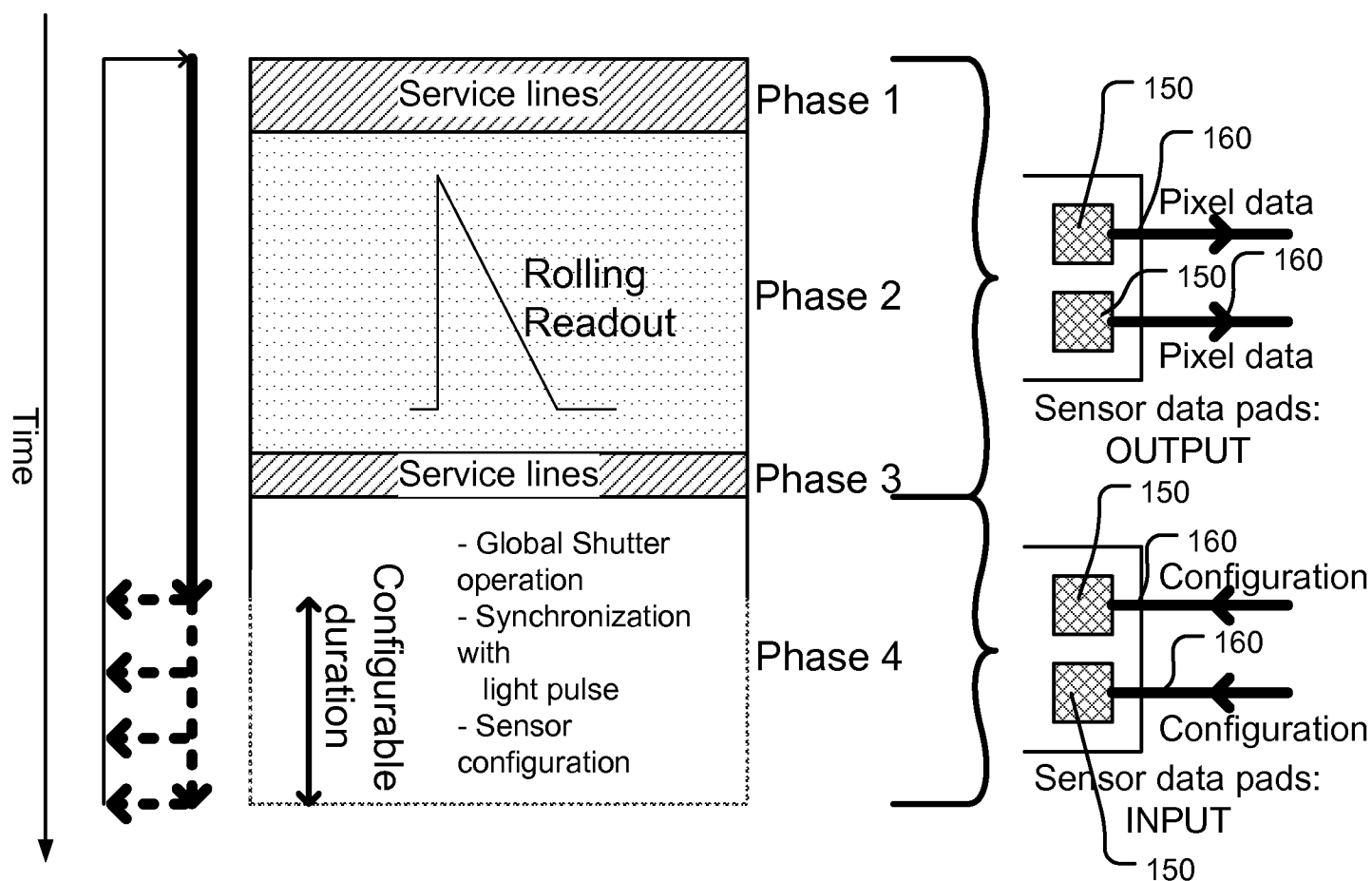


FIG. 1

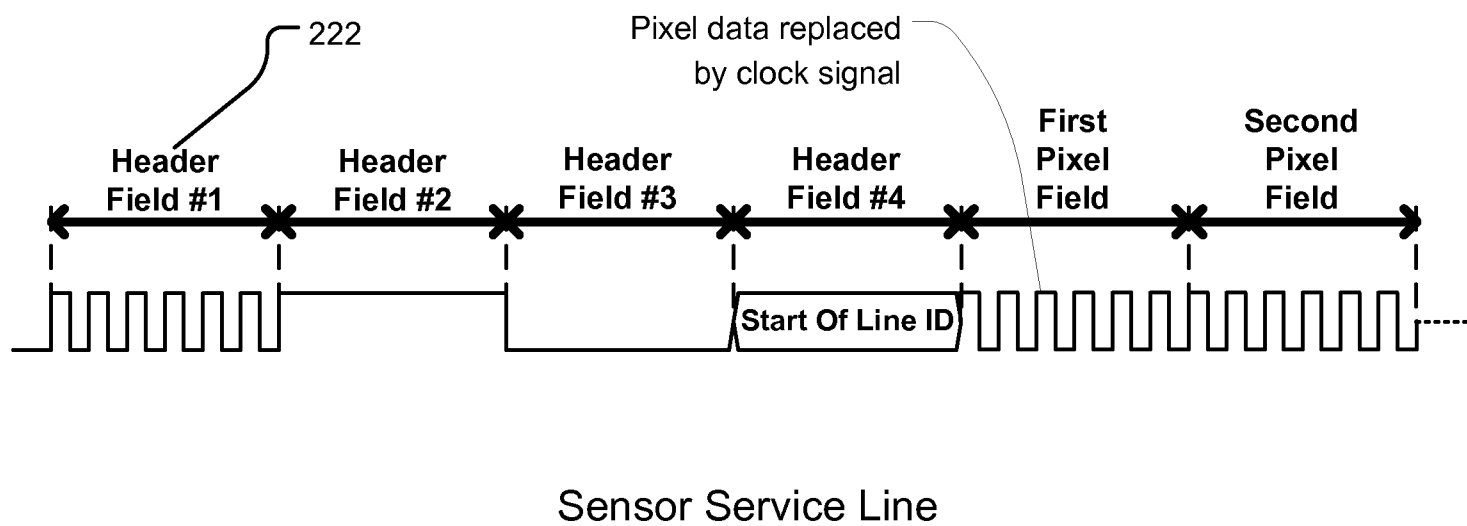


FIG. 2

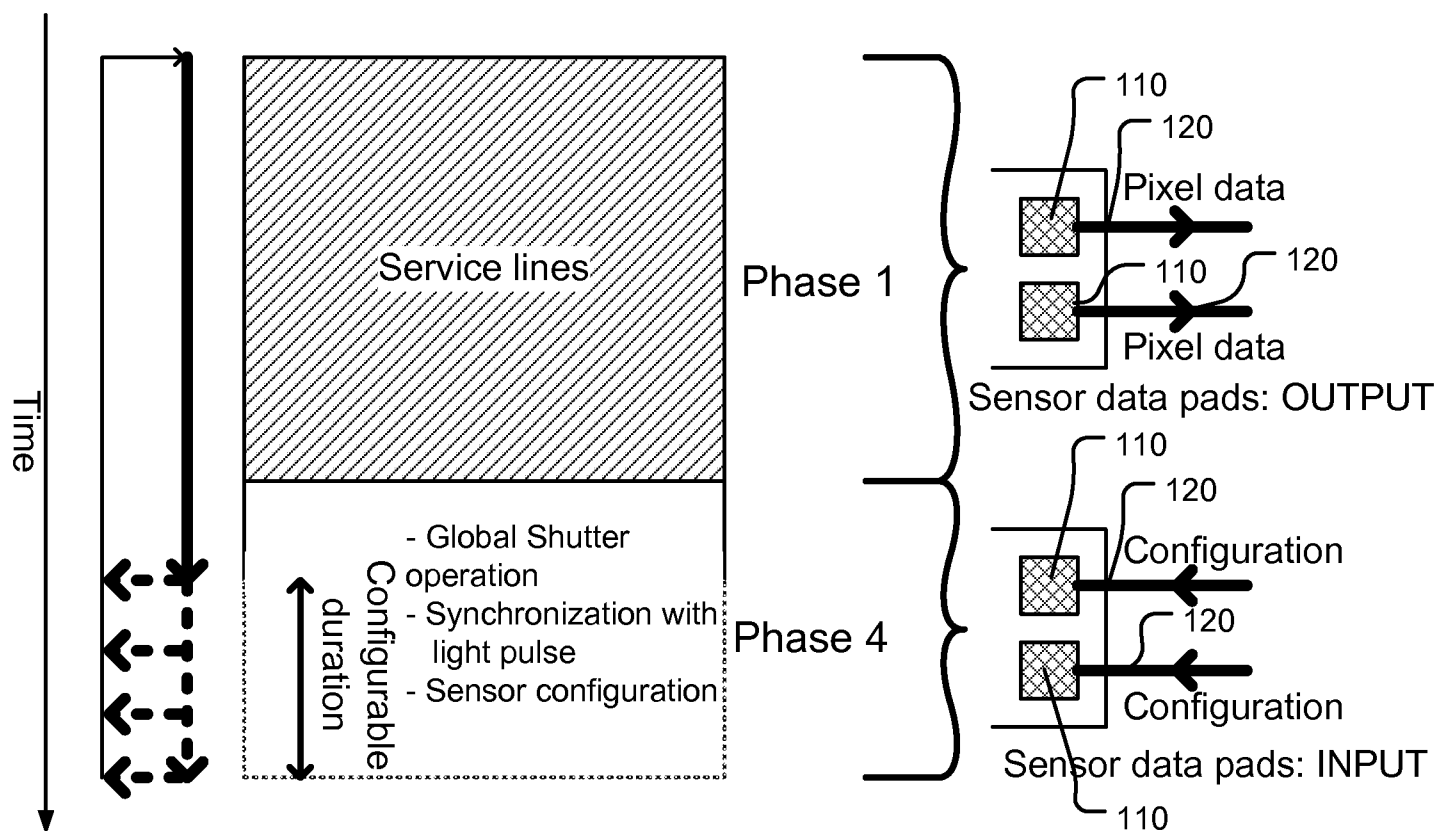


FIG. 3

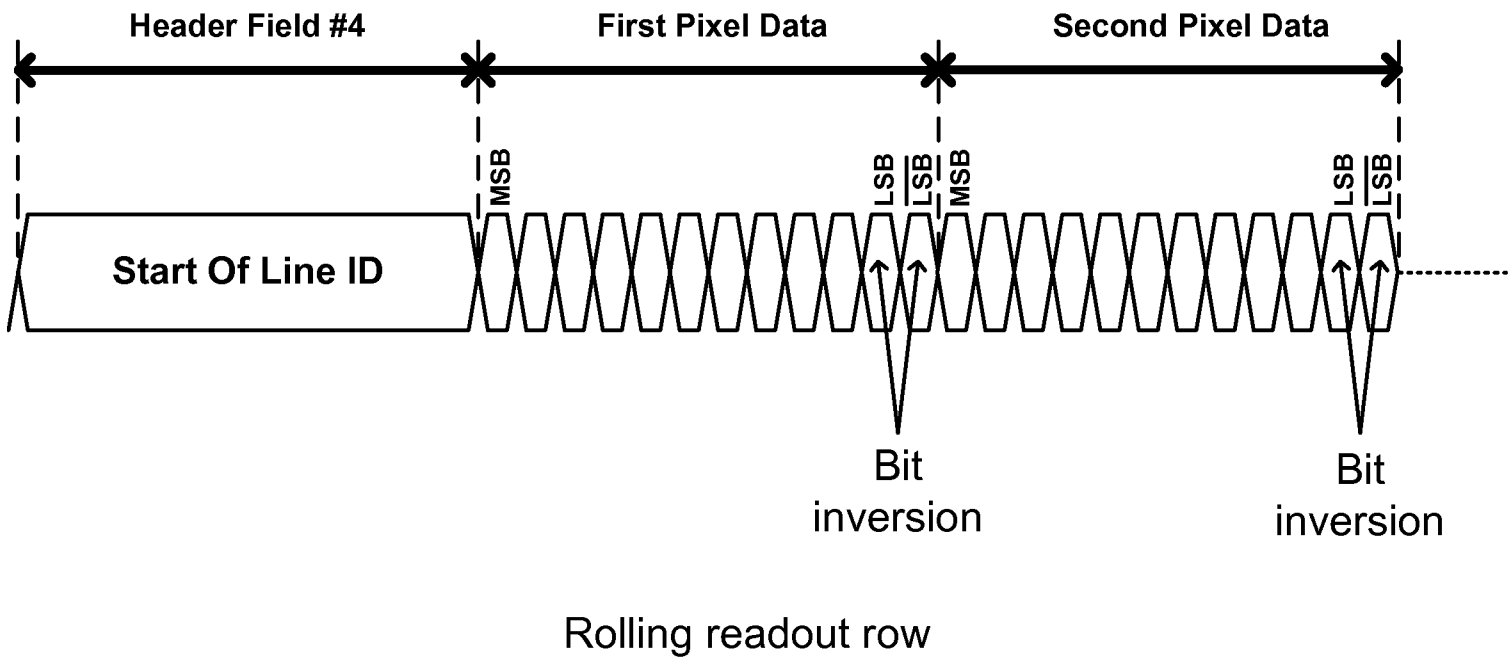


FIG. 4

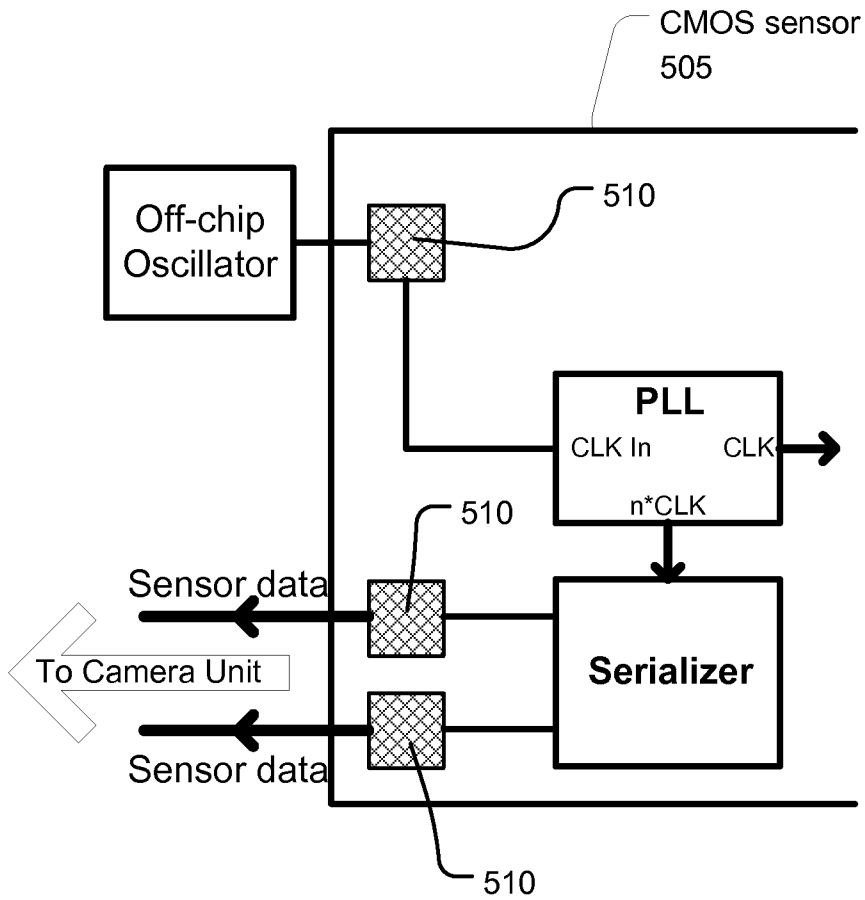


FIG. 5A

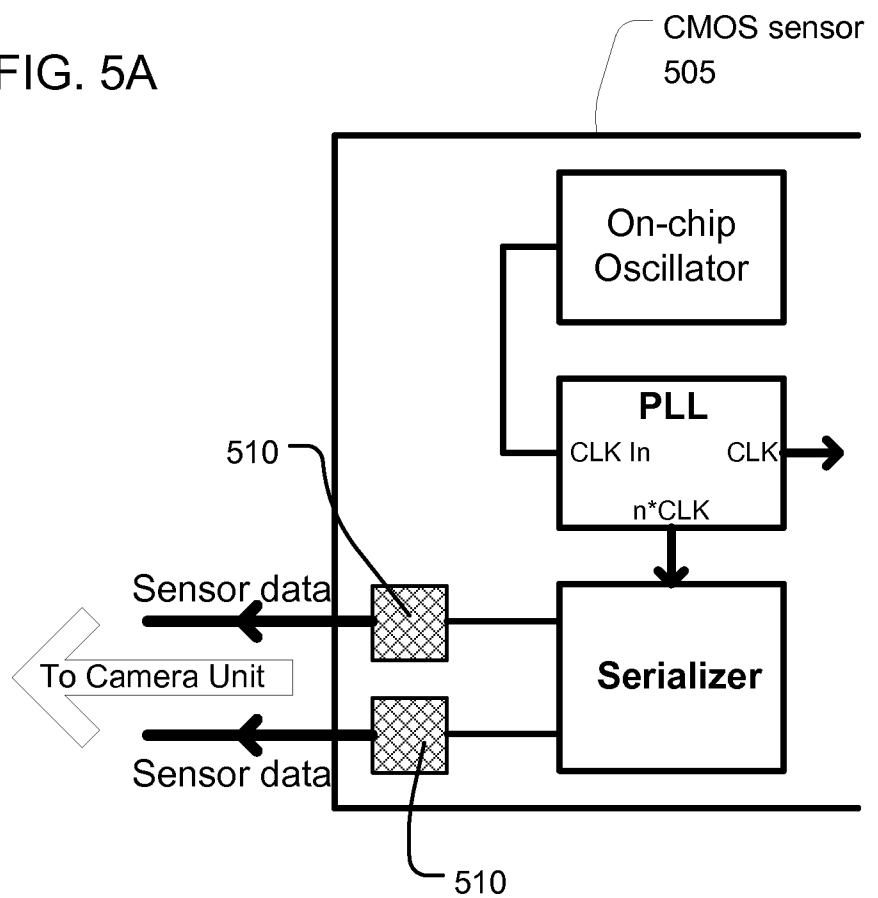


FIG. 5B

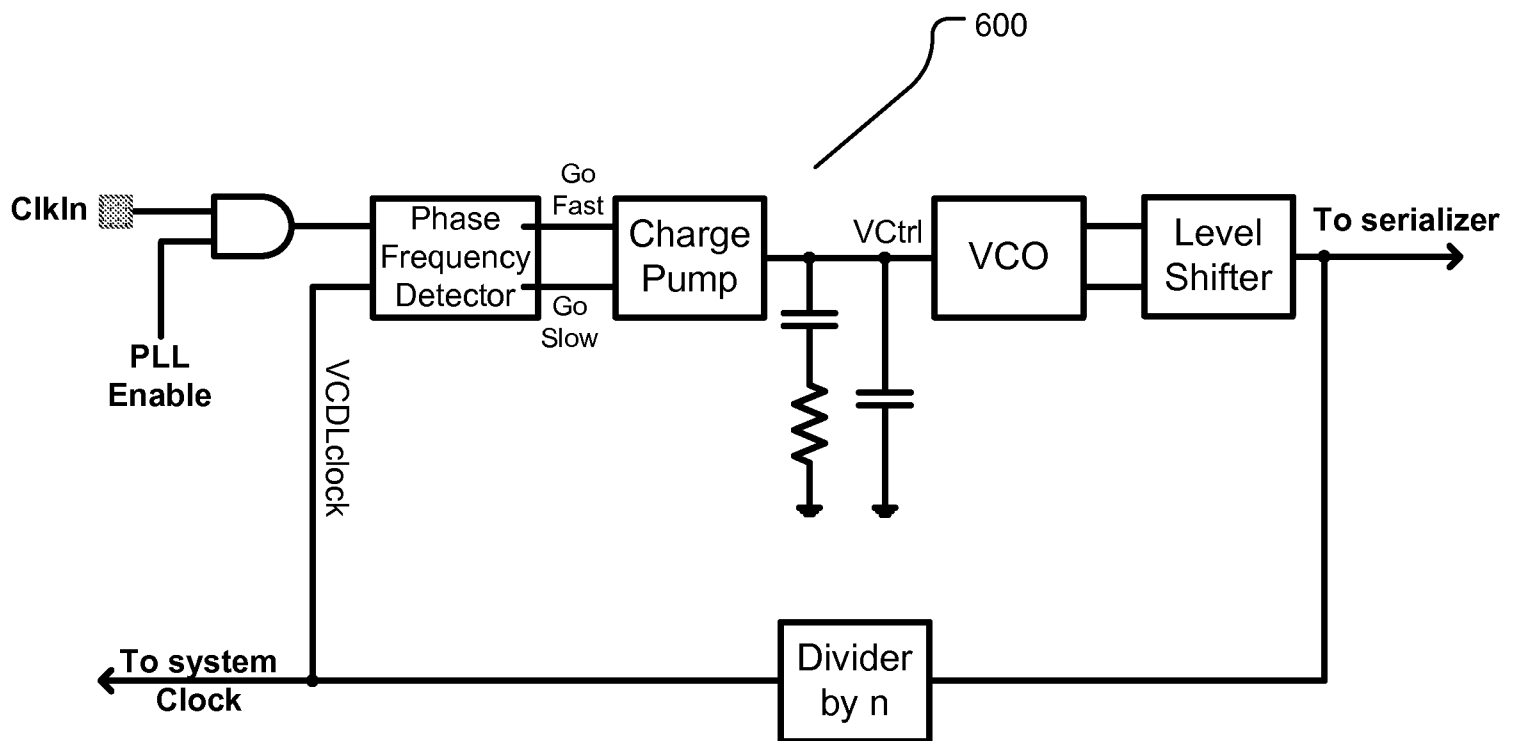


FIG. 6

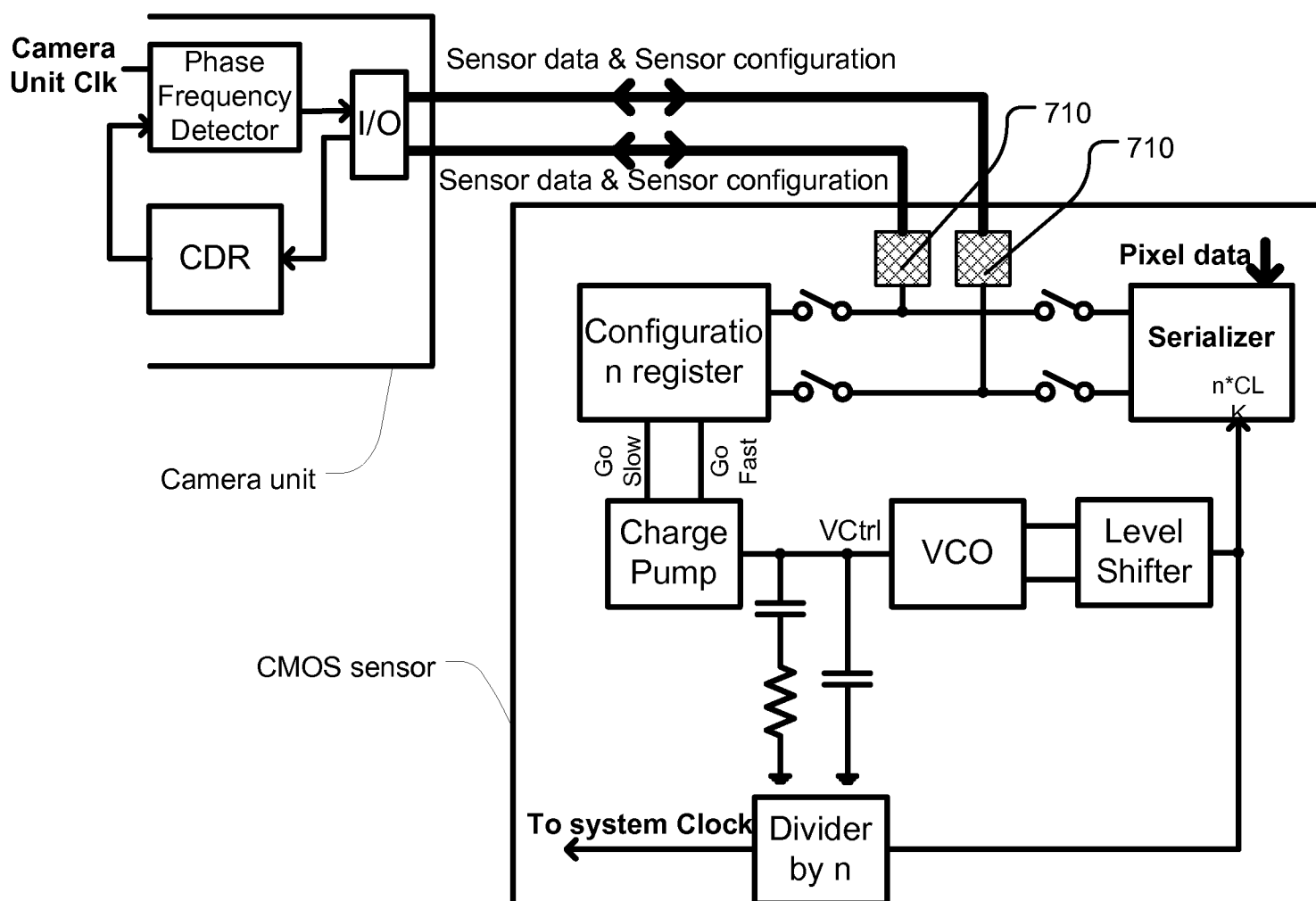


FIG. 7

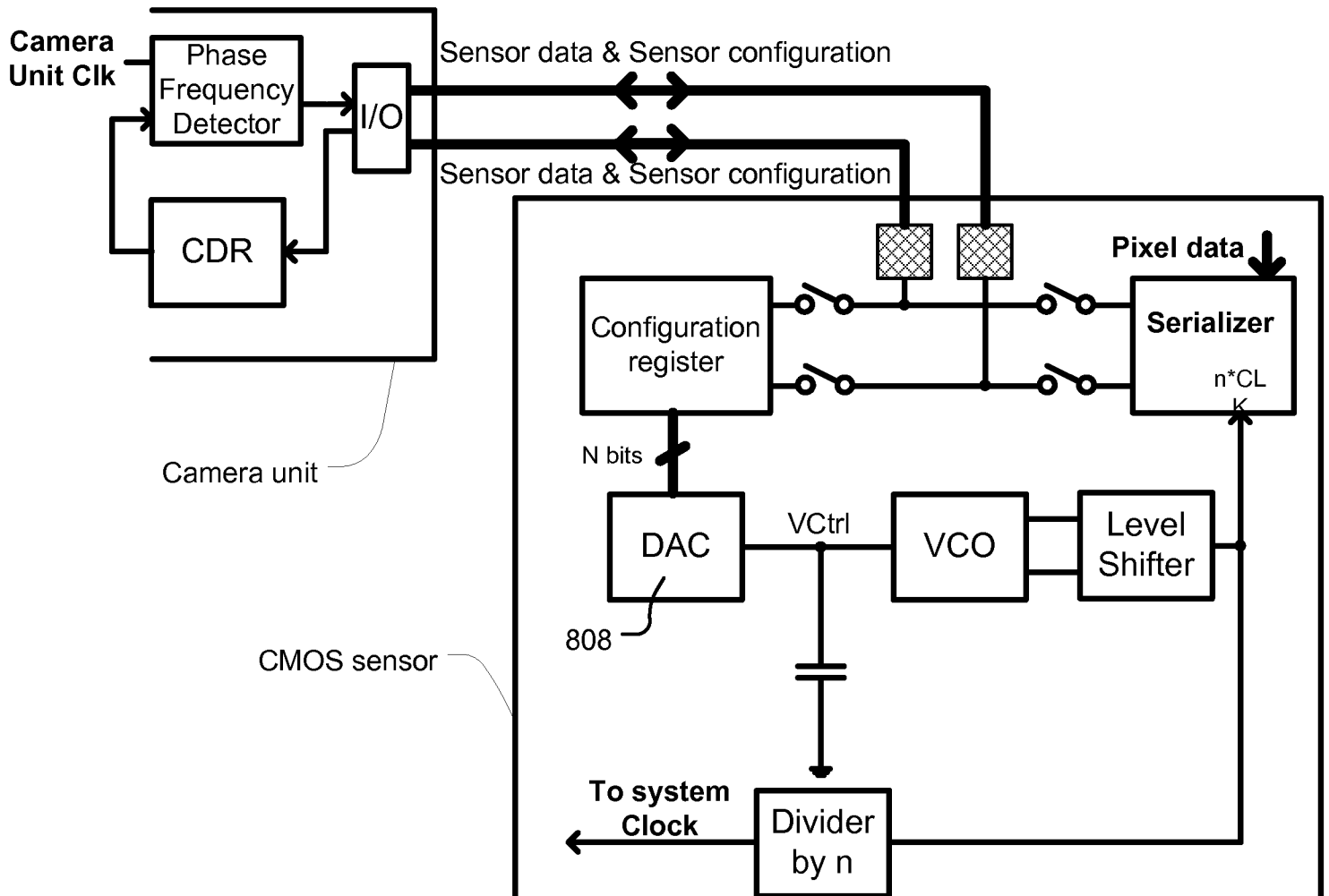


FIG. 8

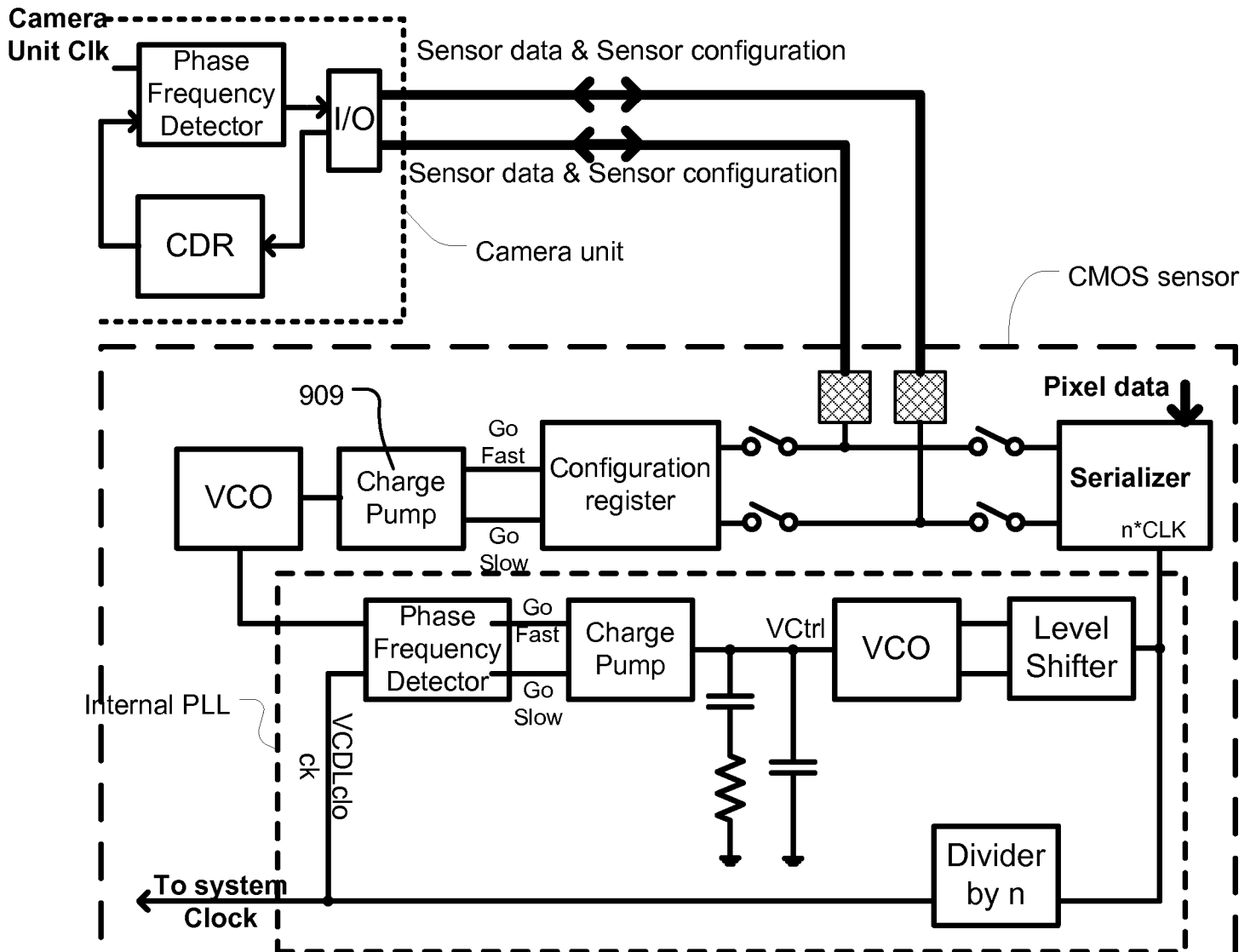


FIG. 9

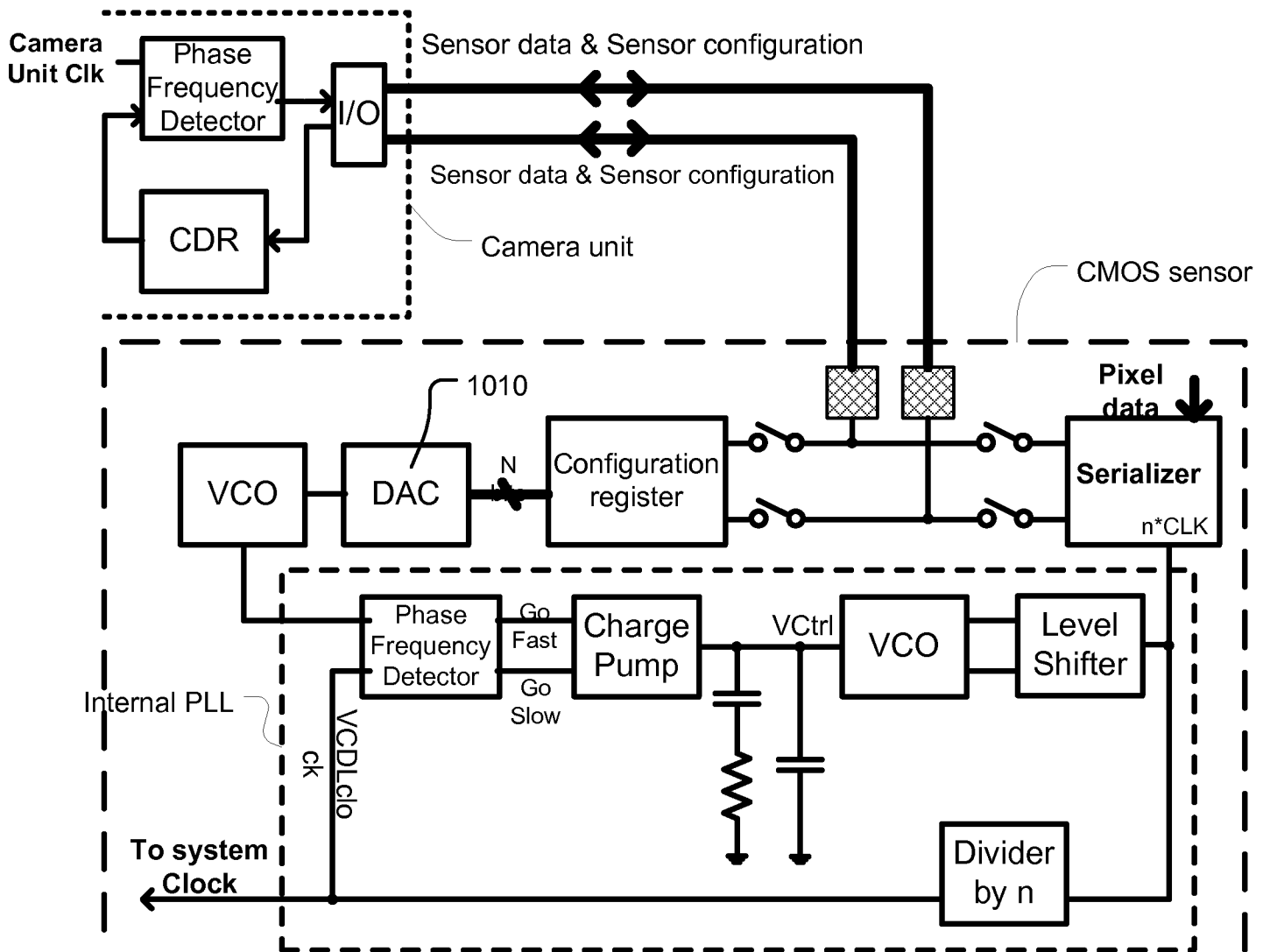


FIG. 10

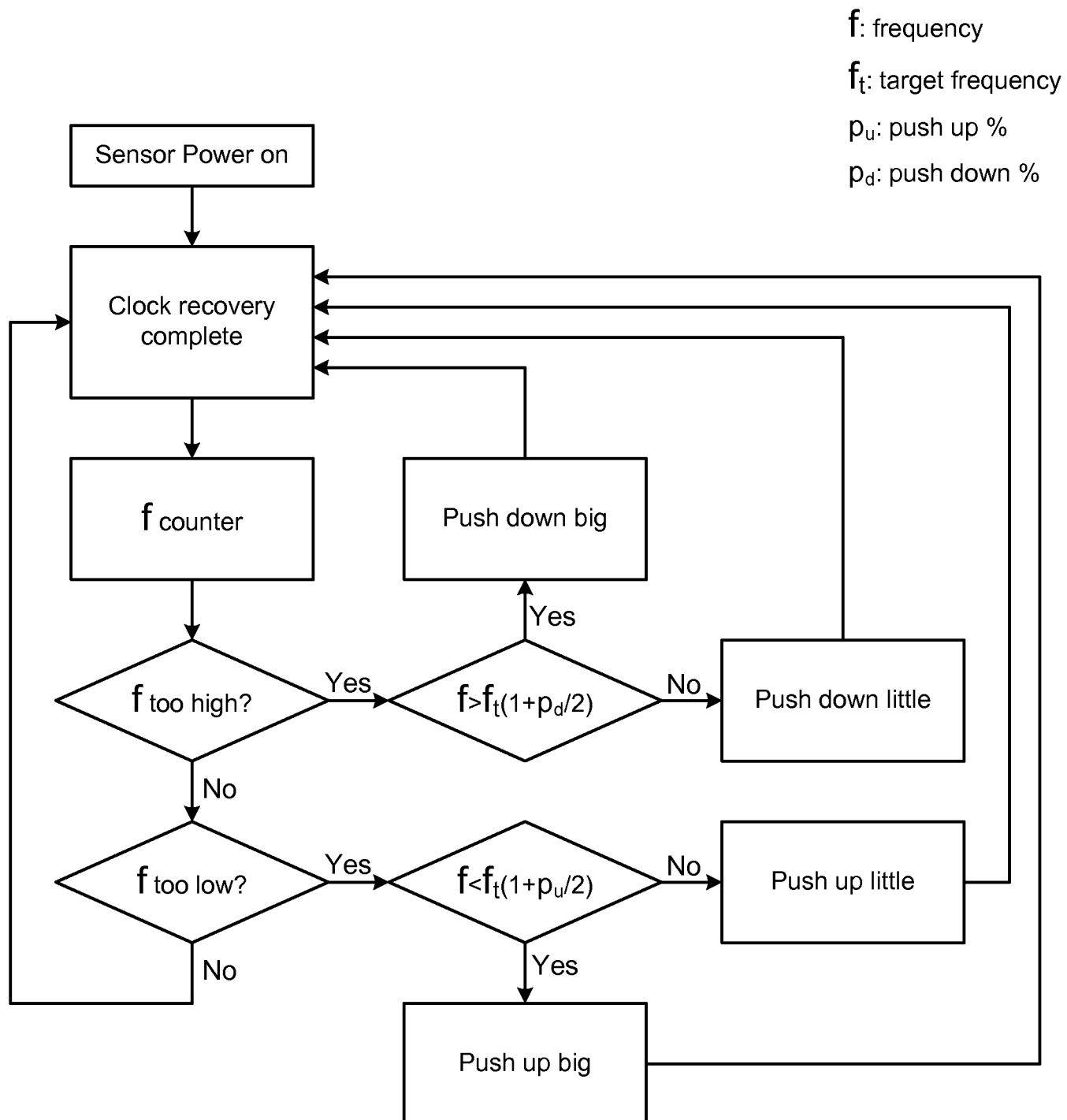


FIG. 11

R_CLK	I	Recovered Clock. This is the input from the clock and data recovery (CDR)
REF_CLK	I	Reference Clock. This is the input from the known reference clock
CTL	I	Control inputs from the supervisory software. This sets the big and little push thresholds as well as the target frequency
PUSH	O	0: don't push the frequency, 1: push the frequency
UP_DOWN	O	0: if PUSH then push down, 1: if PUSH then push up
BIG_LITTLE	O	0: if PUSH then push a little, 1: if PUSH then push big

FIG. 12

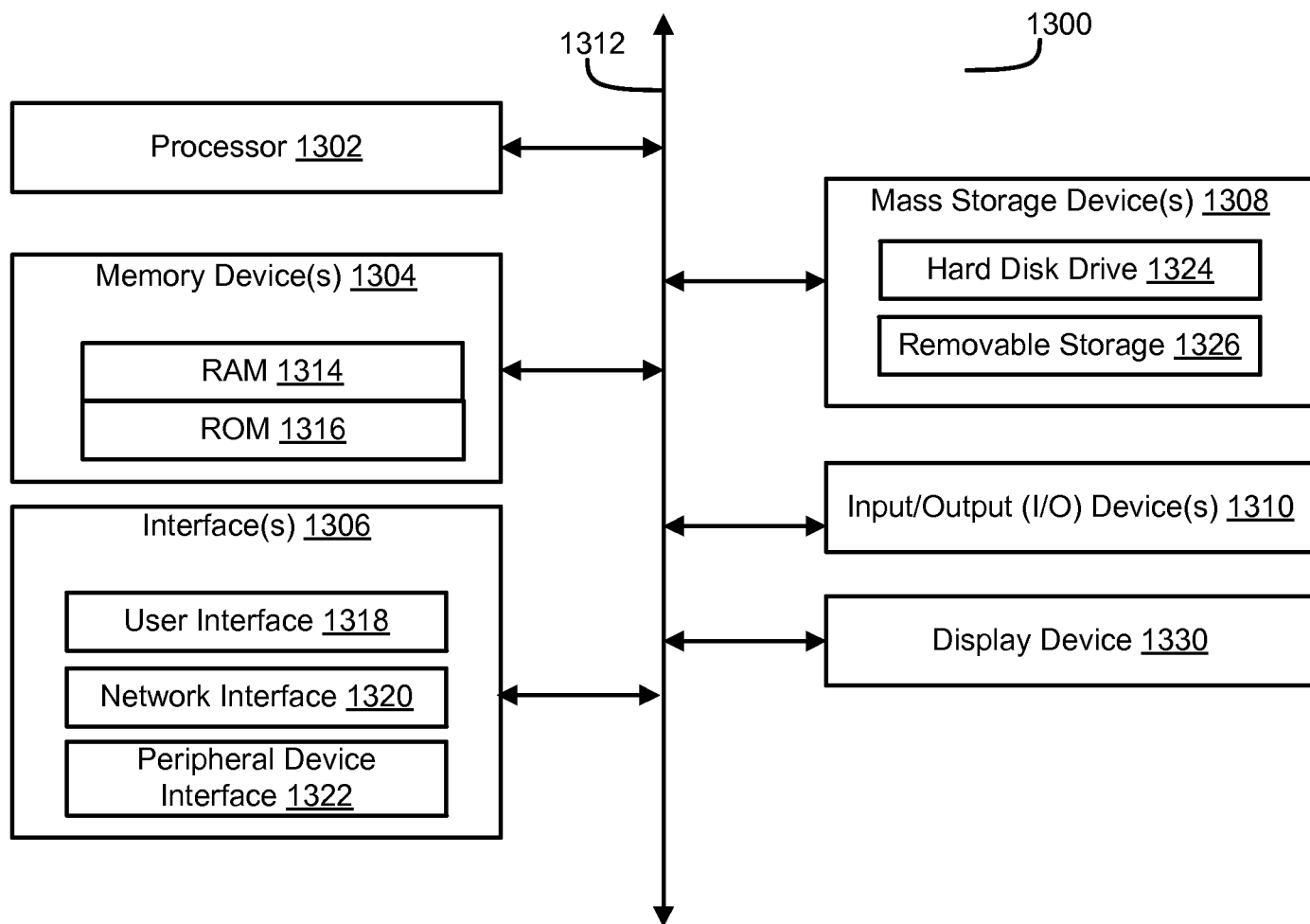


FIG. 13

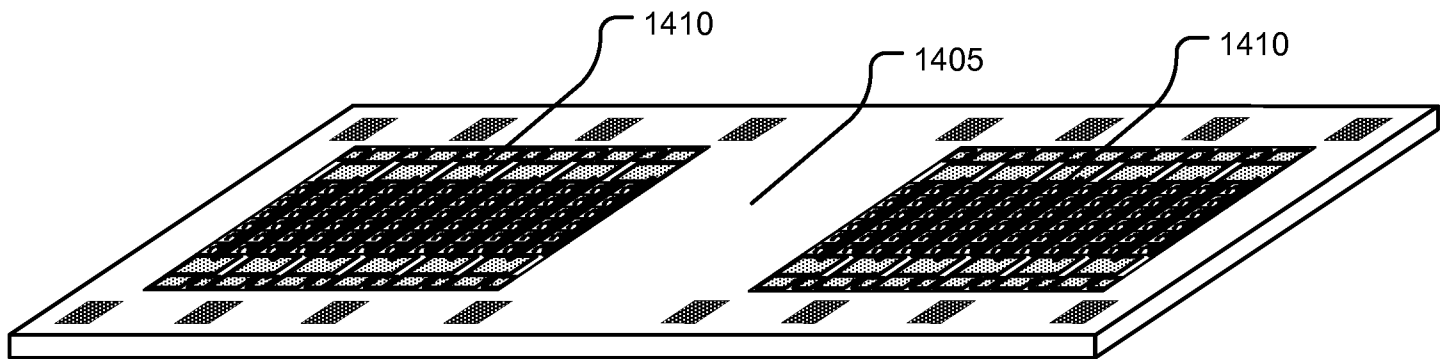


FIG. 14A

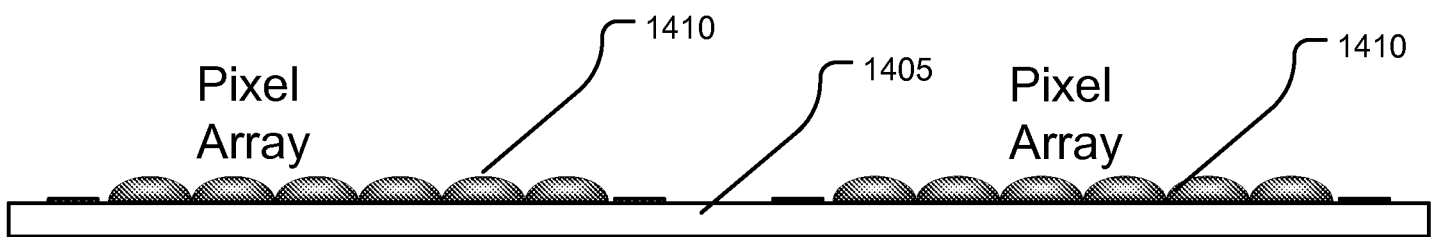


FIG. 14B

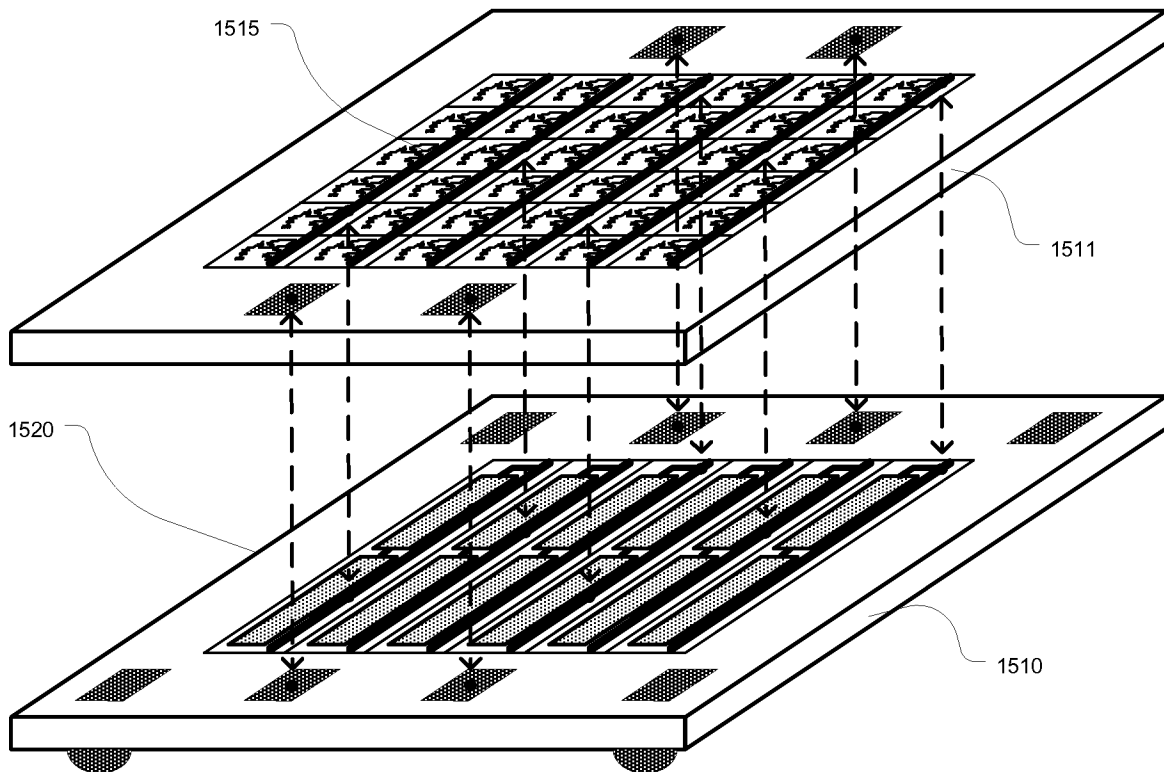


FIG. 15B

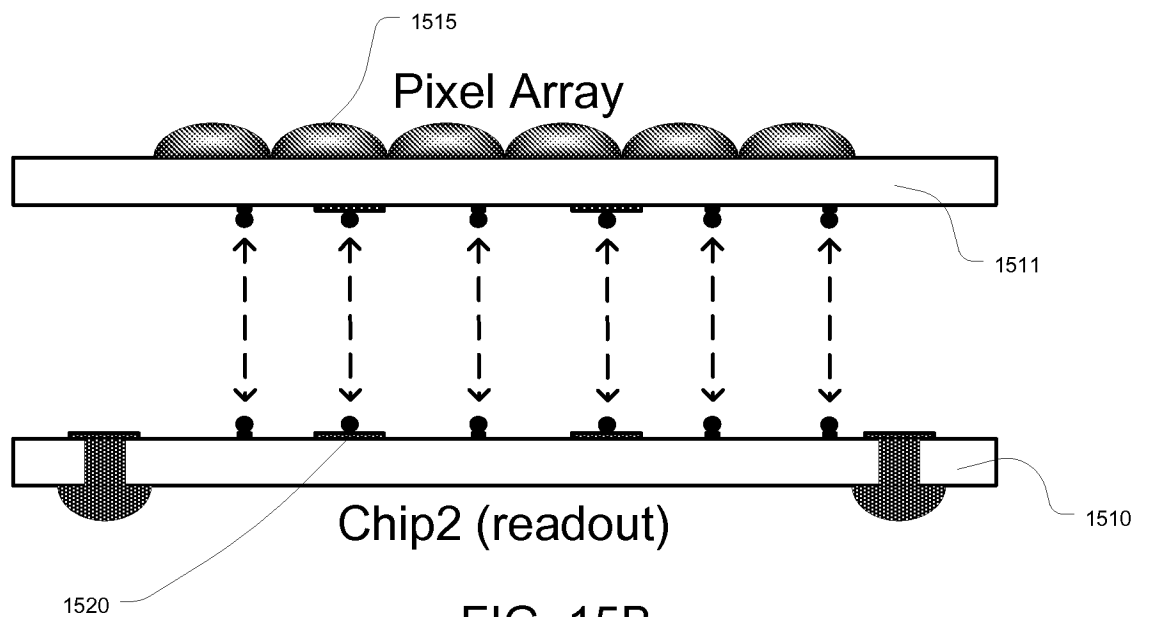


FIG. 15B

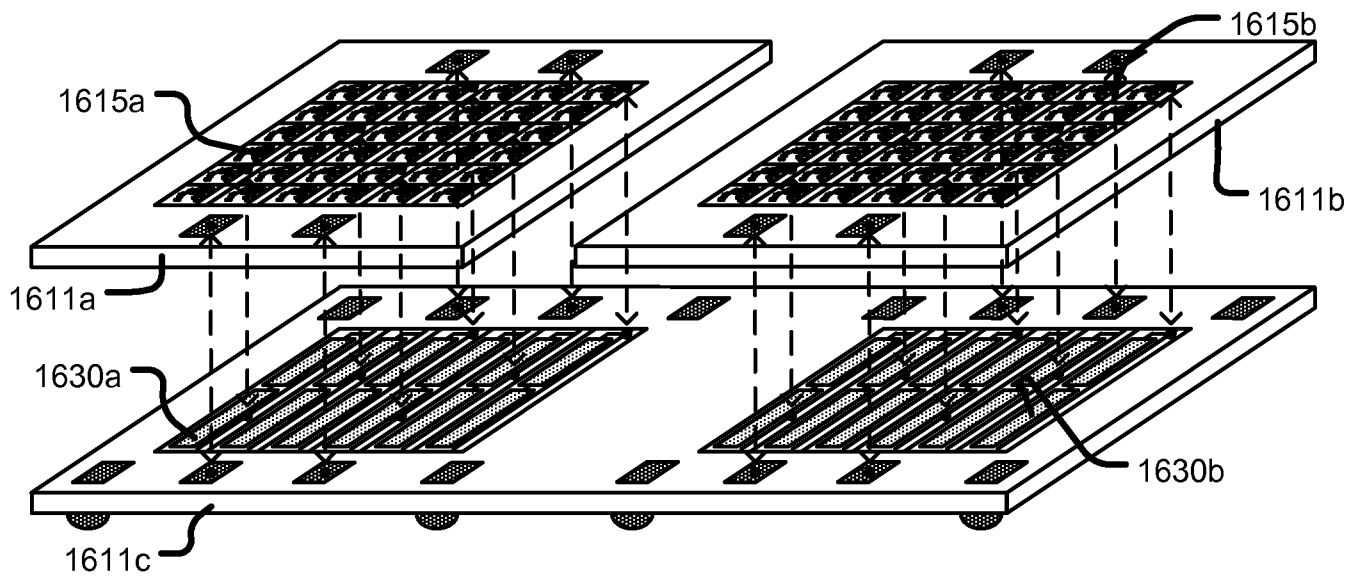


FIG. 16A

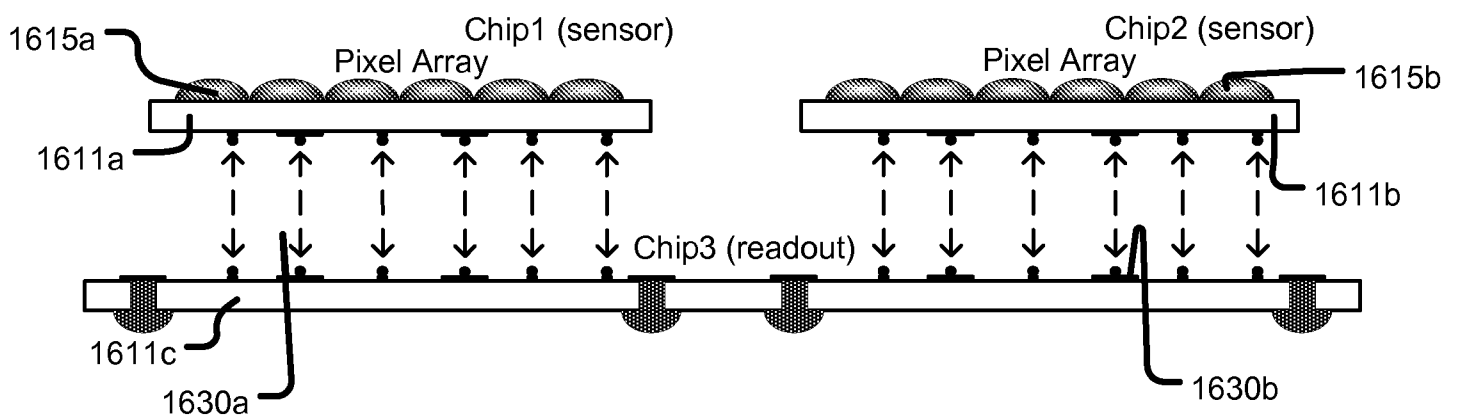


FIG. 16B

INTERNATIONAL SEARCH REPORT

International application No. -----

PCT/US2014/029970

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - A61B 1/04 (2014.01)

USPC - 600/109

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - A61B 1/00, 1/04, 1/06, 1/07; H04N 7/18 (2014.01)

USPC - 348/68, 76, 600/101, 109, 112, 114

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

CPC - A61B 1/04, 1/45, 1/96; H04N 2005/2255, 5/2259 (2014.02)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Orbit, Google Patents, Google Scholar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012/0307030 A1 (BLANQUART) 06 December 2012 (06.12.2012) entire document	1-22
A	US 2012/0035434 A1 (FERREN et al) 09 February 2012 (09.02.2012) entire document	1-22
A	US 2012/0293699 A1 (BLANQUART et al) 22 November 2012 (22.11.2012) entire document	1-22
A	US 5,187,572 A (NAKAMURA et al) 16 February 1993 (16.02.1993) entire document	1-22

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 July 2014

Date of mailing of the international search report

19 AUG 2014

Name and mailing address of the ISA/US

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