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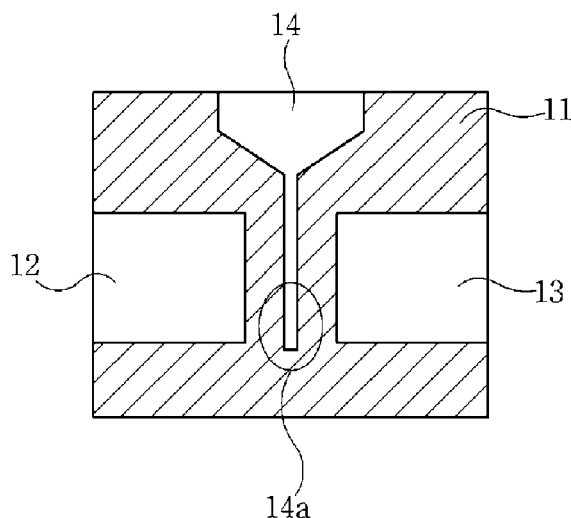
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[Continued on next page]

(54) Title: PLANAR GATE-CONTROLLED ELEMENT AND METHOD FOR FABRICATING THE SAME

[Fig. 1]



(57) Abstract: A planar gate-controlled element and a method for fabricating the same that can facilitate the fabrication of a semiconductor device, such as an organic transistor or a biosensor, which is controlled by a gate electrode. Since source, drain, and gate electrode are formed in the same plane over a substrate, the organic transistor or biosensor can be realized in a simple manner by a process of forming an active layer over the source, drain, and gate electrodes. In addition, it is also possible to use organic matter or a biological substance that is vulnerable to heat.



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Description

PLANAR GATE-CONTROLLED ELEMENT AND METHOD FOR FABRICATING THE SAME

Technical Field

- [1] The present invention relates to a gate electrode-controlled semiconductor element that is applicable to a semiconductor device including an organic transistor, a biosensor, and a biochip, as well as to a biodevice.

Background Art

- [2] An organic transistor is a transistor that has an active layer made of organic matter. Like silicon-based transistors, the organic transistor can control the amount of current flowing between a source electrode and a drain electrode according to the amount of voltage or current applied to a gate electrode.
- [3] A biosensor is a semiconductor element that has been proposed to detect or identify an analyte (i.e., a type of chemical substance) based on the substrate specificity of an enzyme or on an antigen-antibody reaction in which biological substances strongly react with a specific substance. Biosensors are used in medical fields to detect the amount of urea in the urine; in the food industry to detect alcohol produced during the manufacture of foods, to measure organic acids, and to evaluate the freshness of fish meat; and in environmental fields to detect environmental pollutants or the like in wastewater or rivers. The biosensor fixes organic matter such as Deoxyribonucleic Acids (DNAs), proteins, enzymes, antigens, antibodies, hormones, microorganisms, cells, and the like to an electrode so that a computer can read a reaction to a specific chemical substance.
- [4] Both the organic transistor and biosensor are semiconductor elements that are controlled by a gate electrode. In order to fabricate such an element, it is necessary to carry out procedures of coating an active layer made of organic matter or a biological substance over a substrate and then depositing an electrode-forming metal over the active layer. In particular, in order to complete the element, a procedure of forming a metal electrode using thermal deposition, sputtering, electron beams, or the like has to be performed two or more times.
- [5] However, the metal deposition limits the use of organic matter or biological substances such as protein, which are vulnerable to heat.
- [6] The information disclosed in this Background of the Invention section is only for the enhancement of understanding of the background of the invention, and should not be taken as an acknowledgment or any form of suggestion that this information forms a prior art that would be already known to a person skilled in the art.

Disclosure of Invention

Technical Problem

- [7] The present invention has been devised to solve the foregoing problems with a semiconductor element that includes an active layer made of organic matter or a biological substance, such problems being related to the formation of metal electrodes after the formation of the active layer. Various aspects of the present invention provide a planar gate-controlled element and a method for fabricating the same, in which a source electrode, a drain electrode, and a gate electrode are additionally formed in the same plane.

Technical Solution

- [8] According to an aspect of the present invention, the planar gate-controlled element may include a substrate; one or more gate electrodes formed over the substrate, wherein a control voltage or a control current is applied to the gate electrodes; and source and drain electrodes formed in the same plane as the gate electrode over the substrate, wherein signals input into and output from the source and drain electrodes are controlled according to the control voltage or current applied to the gate electrodes.
- [9] The planar gate-controlled element may further include an active layer formed over the gate, source, and drain electrodes.
- [10] In the planar gate-controlled element, the substrate may be made of one selected from among glass, plastic, and metal.
- [11] In the planar gate-controlled element, the source and drain electrodes may be formed parallel to each other at a predetermined interval, and the gate electrodes may include a channel control region extending therefrom, which is positioned between the source electrode and the drain electrode, thereby adjusting a channel interval between the source and drain electrodes.
- [12] In the planar gate-controlled element, the gate electrodes may be two gate electrodes formed on both sides of the source electrode and the drain electrodes, and the source, drain, and two gate electrodes may be arranged in such a manner that the two gate electrodes oppose the source and drain electrodes about the X-shaped diagonals.
- [13] In an aspect of the present invention, the method for fabricating a planar gate-controlled element may include the following steps of forming an electrode layer over a substrate; coating a photoresist over the electrode layer; selectively exposing a portion of the photoresist to be removed using a mask, which is patterned to form a source electrode, a drain electrode, and one or more gate electrodes; exposing a portion of the electrode layer by removing the exposed portion of the photoresist using a developer solution; forming the source electrode, the drain electrode, and the gate electrodes by removing the exposed portion of the electrode layer using thin-film

etching; and stripping the remaining portion of the photoresist from the electrode.

[14] The method for fabricating a planar gate-controlled element may further include the step of forming an active layer over the substrate and the source, drain, and gate electrodes.

[15] In the method for fabricating a planar gate-controlled element, the substrate may be made of one selected from among glass, plastic, and metal.

[16] In the method for fabricating a planar gate-controlled element, the source electrode and the gate electrode may be formed parallel to each other at a predetermined interval, and the gate electrodes may include a channel control region extending therefrom, which is positioned between the source electrode and the drain electrode, thereby adjusting the channel interval between the source and drain electrodes. Alternatively, the gate electrodes may be two gate electrodes formed on both sides of the source electrode and the drain electrodes, and the source, drain, and two gate electrodes may be arranged in such a manner that the two gate electrodes oppose the source and drain electrodes about the X-shaped diagonals.

[17] According to exemplary embodiments of the present invention as set forth above, since source and drain electrodes and one or more charge-controlling gate electrodes are formed in advance in the same plane over the substrate, it is possible to fabricate a biosensor or an organic transistor, which has to be controlled by the gate electrodes, in a simple manner merely by forming an active layer over the electrodes. This can consequently exclude the complicated process of depositing metal over the active layer. Furthermore, it is also possible to advantageously form the active layer using organic matter or a biological substance such as protein, which has been difficult to use together with metal deposition since it is vulnerable to heat.

[18] The methods and apparatuses of the present invention have other features and advantages which will be apparent from, or are set forth in more detail in, the accompanying drawings, which are incorporated herein, and the following Detailed Description of the Invention, which together serve to explain certain principles of the present invention.

Brief Description of Drawings

[19] FIG. 1 is a top plan view showing the structure of a planar gate-controlled element according to one exemplary embodiment of the invention;

[20] FIG. 2 is a photograph of a planar gate-controlled element realized according to the structure shown in FIG. 1;

[21] FIG. 3 is a top plan view showing the structure of a planar gate-controlled element according to another exemplary embodiment of the invention;

[22] FIG. 4 is a photograph of a planar gate-controlled element realized according to the

structure shown in FIG. 3;

[23] FIG. 5 is a cross-sectional view showing a first application example of a planar gate-controlled element according to the invention;

[24] FIG. 6A is a graph showing the variation of current with respect to gate voltage in the element shown in FIG. 5;

[25] FIG. 6B is a graph showing the variation of current with respect to drain voltage in the element shown in FIG. 5;

[26] FIG. 7 is a cross-sectional view showing a second application example of a planar gate-controlled element according to the invention;

[27] FIG. 8A is a graph showing the variation of current with respect to gate voltage in the element shown in FIG. 7; and

[28] FIG. 8B is a graph showing the variation of current with respect to drain voltage in the element shown in FIG. 7.

Best Mode for Carrying out the Invention

[29] Reference will now be made in detail to various exemplary embodiments of the present invention(s), examples of which are illustrated in the accompanying drawings and described below. While the invention(s) will be described in conjunction with exemplary embodiments, it will be understood that the present description is not intended to limit the invention(s) to those exemplary embodiments. On the contrary, the invention(s) is/are intended to cover not only the exemplary embodiments, but also various alternatives, modifications, equivalents and other embodiments that may be included within the spirit and scope of the invention as defined by the appended claims.

[30] In the following description of the present invention, detailed descriptions of known functions and components incorporated herein will be omitted when they may make the subject matter of the present invention unclear.

[31] Throughout this document, reference should be made to the drawings, in which the same reference numerals and signs are used throughout the different drawings to designate the same or similar components.

[32] In addition, throughout this specification and the claims that follow, it will be understood that when an element is referred to as being “connected to” or “coupled to” another element, not only can it be “directly connected or coupled to” the other element; it can also be “indirectly connected or coupled to” the other element via an intervening element. Unless explicitly described to the contrary, the word “comprise” and its variations, such as “comprises” or “comprising” will be understood to imply the inclusion of stated elements but not the exclusion of any other elements.

[33]

- [34] FIG. 1 is a top plan view showing the structure of a planar gate-controlled element according to one exemplary embodiment of the invention.
- [35] Referring to FIG. 1, the planar gate-controlled element of this embodiment includes a source electrode 12, a drain electrode 13, and a gate electrode 14, which are formed in the same plane on a substrate 11. The source and drain electrodes 12 and 13 are disposed to oppose each other with a predetermined interval between them. The gate electrode 14 includes a channel control region 14a extending therefrom. The channel control region 14a is positioned between the source and drain electrodes 12 and 13, thereby adjusting the channel interval between the source and drain electrodes 12 and 13.
- [36] The substrate 11 is made of glass, metal, or plastic.
- [37] In the planar gate-controlled element having the above-described structure, it is possible to variously modify the shape and size of the gate electrode 14 and the channel control region 14a, and thereby control the channel interval between the source and drain electrodes 12 and 13. In addition, the gate, source, and drain electrodes can be made from a conductive oxide, examples of which may include Indium Tin Oxide (ITO), zinc oxide, tin oxide, and the like.
- [38] FIG. 2 is a photograph of an actual planar gate-controlled element, which is realized according to the structure shown in FIG. 1.
- [39] Next, FIG. 3 is a top plan view showing the structure of a planar gate-controlled element according to another exemplary embodiment of the invention.
- [40] Referring to FIG. 3, the planar gate-controlled element of this embodiment includes a source electrode 32, a drain electrode 33, and two gate electrodes 34 and 35, which are present together in the same plane on a substrate 31. The source electrode 32, the drain electrode 33, and the two gate electrodes 34 and 35 are arranged in such a manner that the two gate electrodes 34 and 35 oppose the source and drain electrodes 32 and 33 about the X-shaped diagonals.
- [41] In this case, channels can be activated in both directions to the source and drain electrodes 32 and 33 through the two gate electrodes 34 and 35.
- [42] FIG. 4 is a photograph of an actual planar gate-controlled element, which is realized according to the structure shown in FIG. 3.
- [43] As described above, in the planar gate-controlled element according to the foregoing exemplary embodiments of the invention, the source electrode 12, 32, the drain electrode 13, 33, and one or more gate electrodes 14, 34 and 35 are formed together in the same plane on the substrate 11, 31. Thus, it is possible to realize an organic transistor or a biosensor in a simple matter merely by performing a process of forming an active layer made of organic matter or a biomaterial over the source electrode 12, the drain electrode 13, and the gate electrode 14, or over the source electrode 32, the

drain electrode 33, and the gate electrodes 34 and 35.

[44] Accordingly, it is possible to form an active layer using organic matter or a biological substance such as protein, which has been difficult to use together with the metal deposition in the related art since it is vulnerable to heat. This can consequently increase the usefulness of organic matter and biological substances.

[45] The planar gate-controlled element according to any of the foregoing exemplary embodiments of the invention as illustrated above can be fabricated by a method including the following steps of: forming an electrode layer over a substrate; coating a photoresist over the electrode layer; selectively exposing a portion of the photoresist to be removed using a mask, which is patterned in the form of a source electrode, a drain electrode, and one or more gate electrodes; exposing a portion of the electrode layer by removing the exposed portion of the photoresist using a developer solution; forming the source, drain, and one or more gate electrodes by removing the exposed portion of the electrode layer; and removing the remaining portion of the photoresist from the electrode. In addition, the method can also include the step of forming an active layer over the source, drain, and one or more gate electrodes.

[46]

[47] FIGS. 5 and 7 show application examples of planar gate-controlled elements according to respective exemplary embodiments of the invention. With reference to FIGS. 5 and 7, the method for fabricating a planar gate-controlled element according to exemplary embodiments of the invention will be described in more detail.

[48] The element shown in FIG. 5 is fabricated according to the following process. First, an electrode layer is formed with a predetermined thickness over a glass substrate 51. The electrode layer is made of, for example, Indium Tin Oxide (ITO). The electrode layer is formed by applying the ITO with a predetermined thickness over the glass substrate 51, followed by cleaning and then pre-baking to remove moisture.

[49] Afterwards, a photoresist (not shown) is applied with a uniform thickness over the electrode layer, followed by soft-baking to remove solvent, and a portion of the photoresist to be removed is exposed through a mask, which is patterned in the form of the source, drain, and gate electrodes as shown in FIGS. 1 and 2. Next, the portion of the electrode layer to be removed is exposed by selectively removing the exposed portion of the photoresist using a developer solution. Afterwards, hard-baking is performed in order to increase the bonding force of the photoresist, the exposed portion of the electrode layer is removed using etchant, and the remaining portion of the photoresist is removed. Then, as shown in FIG. 5, a source electrode 52, a drain electrode 53, and a gate electrode 54 are formed in the same plane.

[50] Afterwards, an active layer 55 made of Poly 3-Hexylthiophene (P3HT) is formed by spin-coating P3HT with a predetermined thickness, followed by evaporating solvent at

50 °C for 15 minutes.

- [51] FIGS. 6A and 6B are graphs showing the quantities of variation of current with respect to gate and drain voltages in an element realized as shown in FIG. 5. As shown in FIGS. 6A and 6B, it can be seen that a drain current I_{ds} varies according to a gate voltage V_g applied to the gate electrode 54 or a drain voltage V_{ds} applied to the drain electrode 53. From this, it can be understood that the planar gate-controlled element according to an exemplary embodiment of the invention can be controlled through the gate electrode 54.
- [52] Next, the element shown in FIG. 7 is fabricated by forming source, drain, and gate electrodes 72, 73, and 74 over a glass substrate 71 by the same fabrication process as above, and forming an active layer 75 by coating Horseradish Peroxidase (HP) over the source, drain, and gate electrodes 72, 73, and 74.
- [53] FIGS. 8A and 8B are graphs showing the quantities of variation of current with respect to drain and gate voltages in an element realized as shown in FIG. 7. It can be seen that a drain current I_d varies according to the drain voltage V_d or the gate voltage V_g . From this, it can be understood that the planar gate-controlled element can be controlled through the gate electrode 74.
- [54]
- [55] An aspect of the present invention also provides a field effect transistor by forming an insulating layer over the planar gate-controlled element.
- [56] A conventional organic field effect transistor is fabricated by forming a gate electrode over a substrate, forming an insulating layer over the gate electrode, forming an active layer over the insulating layer, and then forming source and drain electrodes over the active layer. However, the field effect transistor according to an exemplary embodiment of the invention is fabricated by forming all of source, drain, and gate electrodes in the same plane, forming an insulating layer around only the gate electrode, and then forming an active layer over the source, drain, and gate electrodes. The advantage is that it can be realized by forming only the insulating layer and the active layer without undergoing complicated processes, unlike conventional approaches.
- [57] This is because, when a voltage is applied to the gate electrode, an electric charge is induced between the active layer and the insulating layer due to electric field effect caused by the gate voltage, and the induced electric charge flows between the source and the drain.
- [58] The field effect transistor can be fabricated by depositing a material intended to function as an insulating layer over the planar gate-controlled element produced by the above-described process, and forming an active layer made of organic matter or a biological substance (e.g. protein and DNA) over the element, over which the insulating

layer has been deposited.

[59]

[60] Below, the present invention will be described more fully with reference to Example and Experimental Examples.

[61] However, it should be understood that Example and Experimental Examples below illustrate, but by no means limit, the present invention.

Mode for the Invention

[62] Example 1: Fabrication of Planar Gate-Controlled Element

[63] An ITO layer deposited with a uniform thickness over a glass substrate was cleaned, followed by preheating (at about 100°C for about 100 seconds) in order to remove moisture, and then a photosensitizer was applied with a uniform thickness over the ITO-deposited substrate. Heating was performed again at about 100°C for 100 about seconds to remove residual solvent from the photosensitizer. A pattern mask was exposed to light, and the portion of the photosensitizer exposed to light was selectively removed using a developer solution. Afterwards, the substrate was heated at 250 °C for about 2 minutes in order to increase the bonding force of the remaining photo-sensitizer. A pattern was formed in the ITO layer using an etchant solution, and then the remaining photosensitizer was removed, thereby producing a planar gate-controlled element having the pattern.

[64]

[65] Experimental Example 1: Measurement of Variation of Current in Planar Gate-Controlled Element on Which Polymer Material is Applied

[66] Experimental Example using a planar gate-controlled element is as follows: Poly 3-Hexylthiophene (P3HT) was spin-coated with a thickness of about 55 nm over the planar gate-controlled element, followed by evaporating solvent at 50 °C for about 15 minutes. Gate voltage (V_g), drain voltage (V_d), and drain current (I_d) were measured from the planar gate-controlled element, on which P3HT was deposited, using a measuring instrument (Keithley SCS-4200). The results are reported in FIGS. 6A and 6B as below.

[67] As seen in FIGS. 6A and 6B, it can be appreciated that almost no current flowed when the gate voltage was 0 and the drain voltage increased when the gate voltage increased negatively from zero. It can also be appreciated that the amount of current was limited according to a given amount of drain voltage.

[68]

[69] Experimental Example 2: Measurement of Variation of Current in Planar Gate-Controlled Element on Which Polymer Material is Applied

[70] Horseradish Peroxidase (HRP) was coated over a planar gate-controlled element.

Gate voltage (V_g), drain voltage (V_{ds}), and drain current (I_{ds}) were measured from the planar gate-controlled element, on which HRP is deposited, using a measuring instrument (Keithley SCS-4200). The results are reported in FIGS. 8A and 8B as below.

[71] As seen in FIGS. 8A and 8B, it can be appreciated that almost no current flowed when the gate voltage was 0 and the drain voltage increased when the gate voltage increased negatively from zero. It can also be appreciated that the amount of current was limited according to a given amount of drain voltage.

[72]

[73] While the present invention has been shown and described with reference to certain exemplary embodiments thereof and the accompanying drawings, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the appended claims and their equivalents.

[74]

Industrial Applicability

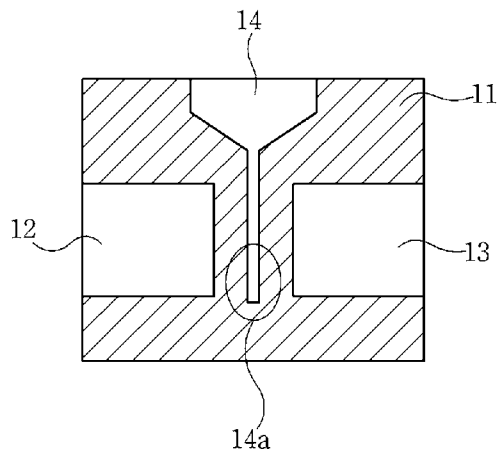
[75] The present invention can be applied to a gate-controlled semiconductor element such as an organic transistor and a biosensor. It is possible to realize the organic transistor and the biosensor by a simple process of forming an active layer over a source electrode, a drain electrode, and one or more gate electrodes. Furthermore, it is also possible to increase the application of organic matter or a biological substance such as protein, which has been difficult to use together with metal deposition in the related art since it is vulnerable to heat.

Claims

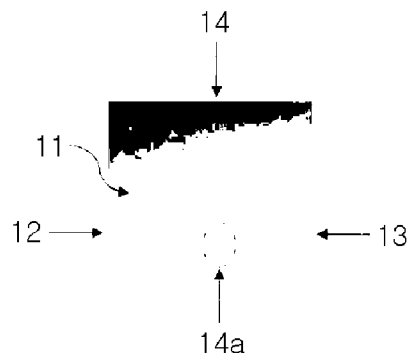
- [1] A planar gate-controlled element comprising:
a substrate;
one or more gate electrodes formed over the substrate, wherein a control voltage or a control current is applied to the gate electrodes; and
source and drain electrodes formed in the same plane as the gate electrode over the substrate, wherein signals input into and output from the source and drain electrodes are controlled according to the control voltage or current applied to the gate electrodes.
- [2] The planar gate-controlled element according to claim 1, further comprising an active layer formed over the gate, source, and drain electrodes.
- [3] The planar gate-controlled element according to claim 1, wherein the substrate is made of one selected from the group consisting of glass, plastic, and metal.
- [4] The planar gate-controlled element according to claim 1, wherein the source and drain electrodes are formed parallel to each other at a predetermined interval.
- [5] The planar gate-controlled element according to claim 1, wherein the gate electrodes include a channel control region extending therefrom, wherein the channel control region is positioned between the source electrode and the drain electrode, thereby adjusting a channel interval between the source and drain electrodes.
- [6] The planar gate-controlled element according to claim 1, wherein the gate electrodes comprise two gate electrodes formed on both sides of the source electrode and the drain electrodes,
wherein the source, drain, and two gate electrodes are arranged in such a manner that the two gate electrodes oppose the source and drain electrodes about the X-shaped diagonals.
- [7] A method for fabricating a planar gate-controlled element, comprising:
forming an electrode layer over a substrate;
coating a photoresist over the electrode layer;
selectively exposing a portion of the photoresist to be removed using a mask, which is patterned to form a source electrode, a drain electrode, and one or more gate electrodes;
exposing a portion of the electrode layer by removing the exposed portion of the photoresist using a developer solution;
forming the source electrode, the drain electrode, and the gate electrodes by removing the exposed portion of the electrode layer using thin-film etching; and
stripping a remaining portion of the photoresist from the electrode.

- [8] The method according to claim 7, further comprising forming an active layer over the substrate and the source, drain, and gate electrodes.
- [9] The method according to claim 7, wherein the substrate is made of one selected from the group consisting of glass, plastic, and metal.
- [10] The method according to claim 7, wherein the source electrode and the gate electrode are formed in parallel to each other at a predetermined interval, and the gate electrodes include a channel control region extending therefrom, the channel control region positioned between the source electrode and the drain electrode, thereby adjusting the channel interval between the source and drain electrodes.
- [11] The method according to claim 7, wherein the gate electrodes comprise two gate electrodes formed on both sides of the source electrode and the drain electrodes, wherein the source, drain, and two gate electrodes are arranged in such a manner that the two gate electrodes oppose the source and drain electrodes about the X-shaped diagonals.
- [12] A field effect transistor comprising one or more insulating layers formed over gate electrodes of a planar gate-controlled element as described in any one of the preceding claims 1 to 6.

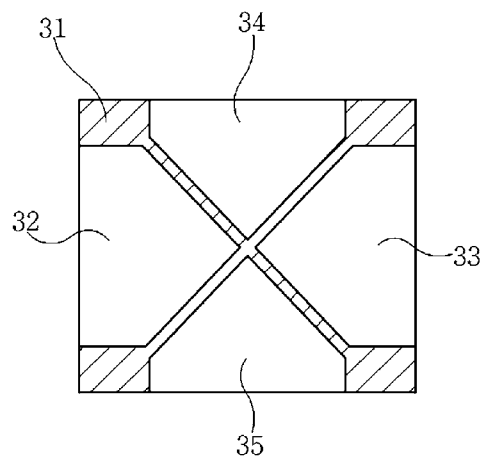
[Fig. 1]



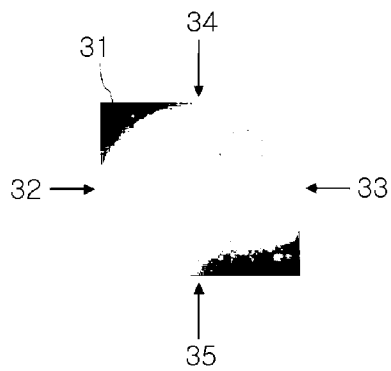
[Fig. 2]



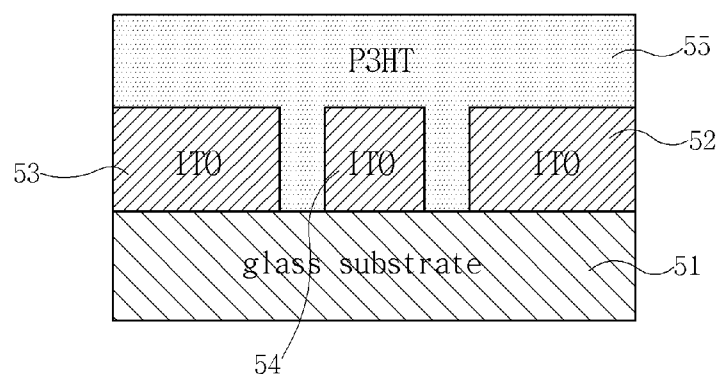
[Fig. 3]



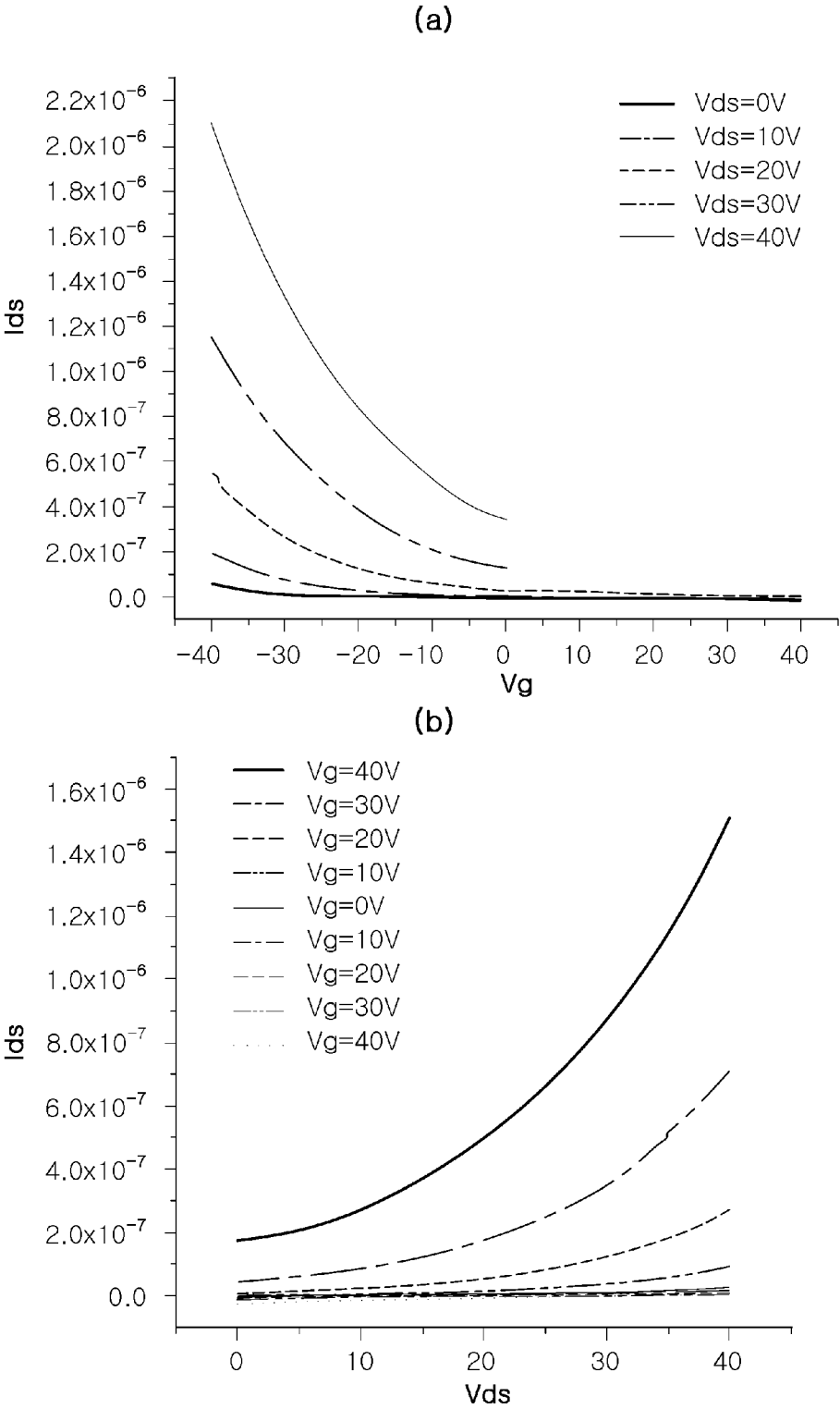
[Fig. 4]



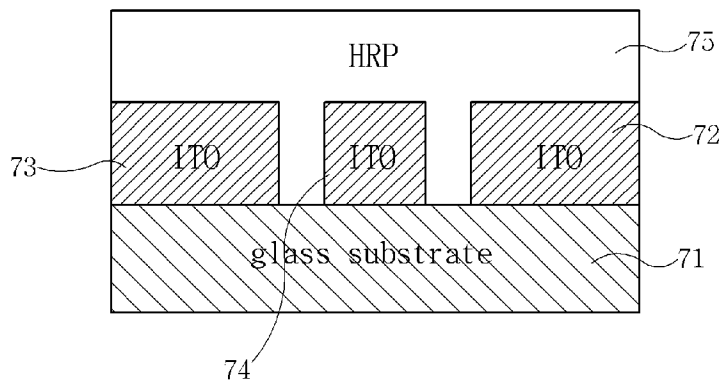
[Fig. 5]



[Fig. 6]



[Fig. 7]



[Fig. 8]

