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Urade et al.

[11] **3,803,585**

[45] **Apr. 9, 1974**

[54] **PLASMA DISPLAY PANEL DRIVING SYSTEM**

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[30] **Foreign Application Priority Data**

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[52] **U.S. Cl.** ... **340/324 M,** 315/169 R, 340/166 EL

[51] **Int. Cl.** **G08b 5/36**

[58] **Field of Search** ..... 340/324 M, 166 EL; 315/169 R, 169 TV

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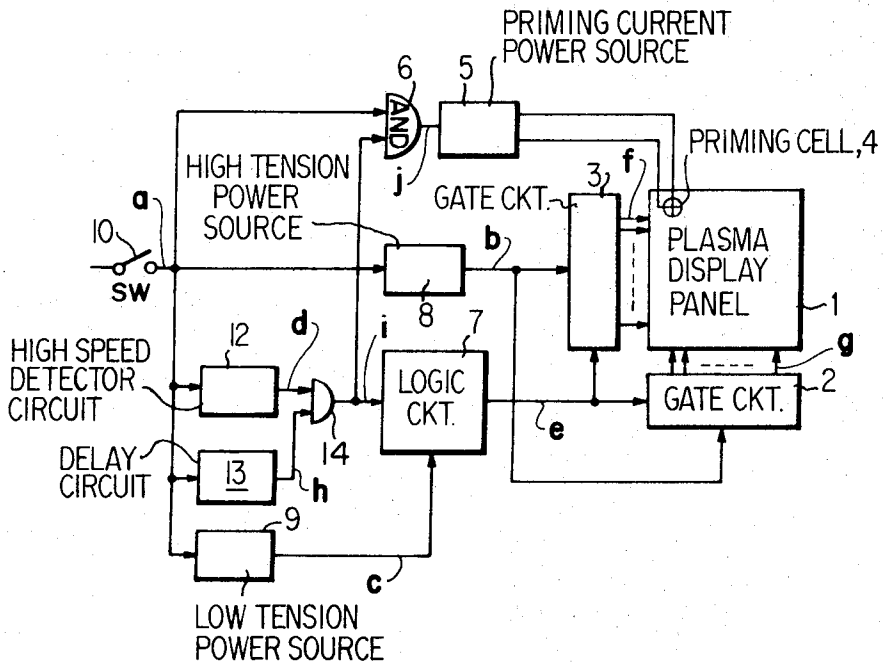
[57] **ABSTRACT**

A plasma display panel driving system in which, at the time of interrupting a power source, the operation of a control logic circuit is stopped before an output voltage from a sustain voltage power source becomes attenuated and, at the time of applying the power source, the operation of the control logic circuit is started after the output voltage from the sustain voltage power source is established, whereby a voltage similar to an erasing pulse is prevented from impression to the plasma display panel, thereby permitting a wall charge pattern to remain alive for a relatively long time.

4 Claims, 4 Drawing Figures



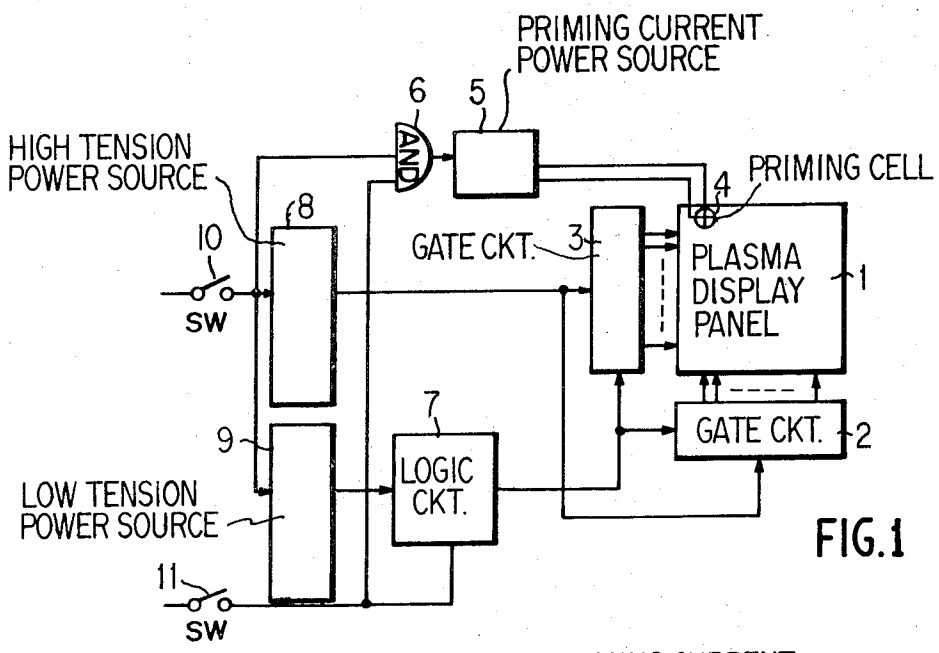

PRIMING CURRENT POWER SOURCE
6
5
AND
HIGH TENSION POWER SOURCE
PRIMING CELL
4
8
10
GATE CKT.
3
PLASMA DISPLAY PANEL
1
SW
7
9
LOGIC CKT.
GATE CKT.
2
LOW TENSION POWER SOURCE
11
SW

FIG.1

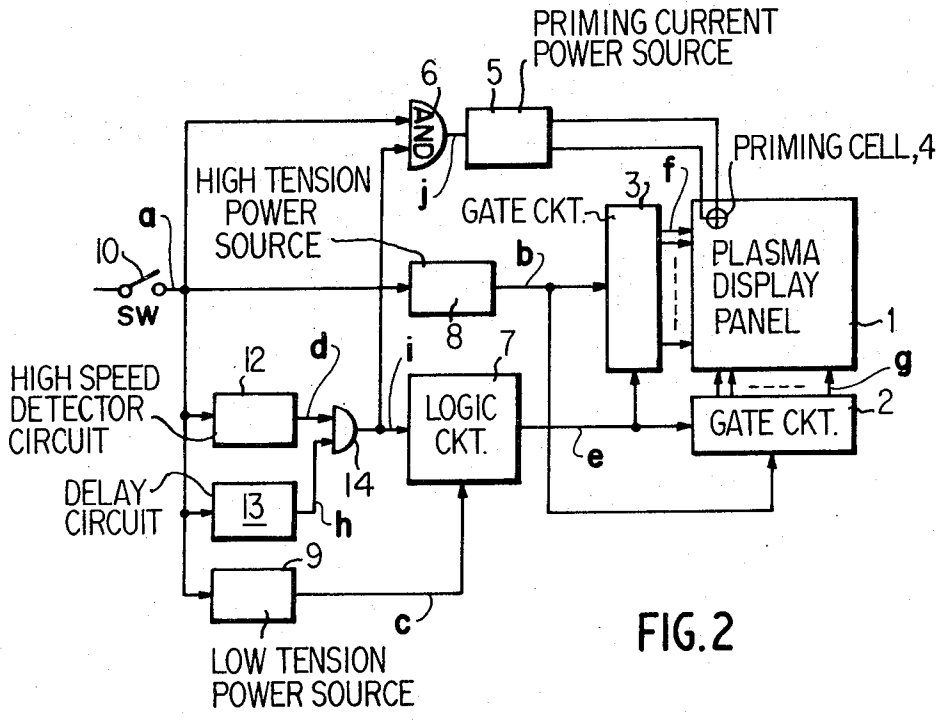

PRIMING CURRENT POWER SOURCE
6
5
AND
PRIMING CELL,4
HIGH TENSION POWER SOURCE
j
GATE CKT.
3
f
a
10
SW
b
8
PLASMA DISPLAY PANEL
1
12
d
i
7
g
HIGH SPEED DETECTOR CIRCUIT
LOGIC CKT.
GATE CKT.
2
e
DELAY CIRCUIT
13
14
h
9
c
LOW TENSION POWER SOURCE

FIG.2

FIG.3

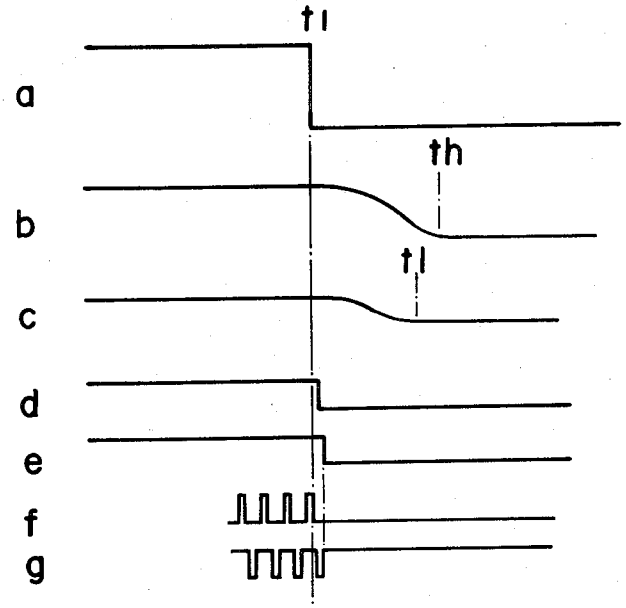
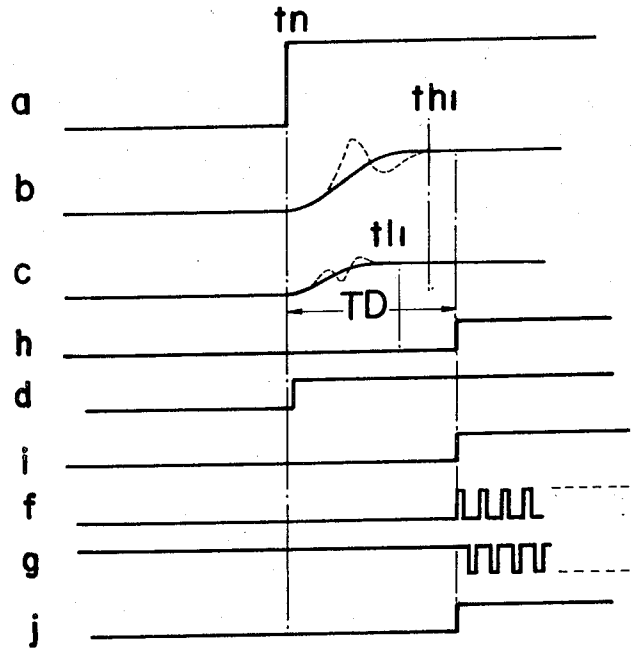


FIG.4



PLASMA DISPLAY PANEL DRIVING SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a plasma display panel driving system which allows information memorized by wall charges to remain alive for a relatively long period of time.

2. Description of the Prior Art

In a plasma display panel, electrodes are covered with dielectric layers are disposed opposite to each other with a discharge gas space defined therebetween and a charge produced by a discharge is stored on the dielectric layers to provide a memory function as well as a display function. The charge stored on the dielectric layer, that is, the so-called wall charge discharges or attenuates a period in the order of a millisecond and cannot be stored for several hours or several days as in a charge storage tube. For example, in order to reproduce a wall charge pattern before it becomes extinguished, it is necessary to impress an alternating sustain voltage of at least about 1KHz and as the repetitive frequency of the sustain voltage is reduced, the memory content becomes thinner. This attenuation is believed to result from the fact that the wall charge leaks due to the surface resistance of the dielectric layer and scatters in the discharge gas space in the intervals of discharge.

However, it has recently been found that even if such a conventional plasma display panel as mentioned above is used, the wall charge pattern can be retained for several hours or several days. This is obtained by removing the influence of a transient phenomenon occurring at the times of connecting and disconnecting the power source. For example, in a conventional driving system, transient phenomena occur depending on the time constants of the sustain voltage source and a logic circuit at the time of connecting and disconnecting in the sustain voltage sources, by which the plasma display panel is caused to operate as if impressed with an erasing pulse of low voltage or small pulse width. Further, there is a statistical tendency of firing being delayed at the time of connecting a firing voltage power source, so that a sustain voltage is impressed before a necessary amount of initial space charge for usual firing is provided. As a result of this, electrons loosely bounded with the dielectric layer are released in the discharge gas space due to field emission and these electrons cause an electron avalanche, resulting in neutralization of the wall charge by several to some dozen cycles of the sustain voltage.

SUMMARY OF THE INVENTION

This invention has for its object to provide a plasma display panel driving system which eliminates the aforesaid cause of attenuation of the wall charge to ensure that a wall charge pattern is stored for a long time after disconnecting a power source and that the original wall charge pattern is reproduced when the power source is connected again.

The plasma display panel driving system according to this invention is characterized in that, at the time of disconnecting a power source, the operation of a control logic circuit is stopped before an output voltage from a sustain voltage power source becomes attenuated and in that, at the time of connecting the power source, the operation of the control logic circuit is started after the output voltage from the sustain voltage power source circuit has been established.

Other objects, features and disadvantages of this invention will become apparent from the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating one example of this invention;

FIG. 2 is a block diagram showing another example of this invention;

FIG. 3 shows a series of waveform diagrams, for explaining the operation of the example of FIG. 2 at the time of disconnecting a power source; and

FIG. 4 shows a series of waveform diagrams, for explaining the operation of the example of FIG. 2 at the time of throwing in the power source.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. 1, there is illustrated in block form one example of this invention, in which a plasma display panel 1 is supplied with a drive voltage from gate circuits 2 and 3 providing for the impression of a sustain voltage, a write-in voltage and an erasing voltage, and in which the gate circuits 2 and 3 are controlled by a logic circuit 7. From a power source such as a commercial power source of the like, power is supplied in common by a switch 10 to a high-tension power source circuit 8, to a low-tension power source circuit 9 and to an AND circuit 6. A switch 11 is provided to control the operation of the logic circuit 7. When the switch 11 and the power source 10 are in thereon state, a priming voltage is impressed by an output of the AND circuit 6 from a priming current power source 5 to a priming cell 4 at a desired position on the plasma display panel 1, for example, at a position on the peripheral area of the panel 1 or between lies in the case of a character display. Further, an operating voltage is impressed to the logic circuit 7 from the low-tension power source circuit 9 and a voltage is impressed from the high-tension power source circuit 8 to the gate circuits 2 and 3 controlled by the logic circuit 7, by which a sustain voltage, a write-in voltage and an erasing voltage are applied to the plasma display panel 1. Namely, the gate circuits 2 and 3 include groups of amplifiers and gates respectively and serve to impress the sustain, write-in and erasing voltages to all or selected ones of electrodes of the plasma display panel 1.

At the time of disconnecting the power source, the first step is to open the switch 11 to stop the operation of the logic circuit 7. Accordingly, no voltage is impressed to the plasma display panel 1, although the high-tension power source circuit 8 is still in operation. Namely, control outputs derived from the gate circuits 2 and 3 are cut off in synchronism with timing of the operation of the logic circuit 7, so that no voltage corresponding to an erasing pulse is applied to the panel 1. At this time, the output from the AND circuit 6 is also reduced to the level zero. Consequently no voltage is impressed to the priming cell 4 from the priming current power source 6 and the priming current becomes extinguished, so that it is possible to prevent a neutralizing action of charges diffusing from the priming cell 4. By opening the switch 10, the output voltages

from the high- and low-tension power source circuits **8** and **9** are reduced to zero. Even if a transient phenomenon occurs at this time, no influence is exerted on the plasma display panel **1** because the gate circuits **2** and **3** are closed.

At the time connecting the power source, the switch **10** is first closed to establish the output voltages from the high- and low-tension power source circuits **8** and **9** and then the switch **11** is closed to actuate the logic circuit **7.** At the instant of actuation of the logic circuit **7,** the respective voltages are in steady state, so that no influence is exerted by the transient phenomenon of the power source circuits. Further, by closing the switch **11,** a priming voltage is impressed to the priming cell **4** to initiate a discharge immediately, and the initial charges thereby produced are supplied to the other discharge cells impressed with the sustain voltage, thus eliminating the possibility of a neutralizing action of a minute electron avalanche due to field oscillation of the cells which are restrained from discharging by the absence of the initial charges.

FIG. **2** illustrates in block form another example of this invention, in which parts corresponding to those in FIG. **1** are identified by the same reference numerals. This example automatically performs operations similar to those of the foregoing example and also in the case where power is cut off. FIG. **3** and **4** are diagrams, for explaining its operations.

In the case of power suspension or opening the switch **10** at an instant *t*1 in FIG. **3***a*, output voltages from the high- and low-tension power source circuits **8** and **9** is reduced to zero after periods of time *th* and *tl* respectively as depicted in FIGS. **3***b* and **3***c*. This is caused by the inclusion of a capacitor of large capacitance; the periods of time *th* and *tl* are usually in the order of several milliseconds or longer. This power source interruption is detected by a high-speed detector circuit **12.** Outputs from the high-speed detector circuit **12** and a delay circuit **13** are applied to an AND circuit **14.** The operation of the logic circuit **7** is controlled by an output from the AND circuit **14.** Since the output from the high-speed detector circuit **12** is reduced down to the level zero (FIG. **3***d*) substantially at the same time as the power source is cut off, the operation of the logic circuit **7** is stopped (FIG. **3***e*). Upon suspension of the operation of the logic circuit **7,** no voltage is impressed to the plasma display panel **1** even if the output voltage from the high-tension power source circuit **8** has not yet attenuated. Namely, FIGS. **3***f* and **3***g* show examples of waveforms of the sustain voltages to be impressed to X- and Y-direction electrodes of the panel **1**; in particular, the sustain voltages are cut off concurrently with the suspension of the operation of the logic circuit **7.** With the reduction of the output from the AND circuit **14** down to zero, no priming voltage is applied to the priming cell **4.**

Where the power is recovered or the switch **10** is closed at an instant tn in FIG. **4,** the outputs derived from the high- and low-voltage power source circuits **8** and **9** become steady after periods of time th1 and *tl*1 respectively as shown in FIGS. **4***b* and **4***c*. The output from the high-speed detector circuit **12** rises to the level one substantially at the instant *tn* (FIG. **4***d*) but the output from the delay circuit **13** still remains at the level zero, so that the logic circuit **7** does not operate. The delay time TD of the delay circuit **13** is selected longer than the periods th1 and *tl*1 and at an instant when the output from the delay circuit **13** rises up to the level one (FIG. **4***h*), the output from the AND circuit **14** has the level one (FIG. **4***i*), with the result that the logic circuit **7** starts to operate. Further, since the output from the AND circuit **6** (FIG. **4**j) also becomes of the level one, the priming current power source circuit **5** operates and the priming cell **4** starts discharging to provide a supply of the initial charge to the other cells. Consequently, the X- and Y-direction electrodes are supplied with such sustain voltages as depicted in FIGS. **4***f* and **4***g* , which do not include any spurious erasing pulse.

Since the logic circuit **7** rapidly stops its operation at the time of disconnecting the power source and slowly starts its operation at the time of connecting the power source, it is also possible to constitute a control circuit with a relay or timer of high-speed opening and low-speed closing. Further, it is also possible, of course, to connect or disconnect the sustain voltage source with rapid rise or fall at a timing perfectly synchronous with a clock pulse while the sustain voltage is interrupted or at the level zero.

With the present invention, the plasma display panel is not supplied with a voltage corresponding to an erasing pulse resulting from a transient phenomenon when the power source is disconnected and connected so that a wall charge pattern on the display panel is retained for a long time, as described in the foregoing. Accordingly, written information is maintained even while power is suspended or the operation is stopped in the night and a display content corresponding to the wall charge pattern can be reproduced merely by throwing in a power source without requiring any rewriting operation. Since the wall charge pattern is thus retained even while the power source is cut off, it is also possible to erase the wall charges in selected cells by producing a weak discharge by means of a voltage pen or the like while the power source is cut off and to perform negative writing by similar means. The voltage impression to the priming cell can also be effected slightly before the logic circuit starts to operate.

It will be apparent that many modifications and variations may be effected without departing from the scope of the novel concepts of this invention.

What is claimed is:

1. A control system for selectively energizing a plasma display panel including first and second sets of electrodes disposed to intersect each other to form discharge cells at their points of intersection, said control system comprising:

circuit means for generating as its output a sustain voltage to be applied across said first and second sets of electrodes, said circuit means having the property that upon termination of the power the output of said circuit means decays to zero voltage within a predetermined time period;

logic circuit means operative in a first mode for applying the sustain voltage across said first and second sets of electrodes and in a second mode for disconnecting the sustain voltage from said first and second sets of electrodes; and

control circuit means responsive to the termination of power for effecting operation of said logic circuit substantially instantaneously in its second mode and responsive to the application of power for effecting after a time period not less than the

predetermined time period, the operation of said logic circuit in its first mode.

2. A plasma display control system as claimed in claim 4 wherein said plasma display panel includes a priming cell, and there is included a priming current source for impressing a priming current to said priming cell, said control circuit means responsive to the termination of the power to substantially instantaneously disconnect the application of the priming current to said priming cell and responsive to the application of power for impressing the priming current to said priming cell after the predetermined time period.

3. A plasma display control system as claimed in claim 1, wherein said control current circuit means includes a high speed detector circuit responsive to the termination of the power for generating a first output and responsive to the application of the power to provide a second output, delay means responsive to the application of power to initiate a time delay and a coincidence means responsive to the first output and to the termination of said delay to effect operation of said logic means in its first mode.

4. A plasma display control system as claimed in claim 3 wherein there is included first and second gate circuits respectively connected to said first and second sets of electrodes, said first and gate circuits responsive to the first mode of said logic circuit for applying the sustain voltages thereacross and responsive to the second mode of said logic circuit for disconnecting the sustain voltage therefrom.

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