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(54) **METHODS AND APPARATUS FOR DEVICES HAVING IMPROVED CAPACITANCE**

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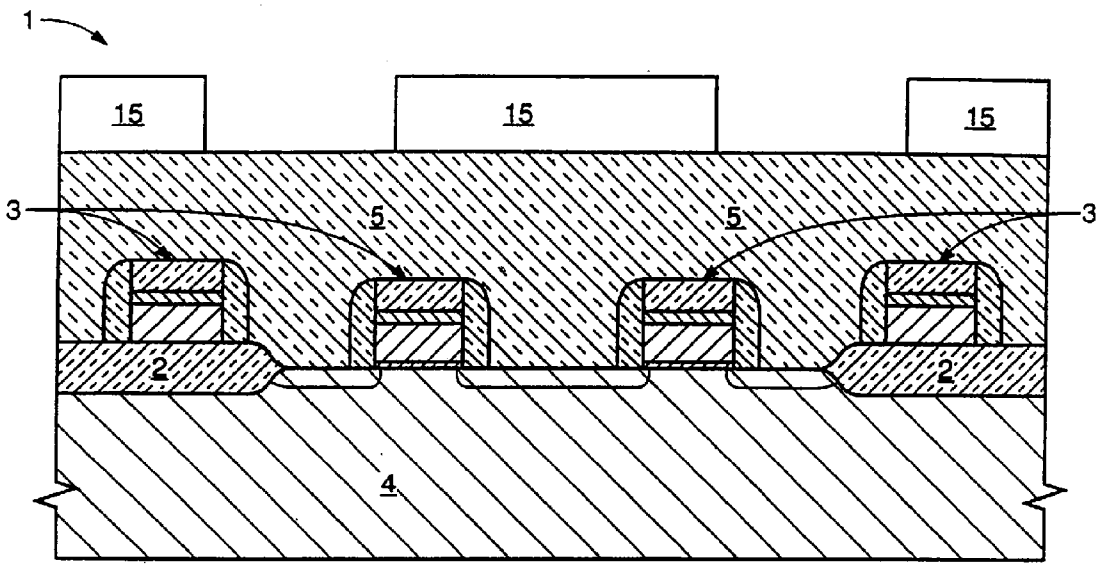
(52) **U.S. Cl.** **428/469**; 257/532

(57) **ABSTRACT**

Some embodiments of the invention include a capacitor in which a dielectric of the capacitor is formed by oxidizing at least a portion of a metal layer. Other embodiments are described and claimed.



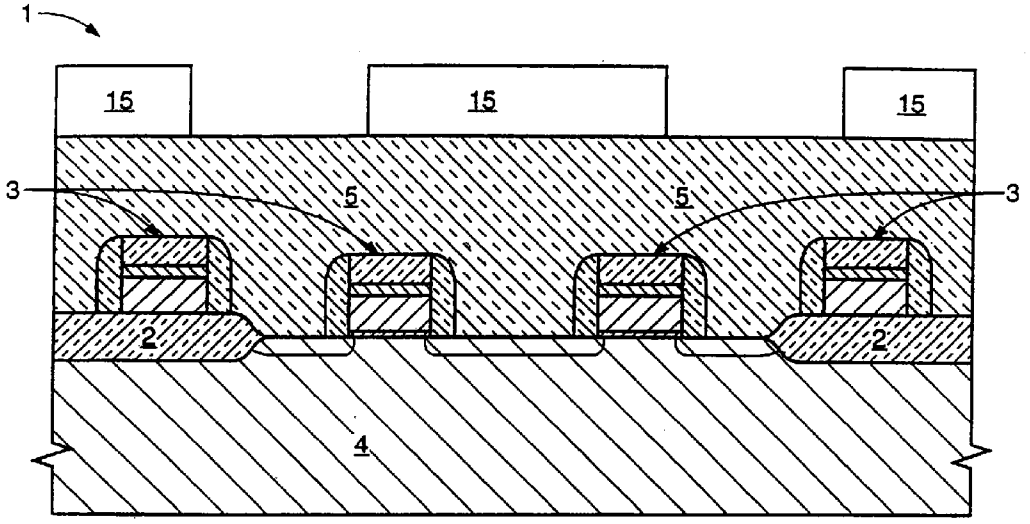


FIG. 1

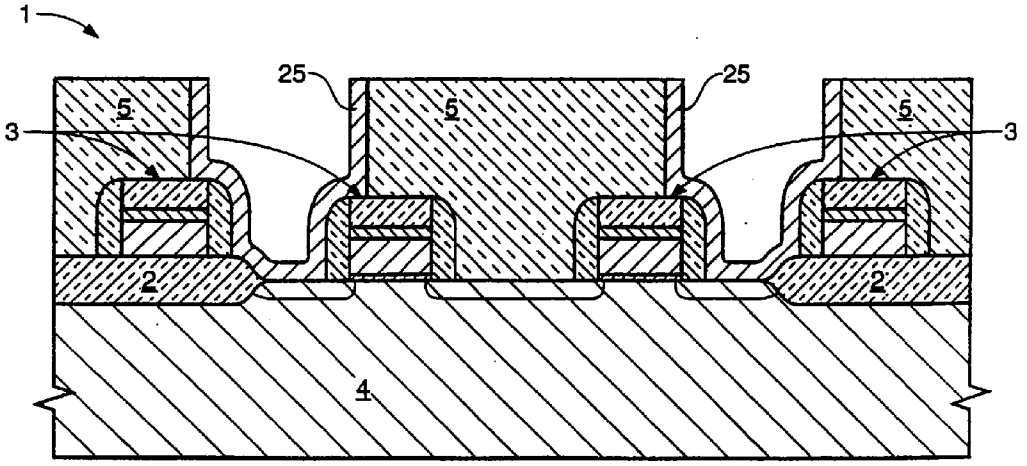


FIG. 2

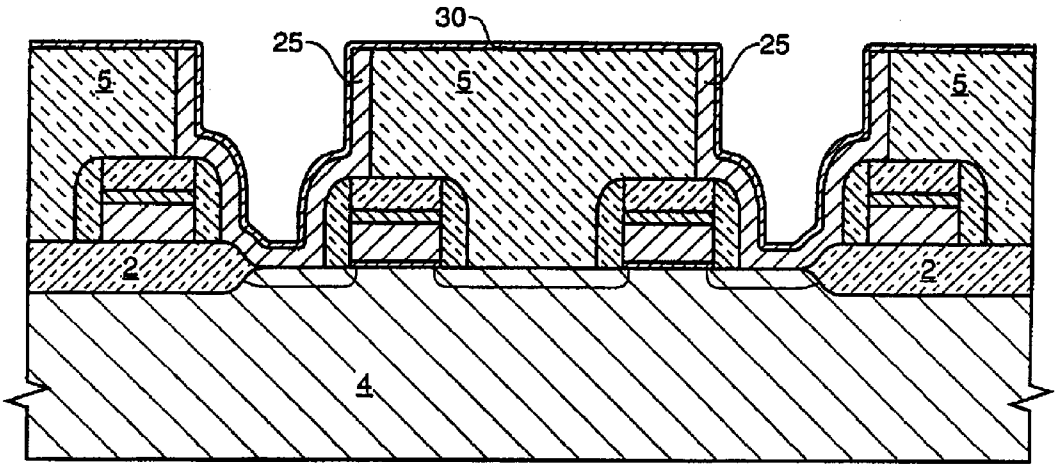


FIG. 3

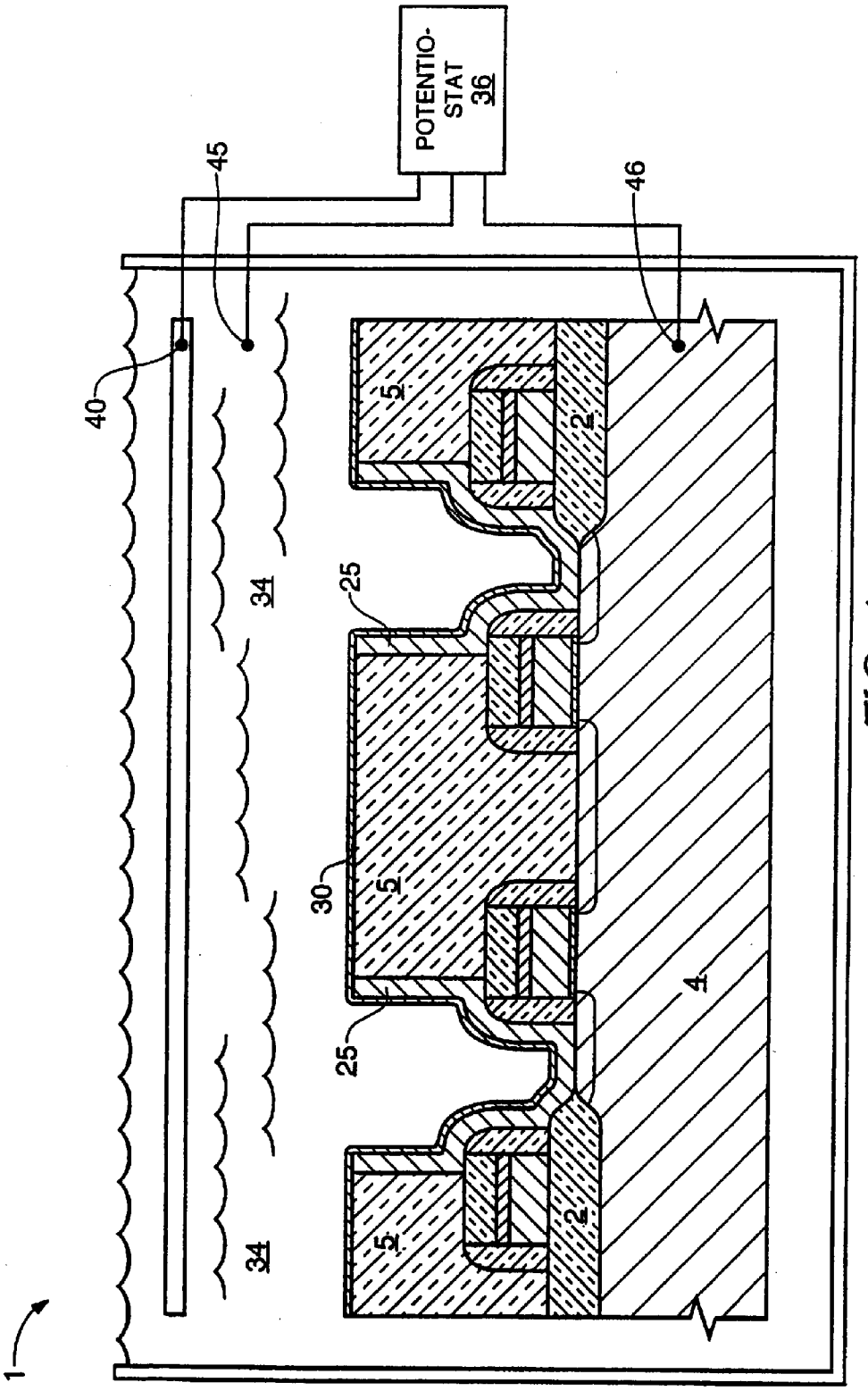


FIG. 4

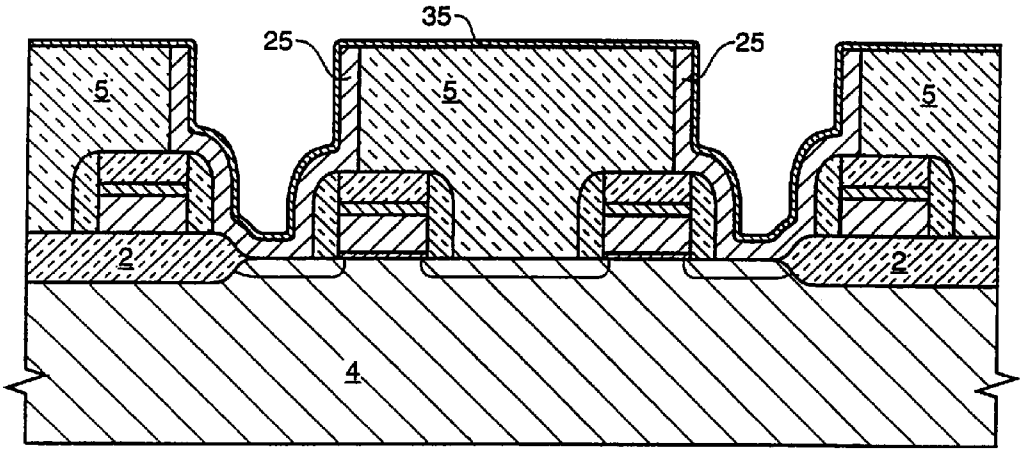


FIG. 5

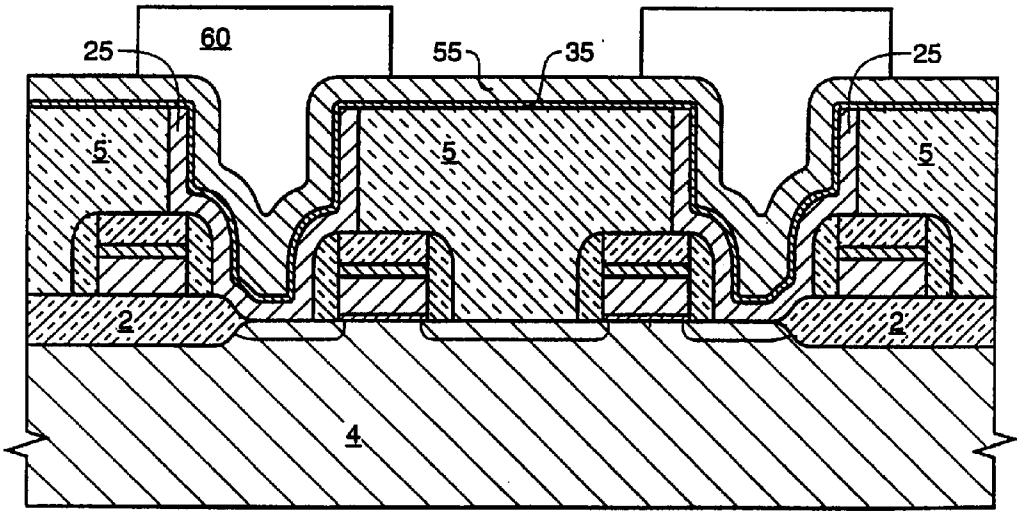


FIG. 6

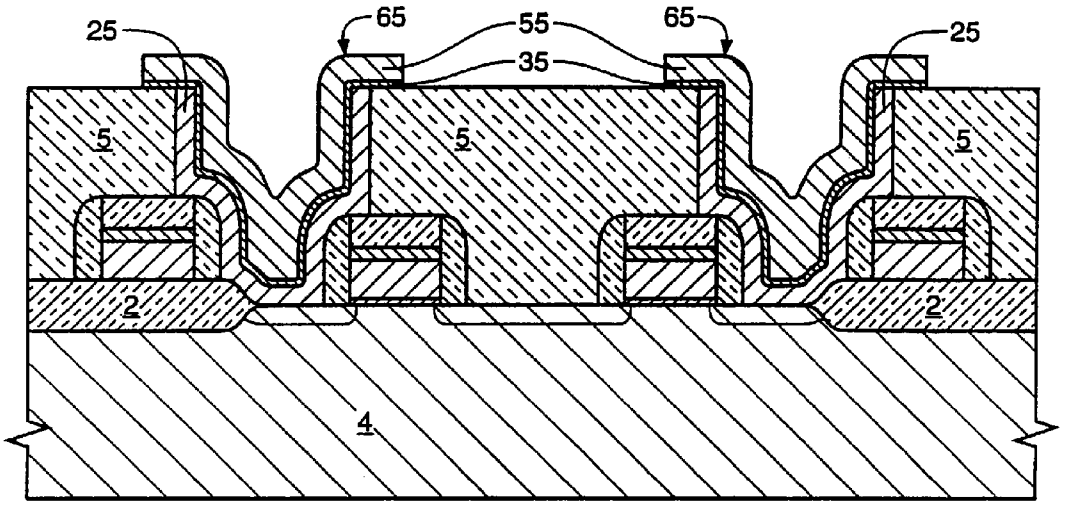


FIG. 7

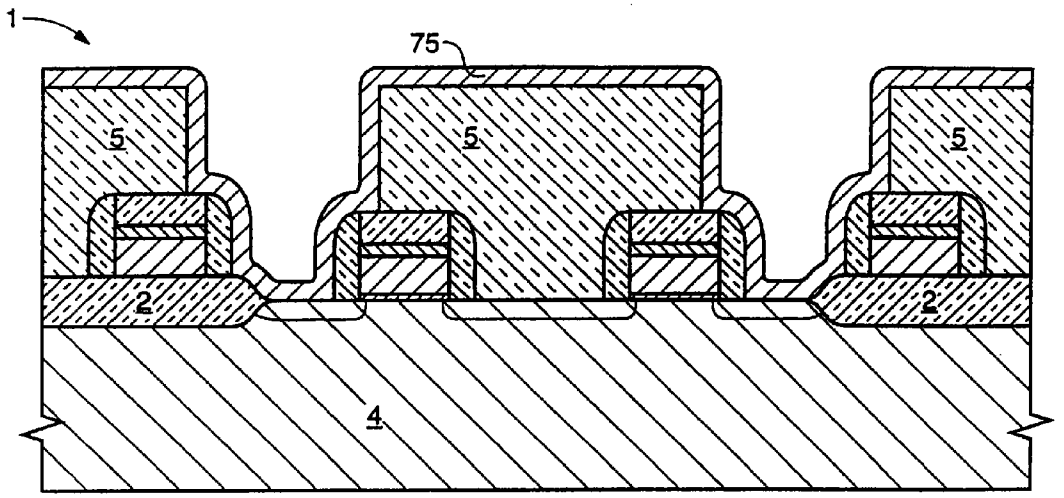


FIG. 8A

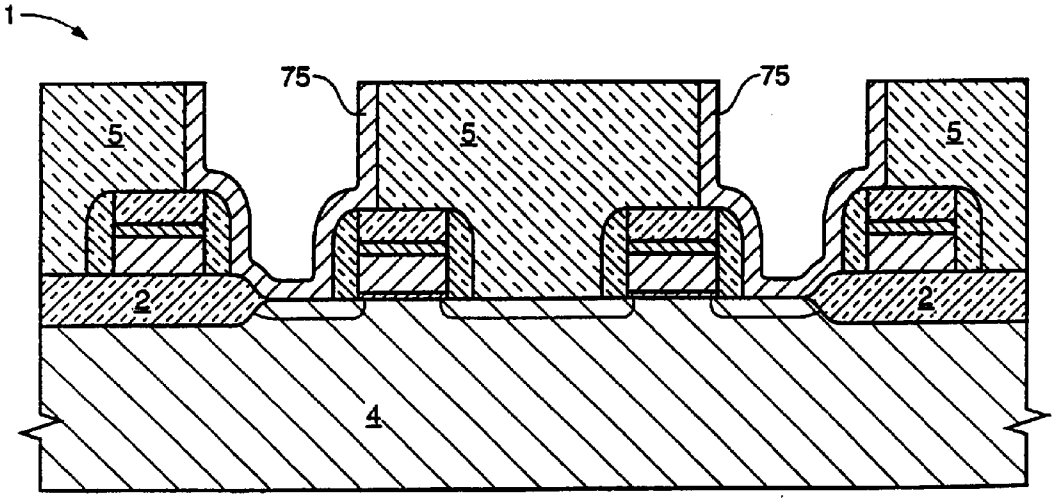


FIG. 8B

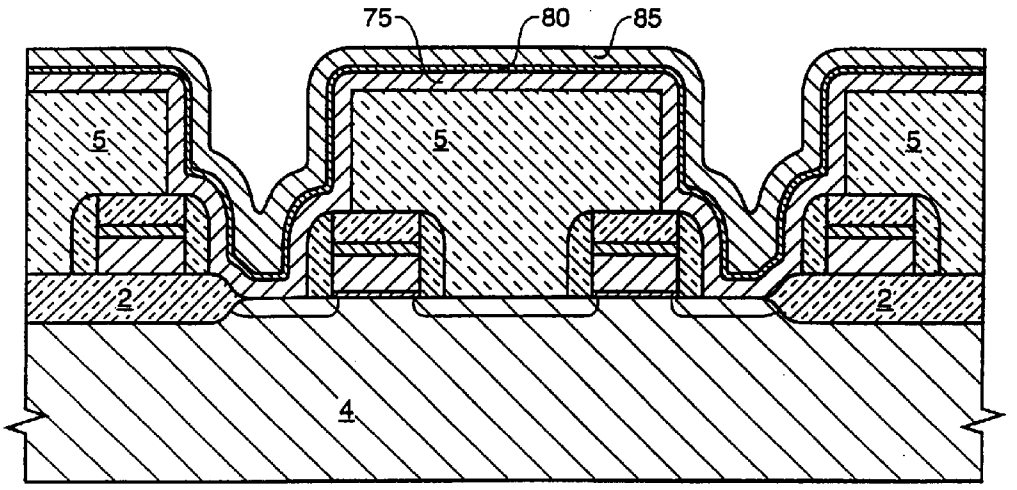


FIG. 9A

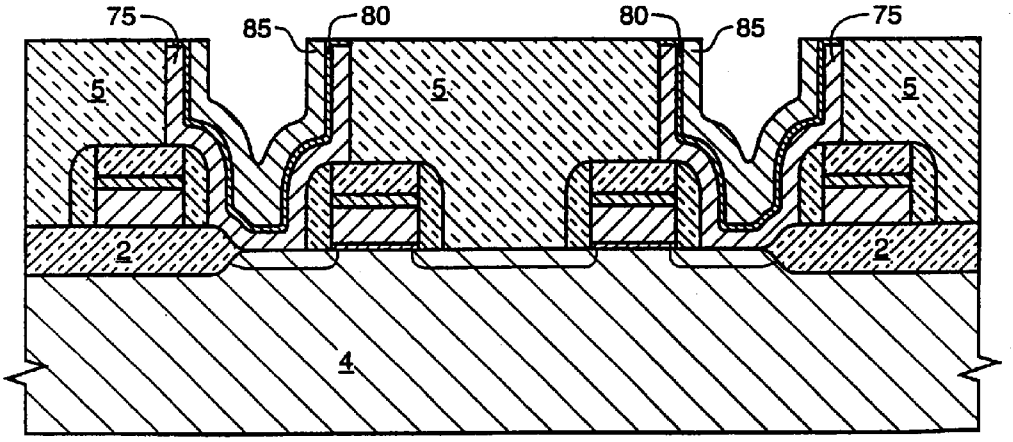


FIG. 9B

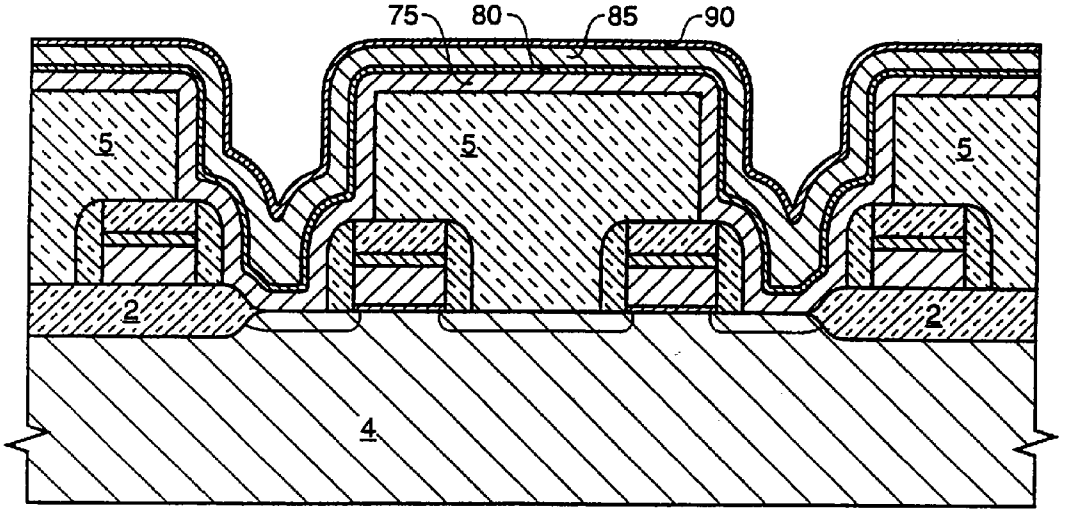


FIG. 10A

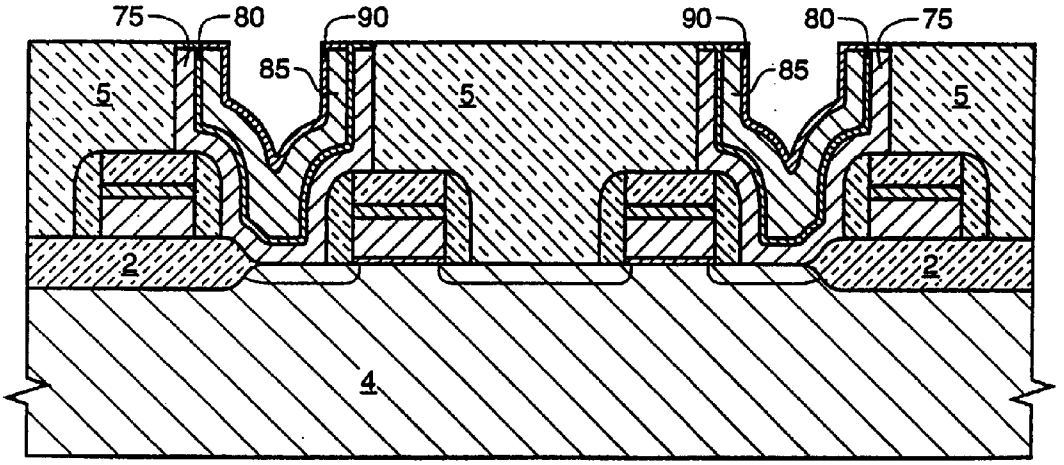


FIG. 10B

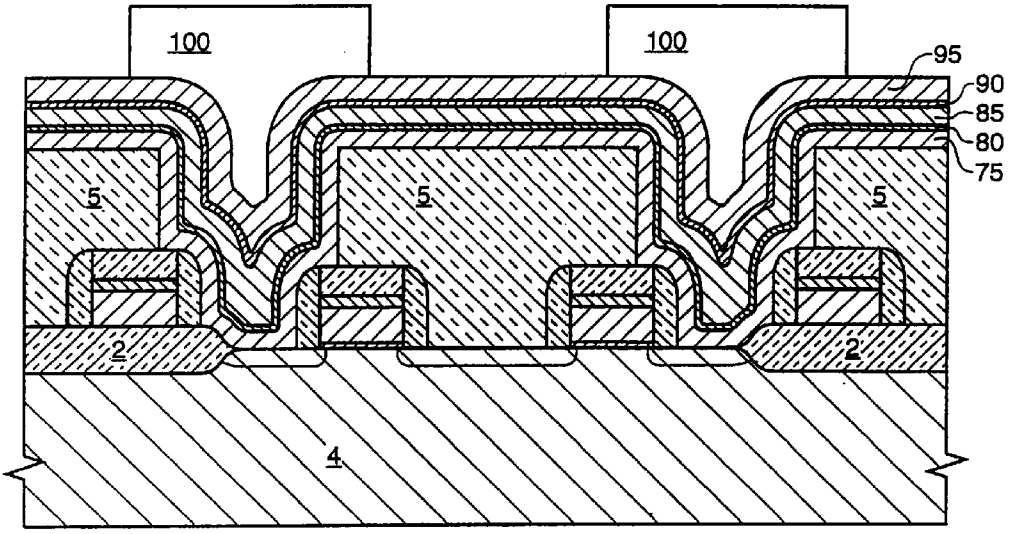


FIG. 11A

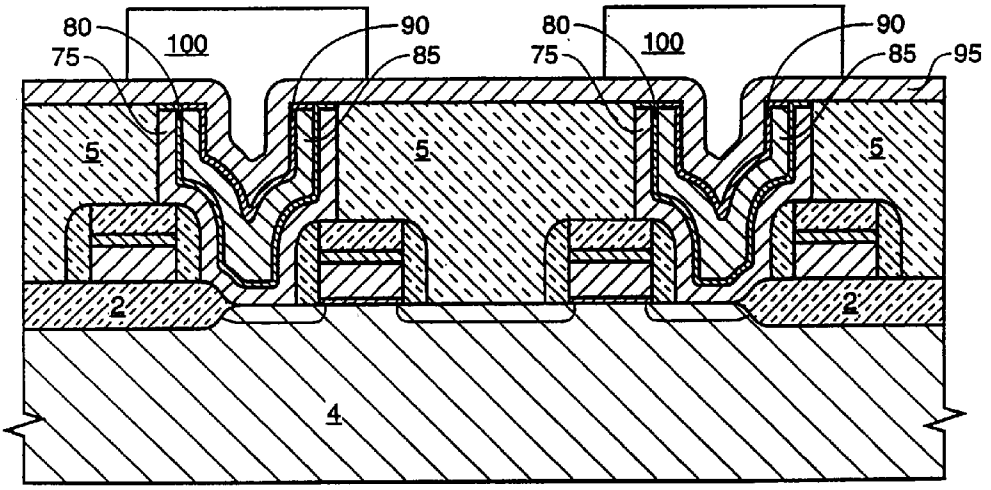


FIG. 11B

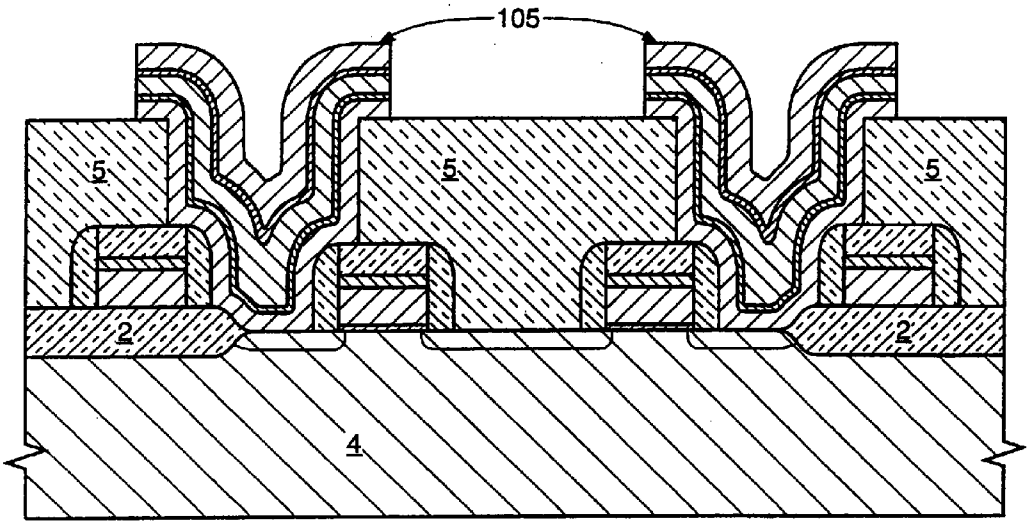


FIG. 12A

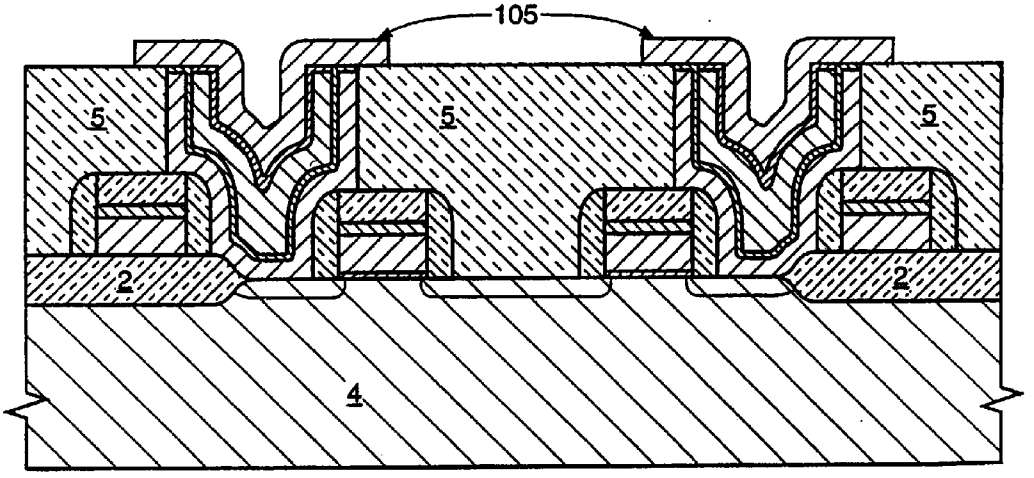


FIG. 12B

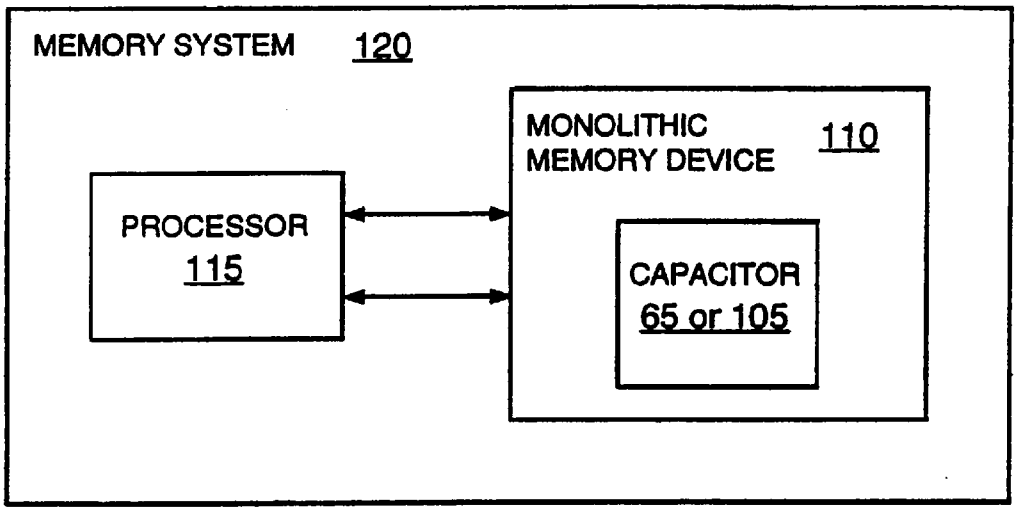

MEMORY SYSTEM 120
MONOLITHIC MEMORY DEVICE 110
PROCESSOR 115
CAPACITOR 65 or 105

FIG. 13

METHODS AND APPARATUS FOR DEVICES HAVING IMPROVED CAPACITANCE

[0001] This application is a Divisional of U.S. application Ser. No. 09/470,265, filed Dec. 22, 1999, which is a Divisional of U.S. application Ser. No. 08/676,708, filed Jul. 8, 1996, now U.S. Pat. No. 6,660,610, both of which are incorporated herein by reference.

BACKGROUND

[0002] Although there have been attempts to deposit metal oxides, such as TiO_2 and $SrTiO_3$, during semiconductor fabrication, thermal oxidation of metals in the fabrication of capacitors has been limited since an initial oxide layer prohibits further diffusion during thermal oxidation. As a result the use of high dielectric constant oxidized metals has been limited in semiconductor capacitor fabrication. One such metal, titanium dioxide, has a dielectric constant 2-15 times greater than present semiconductor capacitor dielectrics such as silicon nitride, while titanates are 2-1000 times greater.

[0003] In the January 1996 issue of Material Research, Vol. 11, No. 1, an article entitled ELECTROCHEMICAL SYNTHESIS OF BARIUM TITANATE THIN FILMS, R. R. Bacsa et al. describes the synthesizing of polycrystalline films of barium titanate on titanium substrates by the galvanostatic anodization of titanium to form a material which has a dielectric constant of 200.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] **FIG. 1** is a cross section of a semiconductor wafer following the formation of a silicon dioxide layer and the masking thereof.

[0005] **FIG. 2** is the cross section of **FIG. 1** following an etch of the silicon dioxide layer and following a deposition and etch of polysilicon.

[0006] **FIG. 3** is the cross section shown in **FIG. 2** following a deposition of titanium.

[0007] **FIG. 4** is the cross section shown in **FIG. 3** when placed in an apparatus configured to perform electrochemical oxidation.

[0008] **FIG. 5** is the cross section shown in **FIG. 4** following the oxidation of the titanium layer.

[0009] **FIG. 6** is the cross section shown in **FIG. 5** following the deposition and masking of a conductive layer.

[0010] **FIG. 7** is the cross section shown in **FIG. 6** following the final capacitor formation.

[0011] **FIG. 8A** is the cross section of the semiconductor wafer shown in **FIG. 1** following an etch of the silicon dioxide layer and a deposit of a first metal layer.

[0012] **FIG. 8B** is the cross section of the semiconductor wafer shown in **FIG. 1** following an etch of the silicon dioxide layer and a deposit and planarization of a first metal layer.

[0013] **FIG. 9A** is the cross section shown in **FIG. 8A** following the electrochemical oxidation of the first metal layer and a deposit of a second metal layer.

[0014] **FIG. 9B** is the cross section shown in **FIG. 8B** following the planarization and electrochemical oxidation of the first metal layer and following a deposit and planarization of a second metal layer.

[0015] **FIG. 10A** is the cross section shown in **FIG. 9A** following an electrochemical oxidation of the second metal layer.

[0016] **FIG. 10B** is the cross section shown in **FIG. 9B** following a electrochemical oxidation of the second metal layer.

[0017] **FIG. 11A** is the cross section shown in **FIG. 10A** following the formation of a capacitor plate and the masking thereof.

[0018] **FIG. 11B** is the cross section shown in **FIG. 10B** following the formation of a capacitor plate and the masking thereof.

[0019] **FIG. 12A** is the cross section shown in **FIG. 11A** following an etch and showing one capacitor of an embodiment of the invention.

[0020] **FIG. 12B** is the cross section shown in **FIG. 11B** following an etch and showing one capacitor of an embodiment of the invention.

[0021] **FIG. 13** is a block schematic of a memory system of an embodiment of the invention.

DETAILED DESCRIPTION

[0022] **FIGS. 1-7** depict cross sections of a semiconductor wafer **1** following the process steps of a first embodiment used in fabricating the wafer **1**. In **FIG. 1** field oxide regions **2** and wordlines **3** have been formed overlying a substrate **4** using conventional semiconductor process methods. Following the wordline formation a thick layer of silicon dioxide **5** is deposited to a thickness approximately equal to 5000 angstroms and then planarized. The silicon dioxide **5** is masked to define future capacitor substrate contact regions with mask layer **15**.

[0023] In **FIG. 2** the silicon dioxide **5** is anisotropically dry etched to expose the substrate **4** in the unmasked regions. Following the etch a substantially conformal first conductive layer **25**, for example a polysilicon layer having a thickness of 200-400 angstroms, is deposited to overlie the exposed substrate **4** and the silicon dioxide **5**. Following the formation of the conductive layer **25** upper portions of the silicon dioxide layer **5** are exposed by removing portions of the conductive layer **25** using a spacer etch or using CMP (chemical mechanical planarization) following a resist deposit. The removal of portions of the conductive layer **25** creates electrically isolated portions of the conductive layer **25**. The isolated portions of conductive layer **25** are first capacitor plates of the capacitor of an embodiment of the invention. Conventional methods for depositing the conductive layer **25** include CVD (chemical vapor deposition), PVD (physical vapor deposition) and electroless deposition. In an alternate embodiment a metal layer is deposited by a conventional method and functions as the first conductive layer **25**.

[0024] Following the deposition and isolation of portions of the first conductive layer **25** a conformal metal layer **30** is deposited by chemical vapor deposition to overlie the first

conductive layer **25** and exposed portions of silicon dioxide layer **5**, see **FIG. 3**. In an embodiment, the conformal metal layer **30** is titanium having a thickness of approximately 16-100 angstrom. Although in this embodiment titanium is used other metals may be used such as copper, gold, tungsten, and nickel. In a case where metal is used as the first conductive layer **25** it may be necessary to form diffusion barrier layer or an oxidation resistant layer or both interposed between the first conductive layer **25** and the metal layers **30**. Thus, it should be noted that the first conductive layer **25** may actually be comprised of more than one material. For example in a ministack application a conductive plug and further conductive layers overlying the conductive plug may form the first conductive layer.

[**0025**] In **FIG. 4** the wafer **1** is placed in electrolytic solution **34** conducive to oxidizing the metal layer **30** when a potential is applied across the electrolytic solution **34** and the metal layer **30**. The electrolytic solution **34** contacts the metal layer **30**. In an embodiment, the electrolytic solution **34** is water, such as one part NH_4OH for 10 parts water or 0.1 Mole $HCLO_4$. However, a basic or acidic solution could also be used. A potentiostat **36** consists of a first electrode **40**, known as a counter electrode, and a second electrode **45**, known as a reference electrode. Both the first **40** and second **45** electrodes are immersed in the electrolytic solution **34**. The potentiostat **36** also provides a third electrode **46**, known as the working electrode, which is connected to the substrate **4**. The substrate **4** is in electrical communication with the metal layer **30**. The potentiostat **36** is a standard device, one of which is a PAR available from E.G.& G. of Princeton, N.J. The reference electrode is an SCE (saturated calomel electrode). The potentiostat **36** monitors the current flowing between the first and third electrodes **40** and **46**. The potentiostat controls the potential between the second and third electrodes **45** and **46**. For example, the potential is in the range of −2.0 volts to 5 volts (i.e. SCE reference electrode) for 5-120 sec depending on the desired thickness of the dielectric. The current is measured between electrodes **40** and **46** and is controlled by varying the potential between the second and third electrodes **45** and **46** to obtain the desired current. The potentiostat allows the potential to be adjusted within a range of potentials conducive to the oxidizing of titanium. The oxidation reaction simultaneously oxidizes the metal layer **30** across the entire wafer surface.

[**0026**] Although in an embodiment, a three electrode potentiostat controls the electrochemical oxidation process, a two electrode rheostat control device may also be used. However, the oxidation is less controllable using the two electrode rheostat. When using the rheostat the second electrode **45** is eliminated and the electrochemical reaction changes the counter electrode chemistry. When this happens the potential changes. Thus the oxidation of the metal layer **30** is uncontrolled. In the three electrode embodiment, the existence of the reference electrode provides better control of the oxidation process.

[**0027**] In the first embodiment substantially all of the metal layer **30** is oxidized during the electrolytic process to form a metal oxide **35**, titanium dioxide in the example embodiment, see **FIG. 5**. The titanium dioxide has a high dielectric constant. For example, the thickness of the metal oxide ranges between 10-1000 Angstroms and the dielectric constant is between 86 and 170.

[**0028**] Following the oxidation step the metal oxide is chemically mechanically planarized and a second conductive layer **55** is deposited to overlie the metal silicon dioxide layer **5**, the silicon oxide **50** and the metal oxide **35**, see **FIG. 6**. The second conductive layer **55** is created using conventional methods such as CVD, PVD, or electroless deposition. In an embodiment, the conductive layer **55** is polysilicon although metal may be used instead of polysilicon, and more than one material may be used to form conductive layer **55**. A mask **60** is then formed to define the future capacitor structures.

[**0029**] In **FIG. 7** the conductive layer **55** has been etched in unmasked regions to complete the capacitor structures **65**. The capacitors **65** made by the method of an embodiment of the invention comprises a first capacitor plate which is first conductive layer **25**, a second capacitor plate which is the second conductive layer **55**, and a dielectric which is the metal oxide **35**.

[**0030**] In an alternate embodiment it is only necessary to oxidize a portion of the metal layer **30** to create a metal/metal oxide layer, or in the example embodiment a titanium/titanium dioxide layer. In this case the unoxidized metal layer **30** and the polysilicon layer **25** form the first capacitor plate while the thin layer of titanium oxide forms the dielectric.

[**0031**] In a still further alternate embodiment multiple layers of metal are deposited and at least a portion of each metal layer is electrochemically oxidized prior to the deposition of a subsequent metal layer. In this case the dielectric comprises alternate layers of oxide and metal. In this embodiment the second conductive layer **55** is deposited on the last metal oxide created.

[**0032**] In a second embodiment of the invention, shown in **FIGS. 8A-12B**, a first metal layer **75**, such as titanium, is sputter deposited to overlie the silicon dioxide layer **5** and to contact exposed portions of substrate **4** following the etch of the silicon dioxide layer **5** shown in **FIG. 1**. The wafer **1** is then placed in an electrolytic solution of acidic water. A current flows in the electrolytic solution in response to a potential applied across the electrolytic solution. The current is controlled with a potentiostat in order to control the oxidation of the metal layer. By controlling the oxidation it is possible to oxidize only a top portion of the first metal layer **75** to form a first metal oxide **80**, see **FIG. 9A**.

[**0033**] Alternately the metal layer **75** is planarized to expose the silicon dioxide prior to oxidation and formation of the first metal oxide **80**, see **FIGS. 8B and 9B**.

[**0034**] Following the first oxidation a second metal layer **85**, **FIG. 9A**, is sputter deposited to overlie the first metal oxide **80**. Again the wafer **1** is placed in the electrolytic solution and an upper portion of the second metal layer **85** is oxidized to form a second metal oxide **90**, see **FIGS. 10A and 10B**.

[**0035**] In the alternate embodiment, shown in **FIGS. 9B and 10B**, the second metal layer **85** has been planarized to expose the silicon dioxide prior to oxidation.

[**0036**] Following the oxidation of the second metal layer **85** a third metal layer **95** is sputter deposited to overlie the second metal oxide layer **90**, and capacitors are defined by a mask **100**, see **FIGS. 11A and 11B**.

[0037] Exposed first, second and third metal layers **75**, **85**, and **95** and exposed first and second metal oxide layers **80** and **90** are etched to form the capacitors **105** of an embodiment of the invention, see **FIGS. 12A and 12B**. First and third metal layers **75** and **95** form first and second capacitor plates of the capacitors **105**, and the first and second metal oxide layers **80** and **90** and second metal layer **85** form the dielectric of the capacitors **105**. In an example embodiment the first, second, and third metal layers **75**, **85**, and **95** are titanium. Therefore in the example embodiment the metal oxide layers **80** and **90** are titanium dioxide. It is also possible to use only one or to use more than the number of metal/metal oxide layers described above as the dielectric layer, or it is possible to oxidize an entire metal layer if it is not the first or last metal layer deposited.

[0038] In further conceived embodiments the metal layer **30** (in this embodiment titanium) may be alloyed with a material, such as Strontium. In this case $SrTiO_3$ is formed during the oxidation performed by the method of an embodiment of the invention. Other titanates may also be formed depending on the alloy used in combination with titanium. For Example, Ba or Pb may be combined with Ti to form $BaTiO_3$ and $PbTiO_3$, respectively, during oxidation. The process also works for TiO_3^{-2} complexes. In a still further embodiment the metal layer **30** (in this embodiment titanium) may be oxidized in a supersaturated Sr^{+2} solution such as $Sr(OH)_2$ to form $SrTrO_3$, in an example embodiment.

[0039] The capacitors **65** and **105** shown in **FIGS. 7 and 12**(A&B) respectively are typically used in a monolithic memory device **110**, such as a dynamic random access memory device, as shown in **FIG. 13**. The monolithic memory device **110** and a processor **115** form part of a memory system **120**. The processor **115** is typically used to generate external control signals which accesses the monolithic memory device **110** either directly or through a memory controller.

CONCLUSION

[0040] Methods and apparatus for devices having improved capacitance are described. In one exemplary embodiment, the capacitor of an embodiment of the invention is formed by a process using only two deposition steps. The capacitor has first and second conductive plates and a dielectric is formed from the first conductive plate. In one exemplary process in accordance with and embodiment of the invention, a metal layer is deposited and at least partially oxidized in an electrolytic solution. The metal oxide formed during this oxidation forms the dielectric of the capacitor. Portions not oxidized may form at least a portion of a capacitor plate. In one exemplary implementation in accordance with an embodiment of the invention, a metal layer is deposited to overlie a first capacitor plate fabricated on a semiconductor wafer. The wafer is placed in an electrolyte conducive to forming an oxide with the metal. A potential is applied across the electrolyte and the metal, and at least a portion of the metal oxidizes. In an embodiment the metal is titanium and titanium dioxide is formed during the electrochemical reaction. The capacitor fabrication is completed with the formation of a second capacitor plate overlying the oxidized metal layer. The oxidized metal layer functions as the dielectric of the capacitor and has a high dielectric constant.

[0041] It will be evident to one skilled in the art that many different combinations of materials, deposits and etch steps may be used to fabricate the capacitor and dielectric according to example embodiments of the invention without departing from the scope of the embodiments of the invention as claimed. The method for forming the dielectric according to an embodiment of the invention is equally applicable to any type of capacitor structure, such as trench, container, and stacked and ministacked or variations thereof.

What is claimed is:

1. A dielectric layer formed by a process comprising:

forming a metal layer overlying a starting substrate;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer; and

oxidizing at least a portion of the metal layer to form an oxidized layer such that the oxidized layer forms at least a portion of the dielectric layer.

2. The dielectric layer of claim 1, wherein the process further comprises forming a capacitor plate overlying the starting substrate prior to forming the metal layer such that the metal layer is overlying the capacitor plate after the metal layer is formed.

3. The dielectric layer of claim 1, wherein a non-oxidized portion of the metal layer forms at least a portion of a capacitor plate.

4. The dielectric layer of claim 1, wherein the process further comprises:

connecting a first electrode in contact with the electrolytic solution to a first terminal of a potential source; and

connecting the starting substrate to a second terminal of the potential source.

5. The dielectric layer of claim 4, wherein the process further comprises:

positioning a second electrode to contact the electrolytic solution; and

connecting the second electrode to the potential source.

6. The dielectric layer of claim 1, wherein the process further comprises adjusting the potential across the electrolytic solution to control the oxidizing of at least the portion of the metal layer.

7. The dielectric layer of claim 1, wherein the process further comprises:

monitoring a current in the electrolytic solution; and

adjusting a potential of the electrolytic solution to maintain an amount of the current in the electrolytic solution.

8. A capacitor formed by a process comprising:

forming a first capacitor plate;

forming a metal layer overlying the first capacitor plate;

contacting the metal layer with an electrolytic solution;

applying a potential across the electrolytic solution and the metal layer; and

oxidizing at least a portion of the metal layer to form an oxidized layer such that the oxidized layer forms at least a portion of a dielectric layer of the capacitor.

9. The capacitor of claim 8, wherein the process further comprises forming a conductive layer overlying the oxidized metal layer such that the conductive layer forms a second capacitor plate.

10. The capacitor of claim 8, wherein the first capacitor plate is formed on a silicon dioxide starting substrate.

11. The capacitor of claim 8, wherein the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

12. The capacitor of claim 11, wherein the metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

13. The capacitor of claim 8, wherein the electrolytic solution is a basic solution.

14. The capacitor of claim 8, wherein the electrolytic solution is an acidic solution.

15. The capacitor of claim 8, wherein the electrolytic solution is a solution of one part NH_4OH to ten parts water.

16. The capacitor of claim 8, wherein the electrolytic solution is a 0.1 molar solution of $HClO_4$.

17. A capacitor formed by a process comprising:

forming an insulative layer overlying a substrate;

masking the insulative layer to define a region in which to fabricate the capacitor;

removing the insulative layer in an unmasked region to expose a portion of the substrate;

depositing a polysilicon layer overlying the insulative layer and the substrate and contacting the substrate;

removing portions of the polysilicon layer to expose an upper surface of the insulative layer;

depositing a metal layer such that the metal layer overlies the polysilicon layer;

contacting the metal layer with an electrolytic solution;

applying an electrical potential to the electrolytic solution and the metal layer;

oxidizing at least a portion of the metal layer to form a metal oxide such that the metal oxide functions as a dielectric layer; and

forming an electrically conductive layer overlying the metal oxide.

18. The capacitor of claim 17, wherein the substrate is formed from silicon dioxide.

19. The capacitor of claim 17, wherein the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

20. The capacitor of claim 19, wherein the metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

21. A dielectric layer formed by a process comprising:

forming a metal capacitor plate on a substrate assembly;

applying a potential across the metal capacitor plate; and

oxidizing at least a portion of the metal capacitor plate to form at least a portion of the dielectric layer.

22. The dielectric layer of claim 21, wherein the substrate assembly is formed from silicon dioxide.

23. The dielectric layer of claim 22, wherein the metal capacitor plate is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

24. The dielectric layer of claim 23, wherein the metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

25. A capacitor formed by a process comprising:

forming a first capacitor plate;

forming a metal layer overlying the first capacitor plate;

oxidizing a portion of the metal layer to form an oxidized portion of the metal layer and a non-oxidized portion of the metal layer; and

forming a second capacitor plate such that the second capacitor plate directly contacts the oxidized portion of the metal layer.

26. The capacitor of claim 25, wherein the metal layer is formed from titanium.

27. The capacitor of claim 25, wherein oxidizing includes contacting the metal layer with an electrolytic solution.

28. The capacitor of claim 25, wherein the metal is alloyed with at least one additional metal.

29. The capacitor of claim 28, wherein the additional metal is strontium.

30. The capacitor of claim 28, wherein the additional metal is barium.

31. The capacitor of claim 28, wherein the additional metal is lead.

* * * * *