Abstract: A chip (100) comprising at least: - a first substrate (102); - a first electronic and/or mechanical circuit (108) arranged in and/or on a front face (104) of the first substrate; - a first deformation compensation layer (120) suitable for compensating a deformation of the chip at room temperature; - a second deformation compensation layer (124) suitable for compensating a deformation of the chip between the room temperature and a first temperature which is higher than the room temperature; and wherein the first and second deformation compensation layers are stacked on a rear face (106) of the first substrate.
CHIP COMPRISING DEFORMATION COMPENSATION LAYERS

DESCRIPTION

TECHNICAL FIELD AND PRIOR ART

The invention concerns a chip comprising at least two deformation compensation layers which compensate the deformation of the chip at room temperature and up to a first temperature higher than room temperature, and a method for making such chip.

In order to obtain integrated components with high performances, low sizes and low power consumptions, especially for mobile applications, the compact and vertical stacking of chips is a very effective solution to make Systems On Chip (SOC) or Systems in Package (SiP). To achieve this vertical integration of components, vertical interconnections must be made to connect the chips together or to a support. A chip or a set of stacked chips can be put on an interposer or a support, e.g. by flip-chip. Compared to wire bonding, a flip-chip connection which uses solder balls, pillars or bumps allows a better integration of the chips and leads to a reduction of lengths of the interconnections and to a lower vertical size of the assembly.

Furthermore, to reduce the vertical size of the assembly, thinner chips are advantageously used. A thinner chip is generally obtained by thinning the substrate of the chip. However, such thinning of the substrate increases the deflection, or bending, of the chip, especially during heating of the chip (e.g. during a soldering of the chip on a support) because the stress of the layers deposited on the substrate of the chip remains constant and thus induces a larger deformation of the chip when its thickness decreases (according to the function: bending = 1 / thickness²).

This effect leads to a non-planarity of the chip due to the deflection of the chip. In this case, when the chip is bonded to a support or a substrate, open connections between the chip and the support are generated and can lead to the non-functionality of the assembly. This problem is exacerbated during the heating of these two parts of the assembly, e.g. during a soldering of the chip on the support, due to the
various coefficients of thermal expansion (CTE) of the layers of the chip (e.g. silicon oxide and interconnect metal) which are different than the CTE of the material of the support, e.g. silicon.

To compensate or limit the deformation of the chip, an adaptation / modification of materials and processes used for the fabrication of the chip is possible to reduce the stress induced by the stack of the chip. It is also possible to add extra layers above the chip as disclosed in the document US 2010/0078773 Al. The method disclosed in this document is however quite complicated to implement because it requires the making of openings in these extra layers to access the electronic circuit of the chip and it should not have any impact on the behavior of the electronic circuit.

Another solution to compensate the problem of co-planarity between the chip and the support is to use solder bumps with different heights to bond the chip on the support, as proposed in the document US 2014/0306343 Al. With this solution, the bow of the chip is not modified, but it is compensated at the bonding interface between the chip and the support. This method requires a rather complicated process to form the bumps with different heights at the position corresponding to the chip profile.

The document "Development of Glass interposer with fine pitch micro-bumps and bow study depending on several glass substrates with different CTE", K. Mori et al., IMAPS 2014 San Diego" proposes using a support having a CTE close to that of the chip to obtain an equivalent deformation of the two parts of the assembly. The curvature, or the bow, of the chip is not modified, but it is compensated by a similar curvature of the support. However, this solution is not always possible, in particular in the case of a stacking of two silicon chips together.

To correct the curvature of the chip, it is also possible to make the assembly of the chip and the support under mechanical pressure in order to flatten both parts of the assembly by thermocompression. In this case, the stress of the chip is however not compensated and reliability problems can occur later.

In order to balance the stress induced by a multilayer film stack arranged on a front face of a substrate, documents US 2004/0092052 Al and US 2006/0245056 Al propose to arrange one or several layers on the rear face of the
substrate. The solutions proposed in these documents are however not suitable to compensate a deformation of a chip intended to be subject to different temperatures, as during a soldering of the chip.

**DESCRIPTION OF THE INVENTION**

Thus there is a need to find a way to compensate the deformation of the chip at different temperatures without the drawbacks of the prior art solutions, e.g. in a temperature range equal to that necessary to achieve a soldering or a bonding of the chip on a support, typically between around 20°C and 260°C.

The invention thus proposes a chip comprising at least:

- a first substrate;
- a first electronic and/or mechanical circuit arranged in and/or on a front face of the first substrate;
- a first deformation compensation layer suitable for compensating a deformation of the chip at room temperature;
- a second deformation compensation layer suitable for compensating a deformation of the chip between the room temperature and a first temperature higher than the room temperature;

and wherein the first and second deformation compensation layers are stacked on a rear face of the first substrate.

The first and second deformation compensation layers enable to compensate statically, at room temperature, and dynamically, according to the temperature undergone by the chip and up to the first temperature, for example for a wide range of temperature between room temperature and 260°C, a stress induced in the chip by the electronic and/or mechanical circuit (which can comprise various materials with various CTE) arranged at the front face of the first substrate. It is thus possible to make a face-to-face assembly of the chip on a support, for example by a soldering carried out at the first temperature, without problem of co-planarity between the chip and the support.
The deformation compensation layers enable to obtain, between the room temperature and the first temperature, a deformation variation, or deflection variation, close to 0, or highly reduced compared to the deformation of a similar chip but without the deformation compensation layers.

The stress induced at room temperature by the first deformation compensation layer on the first substrate may balance the stress induced at room temperature by the other elements of the chip on the first substrate, that is the stress induced at least by the first electronic and/or mechanical circuit and by the second deformation compensation layer on the first substrate.

An advantage of this chip is that the deformation compensation layers are located on a side (rear face) of the first substrate opposite to the one on which the electronic and/or mechanical circuit is located. The deformation compensation layers have thus no impact on the behavior and the features of the electronic and/or mechanical circuit.

The chip may correspond to an electronic or microelectronic or mechanical or micromechanical chip. The expression "electronic and/or mechanical circuit" also designates a microelectronic and/or micromechanical circuit, and the circuit may comprise one or several MOS devices and/or one or several MEMS and/or NEMS devices.

The invention concerns advantageously a thinned microelectronic chip, e.g. thin pixel modules 3D assembly.

The deformation compensation layers can be made at wafer-scale simultaneously for several chips made on a single wafer, and thus with a good reproducibility and a low cost.

Another advantage is that the deformation compensation layers can be made with the implementation of classical microelectronic deposition techniques.

The expression "room temperature" corresponds for example to a temperature between around 20°C and 26°C.

The first temperature may correspond to the highest temperature to which the chip is intended to be exposed during a securing of the first substrate with a
second substrate, or during a securing of the chip with a support, or during operation of
the chip. The securing may correspond to a bonding or a soldering with solder balls.

The first temperature may be higher or equal to around 150°C, which corresponds for example to the lower temperature of soldering used in microelectronics using indium metal. This first temperature may be higher or equal to around 240°C, which corresponds to the temperature for conventional soldering process using lead free solder composed of tin and silver.

The first deformation compensation layer may be arranged between the substrate and the second deformation compensation layer.

A ratio between a coefficient of thermal expansion of a material of the first deformation compensation layer and a coefficient of thermal expansion of a material of the first substrate is between 0.9 and 1.1, and/or a ratio between a coefficient of thermal expansion of a material of the second deformation compensation layer and a coefficient of thermal expansion of a material of the first substrate is less than 0.9 or higher than 1.1.

The first deformation compensation layer may comprise a dielectric material and/or the second deformation compensation layer may comprise a metal.

Advantageously, the first deformation compensation layer is arranged between the substrate and the second deformation compensation layer, and the first deformation compensation layer comprises a dielectric layer. Thus, in addition to its deformation compensation effect at room temperature, the first deformation compensation layer also provides an electrical insulation between the substrate and the second deformation compensation layer, especially when the second deformation compensation layer comprises a conductive material, e.g. a metallic material.

The chip may further comprise a first adhesive and/or barrier layer arranged against the first deformation compensation layer and between the first deformation compensation layer and the substrate, and/or a second adhesive and/or barrier layer arranged against the second deformation compensation layer and between the second deformation compensation layer and the substrate.
The thickness of the first substrate may be less than or equal to around 300 \( \mu \text{m} \), and preferentially less than or equal to around 200 \( \mu \text{m} \), in order to improve the efficiency of the deformation compensation layers.

For an optimal effect of the first deformation compensation layer, a difference between the value of the coefficient of thermal expansion of the material of the first substrate and the value of the coefficient of thermal expansion of the material of the first deformation compensation layer is less than 1. If this difference is higher than 1, the first deformation compensation layer may also have an effect on the dynamical deformation with the temperature.

The chip may further comprise a protective layer arranged on a stack formed by at least the first and second deformation compensation layers.

The chip may further comprise at least:
- a second substrate stacked on the first substrate;
- a second electronic and/or mechanical circuit arranged in and/or on a front face of the second substrate.

The stacking of the second substrate on the first substrate may correspond to a bonding or a soldering of the front face of each of these substrates one onto the other.

In this case, the chip may further comprise at least a third and a fourth deformation compensation layers stacked on a rear face of the second substrate, wherein the first and third deformation compensation layers are together suitable for compensating a deformation of the chip at room temperature, and wherein the second and fourth deformation compensation layers are together suitable for compensating a deformation of the chip between the room temperature and the first temperature.

The invention also concerns a device comprising at least:
- a chip as above-described;
- a support onto which the chip is stacked.

The stacking of the chip on the support may correspond to a bonding or a soldering of the chip on the support.
The invention also concerns a method for making a chip, comprising at least the following steps:

- making a first electronic and/or mechanical circuit in and/or on a front face of a first substrate;
- making a first deformation compensation layer suitable for compensating a deformation of the chip at room temperature;
- making a second deformation compensation layer suitable for compensating a deformation of the chip between the room temperature and a first temperature higher than the room temperature;

and wherein the first and second deformation compensation layers are stacked on a rear face of the first substrate.

The making of the first deformation compensation layer may include at least:

- a step of calculating a deformation induced at room temperature at least by the first electronic and/or mechanical circuit and by the second deformation compensation layer on the first substrate;
- a step of determining at least a thickness, deposition conditions and a material of the first deformation compensation layer such that a deformation induced at room temperature by the first deformation compensation layer on the first substrate compensates the deformation induced at room temperature by the first electronic and/or mechanical circuit and by the second deformation compensation layer on the first substrate.

The making of the second deformation compensation layer may include at least:

- a step of calculating a deformation induced between the room temperature and the first temperature at least by the first electronic and/or mechanical circuit and by the first deformation compensation layer on the first substrate;
- a step of determining at least a thickness, deposition conditions and a material of the second deformation compensation layer such that a deformation induced between the room temperature and the first temperature by the second deformation
compensation layer on the first substrate compensates the deformation induced between the room temperature and the first temperature by the first electronic and/or mechanical circuit and by the first deformation compensation layer on the first substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

This invention will be understood easier in view of the examples of embodiments provided purely for indicative and non-limiting purposes, in reference to the appended drawings wherein:

- Figure 1 shows a chip according to a particular embodiment of the invention;
- Figures 2 and 3 show deflection measurements for illustrating the effect of the deformation compensation layers on the deflection of the chip for a given range of temperature;
- Figure 4 shows a device comprising a chip according to a particular embodiment of the invention.

Identical, similar or equivalent parts of the different figures described below have the same numeric references for the sake of clarity between figures.

The different parts shown in the figures are not necessarily drawn to scale, so as to make the figures more comprehensible.

The different possibilities (alternatives and embodiments) must not be understood to mutually exclude each other and can, thus, be combined with each other.

DETAILED DESCRIPTION OF PARTICULAR EMBODIMENTS

Figure 1 shows a chip 100 according to a particular embodiment.

The chip 100 comprises a substrate 102 having a front face 104 and a rear face 106 opposite one to the other. The substrate 102 comprises here a semiconductor, e.g. silicon.

The chip 100 also comprises an electronic circuit 108 formed by several electronic devices, e.g. transistors and/or other active devices, formed at the front face 104 of the substrate 102. The circuit 108 can also comprise mechanical devices like
MEMS / NEMS devices. The circuit 108 is here electrically connected to several interconnection layers 110 surrounded by IMD (Inter-Metal Dielectric) layers 112. The chip 100 also has connection pads 114, corresponding to solder balls, pillars or bumps, to which the interconnection layers 110 are electrically connected. The connection pads can be made by electroplating deposition through thick resist mask on a Ti/Cu seed layer. The connection pads 114 will be used, once the chip 100 is achieved, to report the chip 100 on a support or on another element (e.g. an interposer), for example by flip-chip. This report can be carried out after a dicing of the chip 100 (several chips 100 are here made simultaneously on a single wafer).

The circuit 108, the interconnection layers 110, the IMD layers 112 and the connection pads 114 are made at the front face 104 of the substrate 102. Then the connection pads 114 are bonded to a temporary handling layer 116 thanks to an adhesive layer 118 surrounding the connection pads 114. The temporary handling layer 116 forms a temporary mechanical support of the chip 100 for the making of deformation compensation layers on the rear face 106 of the substrate 102. Such temporary handling layer 116 is used as the desired thickness of the chip is here low (less than around 200 μm).

Once the bonding to the temporary handling layer 116 is achieved, the substrate 102 is thinned to the desired thickness, for example between about 200 μm and 100 μm, or even less, and for example equal to around 100 μm. This thinning can be obtained by backgrinding of the rear face of the substrate 102, eventually followed by CMP (Chemical-Mechanical Planarization) to obtain a rear face 106 having a mirror type surface state (that is having very small roughness). Such CMP also removes a superficial layer of the substrate damaged by the backgrinding which creates a stress in the structure.

The making of the different elements on the front face 104 of the substrate 102 induces a mechanical stress which involves a deformation of the chip 100. This stress is a consequence of the deposits of various materials like polysilicon, dielectrics (e.g. silicon oxide, silicon nitride) and metals (e.g. tungsten, titanium, tantalum, copper, aluminum) on the substrate 102, these materials having CTE which are different
than that of the material of the substrate 102, which is generally silicon. In addition, the deposits of these materials are carried out at various temperatures according to the type of the deposits.

When a layer is deposited on a substrate, a stress is generated in the substrate. This stress has different origins, or different components: the intrinsic stress and the thermal stress.

The intrinsic stress appears during the deposit of the layer. It is different than the thermal stress because it is present at the deposition temperature and exists even when there is no differential dilatation effect between the layers which are already present on the substrate. The intrinsic stress depends on the type of the deposit (CVD, PVD, epitaxy, ...), the conditions of the deposit (speed, pressure, plasma power, ...), and the characteristics of the layer (material, stoichiometry). It involves various micro-structural actions like particles growing, inter-diffusion or re-crystallization phenomenon.

The intrinsic stress generated by a layer deposit can be calculated by using so-called "Stoney model" which expresses the stress $\sigma_f$ of the deposited layer according to the following equation (when the thickness of deposited layer is low compared to the thickness and the lateral dimensions of the substrate onto which the layer is deposited):

$$
\sigma_f = \frac{E_s t_s^2}{6. R. t_f}
$$

with:

- $E_s$: reduced modulus of the substrate;
- $t_s$: thickness of the substrate;
- $t_f$: thickness of the deposited layer;
- $R$: radius of curvature of the substrate.

Concerning the thermal stress, each layer having its own coefficient of thermal expansion, the stack of the different layers has a non-zero curvature which depends on the temperature also corresponding to equilibrium of the forces and moments applied in each point of the structure at a given temperature. The deflection,
called Bow, variation created during a temperature variation is calculated according to the following formula:

\[ Bow = \frac{3 \Delta T L^2 \cdot E_f A a}{4 \cdot f_s L^2 E_s} \]  

(2)

With:

\( \Delta T \): temperature variation;
\( L \): width (diameter) of the substrate;
\( E_f \): Young’s modulus of the deposited layer;
\( \Delta \alpha \): CTE of the deposited layer - CTE of the substrate.

In the above equations (1) and (2), the physical properties (thickness, width, radius) and the thermo-mechanical properties (Young’s modulus, reduced modulus, CTE) of the layers and of the substrate can be determined by independent experimental methods. For modulus, nano-indentation technique can be used for thin film measurement, as described in the document "An improved technique for determining hardness and elastic modulus using load and displacement sensing indentation experiments", W.C. Olivier and G.M. Pharr, J. Mater. Res., vol. 7, n°6, June 1992, pp. 1564-1583. For CTE determination, deformation with temperature can be used as disclosed in the document "Mechanical characterization and modeling of thin films for processing of microelectronic devices - application to the field of 3D integration", H. Issele, Thesis, Grenoble University, 2014.

Without deformation compensation layers, the Bow of a chip may be positive at room temperature and negative during a bonding process (e.g. soldering) of the chip on a support.

At least two deformation compensation layers are made on the rear face 106 of the substrate 102 in order to compensate the stress and the deflection (Bow) induced by the element arranged on the substrate 102 between room temperature and a desired first temperature, e.g. the maximum temperature at which the chip 100 is exposed during soldering of the chip 100 on a support.

A first deformation compensation layer 120 is made, e.g. by deposition, on the rear face 106 of the substrate 102. This first deformation compensation layer 120
forms a static deformation compensation layer and is such that the deformation, or deflection or Bow, of the chip 100 (that is including all the layers of the chip 100) is close to 0 at room temperature. To obtain such deformation compensation, the first deformation compensation layer 120 induces a stress, at room temperature, on the substrate 102 which compensates the deformation of the substrate 102 generated by the stress induced by all the other elements 108, 110, 112, 114 located at the front face 104 but also by the stress of other layers (especially the second deformation compensation layer 124) located on the first deformation compensation layer 120 (which are described below). The determination of the desired stress for the first deformation compensation layer 120 is obtained by measuring the Bow of the chip 100 before the deposition of the first deformation compensation layer 120, e.g. by confocale spectroscopy, and by simulation using the Stoney model, that is the above equation (1). It is possible to verify experimentally the value of the Bow of the chip 100 after the making of the first deformation compensation layer 120 and, if necessary, to adjust the stress to obtain a Bow close to 0. The adjustment is made by modifying the characteristics of the first deformation compensation layer such as its thickness or its intrinsic stress. The simulation model allows predicting the resulting bow of the chip after deposition of the first deformation compensation layer with its associated characteristics.

The desired stress for the first deformation compensation layer 120 is obtained by varying the intrinsic stress of the deposition of the first deformation compensation layer 120 and also by varying the thickness of the first deformation compensation layer 120. The intrinsic stress of the deposition can be modified by varying the deposition conditions such as the RF power for generating the plasma, or the pressure inside the chamber for example, and the stoichiometry of the deposited material. The CTE of the material of the first deformation compensation layer 120 is close to that of the material of the substrate 102, and thus the stress induced by the first deformation compensation layer 120 on the substrate 102 remains sensibly constant when the temperature of the chip 100 varies. For instance, the difference of CTE between the layer 120 and the substrate 102 is within a range of +/- 10%.
The first deformation compensation layer 120 may correspond to one layer or a stack of at least two different layers. This or these layers can comprise dielectric materia l(s) such as SiO₂, Si₃N₄ or Mg₃Θ (meta llic oxide) deposited by chemical deposition (CVD) or physical deposition (PVD), and with a thickness between about 0.1 µm and 10 µm.

In the particular embodiment shown in fig. 1, a first adhesive and/or barrier layer 122 is first made on the rear face 106 of the substrate 102, and the first deformation compensation layer 120 is then deposited on this layer 122. According to the material of the layer 122, it improves the adhesion of the first deformation compensation layer 120 to the substrate 102 and/or forms a barrier to the diffusion of atoms between the first deformation compensation layer 120 and the substrate 102. This layer 122 can be a thin SiO₂ film for example. The thickness of the layer 122 is advantageously at least 10 times less than the thickness of the first deformation compensation layer 120. The thermo-mechanical effect of the layer 122 on the chip 100 is insignificant.

As a variant of this particular embodiment, it is possible that the chip 100 doesn't include the first adhesive and/or barrier layer 122. In this case, the first deformation compensation layer 120 is deposited directly on the rear face 106 of the substrate 102.

A second deformation compensation layer 124 is made, e.g. by deposition, on the first deformation compensation layer 120. This layer 124 forms a temperature dynamic deformation compensation layer and is such that the deformation, or the Bow, of the chip 100 (that is including all the layers of the chip 100) is maintained close to 0 between the room temperature and another temperature, called first temperature, higher than the room temperature and corresponding to a maximum temperature to which the chip 100 is intended to be exposed. This first temperature can correspond to the maximum temperature necessary to achieve a soldering of the chip 100 on a support, for example 260°C. This first temperature can be lower than 260°C, for example 150°C at the lowest soldering temperature conventionally used. To obtain such deformation compensation, the material of the second deformation compensation layer 124 and its thickness are chosen such that its thermal expansion compensates the
thermal expansion of the other elements of the chip 100, especially the elements located on the front face 104 of the substrate 102. The material of the second deformation compensation layer 124 is chosen according to the desired value for the CTE of this material. A measure, e.g. by confocal spectroscopy, of the Bow variation according to the temperature at which the chip 100 is exposed after the deposition of the second deformation compensation layer 124 is used to verify the dynamic compensation of this layer 124 and eventually to adjust its features to obtain of Bow variation close to 0. The criteria for a good compensation is achieved when the yield of the connections between the chip and the substrate is at 100% meaning that the co-planarity is good enough to warranty that all the connections are functional. There is a tolerance on the co-planarity to obtain such a result since the soldering process has some tolerance depending on the type of the interconnections.

The second deformation compensation layer 124 can correspond to one layer or a stack of at least two different layers. This or these layers can comprise high CTE material, e.g. metal(s) such as titanium, copper, aluminum, tantalum, AlSi, and/or metallic oxide(s) such as TiO, Al2O3, and/or metal nitrides such as AlN, TiN, TaN, ... The thickness of the layer 124 can be between about 0.1 μm and 10 μm.

In the particular embodiment shown in figure 1, a second adhesive and/or barrier layer 126 is made on the first deformation compensation layer 120, and the second deformation compensation layer 124 is then deposited on the layer 126. According to the material of the layer 126, it improves the adhesion of the second deformation compensation layer 124 to the first deformation compensation layer 120 and/or forms a barrier to the diffusion of atoms between the first and second deformation compensation layers 120 and 124. In this embodiment, the layer 126 corresponds to a titanium layer. Other diffusion layers such as TiN, TaN, WN can also be used. The thickness of the layer 126 is at least 10 times less than the thickness of the second deformation compensation layer 124. The thermo-mechanical effect of the layer 126 on the chip 100 is insignificant.

As a variant of this particular embodiment, it is possible that the chip 100 doesn't include the second adhesive and/or barrier layer 126. In this case, the second
deformation compensation layer 124 is deposited directly on the first deformation compensation layer 120.

Figure 2 shows the effect of the first deformation compensation layer 120 on the deflection, or Bow, of the chip 100 during a temperature variation between room temperature and the first temperature here equal to 260°C. The heating rate is here equal to 10°C/min and the cooling rate is the natural cooling of the experiment (heater off). Curve 10 represents the Bow of the chip 100 when the first deformation compensation layer 120 is not present on the rear face 106 of the substrate 102 (only the second deformation compensation layer 124 corresponding to an AISi layer having a thickness equal to 2 μm is arranged on the rear face 106). Curve 20 represents the Bow of the chip 100 when the first deformation compensation layer 120 (here corresponding to a compressive SiN layer having a thickness equal to 2 μm and deposited by CVD at 200°C, such layer having a Young's modulus equal to 45 GPa and a CTE equal to 2.7 \times 10^{-6} \text{ K}^{-1}, generating a compressive stress equal to -176 MPa) is added on the rear face 106, between the substrate 102 and the second deformation compensation layer 124. This figure 2 shows that the addition of the first deformation compensation layer 120 changes the value of the Bow similarly whatever the temperature, thus without impacting the dynamic behavior of the Bow. Thus the first deformation compensation layer 120 can be seen as defining the "offset" value of the chip deflection. In view of the example shown in figure 2, the thickness of the SiN layer 120 can be adjusted to obtain 0 offset of the Bow at room temperature.

Figure 3 shows the effect of the second deformation compensation layer 124 on the Bow of the chip 100 during a temperature variation between room temperature and the first temperature here equal to 260°C. Curve 30 represents the Bow of the chip 100 when the deformation compensation layers 120, 124 are not made on the rear face 106 of the substrate 102. Curve 40 represents the Bow of the chip 100 when a first deformation compensation layer 120, here corresponding to compressive SiN layer having a thickness equal to 0.5 μm, and a second deformation compensation layer 124, here corresponding to an AISi layer having a thickness equal to 4 μm and deposited by PVD at 175°C (having a Young's modulus equal to 66 GPa and a CTE equal to 19.6 \times 10^{-6} \text{ K}^{-1},

...
generating a tensile stress at room temperature equal to 90 MPa), are made on the rear face 106 of the substrate 102 (for the curve 40, an adhesive layer 126 comprising titanium is formed between the first and second deformation compensation layers 120 and 124). This figure shows that the addition of the first and second deformation compensation layers 120 and 124 leads to a partial compensation of the Bow variation when the temperature changes between room temperature and the first temperature.

In the embodiment previously described, the first deformation compensation layer 120 is arranged between the substrate 102 and the second deformation compensation layer 124. However, it is possible that the second deformation compensation layer 124 is first made on the substrate 102, and then that the first deformation compensation layer 120 is made on the second deformation compensation layer 124. In this case, the second deformation compensation layer 124 is arranged between the substrate 102 and the first deformation compensation layer 120. Moreover, the second adhesive and/or barrier layer 126 can be arranged or not between the substrate 102 and the second deformation compensation layer 124, and the first adhesive and/or barrier layer 122 can be arranged or not between the first and second deformation compensation layers 120 and 124. However, the arrangement of the first and second deformation compensation layers 120 and 124 as shown in figure 1, that is such that the first deformation compensation layer 120 is arranged between the substrate 102 and the second deformation compensation layer 124, is advantageously made, especially when the first deformation compensation layer 120 comprises a dielectric material which insulates electrically and physically the substrate 102 from the second deformation compensation layer 124 which can comprise a conductive material, e.g. a metal. In addition, the thermal expansion of the second deformation compensation layer 124 is reduced if this layer 124 is arranged between the substrate 102 and the first deformation compensation layer 120.

In the embodiment shown in figure 1, the chip 100 also comprises a protective layer 128 arranged above the last deformation compensation layer (the second deformation compensation layer 124 in the embodiment of figure 1) in order to protect this last layer from the external environment (oxidation, humidity, ...) and thus keeps its
properties all long of the lifetime of the chip 100. The thickness of the layer 128 is at least 10 times less than the thickness of the first deformation compensation layer 120. The thermo-mechanical effect of the layer 128 on the chip 100 is insignificant.

The depositions for making the different layers on the rear face 106 of the substrate 102 are carried out at temperatures which are compatible with the bonding of the chip 100 on the temporary handling layer 116, for example at temperatures less than around 200°C.

Once all the elements previously described are made, the temporary handling layer 116 and the adhesive layer 118 are removed. The wafer into which the chip 100 is made is diced in order to obtain several unitary chips. Each chip 100 can then be reported on a support through the connection pads 114, e.g. by soldering, without deformation problems given that each chip 100 comprises the deformation compensation layers 120, 124.

The chip 100 previously described comprises one substrate 102. As a variant embodiment, it is possible that the chip 100 comprises at least a second substrate, that is several substrates bonded one onto the other by direct bonding, or by the use of adhesive layers or connection pads. In this case, the first and second deformation compensation layers 120 and 124 can be arranged on one side (the side onto which no circuit is made) of one of the substrates, and these first and second deformation compensation layers 120, 124 are in this case designed, in terms of number, deposition conditions, materials, stoichiometry, thicknesses, such that these layers compensate the deformation of all the substrates of the chip 100. In a variant, it is possible that the passive side of each substrate is covered by a stack of deformation compensation layers similar to the stack formed by the first and second deformation compensation layers 120, 124 and able to compensate the static deformation (at room temperature) and the temperature dynamic deformation (up to the first temperature) of said substrate. For example, a first substrate can comprise a first side forming an active side with electronic circuits, and a second side onto which stress compensation layers are arranged. A second substrate can also comprise a first side forming an active side with electronic circuits, and
a second side onto which stress compensation layers are arranged. The active sides of the first and second substrates are bonded one to the other, for example with solder balls.

Several chips similar to the chip 100 can be made collectively on a single wafer. The chips are then diced, and each chip can be reported on a support, e.g. by flip-chip. Figure 4 shows a device 1000 comprising a chip 100 bonded by flip-chip on a support 1002. The connection pads 114 of the chip 100 here connect mechanically the chip 100 to the support 1002. These connection pads 114 also connect electrically the electronic devices 108 to the support 1002.
CLAIMS

1. A chip (100) comprising at least:
   - a first substrate (102);
   - a first electronic and/or mechanical circuit (108) arranged in and/or on a front face (104) of the first substrate (102);
   - a first deformation compensation layer (120) suitable for compensating a deformation of the chip (100) at room temperature;
   - a second deformation compensation layer (124) suitable for compensating a deformation of the chip (100) between the room temperature and a first temperature higher than the room temperature;
   and wherein the first and second deformation compensation layers (120, 124) are stacked on a rear face (106) of the first substrate (102).

2. The chip (100) according to claim 1, wherein the first temperature corresponds to the highest temperature to which the chip is intended to be exposed during a securing of the first substrate with a second substrate, or during a securing of the chip with a support, or during operation of the chip (100).

3. The chip (100) according to one of previous claims, wherein the first temperature is higher or equal to around 150°C.

4. The chip (100) according to one of previous claims, wherein the first deformation compensation layer (120) is arranged between the substrate (102) and the second deformation compensation layer (124).

5. The chip (100) according to one of previous claims, wherein a ratio between a coefficient of thermal expansion of a material of the first deformation compensation layer (120) and a coefficient of thermal expansion of a material of the first substrate (102) is between 0.9 and 1.1, and/or wherein a ratio between a coefficient of
thermal expansion of a material of the second deformation compensation layer (124) and a coefficient of thermal expansion of a material of the first substrate (102) is less than 0.9 or higher than 1.1.

6. The chip (100) according to claim 5, wherein the first deformation compensation layer (120) comprises a dielectric material and/or wherein the second deformation compensation layer (124) comprises a metal.

7. The chip (100) according to one of previous claims, further comprising a first adhesive and/or barrier layer (122) arranged against the first deformation compensation layer (120) and between the first deformation compensation layer (120) and the substrate (102), and/or a second adhesive and/or barrier layer (126) arranged against the second deformation compensation layer (124) and between the second deformation compensation layer (124) and the substrate (102).

8. The chip (100) according to one of previous claims, wherein the thickness of the first substrate (102) is less than or equal to around 200 μm.

9. The chip (100) according to one of previous claims, further comprising a protective layer (128) arranged on a stack formed by at least the first and second deformation compensation layers (120, 124).

10. The chip (100) according to one of previous claims, further comprising at least:
- a second substrate stacked on the first substrate (102);
- a second electronic and/or mechanical circuit arranged in and/or on a front face of the second substrate.

11. The chip (100) according to claim 10, further comprising at least a third and a fourth deformation compensation layers stacked on a rear face of the second
substrate, wherein the first and third deformation compensation layers are together suitable for compensating a deformation of the chip (100) at room temperature, and wherein the second and fourth deformation compensation layers are together suitable for compensating a deformation of the chip (100) between the room temperature and the first temperature.

12. A device (1000) comprising at least:
   - a chip (100) according to one of previous claims;
   - a support (1002) onto which the chip (100) is stacked.

13. A method for making a chip (100), comprising at least the following steps:
   - making a first electronic and/or mechanical circuit (108) in and/or on a front face (104) of a first substrate (102);
   - making a first deformation compensation layer (120) suitable for compensating a deformation of the chip (100) at room temperature;
   - making a second deformation compensation layer (124) suitable for compensating a deformation of the chip (100) between the room temperature and a first temperature higher than the room temperature;
   and wherein the first and second deformation compensation layers (120, 124) are stacked on a rear face (106) of the first substrate (102).

14. The method according to claim 13, wherein the making of the first deformation compensation layer (120) includes at least:
   - a step of calculating a deformation induced at room temperature at least by the first electronic and/or mechanical circuit (108) and by the second deformation compensation layer (124) on the first substrate (102);
   - a step of determining at least a thickness, deposition conditions and a material of the first deformation compensation layer (120) such that a deformation induced at room temperature by the first deformation compensation layer (120) on the
first substrate (102) compensates the deformation induced at room temperature by the
first electronic and/or mechanical circuit (108) and by the second deformation
compensation layer (124) on the first substrate (102).

15. The method according to one of claims 13 or 14, wherein the
making of the second deformation compensation layer includes at least:

- a step of calculating a deformation induced between the room
temperature and the first temperature at least by the first electronic and/or mechanical
circuit (108) and by the first deformation compensation layer (120) on the first substrate
(102);

- a step of determining at least a thickness, deposition conditions and a
material of the second deformation compensation layer (124) such that a deformation
induced between the room temperature and the first temperature by the second
deformation compensation layer (124) on the first substrate (102) compensates the
deformation induced between the room temperature and the first temperature by the
first electronic and/or mechanical circuit (108) and by the first deformation compensation
layer (120) on the first substrate (102).
### INTERNATIONAL SEARCH REPORT

**International application No**
PCT/IB2015/000500

**A. CLASSIFICATION OF SUBJECT MATTER**

INV. H91L23/00
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

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<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
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- **X** Further documents are listed in the continuation of Box C.  
- **X** See patent family annex.

- **A** document defining the general state of the art which is not considered to be of particular relevance
- **E** earlier application or patent but published on or after the international filing date
- **L** document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another invention or other special reason (as specified)
- **O** document referring to an oral disclosure, use, exhibition or other means
- **P** document published prior to the international filing date but later than the priority date claimed

**Date of the actual completion of the international search**
30 November 2015

**Date of mailing of the international search report**
08/12/2015

**Name and mailing address of the ISA/European Patent Office, P.B. 5818 Patentioon 2 NL-2280 HV Rijswijk**
Tel (010-70) 540-2040, Fax (010-70) 340-3016

**Authorized officer**
Edmeades, Michael

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