

Jan. 7, 1964

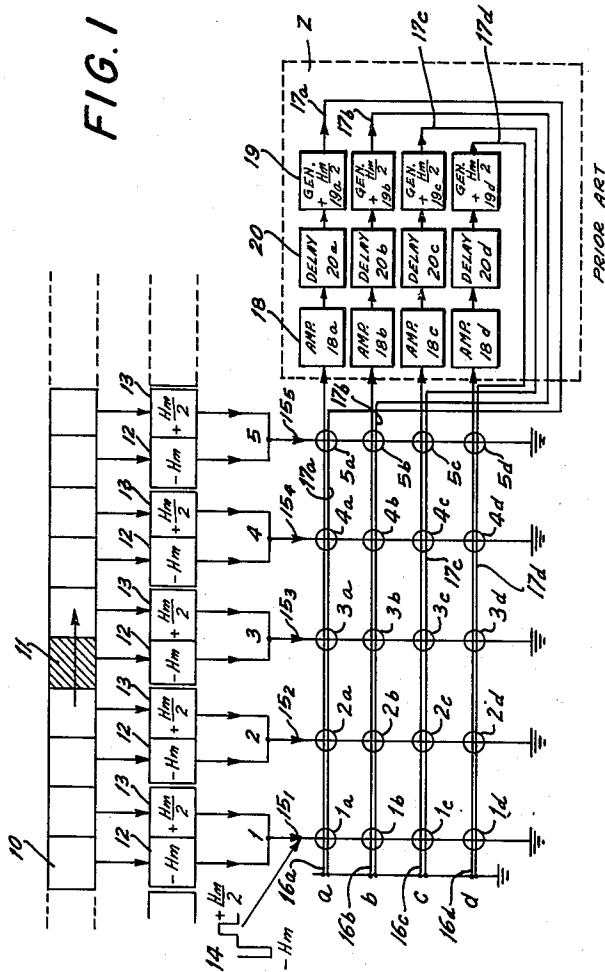
G. WOLF

3,117,309

ARRANGEMENT FOR CONTROLLING A MAGNET CORE MATRIX

Filed Feb. 21, 1962

6 Sheets-Sheet 1



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Jan. 7, 1964

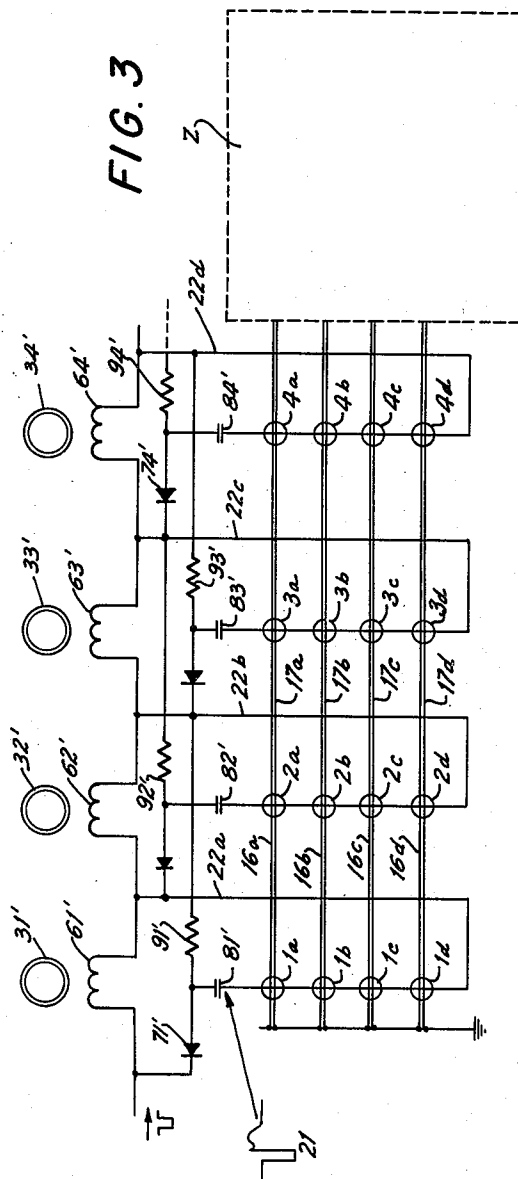
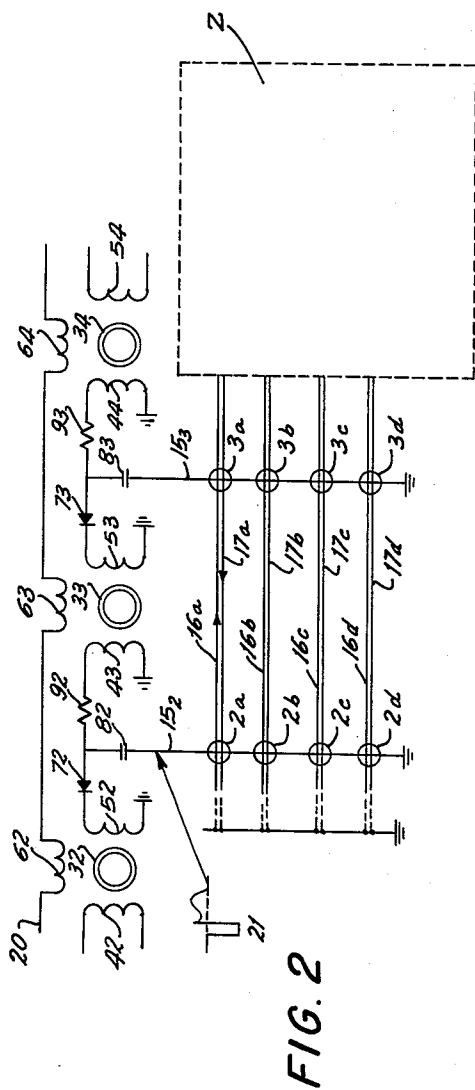
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ARRANGEMENT FOR CONTROLLING A MAGNET CORE MATRIX

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6 Sheets-Sheet 2



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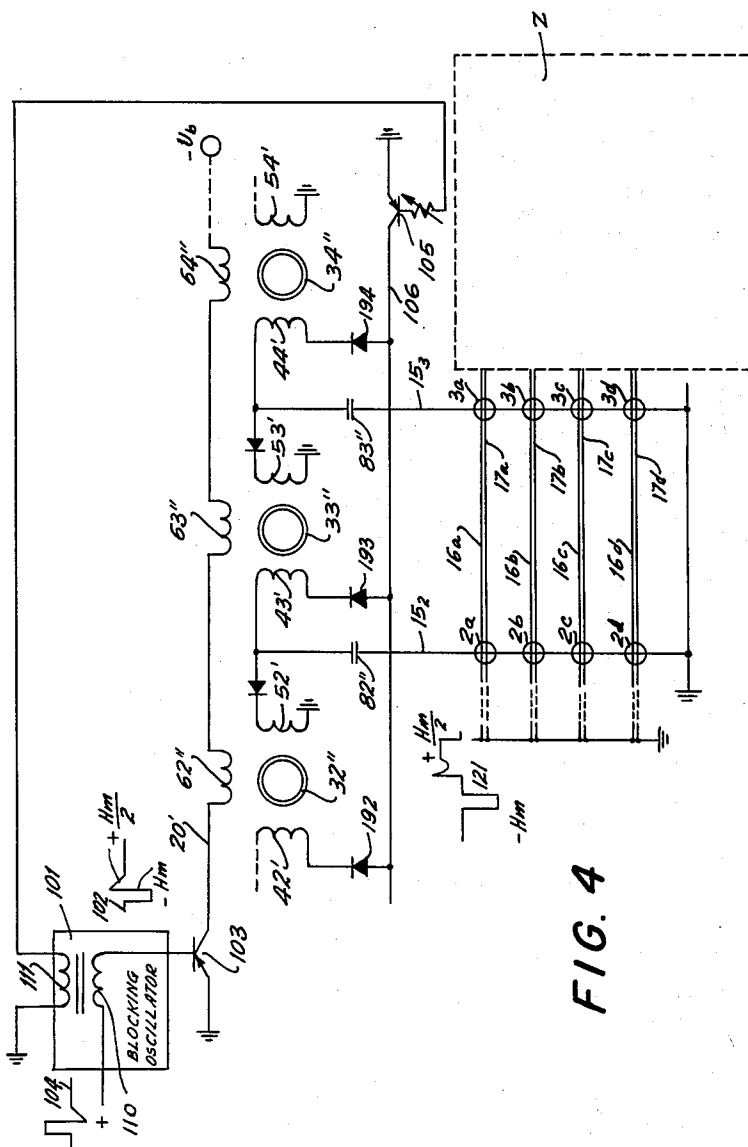
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ARRANGEMENT FOR CONTROLLING A MAGNET CORE MATRIX

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6 Sheets-Sheet 3



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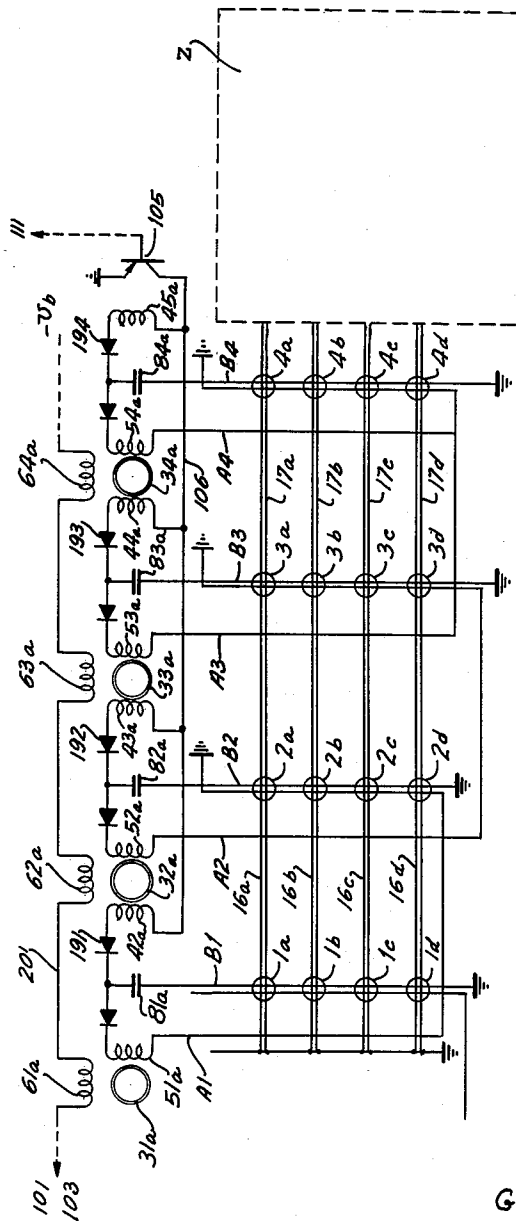
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ARRANGEMENT FOR CONTROLLING A MAGNET CORE MATRIX

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FIG. 5



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ARRANGEMENT FOR CONTROLLING A MAGNET CORE MATRIX

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FIG. 6

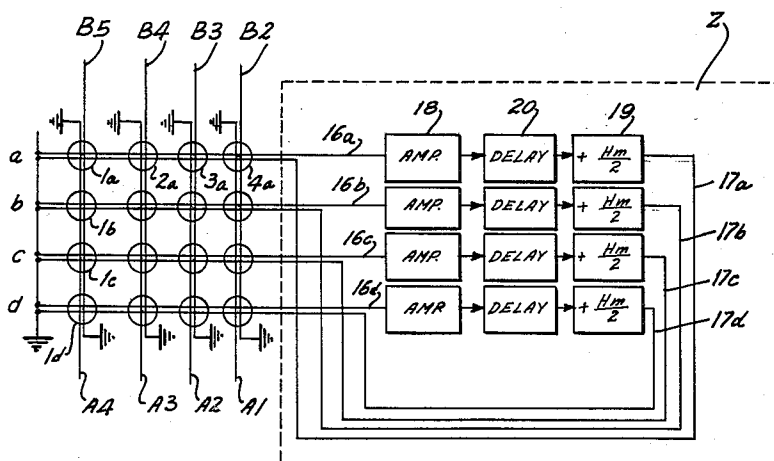


FIG. 6a

BY STEP NO.	STORAGE CONTENT	
	OF COLUMN	15
1	4	OBLITERATED
2	3	SHIFTED TO 4
3	2	" " 3
4	1	" " 2

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ARRANGEMENT FOR CONTROLLING A MAGNET CORE MATRIX

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FIG. 7

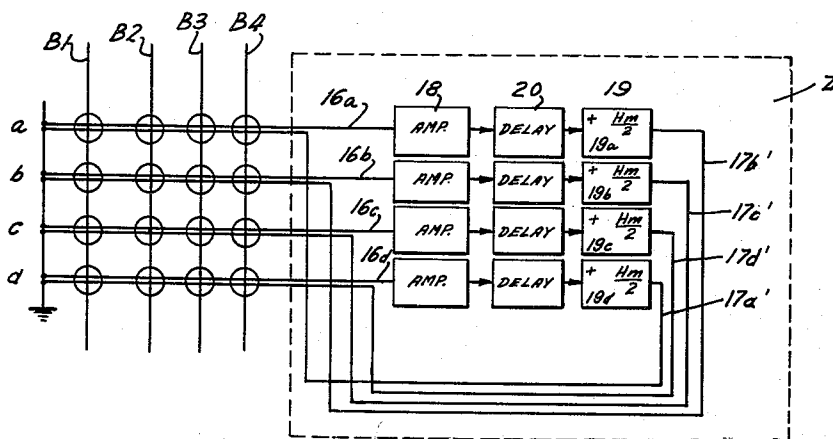


FIG. 5a

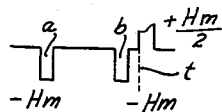
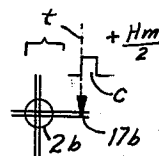


FIG. 5b



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ARRANGEMENT FOR CONTROLLING A MAGNET CORE MATRIX

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Filed Feb. 21, 1962, Ser. No. 174,779

Claims priority, application Germany Feb. 23, 1961

6 Claims. (Cl. 340—174)

The present invention concerns a magnet core matrix, and more particularly an arrangement for subjecting such a matrix to "non-obliterating read-out" by which information stored in the matrix is first read out and thereafter immediately re-introduced and stored again in the matrix.

Magnet core matrices are being used extensively as storage means in the field of electronic calculating machines. These matrices comprise a plurality of magnet cores of annular shape and made of material having a substantially rectangular hysteresis characteristic. As is well known, these cores can be changed between magnetic saturation of one polarity representing information storage and a magnetic saturation of opposite polarity representing no-information storage. For changing the magnetic saturation by the application of suitable pulses and for reading out stored information by application of other pulses column wires are arranged extending through the cores of each column thereof, and row wires are arranged extending through the cores of each row thereof.

There are various ways of operating such a matrix. For instance, information stored in the matrix is read out and is thereafter re-introduced and stored again at the same core from which it was first read out. It is further possible to read out information stored, e.g., in a particular column and to transmit such information to another device for the purpose of carrying out a calculating operation. Thereafter a new information, preferably a portion of the result of the calculating operation, is introduced into the matrix and stored in the particular column from which the first mentioned information has been read out. Moreover, one can read out information stored at a particular point of the matrix and re-store this information at a different point of the same matrix. This last mentioned procedure serves to shift digital values or other information within the matrix.

All the above examples of modes of operation have the common feature that first stored information is read out and thereafter information is stored again in the matrix.

While the structure of the matrix itself is comparatively simple, it has been found that the known arrangements for reading out and re-storing information are rather complicated and require great numbers of components.

It is therefore one object of this invention to provide for an arrangement in which the means for reading out and for re-storing information in a matrix are comparatively simple and require only a small number of components.

It is a further object of this invention to provide for an arrangement of the type set forth which may be operated at high speeds and is entirely reliable in operation.

With above objects in view the invention includes in an arrangement of the type set forth, in combination, matrix means comprising a plurality of magnet cores arranged in a plurality of rows and in a plurality of columns and being individually changeable from information storage representing magnetic saturation of one polarity to no-information storage representing magnetic saturation of opposite polarity by application thereto of a read-out pulse of one polarity, and changeable from no-information storage representing saturation to information storage rep-

resenting saturation by simultaneous application thereto of two half-re-storing pulses of the opposite polarity, each of said cores delivering an output pulse upon a change thereof to no-information representing saturation; pulse return means connected with said matrix means so as to receive said output pulses from any one of said cores and for returning, upon receiving an output pulse, a first half-re-storing pulse of said opposite polarity to at least one of said cores being in no-information representing saturation and located in at least one of said rows thereof; shift register means having a plurality of stages sequentially energizable by application of a sequence of shift pulses to one stage after the other, respectively, and including energy transfer means for transmitting energy from each stage energized by a shift pulse to the next following stage, said energy transfer involving the appearance of a sequence of consecutive pulses of respectively opposite polarities in the respective transfer means; shift pulse generator means for applying shift pulses to said shift register means; and a plurality of circuit means connecting said energy transfer means respectively with different ones of said columns of cores for channeling each of said sequences of pulses of opposite polarities through the respective columns and for applying out of such pulse sequence the pulse of one polarity as a read-out pulse to at least one of the cores being in information storage representing saturation, and for applying the pulse of opposite polarity as a second half-re-storing pulse to that core to which said first half-re-storing pulse is being applied so as to change this particular core to information storage representing saturation.

The novel features which are considered as characteristic for the invention are set forth in particular in the appended claims. The invention itself, however, both as to its construction and its method of operation, together with additional objects and advantages thereof, will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings, in which:

FIG. 1 is a schematic diagram illustrating a conventional matrix and conventional read-out and re-storing means, for the purpose of explaining the basic principle of the operation;

FIG. 2 is a schematic circuit diagram of one embodiment of the invention including a Woo-type register;

FIG. 3 is a schematic diagram of another embodiment of the invention including a different type of a shift register;

FIG. 4 is a schematic diagram illustrating a further embodiment of the invention including electronic switch means;

FIG. 5 is a schematic diagram illustrating a modification of the embodiment shown by FIG. 4;

FIGS. 5a and 5b are explanatory pulse diagrams illustrating the operation of the arrangement according to FIG. 5;

FIG. 6 is a schematic diagram illustrating a modification of a portion of the arrangement of FIG. 5, serving to shift information within the matrix;

FIG. 6a is a chart illustrating the operation of the arrangement according to FIG. 6; and

FIG. 7 is a further modification of a portion of the arrangement according to FIG. 2, for the purpose of shifting information within the matrix in a different manner.

FIG. 1 illustrates a conventional arrangement which serves to read out information stored in the matrix and to re-introduce this information immediately after the read-out information, or to re-introduce into the matrix the result of a calculating operation.

The illustrated matrix of conventional type comprises a plurality of magnet cores as mentioned above and arranged in rows *a*, *b*, *c*, *d* and in columns 1, 2, 3, 4, 5,

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respectively. Magnet cores having a substantially rectangular hysteresis characteristic, marked 1a to 5d, are located at the respective intersections between rows and columns. While the illustrated example comprises only four rows and five columns it is evident that the following description applies analogously to matrices having any number of rows and of columns.

Since matrices of the above mentioned type are entirely known, and in order not to confuse the drawing, the means for storing information in one or the other of the magnet cores have been purposely omitted. The storing operation is not part of this invention.

A column wire 15₁ . . . 15₅ is respectively associated with each of the columns 1 to 5 and is taken through the cores of the respective column, e.g., wire 15₁ through the cores 1a to 1d. The cores of each row are associated with an output wire taken through the cores of the particular row and marked 16a to 16d, respectively. A second input wire is associated with each of the rows of cores and extends therethrough, these input wires being marked 17a to 17d, respectively.

The above described matrix is supplemented by a pulse returning arrangement Z. This arrangement comprises in association with each of the rows a to d a set of devices 18, 20 and 19 of which the unit 18 is an amplifier, the unit 20 may be a delay device and the unit 19 is a pulse generator. For the purpose of correlation the reference numerals of these devices are provided with a suffix referring to the designation of the respectively associated row a to d. The output lines 16a to 16d are respectively connected with the corresponding amplifier 18a to 18d, respectively. The outputs of the pulse generators 19a to 19d are respectively connected with the corresponding input lines 17a to 17d.

It may be assumed that information is stored in the matrix by positive magnetization of the respective core or cores by production of a magnetic field strength +Hm. If now in the above described arrangement information stored in one of the cores is to be read out, a negative impulse is to be applied to the respective one of the column lines 15₁ to 15₅ in order to produce a magnetic field strength -Hm. The reversal of the magnetic saturation of the particular core creates an E.M.F. which is applied as an output pulse through the respective one of the lines 16a to 16d to the corresponding read-out amplifier 18a to 18d. If now the information thus obliterated from the particular core is to be re-introduced into the matrix, then it is necessary to render two half-restoring pulses effective on that core in which the respective information is to be re-stored. These two half-restoring pulses have to coincide and each should have the effect of producing a magnetic field strength of

$$+\frac{Hm}{2}$$

For the sake of simplicity here below a pulse or current or voltage producing a magnetic field strength Hm or a field strength Hm/2 will be called a pulse or current or voltage Hm or a current, pulse, or voltage Hm/2.

The coincidence of the two pulses

$$+\frac{Hm}{2}$$

has to occur at the particular core, i.e., at the intersection of the corresponding column and row. Therefore, a first half-restoring pulse

$$+\frac{Hm}{2}$$

is to be introduced into the respective column wire, and a second half-restoring pulse

$$+\frac{Hm}{2}$$

is to be introduced into the corresponding row wire or input wire 17a to 17d, respectively. It will be under-

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stood that the output pulse produced by the reversal of the magnetic saturation of the particular core and applied to the respective read-out amplifier 18 is amplified thereby and is applied, if desired via the corresponding delay device 20, to the pulse generator 19 which produces the desired half-restoring pulse

$$+\frac{Hm}{2}$$

and returns from its output the desired half-restoring pulse

$$+\frac{Hm}{2}$$

through the corresponding input line 17a to 17d to the above mentioned intersection of the particular column and the particular row.

In order to apply in this operation to a particular column first a read-out pulse -Hm and immediately thereafter a half-restoring pulse

$$+\frac{Hm}{2}$$

it is necessary to apply to the particular one of the column lines 15₁ to 15₅ a two-polarity pulse as illustrated at 14. For this purpose each of the columns 1 to 5 is associated with a pair of impulse generators 12 and 13, the one furnishing to the respective column wire a pulse -Hm, the other furnishing to that line a pulse

$$+\frac{Hm}{2}$$

Of course, each of these impulse generators must be triggered by a suitable pulse timing arrangement. In the example of FIG. 1 a mechanical or electronic shift register 10 is provided for this purpose in which some energy storage 11 is shifted in well known manner stepwise in the direction of the arrow. With every step of this shift register a triggering pulse is applied to the consecutive pulse generators 12, 13.

Various types of shift registers may be used for this purpose, e.g., a register composed of flip-flops or of interconnected flip-flop tetrads, or also magnetic shift registers of suitable type. However, it is to be noted at this point that the requirement of using two impulse generators for each column of the matrix in addition to a shift register for triggering these impulse generators entails a great complication of the arrangement and the use of many delicate components. It is therefore an important advantage of this invention that this disadvantage is eliminated.

The operation of the above described arrangement is as follows:

It may be assumed that information is stored in the core 1a which means that this core is in a state of positive magnetic saturation. In order to simplify the description it may be assumed that all the other cores are in a state of negative magnetic saturation. The first impulse generator 12 applies a negative pulse -Hm to the column wire 15₁. Hereby the magnetization of the core 1a is reversed so that the output line 16a carries an output pulse which appears in amplified form at the output of the read-out amplifier 18a. The magnet cores 1b, 1c, 1d having been already in a state of negative magnetic saturation are not affected by the negative read-out pulse -Hm. Consequently no pulse is applied to or delivered by the read-out amplifiers 18b, 18c and 18d.

Now the information that was stored in the core 1a has been obliterated by the pulse -Hm. In order to re-introduce this information into the same core 1a it is necessary that both the impulse generator 13 of column 1 and the impulse generator 19a furnish simultaneously half-restoring impulses

$$+\frac{Hm}{2}$$

For this purpose the generator 13 of column 1 is now triggered upon the next step of the shift register 10, while the generator 19a is triggered by the read-out amplifier 18a. Between the latter and the generator 19a an intermediate unit 20a is arranged which may be for instance a delay circuit. This is necessary because the above mentioned generator 13 is triggered one step after the read-out generator 12 has been triggered. The resulting time difference must be taken into consideration. Consequently, the unit 20a is provided so as to cause the two generators 13 and 19a to be triggered simultaneously whereby the desired coincidence of the two half-restoring pulses at the respective matrix intersection is assured.

It is to be understood that with the arrangement according to FIG. 1 it is not only possible to reintroduce an obliterated information immediately after the read-out operation, but also to first read out a column, carrying out a calculating operation and to reintroduce instead of the obliterated information a new calculated information into the same column of the matrix. In this case it is only necessary to replace the delay units 20 by a calculating arrangement which applies, depending upon the result of the calculation, a pulse to the respective pulse generator 19a to 19d. It is only necessary to take care of timing in such a manner that even in this case the two half-restoring pulses coincide at the desired intersection point in the matrix.

Reference is now made to FIG. 2. As far as the matrix and the pulse returning arrangement Z is concerned, the embodiment according to FIG. 2 does not differ from that of FIG. 1. Therefore a description of the identical elements appears to be superfluous. However, FIG. 2 illustrates for the sake of clarity only a fraction of the matrix of FIG. 1, namely only the columns 2 and 3 with the respective magnet cores 2a to 2d and 3a to 3d. While according to FIG. 1 a two-polarity pulse 14 had to be produced by separate impulse generators 12 and 13 and applied to the respective column, a corresponding two-polarity pulse 21 is obtained according to the invention as illustrated by FIG. 2 by connecting a magnetic shift register directly with the matrix in such a manner that the charging and discharging currents of an intermediate storage condenser associated with each stage of the shift register are applied to the matrix. It can be seen that in this manner the conventional two impulse generators and the pertaining control means are rendered unnecessary.

FIG. 2 shows as a read-out control means a shift register of the well known Woo-type. It may be mentioned here that instead of a Woo-type register also a register of the An Wang-type may be used. Both types of shift registers are described for instance in an article "Static Magnetic Storage and Delay Line" in Journal of Applied Physics, vol. 21, No. 6, pages 49-54 (1950).

In FIG. 2 the shift register comprises a plurality of cores 32, 33 and 34, input windings 42, 43 and 44 and output windings 52, 53 and 54, respectively associated with the cores and shift windings 62, 63, 64 respectively associated with the cores and connected in series with each other by a control line 20. Each stage of the register further includes a diode 72, 73 etc., and an intermediate storage condenser 82, 83 etc. connected between consecutive stages. As is well known, every step of shifting information through the shifting register produces a cycle of charge and discharge of the respective intermediate storage condenser. According to the invention the charge and discharge circuit of each of these condensers is connected with a different one of the column lines of the matrix. For example, one side of the condenser 82 is directly connected with the column line 15₂.

For the purpose of explanation, now the operation in connection with the first stage of the shift register and the condenser 82 will be described. It may be

assumed that the shift register core 32 is in a state of positive magnetic remanence. By the application of a shift impulse to line 20 the shift winding 62 is energized and causes reversal of the magnetic remanence of core 32. This generates a voltage across the output winding 52 whereby the condenser 82 is charged via line 15₂ and diode 72. Now the condenser is negatively charged.

This charging current has the form of the negative portion of the pulse 21 and passing through the line 15₂ it obliterates an information that may have been stored in the core 2a. The resulting delivery of an output pulse to the arrangement Z and the return of a half-restoring pulse from there is the same as described above. However, the application of the other half-restoring pulse to the column wire 15₂ is now obtained by the discharge of the condenser 82 immediately after its charging. The condenser 82 discharges across the resistor 92 and the input winding 43 of the next stage and of course also via the column wire 15₂. Of course, the resistor 92 must be so dimensioned that the amplitude of the discharge current corresponds to the value

$$+\frac{Hm}{2}$$

It can be seen, therefore, that upon coincidence of the positive discharge pulse of the condenser 82 with the half-restoring pulse returned by the arrangement Z, the previously obliterated information is re-introduced into the core 2a.

The discharge of condenser 82 shifts the information into the core 33 of the shift register whereafter, upon the application of the next shift pulse in line 20 the same cycle of operation repeats in relation to the charging and discharging of the next following intermediate storage condenser 83 which is associated with column 3 of the matrix. Consequently, in this manner the two-polarity pulses 21 derived from the sequential charge and discharge of the consecutive condensers of the shift register cause sequentially in the respectively associated columns of the matrix an obliteration of any stored information therein and the re-introduction thereof.

Now it will be seen that the arrangement according to the invention as illustrated by FIG. 2 is remarkably simpler than the conventional arrangement according to FIG. 1 because the required two-polarity pulses are derived in a direct and simple manner from the charge and discharge of the intermediate condenser in the shift register which is required in any case for a stepwise read-out operation of the matrix. It is not even necessary to produce the required two-polarity pulse by decoupling from two different windings and via special distributing means. Instead all that is required is to arrange for one connection of the condenser to extend as a single wire through the cores of the respectively associated column of the matrix. Thus at least two blocking oscillators or other impulse generators per column are saved by the invention.

FIG. 3 illustrates an embodiment of the invention which differs from FIG. 2 only by incorporating a different type of a magnetic shift register of the type disclosed in German Patent No. 1,058,285, or in my copending U.S. patent application Serial No. 63,314. This register comprises a plurality of cores 31', 32', 33' and 34', and in each stage respectively associated with these cores a circuit arrangement comprising, respectively, windings 61' to 64', diodes 71' to 74', intermediate storage condensers 81' to 84', and resistors 91' to 94', respectively, interconnected as shown in FIG. 3. In the same manner as in FIG. 2 one connection of each of the intermediate storage condensers 81' to 84' is taken through the respectively associated column of cores so that again the two-polarity pulse 21 is applied to the particular column upon every step of the shift register as described above. However,

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while according to FIG. 2 the charge and discharge circuits of each condenser are completed via ground, in the embodiment of FIG. 3 the respective circuits are closed directly by a connection 22a to 22d, respectively, taken back to the network of the shift register. The operation of this embodiment is exactly like the one described above for FIG. 2.

In certain cases it may be somewhat difficult to adjust the ampere-turns of the windings of the shift register so as to match the currents required for operating the matrix. These currents may have to be of the order of .5 amp. or even larger. It is rather inconvenient to use currents of this magnitude in a shift register. Therefore, an arrangement as illustrated by FIG. 4 is more advantageous and facilitates the selection of proper winding specifications for the shift register. FIG. 4 again illustrates only a portion comprising columns 2 and 3 of the matrix and the corresponding portions of the shift register. The shift register of FIG. 4 is fundamentally the same as that shown and described with reference to FIG. 2. This arrangement has the further advantage of being operable at a higher step frequency without an increase of the energy consumption because no resistors are provided in the discharge circuits of the intermediate storage condensers. Instead electronic switch means are provided as will be described further below. The energy consumption of this arrangement is particularly low because not only no energy is consumed in resistors, but also no discharge current can be delivered by the condensers during their charging.

According to FIG. 4 the shift register proper is supplemented by a shift impulse generator which may be any suitable type of a blocking oscillator 101 comprising on a magnetizable core a first winding 110 and a second winding 111. The output of winding 110 is connected with the shift impulse line 20' via a transistor 103. This transistor must be of such a construction that it is rendered conductive when its base is given negative polarity. Upon excitation the blocking oscillator 101 delivers a two-polarity pulse as illustrated at 102 which has a negative portion corresponding to $-Hm$ and a positive portion corresponding to

$$+\frac{Hm}{2}$$

Only the negative portion $-Hm$ is capable of rendering the control transistor 103 conductive. When this transistor is conductive the shift windings 62'', 63'' and 64'' are supplied with energy from a source $-U_b$.

The second winding 111 of the blocking oscillator 101 furnishes also a two-polarity pulse as shown at 104 which is identical with the pulse 102 except that its polarity is reversed. The output of the winding 111 is connected with the base of a second control transistor 105 of the same type as transistor 103, the transistor 105 acting as a gate for the discharge line 106 which is connected via diodes 192, 193, 194, respectively, with the input windings 42', 43', 44', respectively, of the shift register. The transistor 105 is rendered conductive by the negative portion of the pulse 104 only at that time when a particular one of the condensers 82'', 83'' etc. is to be discharged.

It may be assumed that only the magnet core 32'' is in a state of positive magnetic remanence. By a shift impulse furnished by the blocking oscillator 101 and applied to the shift control line 20' the winding 62'' is energized whereby in the above described manner a voltage is generated across the output winding 52' resulting in charging the condenser 82'' in the manner described above. This and the immediately following discharge of this condenser 82'' causes the application of a two-polarity pulse as illustrated at 121 to the column wire 15₂. After the negative portion $-Hm$ of the shift impulse 102 has decayed the negative portion of the pulse 104 produced by the winding 111 renders the transistor 105 conductive so that only at this moment the capacitor 82'' is able to discharge

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through winding 43' and diode 193. Thus the positive portion

$$+\frac{Hm}{2}$$

of the pulse 121 is applied to the column wire 15₂.

The discharge of the capacitor 82'' causes energization of the input winding 43'' and thus reversal of magnetization of core 33''. In this manner the cycle of operations described above repeats for one stage of the shift register after the other and correspondingly for the consecutive columns of the matrix.

It should be noted that upon establishment of full conductivity of the transistor 105 the entire stored condenser energy is permitted to be transferred into the next following magnet core. Consequently the number of turns of the input windings 42', 43', 44' is not critical and can be adjusted to desired conditions at will.

Each column wire of the matrix is supplied with the required impulses by the individual intermediate storage condensers of the register. It is only necessary to see to it that the form of the two-polarity pulse 121 is such that the impulse portion

$$+\frac{Hm}{2}$$

follows the preceding negative pulse portion $-Hm$ with a slight delay resulting of the unblocking of the transistor 105. The small time interval between the just mentioned pulse portions may be used for inserting between the obliteration of stored information and the re-introduction of this information a calculating operation. However, should in a particular case the available delay or time interval not be sufficient for this purpose, then means can be provided for increasing this time interval to a desirable magnitude.

An arrangement satisfying this demand is illustrated by FIG. 5 which illustrates mainly only those portions of the arrangement which differ from those in FIG. 4. In this case not only one connection of each of the intermediate storage transistors 81a to 84a are taken through the matrix columns but also the connections from one end of the various output windings 51a to 54a, respectively. Consequently, each stage of the shift register has two connections A and B taken through the matrix, for instance the first stage a line A₁ from the winding 51a and a line B₁ from the condenser 81a. It will be readily understood that the lines A₁ to A₄ carry positive pulses $+Hm$ when the respective condensers are charged. The lines B₁ to B₄ however carry two-polarity pulses $-Hm$ and

$$+\frac{Hm}{2}$$

By properly arranging the connections taken from the output windings 51a to 54a and by thus causing the direction of the flow of current in the lines A₁ to A₄ where they pass through the cores of the respective columns to produce a magnetic field strength $-Hm$, the current flowing through each output winding 51a to 54a when the latter is energized will produce an advance read-out pulse $-Hm$ in the cores of the column associated with the respectively next following shift register stage. For instance, in column 2 the line A₁ from the first stage is taken through the cores 2a to 2d in a direction opposite to the direction of the line B₂ taken from the second stage through the just mentioned cores. Consequently with the first step in the shift register a first read-out impulse $-Hm$ (as indicated at a in FIG. 5a) is applied through line A₁ to the cores 2a to 2d of column 2. When with the next step in the shift register the condenser 82a is first charged and thereafter discharged as described above, the above described two-polarity pulse as shown in FIG. 5a is ap-

plied through line B₂ to the cores of column 2. However, of this two-polarity pulse only the positive portion

$$+\frac{Hm}{2}$$

is effective as a half-restoring pulse as described above. Consequently, between the first read-out impulse $-Hm$ furnished by one stage and the following half-restoring pulse furnished by the respectively following stage there appears a time interval of arbitrarily predeterminable duration corresponding to the interval between consecutive steps in the shift register. This time interval may be used for carrying out intercalated calculating operations. It is true that the two-polarity pulse delivered by the respectively second stage has a negative pulse portion $-Hm$ as indicated at *b* in FIG. 5*a* is delivered. However this is not disturbing or detrimental because the respective magnet core has been changed already by the preceding advance read-out pulse to a state of negative magnetic remanence so that no output voltage is induced any more by the second pulse $-Hm$. This second impulse can only have the favorable effect to make absolutely sure that in the particular column all cores are placed in a state of negative magnetic remanence. FIG. 6 illustrates a modification of only a portion of the arrangement according to FIG. 5 for the purpose of shifting the entire information storage existing in a matrix in the direction of the rows thereof. It is to be noted that this mode of operation requires providing one additional column in addition to the normally required columns in the matrix so that any one of the existing columns may serve as a transfer column because at the moment when information is to be shifted from one core in a row to the next following core in that row, information from a core preceding said one core cannot be shifted simultaneously into that one core. However, information can be shifted in the direction of the rows in the following manner. For instance, first information may be shifted from the core 3*a* to the core 4*a*. In a next step information may be shifted from core 2*a* into core 3*a*, hereafter the information from core 1*a* may be shifted into core 2*a* etc.

The individual line portions A₁ to A₄ are shown in FIG. 6 in the same respective relation to the corresponding line portions B₂ to B₅, however, for the sake of clarity of the drawing, in reversed order from right to left.

The operation of this arrangement is as follows:

By the application of a first read-out pulse $-Hm$ to line A₁ the information stored in core 4*a* is obliterated and an output pulse is applied to the units 18, 20 and 19 associated with row *a*. By the next step a read-out impulse $-Hm$ is applied to line A₂. By that time the delayed half-restoring pulse

$$+\frac{Hm}{2}$$

delayed by the unit 20, is returned from the respective pulse generator 19 through line 17*a* so as to coincide with the other half-restoring pulse arriving through line B₂ in the second step of the operation. Consequently, the information first read out from core 3*a* is now re-introduced into core 4*a*. Hereafter the information stored in core 2*a* is read out by a read-out impulse applied to line A₃ and this information is re-introduced in the same manner as described above into the core 3*a* upon the arrival of the half-restoring impulse through line B₃. In the same manner core 1*a* is read out by an impulse through line A₄ and is re-introduced into core 2*a* upon the arrival of the respective pulse through line B₄. It can be seen that by a complete cycle of operation of the shift register, i.e., when information has been shifted through all the stages thereof, the entire information that may have been stored in the various columns of the matrix is shifted one step to the right, i.e., from each column to the next following column. Of course, by minor changes of the arrangement a shift of information in the direction toward the

left may be carried out in the same manner. If *n* cycles of operation of the shift register are carried out, the shift of information within the matrix will amount also to *n* steps. This operation is preferably suitable for carrying out decimal shifts in a decimal matrix in which case every step of shift in the matrix would correspond to a multiplication with the factor 10, or the factor 1/10.

While the arrangement of FIG. 6 serves to produce a shift of stored information in the direction of the rows it is also possible to modify the arrangement of, e.g., FIG. 2 in such a manner that a shift of information stored in the matrix is carried out in the direction of the columns. This may be effected by cyclically changing the connections between the outputs of the generators 19*a* to 19*d* with the rows to which the half-restoring pulses

$$+\frac{Hm}{2}$$

furnished by these generators, respectively, are returned. As can be seen from FIG. 7, line 17*a*' being the input line for the row *a* is taken from the generator 19*d*, similarly line 17*b*' is taken from generator 19*a*, line 17*c*' is taken from generator 19*b* and line 17*d*' is taken from generator 19*c*. Consequently, information read out from one row is re-introduced into the next following lower row. Otherwise the operation is exactly as described further above. An arrangement of this type is particularly suitable to be used for the control of parallel printing arrangements based on the decimal number system. Of course, in such case a matrix not with only four rows *a-d* as shown in FIG. 7 will be used but a matrix with ten rows. However, this does not mean any departure from the basic principles of this invention.

It will be understood that each of the elements described above, or two or more together, may also find a useful application in other types of arrangement for controlling a magnet core matrix differing from the types described above.

While the invention has been illustrated and described as embodied in an arrangement including a shift register for controlling a magnet core matrix, it is not intended to be limited to the details shown, since various modifications and structural changes may be made without departing in any way from the spirit of the present invention.

Without further analysis, the foregoing will so fully reveal the gist of the present invention that others can by applying current knowledge readily adapt it for various applications without omitting features that, from the standpoint of prior art, fairly constitute essential characteristics of the generic or specific aspects of this invention and, therefore, such adaptations should and are intended to be comprehended within the meaning and range of equivalence of the following claims.

What is claimed as new and desired to be secured by Letters Patent is:

1. In an arrangement of the type set forth, in combination, matrix means comprising a plurality of magnet cores arranged in a plurality of rows and in a plurality of columns and being individually changeable from information storage representing magnetic saturation of one polarity to no-information storage representing magnetic saturation of opposite polarity by application thereto of a read-out pulse of one polarity, and changeable from no-information storage representing saturation to information storage representing saturation by simultaneous application thereto of two half-re-storing pulses of the opposite polarity, each of said cores delivering an output pulse upon a change thereof to no-information representing saturation; pulse return means connected with said rows of said matrix means so as to receive said output pulses from any one of said cores and for returning, upon receiving an output pulse, a first half-restoring pulse of said opposite polarity to at least one of said cores being in non-information representing saturation and located in at least one of said rows thereof;

shift register means having a plurality of stages respectively associated with said different columns and sequentially energizable by application of a sequence of shift pulses to one stage after the other, respectively, and including energy transfer means for transmitting energy from each stage energized by a shift pulse to the next following stage, said energy transfer involving the appearance of a sequence of consecutive pulses of respectively opposite polarities in the respective transfer means; shift pulse generator means for applying shift pulses to said shift register means; and a plurality of circuit means connecting said energy transfer means respectively with different ones of said columns of cores for channeling each of said sequences of pulses of opposite polarities through the respective columns and for applying out of such pulse sequence the pulse of one polarity as a read-out pulse to at least one of the cores being in information storage representing saturation, and for applying the pulse of opposite polarity as a second half-re-storing pulse to that core to which said first half-re-storing pulse is being applied so as to change this particular core to information storage representing saturation.

2. In an arrangement of the type set forth, in combination, matrix means comprising a plurality of magnet cores arranged in a plurality of rows and in a plurality of columns and being individually changeable from information storage representing magnetic saturation of one polarity to no-information storage representing magnetic saturation of opposite polarity by application thereto of a read-out pulse of one polarity, and changeable from no-information storage representing saturation to information storage representing saturation by simultaneous application thereto of two half-re-storing pulses of the opposite polarity, each of said cores delivering an output pulse upon a change thereof to no-information representing saturation; pulse return means connected with said rows of said matrix means so as to receive said output pulses from any one of said cores and for returning, upon receiving an output pulse, a first half-re-storing pulse of said opposite polarity to at least one of said cores being in no-information representing saturation and located in at least one of said rows thereof; shift register means having a plurality of stages respectively associated with said different columns and sequentially energizable by application of a sequence of shift pulses to one stage after the other, respectively, and including energy transfer means comprising intermediate storage capacitor means for transmitting energy from each stage energized by a shift pulse to the next following stage by first charging said capacitor means and thereafter applying its discharge to the next following stage, said energy transfer involving the appearance of a sequence of a charge pulse of one polarity and a discharge pulse of opposite polarity; shift pulse generator means for applying shift pulses to said shift register means; and a plurality of circuit means connecting said intermediate storage capacitor means respectively with different ones of said columns of cores for channeling each of said sequences of charge and discharge pulses through the respective columns and for applying out of such pulse sequence the charge pulse of one polarity as a read-out pulse to at least one of the cores being in information storage representing saturation, and for applying the discharge pulse of opposite polarity as a second half-re-storing pulse to that core to which said first half-re-storing pulse is being applied so as to change this particular core to information storage representing saturation.

3. In an arrangement of the type set forth, in combination, matrix means comprising a plurality of magnet cores arranged in a plurality of rows and in a plurality of columns and being individually changeable from information storage representing magnetic saturation of one polarity to no-information storage representing magnetic saturation of opposite polarity by application thereto of

a read-out pulse of one polarity, and changeable from no-information storage representing saturation to information storage representing saturation by simultaneous application thereto of two half-re-storing pulses of opposite polarity, each of said cores delivering an output pulse upon a change thereof to no-information representing saturation; pulse return means connected with said rows of said matrix means so as to receive said output pulses from any one of said cores and for returning, upon receiving an output pulse, a first half-re-storing pulse of said opposite polarity to at least one of said cores being in no-information representing saturation and located in at least one of said rows thereof; shift register means having a plurality of stages respectively associated with said different columns and sequentially energizable by application of a sequence of shift pulses to one stage after the other, respectively, and including energy transfer means comprising for each stage pulse output means and intermediate storage capacitor means changeable by a one-polarity pulse from the respective pulse output means for transmitting energy from each stage energized by a shift pulse to the next following stage by first charging said capacitor means and thereafter applying its discharge to the next following stage, said energy transfer involving the appearance of a sequence of a charge pulse of one polarity and a discharge pulse of opposite polarity; shift pulse generator means for applying shift pulses to said shift register means; a plurality of first circuit means connecting said pulse output means respectively with different ones of said columns of cores for channeling each of said one-polarity pulses of said pulse output means as a read-out pulse to at least one of the cores being in information storage representing saturation and located in a column associated with a shift register stage different from the one furnishing the particular one-polarity pulse; and a plurality of second circuit means connecting said intermediate storage capacitor means respectively with different ones of said columns of cores for channeling each of said sequences of charge and discharge pulses of opposite polarities through the respective columns and for applying out of such pulse sequence the charge pulse of one polarity as a second read-out pulse to at least one of the cores being in information storage representing saturation and located in said column associated with said different register stage, and for applying the discharge pulse of opposite polarity as a second half-re-storing pulse to that core to which said first half-re-storing pulse is being applied so as to change this particular core to information storage representing saturation, whereby between the occurrence of the first read-out pulse and the simultaneous application of the two half-re-storing pulses a time interval is provided depending on the time between energization of the respective shift register stages.

4. An arrangement as claimed in claim 2, wherein said pulse return means are so connected with said rows of said matrix means that in response to an output pulse received from one of said rows the corresponding half-re-storing pulse is applied to a different row adjacent to said one row, so that after a complete cycle of operation of said shift register means any information stored in said matrix means is shifted therein one step in direction of the columns from respective row to respectively adjacent row.

5. An arrangement as claimed in claim 3, wherein said first and second circuit means are so connected with said different columns that upon energization of any one of the shift register stages any information stored in a particular core of the respectively associated column is read out by the application of a read-out pulse thereto, while subsequently said two half-re-storing pulses are applied to a core located in the same row as said particular core but in the column adjacent to the column of said particular core, whereby after a complete cycle of operation of said shift register means any information stored in said matrix means is shifted therein one step in di-

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rection of the rows from respective column to respectively adjacent column.

6. An arrangement as claimed in claim 2, wherein said shift pulse generator means is adapted to furnish at the termination of said shift pulse additionally a control signal, and including control transistor means con-

nected with all said intermediate capacitor means and controllable by said control signal so as to permit discharge of any of said capacitor means only upon application of said control signal.

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No references cited.