ELECTRONIC CIRCUIT FOR DC CONVERSION OF FLUORESCENT LIGHTING BALLAST

Abstract

Embodiments of an illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast described. One illumination device includes protection circuitry configured to protect the illumination device from the ballast current signal, a full-wave rectifier, a smoothing filter electrically coupled to the full wave rectifier, and a current regulator power circuit electrically coupled to the smoothing filter and the LEDs. The current regulator power circuit can include a first switching element configured to operate in response to a first (PWM) ON/OFF control signal; a current controller electrically coupled to a gate of the first switching element, the current controller configured to generate the first PWM control signal; and a current sense resistor electrically coupled to the first switching element and configured to sense the current through the LEDs, wherein the sensed current is fed back to the current controller.
ELECTRONIC CIRCUIT FOR DC CONVERSION OF FLUORESCENT LIGHTING BALLAST

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of co-pending U.S. patent application Ser. No. 12/778,632 filed May 12, 2010, which claims priority to provisional Application Ser. No. 61/178,093, filed May 14, 2009, which are both hereby incorporated by reference in their entireties.

TECHNICAL FIELD

[0002] The present invention relates in general to LED fluorescent lamp replacements.

BACKGROUND

[0003] Fluorescent lamps are commonly installed with an additional device to regulate the voltage and current provided to the fluorescent lamp. This device, known as a ballast, can be designed to provide the proper starting voltage to establish an arc between two electrodes of the fluorescent lamp. Additionally, the ballast can be designed to provide a controlled voltage to limit the amount of current to the fluorescent lamp during operation thereof. The starting and operating voltages provided by the ballast to power the fluorescent lamp can depend on, for example, the length and/or diameter of the fluorescent lamp. Accordingly, a fluorescent lamp may contain a ballast particularly designed to provide the proper starting and operating voltages.

[0004] Fluorescent lamps are gradually being replaced by light-emitting diodes (LEDs) in many applications. LEDs have many advantages over traditional fluorescent lamps in that they have, for example, longer operational life, reduced power consumption, greater durability and increased design flexibility.

[0005] Accordingly, LED replacement lamps have been developed that retrofit fluorescent lamp fixtures using existing ballasts. These LED replacements commonly contain electrical circuitry for power conversion that may not be, for example, universally compatible with any type of ballast found in existing fixtures.

BRIEF SUMMARY

[0006] Embodiments of an illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast, the ballast configured to provide a current signal are disclosed herein. One such embodiment includes protection circuitry configured to protect the illumination device from the ballast current signal, a full-wave rectifier electrically coupled to the protection circuitry and configured to produce a rectified voltage output, a smoothing filter electrically coupled to the full wave rectifier and configured to produce a smoothed rectified voltage output and a current regulator power circuit electrically coupled to the smoothing filter and the LEDs. The current regulator power circuit includes a first switching element configured to operate in response to a first pulse width modulated (PWM) ON/OFF control signal, the first switching element delivering current to the LEDs in response to the ON control signal and the first switching element not delivering current to the LEDs in response to the OFF control signal, a current controller electrically coupled to a gate of the first switching element, the current controller configured to generate the first PWM control signal and a current sense resistor electrically coupled to the first switching element and configured to sense the current through the LEDs, wherein the sensed current is fed back to the current controller.

[0007] Embodiments of another illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast are disclosed herein. One such embodiment includes means for receiving a current signal from the conventional ballast and means for protecting the illumination device from the received current signal. The illumination device also includes means for rectifying the received current signal to produce a rectified voltage output and means for sensing the current through the LEDs. Further, the illumination device includes means for generating a pulse width modulated (PWM) control signal from a current control circuit based on the sensed current and means for supplying current to the LEDs in response to the PWM control signal so that the LED current reaches an average LED current.

[0008] Further, embodiments of a method of supplying power to an illumination device including LEDs and connected to an existing fluorescent lamp fixture including a conventional ballast are also disclosed herein. One such method includes receiving a current signal from the conventional ballast, protecting the illumination device from the received current signal, rectifying the received current signal to produce a rectified voltage output, sensing the current through the LEDs, generating a pulse width modulated (PWM) control signal from a current control circuit based on the sensed current and supplying current to the LEDs in response to the PWM control signal so that the LED current reaches an average LED current.

[0009] Other embodiments of the invention are described in additional detail hereinafter.

BRIEF DESCRIPTION OF THE DRAWING

[0010] The various features, advantages and other uses of the present invention will become more apparent by referring to the following detailed description and drawing in which:

[0011] FIG. 1 is a block diagram of a light system containing a power converter in accordance with an embodiment of the invention.

[0012] FIG. 2 is a circuit schematic illustrating various components of the power converter of FIG. 1;

[0013] FIG. 3 is a circuit schematic of a current controller used in the power converter of FIG. 2;

[0014] FIG. 4 is a circuit schematic of a voltage controller used in the power converter of FIG. 2;

[0015] FIG. 5 is a circuit schematic of a voltage regulator used in the power converter of FIG. 2;

[0016] FIG. 6 is a circuit simulation waveform of an output forward voltage of an LED array along with a rectified DC voltage and a DC link voltage from the power converter of FIG. 2;

[0017] FIG. 7A is a circuit simulation waveform of switch turn-on dv/dt changing as a function of a gate drive resistor value from the power converter of FIG. 2;

[0018] FIG. 7B is a circuit simulation waveform of switch turn-on dv/dt changing as a function of a gate drive resistor value from the power converter of FIG. 2.
DETAILED DESCRIPTION

[0019] FIG. 1 is a block diagram of a light system 10 according to one embodiment of the invention. LED light system 10 can include a fixture (not shown) and an LED replacement lamp 12 powered by a signal source 14. The fixture can be, for example, an existing fluorescent lamp fixture that may have been previously used in a light system for a fluorescent lamp. According to the embodiments discussed herein, replacement lamp 12 can be retrofitted to the existing fixture. The fixture can contain a ballast 16, which can be connected between signal source 14 and replacement lamp 12. Replacement lamp 12 can include a power converter 18 and an LED array 20. Although the embodiments will be discussed with reference to a replacement lamp that solely contains LEDs, other embodiments of light system 10 do not have to be exclusively limited to LEDs. For example, other embodiments of light system 10 may contain a replacement lamp that contains a combination of a fluorescent lamp and LEDs.

[0020] Signal source 14 can be any suitable alternating current (AC) source or direct current (DC) source. For example, signal source 14 can be a 110-220 VAC single phase direct connect. As discussed previously, signal source 14 provides power to ballast 16. Ballast 16 can convert the power from signal source 14 to a power level designed to activate and operate a fluorescent lamp. Ballast 16 can be any type of ballast suitable for lighting fluorescent lamps by, for example, modifying the electrical voltage and frequency levels of signal source 14. Some non-limiting examples of ballast 16 are rapid start electronic ballasts, instant start electronic ballasts, magnetic ballasts or a hybrid containing components of both the electric and magnetic ballasts.

[0021] Power converter 18 can receive the power output from the ballast, by, for example, leads from the ballast that would have previously been connected to the lamp sockets for a fluorescent lamp. Power converter 18 can convert the power output by the ballast into power usable by and suitable for LED array 20. Power converter 18 can include an inrush protection circuit 22, a surge suppressor circuit 24, a noise filter circuit 26, a rectifier circuit 28, a main filter circuit 30, a current regulator circuit 32 and a shunt voltage regulator circuit 34. Current regulator circuit 30 can be connected to LEDs 20. As will be described in additional detail, power converter 18 is suitably designed to receive a wide range of currents and/or voltages from ballast 16.

[0022] LEDs 20 in replacement lamp 12 can include at least one LED, a plurality of series-connected or parallel-connected LEDs, or an LED array. At least one LED array can include a plurality of LED arrays. Any type of LED may be used in LEDs 20. For example, LEDs can be high-brightness semiconductor LEDs, an organic light emitting diodes (OLEDs), semiconductor dies that produce light in response to current, light emitting polymers, electro-luminescent strips (EL) or the like.

[0023] FIG. 2 is a circuit schematic of illustrating various details of power converter 18 of FIG. 1. Signal source 14 can provide, for example, an AC signal to inrush protection circuit 22. Inrush protection circuit 22 can be realized by inrush current limiters 42 and 44. Capacitor 40 can be connected in parallel to output of the ballast 16 for filtering incoming voltage spikes. Inrush current limiter 40 can have one end connected to a common point between the output of ballast 16 and capacitor 40 for receiving the positive half cycle of the ballast output and the other end connected to surge suppressor circuit 24. Similarly, inrush current limiter 42 can have one end connected to a common point between the output of ballast 16 and capacitor 40 for receiving the negative half cycle of the ballast output and the other end connected to surge suppressor circuit 24.

[0024] When signal source 14 is initially connected, high inrush current can pass from the output of ballast 16 to components of power converter 18. High inrush currents may be moderated by placing inrush current limiters 42 and 44 in series with the current flow. In one embodiment, inrush current limiters 42 and 44 can be negative temperature coefficient (NTC) resistors. When signal source 14 is first connected, for example, NTC resistors can be cool and have a high resistance value thereby limiting inrush current. After a period of operation, NTC resistors can be warmed by current flowing therein, which in turn, can lower its resistance value. Alternate embodiments may use any other suitable inrush current limiter. One non-limiting example may be a fixed resistor or the like.

[0025] Selection of inrush current limiters 42 and 44 can be accomplished by, for example, calculating the maximum input energy the inrush current limiter will absorb when the device is turned on using equation (1):

$$E = \frac{1}{2} \times C_{bus} \times V_{max}^2$$

wherein

- \(E\) is the maximum energy rating;
- \(C_{bus}\) is the amount of bus capacitance; and
- \(V_{max}\) is the peak AC voltage or the maximum DC voltage.

[0026] Thus, for example, if \(C_{bus}\) is 100 \(\mu\)F and \(V_{max}\) is 1500V, then the maximum energy rating will be 112.5 J. Accordingly, inrush current limiters 42 and 44 can be selected to have an energy rating greater than 112.5 J. Further, the resistance of the inrush current limiter can be of a value such that components of rectifier circuit 28 are not stressed. An example of an inrush current limiter that fulfills these preferences is Ametherm Inrush Current Limiter Part No. MS22212103, which contains a maximum energy rating of 220 J and a resistance of 120 ohms at 25° C. Other suitable inrush current limiters and techniques for selecting inrush current limiters are also available.

[0027] Referring still to FIG. 2, surge suppressor circuit 24 can be realized by varistor 46. Varistor 46 is connected in parallel between inrush protection circuit 22 and noise filter circuit 26. Varistor 46 can be used to absorb high voltage transients or surges that may occur from the output of ballast 16. Selection of varistor 46 can be accomplished by, for example, selecting a varistor that has a maximum allowable voltage no less than \(V_{max}\) where \(V_{max}\) is the peak AC voltage or the maximum DC voltage from the output of ballast 16. In this manner, varistor 46 will not clamp as long as the voltage does not exceed \(V_{max}\). An example of a surge suppressor that fulfills these preferences is Panasonic ZNR Transient/Surge Absorber Part No. ERZ10D182CS, which has a maximum allowable voltage of 1000 VACmax (1465 VDC). Other suitable surge suppressor devices and techniques for determining suitable surge suppressor devices are also available.

[0028] Incoming current passes through noise filter 26 to prevent noise interference from being received by power converter 18. Noise filter circuit 26 can be realized by X-class capacitor 56, Y-class capacitors 48 and 50 and discharge resistors 52, 54 and 56. Selection of the type and number of X-class capacitors can be accomplished by any suitable technique in order to, for example, pass EMC testing. One suitable technique is to select a specific capacitor, calculate the
power dissipation of that capacitor and, if the calculated power dissipation for the selected capacitor is higher than the maximum allowed power dissipation for the specific capacitor, determining how many capacitors should be placed in parallel to achieve a power dissipation that is less than or equal to the maximum allowed power dissipation.

Accordingly, the RMS current of the X-class capacitor can be estimated, which as discussed in more detail below, to calculate the worst case power dissipation of X-class capacitor 56. RMS current of the X-class capacitor can be calculated using equations (2) and (3):

\[ Z_c = \frac{1}{C_x \cdot \frac{2}{\pi} \cdot F_b} \]  

wherein

- \( Z_c \) is the impedance of the X-class capacitor at the ballast switching frequency \( F_b \);
- \( C_x \) is the value of the X-class capacitor; and
- \( F_b \) is the switching frequency of the ballast voltage.

\[ I_{rms} = \frac{4V_{max}}{\pi \cdot \sqrt{2} \cdot Z_c} \]  

wherein

- \( I_{rms} \) is the RMS current for the X-class capacitor;
- \( V_{max} \) is the peak AC voltage or the maximum DC voltage; and
- \( Z_c \) is the impedance of the X-class capacitor at the ballast switching frequency \( F_b \).

In equation (3), \( I_{rms} \) is found for the first harmonic of an input square wave. Alternatively, the RMS current for the X-class capacitor can be determined for a sinusoid, sawtooth or any other input waveform.

Once the type and value of X-class capacitor 56 is selected, X-class capacitor 56 can be evaluated based on its estimated power loss during operation of power converter 18 using equation (4) to determine the ESR of the X-class capacitor, equation (5) to determine the number of capacitors to place in parallel so that the power dissipation is less than the maximum allowable power dissipation and equation (6) to determine the estimated power loss of the X-class capacitor:

\[ Resr = \frac{DF}{2 \cdot \pi \cdot f \cdot C_x} \]  

wherein

- \( Resr \) is the theoretical equivalent series resistance of the X-class capacitor;
- \( DF \) is the dissipation factor for the X-class capacitor;
- \( f \) is the frequency at which the dissipation factor has been specified for the X-class capacitor; and
- \( C_x \) is the value of the X-class capacitor.

\[ n = \left\lfloor \frac{I_{rms}^2}{Resr} \right\rfloor \cdot \frac{Resr > P_c}{n - n + 1} \]  

wherein

- \( n \) is the number of X-class capacitors in parallel;
- \( I_{rms} \) is the RMS current for the X-class capacitor;
- \( Resr \) is the equivalent series resistance of the X-class capacitor; and
- \( P_c \) is the maximum allowed power dissipation value for the X-class capacitor.

\[ P_{esr,n} = \left( \frac{I_{rms}}{n} \right)^2 \cdot Resr \]  

wherein

- \( P_{esr,n} \) is the maximum power dissipation of an X-class capacitor;
- \( I_{rms} \) is the RMS current for an X-class capacitor;
- \( Resr \) is the equivalent series resistance of an X-class capacitor; and
- \( n \) is the number of X-class capacitors in parallel.

The ESR of the X-class capacitor determined by equation (4) may be different from the ESR at the operating frequency. Accordingly, the ESR at the operating frequency may be used to calculate the power dissipation of the X-class capacitor instead of the ESR of the X-class capacitor as determined by equation (4). An example of a suitable X-class capacitor 56 that can be used in noise filter 26 can have a value of 100 pf, a maximum allowed power dissipation of 0.25 W, and a DF of 0.001 at 1000 kHz. Other suitable capacitors and techniques for determining suitable capacitors for noise filter 26 are also available.

Rectifier 28 receives the filtered AC signal and outputs a rectified voltage using diodes 60, 62 64 and 66. Selection of diodes 60, 62 64 and 66 can be accomplished by, for example, selecting a type of diode that has a reverse voltage rating at least as high as \( V_{max} \) so that the diode is able to withstand reverse voltages as high as the peak voltage or the maximum DC voltage. An example of a diode that fulfills these preferences is STMicroelectronics Part No. DTV1500SD, which has a maximum voltage rating of 1500V. Other suitable rectifier devices and techniques for determining suitable rectifier devices are also available.

The rectified voltage is smoothed by main filter 30, which is connected across rectifier 28. Main filter 30 can be realized electrolytic capacitor 68, 74, 80 and 86. Alternatively, main filter 30 can be realized by one or any other suitable number of capacitors. Electrolytic capacitors 68, 74, 80 and 86 act as a reservoir, supplying current to the output when the varying DC voltage from rectifier 28 is falling (i.e. resulting in a smoothed DC link voltage VDC). Selection of electrolytic capacitors can be accomplished by, for example, choosing a specific capacitor bus value (i.e. total electrolytic capacitance value) and verifying that this bus capacitance value permits the DC link voltage to be greater than the maximum LED forward voltage drop.
Referring to FIG. 6, a circuit simulation waveform 600 illustrates an example of how the selected bus capacitance value results in the DC link voltage (illustrated by a solid line 602) being greater than the maximum output forward voltage of LEDs 20 (illustrated by a dotted line 604) during both the charging and discharging of the selected bus capacitor. The point where DC link voltage and rectified output voltage (illustrated by a dashed line 606) intersect is greater than the maximum output forward voltage. If the selected bus capacitor did not begin recharging the DC link voltage, the DC link voltage would fall below the maximum output forward voltage. However, since the capacitor begins charging at the intersection point of the rising edge of the rectified output voltage, the DC link voltage does not fall below the maximum output forward voltage of LEDs 20. Accordingly, selection of a bus capacitance value, such as 100 g, can fulfill these preferences and can also prevent the current regulator from entering discontinuous conduction mode. Other suitable bus capacitance values are also available. The maximum output forward voltage of LEDs 20, the rectified output voltage and DC link voltage can be represented using equations (7) and (8):

\[ V_{\text{max}} = \text{Vin}_{\text{drop}} + \text{Num}_{\text{LEDs}} \] (7)

\[ V_{\text{Vin}} = \text{Vin} \times (\text{Vin}_{\text{drop}} \times \text{Vin}_{\text{drop}}) \] (8)

wherein

\[ V_{\text{Vin}} \] is the maximum output forward voltage of the series connected LEDs;

\[ V_{\text{Vin}} \text{drop} \] is the maximum LED forward voltage drop; and

\[ \text{Num}_{\text{LEDs}} \] is the number of series connected LEDs.

The DC link voltage can be estimated and represented by using equations (9)-(12):

\[ V(t) = \frac{1}{C_{\text{bus}}} \int_{0}^{t} I_{\text{dc}} \, dt \] (9)

wherein

\[ V(t) \] is the DC link voltage;

\[ C_{\text{bus}} \] is the bus capacitance;

\[ I_{\text{dc}} \] is the current drawn from the DC supply; and

\[ t \] is the time. Finding the integral of equation (9) results in equation (10):

\[ V(t) = -\frac{1}{C_{\text{bus}}} I_{\text{dc}} \cdot t + C \] (10)

\[ V_{r}(t) = \frac{1}{2 \cdot C_{\text{bus}}} [C_{\text{bus}}(C_{\text{bus}}^2 - 4 \cdot C_{\text{bus}} \cdot P_{\text{o}} \cdot t)^{1/2}] \] (12)

To solve equation (12) for the constant of integration, we can approximate a worst case value for \( C \) when the initial condition (i.e., \( t=0 \)) of the DC link voltage is valid from the peak of the rectified voltage \( V_{pk} \), which results equation (13):

\[ V_{r}(t) = \frac{1}{2 \cdot C_{\text{bus}}} [V_{pk} - C_{\text{bus}} \cdot (V_{pk}^2 - 4 \cdot C_{\text{bus}} \cdot P_{\text{o}} \cdot t)^{1/2}] \] (13)

However, if there is more than one capacitor in main filter 30, voltage may not be evenly distributed across each capacitor. Balancing resistors 70 and 72 can be placed in parallel with capacitor 68, balancing resistors 76 and 78 can be placed in parallel with capacitor 74, balancing resistors 82 and 84 can be placed in parallel with capacitors 80 and 88, and balancing resistors 88 and 90 can be placed in parallel with capacitor 86 so that each of the balancing resistors can assist in permitting capacitors 68 to assist capacitors 68, 74, 80 and 86 to share voltage evenly. Selection of the number and type of balancing resistors 70, 72, 76, 78, 82, 84, 88, and 90 can be accomplished by any suitable technique, such as by the resistors maximum voltage rating, and have any suitable value, such as 100 kΩ.

Current regulator power section 32 applies the DC link voltage across LEDs 20. Current regulator circuit 32 can be realized by inductor 92, low-side switch 96, diode 98, capacitor 100, current controller circuit 102, a gate resistor 104, sense resistors 108, 110, 112, 114, 116, 118, and 120, feedback resistor 122 and feedback capacitor 124. One end of LEDs 20 are connected to inductor 92 while the other end of LEDs 20 are connected to low-side switch 96. Diode 98 is connected in parallel to LEDs 20 and inductor 92 and prevents reverse currents from flowing through current regulator 32. Capacitor 100 is Switch 96 is connected and connected in series Current regulator power section 32 applies the DC link voltage across LEDs 20. Alternatively, although only one inductor is shown in the circuit, more than one inductor can be implemented in series with inductor 92.
(also the average inductor current). During turn-on of switch 96, a function for current $i_{L,on}$ can be represented using equations (14)-(16):

$$v_{L,on}(t) = L_f \cdot \frac{d}{dt} i_{L,on}(t)$$

wherein:
- $t$ is the time;
- $v_{L,on}(t)$ is the inductor voltage at time $t$;
- $L_f$ is the value of the inductor(s); and
- $i_{L,on}(t)$ is the inductor current at time $t$. Taking the integral of both sides of equation (14) results in equation (15):

$$i_{L,on}(t) = \frac{1}{L_f} \cdot \int_0^t (V_{in} - V_o) \, dt$$

wherein:
- $V_{in}$ is the DC link voltage; and
- $V_o$ is the output voltage for the LEDs. $V_o$ can be calculated using equation (16):

$$V_o = \frac{V_{in}}{N_{led}} \cdot \sum_{n=1}^{N_{led}}$$

Finding the integral of equation (15) results in equation (17):

$$i_{L,on}(t) = \frac{1}{L_f} \cdot (V_{in} - V_o) \cdot t + C$$

Evaluating the integration constant $C$ at the beginning and end of the turn-on cycle of switch 96 results in two solutions as represented by equations (18) and (19):

$$i(0) = C = I_o$$

$$i(D.T_s) = C = I_{pk} - \frac{V_{in} - V_o}{I_f} \cdot (1 - D) \cdot T_s$$

An expression for the average inductor current $I_o$ can be represented by equation (25):

$$I_o = \frac{V_o}{(1 - D) \cdot T_s}$$

During turn-off of switch 96, a function for current $i_{L,off}$ can be represented using equations (20)-(22):

$$v_{L,off}(t) = L_f \cdot \frac{d}{dt} i_{L,off}(t)$$

Taking the integral of both sides of equation (20) results in equation (21):

$$i_{L,off}(t) = \frac{1}{L_f} \cdot \int_0^t (-V_o) \, dt$$

Finding the integral of equation (21) results in equation (22):

$$i_{L,off}(t) = \frac{-V_o}{I_f} \cdot t + C$$

Evaluating the integration constant $C$ at the beginning and end of the turn-off cycle of switch 96 results in two solutions as represented by equations (23) and (24):

$$i(0) = C = I_{pk}$$

$$i(D.T_s) = C = I_o - \frac{V_o}{I_f} \cdot (1 - D) \cdot T_s$$

A expression for the average inductor current $I_o$ can be represented by equation (25):

$$I_o = \frac{1}{T_s} \cdot \int_0^{T_s} i_{L,off}(t) \, dt$$

Substituting $V_o/V_{in}$ for the duty cycle $D$ and solving for $I_o$ results in an equation (27):

$$I_o = \frac{1}{2} \cdot \frac{2 \cdot I_f \cdot V_{in} \cdot (V_o \cdot T_s + V_o^2 \cdot T_s)}{V_{in} \cdot I_f}$$

Setting equation (27) equal to zero and solving for $I_f$ results in a value for inductor $I_f$ that will provide inductor current operating at the boundary between discontinuous conduction mode and continuous conduction mode as represented by equation (28):

$$I_f = \frac{-1}{2} \cdot \frac{V_o \cdot T_s}{I_o \cdot V_{in}}$$

Selecting an inductor value $I_f$ that is larger than the value calculated by equation (28) can permit current regulator 32 to
provide inductor current for maintaining continuous conduction mode. In other embodiments, inductor value $L_f$ may be selected so that current regulator 18 is in discontinuous conduction mode.

For instance, if the maximum DC link voltage $V_{in}$ is 400 V, maximum output voltage for the LEDs $V_o$ is 117 V, the desired average LED current $I_{avg}$ is 0.35 A, and the switching period of the converter $T_s$ is 0.01 ms, will result in an inductor value $L_f$ of 1200 µH. One or more inductors can be used to realize the $L_f$ inductor value in current regulator power section 32. For example, two inductors connected in series each having a value of 750 µH can be sufficient to meet an inductor value $L_f$ of 1200 µH. Other suitable inductor values $L_f$ are also available.

The average for the average current $I_{avg}$ from equation (25) can also be used to calculate the peak inductor current $I_{pk}$. Substituting equation (17) (using the integration constant from equation (19)) and equation (22) (using the integration constant from equation (23)) into equation (25) results in equation (29):

$$I_{pk} = \frac{1}{N} \int_0^{\infty} \left( \frac{1}{L_f} \left( V_{in} - V_o - t + I_{pk} \right) \right) dt + \int_0^{\infty} \left( \frac{1}{L_f} \left( V_{in} - V_o \right) \right) dt$$

Substituting $V_o/V_{in}$ for the cycle duty $D$ and solving for $I_{pk}$ results in an equation (30):

$$I_{pk} = \frac{1}{2} \frac{2 \cdot I_{avg} \cdot L_f + V_o \cdot T_s \cdot V_{in} - V_o \cdot T_0}{V_{in} \cdot L_f}$$

When switch 96 is closed, current controller 102 monitors the current through LEDs 20 by measuring the voltage drop across sense resistors 108, 110, 112, 114, 116, 118 and 120. This current feedback I$w_{Fbk}$ can be fed through a first order RC filter composed of feedback filter resistor 122 and feedback filter capacitor 124. A time constant $\tau_0$ can be calculated for the current feedback using equation (31):

$$\tau_0 = \frac{1}{N \cdot F_c}$$

wherein

- $N$ is a constant indicating the magnitude of $\tau$ as compared to the switching period of the DC-DC converter;
- $\tau$ is the time constant for the current feedback; and
- $F_c$ is the switching frequency of the power converter.

In conjunction with equation (31), values for resistor 122 and capacitor 124 can be calculated using equation (32):

$$\tau = \tau_0 \cdot CF$$

After passing through feedback filter resistor 122 and feedback filter capacitor 124, current feedback is fed to current controller 102, which can provide a pulse width modulated (PWM) control signal through a gate resistor 104 to switch 96.

As illustrated in FIG. 3, current controller 102 can be realized by an IC 200 that can control the average LED current $I_{avg}$ by comparing the current feedback to an internal reference. In response to the current feedback, current controller 103 provides a PWM control signal through gate resistor 104 to the gate of switch 96. According to techniques such as that described by UCC3800 BiCMOS Current Mode Control ICs, which is incorporated herein in its entirety by reference, the oscillator frequency, voltage reference $V_{5RF}$ and compensation waveform can be configured to provide the appropriate output $V_{G1}$ for driving the gate of switch 96.

Generally, as shown in FIG. 3, the oscillator frequency can be configured to, for example, 100 kHz by selecting appropriate values for a timing capacitor 202 and serially connected timing resistors 204 and 205. Timing resistors 204 and 205 can be connected between voltage reference $V_{5RF}$ and an RC input of the IC 200. Alternatively, timing resistors may be implemented using a single resistor, multiple resistors in series, multiple resistors in parallel, or any other suitable series or parallel combination of resistors. Timing capacitor 202 can be connected between the RC input and a digital ground DGND.

For example, a sawtooth waveform can be generated by IC 200. The oscillator waveform can be generated by a ramp up waveform and a ramp down waveform represented by equations 33 and 34, respectively:

$$V_{rmp}(t) = V_{low} + V_{ref} \left(1 - e^{-\frac{t}{R \cdot C}}\right)$$

$$V_{rmd}(t) = V_{high} - V_{ref} \left(1 - e^{-\frac{t}{R \cdot C}}\right)$$

wherein

- $V_{rmp}(t)$ is the ramp up interval;
- $t$ is the time;
- $V_{low}$ is the low oscillator threshold voltage;
- $V_{ref}$ is the reference voltage $V_{5RF}$;
- $R$ is the timing resistor; and
- $C$ is the timing capacitor.

Similarly, substituting $V_{low}$ for $V_{rmp}(t)$ in equation (33) and solving equation (33) for time $t$ results in the time to ramp up to the high oscillator threshold voltage as represented by equation (35):

$$t_{rmp}(R, C) = -\frac{\ln \left(\frac{V_{low} + V_{ref}}{V_{ref}}\right)}{R \cdot C}$$

wherein

- $t_{rmp}$ is the time to ramp up to the high oscillator threshold voltage.

Similarly, substituting $V_{low}$ for $V_{rmp}(t)$ in equation (34) and solving equation (34) for time $t$ results in
the time to ramp down to the low oscillator threshold voltage as represented by equation (36):

\[ t_{\text{down}}(C_T) = -\log\left(\frac{V_{\text{low}, \text{th}}}{V_{\text{th}}}ight) R_{\text{d}} C_T; \]  

(36)

wherein

\[ t_{\text{up}} \] is the time to ramp up to the high oscillator threshold voltage.

Accordingly, from equations (33)-(36) the oscillator waveform can be represented by equation (37):

\[ V_{\text{osc}}(t) = \begin{cases} V_{\text{rpm}, \text{up}}(t) & \text{if } t < t_{\text{up}}(R_T, C_T) \\ V_{\text{rpm}, \text{up}}(t - t_{\text{up}}(R_T, C_T)) & \text{if } t \geq t_{\text{up}}(R_T, C_T); \end{cases} \]  

(37)

wherein

\( V_{\text{osc}}(t) \) is the oscillator waveform.

Current controller 102 can also include a slope compensation scheme for providing constant current regulation. Preferably, the slope of the oscillator waveform \( V_{\text{osc}}(t) \) should be constant so as to not affect the slope compensation technique. The slope compensation scheme can be realized by a transistor 206 and compensation resistor 208 to buffer the oscillator waveform generated from timing capacitor 202. Transistor 206 and compensation resistor 208 may cause the ramp up waveform \( V_{\text{rpm}, \text{up}}(t) \) to have a different shape due to, for example, current gain of transistor 206. For example, still referring to FIG. 3, the altered ramp up waveform can be represented by equation (38):

\[ V_{\text{rpm}, \text{up}}(t) = \frac{-R_e \cdot \beta \cdot R_{R2} \cdot R_{VBE} \cdot V_{R2} \cdot \beta \cdot V_{ref} \cdot R_{R3} - V_{\text{rpm}, \text{up}}(t)}{R_{R1} \cdot \beta \cdot R_{R2} \cdot R_{R2} + R_{R2} \cdot \beta \cdot \beta}; \]  

(38)

\( V_{\text{rpm}, \text{up}}(t) \) is the altered ramp up waveform as a function of time \( t \);
\( R_e \) is the emitter resistance of transistor 206;
\( \beta \) is the current gain of transistor 206;
\( V_{\text{BE}} \) is the base-emitter voltage of transistor 206;
\( R_{R1} \) and \( R_{R2} \) are the timing resistors 204 and 205;
\( V_{\text{ref}} \) is the reference voltage \( V_{\text{REF}} \); and
\( V_{\text{rpm}, \text{up}}(t) \) is the ramp up interval as a function of time \( t \).

Preferably, the current feedback at the minimum DC link voltage \( V_{\text{link}_{\text{min}}} \) and maximum voltage \( V_{\text{link}_{\text{max}}} \) will be the same. Using, for example, superposition, feedback current can be represented by equation (39):

\[ i_{\text{LS}}(t) = \frac{i_{\text{FB}}(t) - R_s \cdot R_{\text{comp}}}{R_s + R_{\text{ref}} + R_{\text{comp}}} \cdot V_{\text{rpm}, \text{up}}(t) + \frac{R_s + R_{\text{ref}} + R_{\text{comp}}}{R_s + R_{\text{ref}} + R_{\text{comp}}}; \]  

(39)

wherein

\( i_{\text{FB}}(t) \) is the feedback current;
\( i_{\text{FB}}(t) \) is the inductor current as a function of time \( t \);
\( R_s \) is the current sense resistor;
\( R_{\text{comp}} \) is the compensation resistor;
\( R_f \) is the feedback filter resistor; and
\( V_{\text{rpm}, \text{up}}(t) \) is the altered ramp up interval waveform as a function of time \( t \).

If the inductor value \( L_f \) calculated in equation (28) provides a peak value of current feedback that is over a preferred peak value of current feedback, such as 0.5 A, the value of the inductor \( L_f \) can be varied so that the peak value does not exceed this preferred value. Specifically, the peak values of the current at the minimum DC link voltage \( V_{\text{link}_{\text{min}}} \) and the maximum voltage \( V_{\text{link}_{\text{max}}} \) can be calculated using equation (30). Further, the peak ramp waveform values at the minimum DC link voltage \( V_{\text{link}_{\text{min}}} \) and the maximum voltage \( V_{\text{link}_{\text{max}}} \) can be calculated using equation (38). Accordingly, substituting these values into equation (39) can give equations for the peak feedback current at the minimum and maximum DC link voltage operating points as represented by equations (40) and (41):

\[ i_{\text{LS}, \text{pk}} = \frac{i_{\text{FB}, \text{pk}} \cdot R_s + R_{\text{comp}}}{R_s + R_{\text{ref}} + R_{\text{comp}}} \cdot V_{\text{rpm}, \text{pk}}(t) + \frac{R_s + R_{\text{ref}} + R_{\text{comp}}}{R_s + R_{\text{ref}} + R_{\text{comp}}}; \]  

(40)

wherein

\( i_{\text{FB}, \text{pk}} \) is the peak feedback current at the maximum voltage \( V_{\text{link}_{\text{max}}} \);
\( i_{\text{FB}, \text{pk}} \) is the peak value of the inductor current at the maximum voltage \( V_{\text{link}_{\text{max}}} \); and
\( V_{\text{rpm}, \text{pk}}(t) \) is the peak ramp waveform value at the maximum voltage \( V_{\text{link}_{\text{max}}} \).

\[ i_{\text{LS}, \text{pk}} = \frac{i_{\text{FB}, \text{pk}} \cdot R_s + R_{\text{comp}}}{R_s + R_{\text{ref}} + R_{\text{comp}}} \cdot V_{\text{rpm}, \text{pk}}(t) + \frac{R_s + R_{\text{ref}} + R_{\text{comp}}}{R_s + R_{\text{ref}} + R_{\text{comp}}}; \]  

(41)

wherein

\( i_{\text{FB}, \text{pk}} \) is the peak feedback current at the minimum voltage \( V_{\text{link}_{\text{min}}} \);
\( i_{\text{FB}, \text{pk}} \) is the peak value of the inductor current at the minimum voltage \( V_{\text{link}_{\text{min}}} \); and
\( V_{\text{rpm}, \text{pk}}(t) \) is the peak ramp waveform value at the minimum voltage \( V_{\text{link}_{\text{min}}} \).

Setting equations (40) and (41) equations equal to each other gives a peak value of current feedback that is the same at the minimum and maximum DC link voltage operating points. From these equations, appropriate values for current sense resistor 108 (\( R_s \)) and compensation resistor 208 (\( R_{\text{comp}} \)) can be determined. Power loss calculations can be performed, by assuming worst case RMS currents, for current sense resistor 108 and compensation resistor 208. However, power loss may be minimal in, for example, compensation resistor 208 so that a value, such as 7.5 k, can be utilized without a power loss analysis. Other suitable compensation resistor values and techniques for selecting compensation resistor values are also available.

A realizable value and a number of resistors can be chosen for current sense resistor by determining the worst case power loss. One technique to determine the worst case power loss is to assume that the ramp waveform \( V_{\text{rpm}, \text{up}}(t) \) is not added to the feedback current. The scalar for the current can be represented by equation (42) and the limited peak current can be represented by equation (43)
The peak current that

$$i_{\text{peak}} = \frac{\text{Vref}}{K_{\text{load}}}$$

wherein $K_{\text{load}}$ is the scalar for the feedback current. The peak current that

$$P_{\text{tot}} = \frac{1}{2} R_s i_{\text{peak}}^2$$

wherein $R_s$ is the power rating for the current sense resistor; $i_{\text{peak}}$ is the maximum current cycle;

$$V_{\text{drain}}$$

is the peak current limited by the maximum voltage reference in the IC current controller; and $\text{Vref}_{\text{max}}$ is the maximum voltage reference in the in the IC current. Accordingly, the worst case power loss can be

$$P_{\text{tot}} = (V_{\text{ref}})^2 i_{\text{peak}}^2 R_s$$

wherein $V_{\text{ref}}$ is the voltage reference of the IC; $i_{\text{peak}}$ is the peak current; and $R_s$ is the maximum cycle.

An example of such a resistor can be implemented in lieu of one current sense resistor $108$ such that the power rating of current sense resistor $108$ is not exceeded. For example, 7 resistors can be connected in parallel, each having a value of 2.7Ω. Other suitable current sense resistor values and techniques for selecting current resistor values are also available.

UCS3800 BiCMOS Current Mode Control ICs, referenced above, also provides a technique to set up the internal current reference of IC $200$. Still referring to FIG. 3, a potentiometer $210$ is connected between voltage reference $5 \text{Vref}$ and $\text{GND}$. Connected in parallel to potentiometer $210$ are resistors $212$ and $214$. Capacitor $216$ is connected in parallel to resistor $214$. Resistor $218$ has one end connected to capacitor $216$ and the other end connected to a point connecting the inverting input of the error amplifier (FB) as well as the output of the error amplifier (COMP), which is connected through capacitor $220$ and resistor $222$. Other suitable current resistor values and techniques for selecting current resistor values are also available.

Referring to FIG. 5, IC $200$ can be powered by providing a voltage reference $V_{12}$ to pin VCC by using power circuitry $400$. Referring to FIG. 5, voltage reference $V_{12}$ is generated through IC $401$. IC $401$ can be a positive voltage regulator such as Texas Instruments Part No. UA782012. DC link voltage VDC is provided through a bias resistor $402$ to create a voltage potential Vz. A zener diode $404$ is connected to a point between bias resistor $402$ and VIN and to one end of a resistor $406$ to absorb excess voltage. The other end of resistor $406$ is connected to GND. Vz is filtered by an input filter capacitor $406$ and is fed into the input of IC $401$ (VIN).

VIN can also be fed from the drain-source voltage of switch $96$ through a boost resistor $126$. Accordingly, the drain source-voltage of switch $96$ may provide the power to permit control circuits of power converter $18$ to operate over a wide range. The output of IC $401$ provides the voltage reference $V_{12}$ filtered by an output filter capacitor $408$. Other suitable techniques, components and configurations for powering IC $200$ are also available.

Returning to FIG. 1, selection of switch $96$ can be accomplished by, for example, estimating the maximum power loss of the switch using equation (45):

$$P_{\text{tot}} = P_{\text{sw}} + P_{\text{cond}}$$

wherein

$$P_{\text{tot}}$$

is the total power loss of the switch; $P_{\text{sw}}$ is the switching loss of the switch; and $P_{\text{cond}}$ is the conduction loss of the switch. The maximum switching loss $P_{\text{sw}}$ of switch $96$ can be calculated using equation (46):

$$P_{\text{sw}} = \frac{1}{2} (V_{\text{link}} - V_{\text{link}}_{\text{max}}) i_{\text{link}}^2$$

wherein

$F_{\text{sw}}$ is the switching frequency of the converter; $V_{\text{link}}$ is the maximum DC link voltage; $V_{\text{link}}_{\text{max}}$ is the maximum DC link voltage; $i_{\text{link}}$ is the average inductor current; $t_{\text{r}}$ is the switching rise time; and $t_{\text{f}}$ is the switching fall time. Assuming that switch $96$ is continuously on at the highest temperature, the maximum conduction loss $P_{\text{cond}}$ of switch $96$ can be estimated using equation (47):

$$P_{\text{cond}} = \frac{1}{2} i_{\text{r}}^2 (R_{\text{ds}_{\text{on}}})_{\text{max}}$$

wherein

$R_{\text{ds}_{\text{on}}}$ is the maximum resistance between the drain and the source when the switch is closed. The resistance $R_{\text{ds}_{\text{on}}}$ can also be scaled by a temperature scale factor to obtain a more accurate conduction loss $P_{\text{cond}}$.

If switch $96$ were to operate without a heatsink, the temperature rise of switch $96$ due to power dissipation can be estimated using equation (48):

$$\text{Temp Rise} = \frac{P_{\text{tot}}}{\theta_{\text{ja}}}$$

wherein

$\theta_{\text{ja}}$ is the junction to ambient thermal resistance of the switch; $\theta_{\text{jc}}$ is the junction to case thermal resistance of the switch; and $\Delta T$ is the change between the maximum temperature of the switch and the ambient temperature.

Switch $96$ may be any suitable controllable switching device such as a BJT, IGBT, standard FET, etc., that can be controlled through application of a control signal. An example of such a suitable switch $96$ is STMmicroelectronics N-Channel Power MOSFET Part No. STFV4N1050. Other suitable switching devices and techniques for determining suitable switching devices are also available.

The rise time rate of change of current $\frac{\text{di}}{\text{dt}}$ and rise time rate of change of voltage $\frac{\text{dv}}{\text{dt}}$ of switch $96$ can change depending on the value of gate resistor $104$. Equation (50) represents an estimation of turn-on $\frac{\text{di}}{\text{dt}}$:

$$\frac{\text{di}}{\text{dt}} = \frac{1}{L_{\text{on}}}$$

wherein

$\text{di/dt}$ is the rise time rate of change of current of the switch;
Id is the load current during the switching time test circuit; and
t\text{rise} is the rise time scaled by the gate resistor value. The rise time scaled by the gate resistor value \( t_{\text{rise}} \) can be calculated using equation (51):

\[
t_{\text{rise}} = \frac{R}{R_{\text{avg}}} \cdot t_r.
\]  

(51)

wherein:
- \( R \) is the gate resistor value;
- \( t_r \) is the rise time of the switch;
- \( R_{\text{avg}} \) is the minimum average resistor value to achieve the rise and fall times of the switch. The minimum average resistor value \( R_{\text{avg}} \) can be calculated using equation (52):

\[
R_{\text{avg}} = \frac{V_{G\text{S}} - V_{G\text{S,th}}}{\frac{t_r}{2}}.
\]  

(52)

wherein:
- \( V_{G\text{S}} \) is the gate to source voltage of the switch;
- \( V_{G\text{S,th}} \) is the gate to source threshold voltage of the switch;
- \( t_r \) is the rise time of the switch; and
- \( t_f \) is the fall time of the switch.

The rise time rate of change of voltage \( \frac{dV}{dt} \) of switch 96 can be estimated using equation (53):

\[
\frac{dV_{dt}}{dt} = \frac{V_{DD} \cdot 80\%}{t_{\text{rise}}},
\]  

(53)

wherein:
- \( \frac{dV_{dt}}{dt} \) is the rise time rate of change of voltage of the switch;
- \( V_{DD} \) is the DC link voltage during the switching time test circuit; and
- \( t_{\text{rise}} \) is the rise time scaled by the gate resistor value (as calculated by equation (51)).

FIGS. 7A and 7B illustrate \( \frac{dV}{dt} \) and \( \frac{dV}{dt} \), respectively, as a function of different values of gate resistor 104. Preferably, a value for gate resistor 104 is chosen so that both \( \frac{dV}{dt} \) and \( \frac{dV}{dt} \) are relatively constant. Gate resistor 104 may be implemented using a single resistor, multiple resistors in series, multiple resistors in parallel, or any other suitable series or parallel combination of resistors. For example, gate resistor may be implemented using a combination of two 100 ohm resistors. Other suitable gate resistor values and techniques for selecting gate resistor values are also available.

A shunt voltage regulator circuit 34 is optionally coupled in parallel to the current regulator power section 31. Shunt voltage regulator 34 as shown clamps the DC link voltage VDC so that it does not exceed, for example, a maximum DC link voltage Vlink_{max}. The voltage clamping can be accomplished by, for example, PWM of a power switch 130 to provide a controllable power loss in the shunt regulator load 132 (e.g., one or more resistors). In other words, shunt voltage regulator 34 draws increasing current from the ballast 16 through the rectifier 28 and main filter capacitor 30 and wastes that power in the shunt regulator load 132 if the voltage exceeds a preset value. This prevents the output voltage from the ballast 16 from rising excessively by having an amount of power dissipation. Accordingly, the operating point (e.g., 120 V) of light 10 can be controlled based on the impedance of the shunt regulator load 132.

As one non-limiting example, the normal operating point of the replacement lamp 30 can be around 120 V and 220 mA. Of course, other replacement lamps can operate at different points. When replacement lamp 30 is operating from ballast 34, the power in lamp 30 increases as the current in lamp 30 decreases, and vice versa, because the operating point voltage of lamp 30 is below the maximum power point of the ballast.

A first end of shunt regulator load 132 is connected to the cathode of recirculation diode 98 the second end of shunt regulator load 132 is connected to a first end of power switch 130. The second end of power switch 130 is connected to PGND. Further, a recirculation diode 134 is connected in parallel to shunt regulator load 132. While shunt voltage regulator 34 functions in part to protect components from high voltages, it also causes power dissipation through a shunt regulator load 132. The resistance of shunt regulator load can be calculated by using equation (54):

\[
r_{\text{load}} = \frac{V_{\text{link}}^{2}}{P_{\text{max}}},
\]  

(54)

wherein:
- \( V_{\text{link}} \) is the maximum DC link voltage; and
- \( P_{\text{max}} \) is the maximum output power of the LEDs. Shunt regulator load 132 may be implemented with one resistor, multiple resistors in series, multiple resistors in parallel, or any other suitable series or parallel combination of resistors.

A voltage controller 136 provides a PWM control signal through gate resistor 138 to the gate of switch 130. A suitable value for gate resistor 138 can be determined by using techniques similar to that described in connection with gate resistor 104 of current controller 102. Further, the type of switch 130 can be chosen using techniques similar to that described in connection with switch 96 of current controller 102. Although gate resistor 138 is shown as one resistor, gate resistor may be implemented multiple multiple resistors in series, multiple resistors in parallel, or any other suitable series or parallel combination of resistors.

The embodiments of the present invention are not limited to shunt voltage regulator circuit 34. For example, a linear regulator in the form of an integrated circuit can be used in lieu of or in addition to shunt voltage regulator circuit 34. Of course, other regulator circuits are also available.

Referring to FIG. 4, voltage controller 136 can be realized by an IC 300 that can control the voltage to shunt regulator lead 32. The DC link voltage VDC is fed into a resistor divider network, which can include resistors 304 and 306. Each resistor 304 and 306 may be implemented by any number of resistors and may be in any suitable series or parallel configuration. For example, six resistors can be serially and parallelly connected in lieu of one resistor 304 so that the power rating of each of the resistors is not exceeded. A filtering capacitor is connected in parallel to resistor 306, each having one end connected to ground. At the opposing end of capacitor 308 is connected to the inverting input of the error amplifier (FB), the ends of capacitor. The opposing end of capacitor 308 is also connected to the output of the error amplifier (COMP), which is connected through a capacitor 310 in parallel with a resistor 312 connected in series with a capacitor 314.
The oscillator frequency can be configured to, for example, 100 kHz by selecting appropriate values for a timing resistors 316. Timing resistor 316 can be connected between RT and GND. Timing capacitor 202 can be connected between the RC input and a digital ground DGND.

3. The short-circuit protection pin (SCP) and dead-time control pin (DTC) can be grounded.

4. The output driver may not have enough drive capability to supply the proper gate drive through gate resistor 138 to the gate of switch 130. Accordingly, an optional driver IC 402 can be connected to the output of IC 300 (OUT) to supply a suitable gate voltage drive. One suitable driver is Texas Instruments Mosfet Driver Part No. TPS2829. Other suitable drivers are also available.

While the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiments but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, which scope is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures as is permitted under the law.

What is claimed is:

1. An illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast, the ballast configured to provide a current signal, the illumination device comprising:
   a smoothing filter circuitry configured to provide a rectified voltage output;
   a full-wave rectifier electrically coupled to the protection circuitry and configured to produce a rectified voltage output.

2. The illumination device of claim 1, wherein the protection circuitry comprises:
   a surge suppressor configured to limit inrush current from the ballast.

3. The illumination device of claim 1, wherein the protection circuitry comprises:
   at least one discharge resistor electrically coupled in parallel to the at least one capacitor.

4. The illumination device of claim 1, wherein the current regulator power circuit further comprises:
   at least one inductor in series with the LEDs.

5. The illumination device of claim 1, wherein the current regulator power circuit further comprises:
   a recirculation diode electrically coupled in parallel with the at least one inductor and the LEDs.

6. A method of supplying power to an illumination device including LEDs and connected to an existing fluorescent lamp fixture including a conventional ballast, the method comprising:
   receiving a current signal from the conventional ballast;
   protecting the illumination device from the received current signal;
   rectifying the received current signal to produce a rectified voltage output;
   supplying current to the LEDs in response to the PWM control signal so that the LED current reaches an average LED current.

7. The method of claim 7, wherein the average LED current is determined based on the rectified voltage output and an output voltage of the LEDs.

8. The method of claim 7, wherein the PWM control signal is supplied to a switching element.

9. The method of claim 7, further comprising:
   filtering the rectified current signal.

10. An illumination device including LEDs for connection to an existing fluorescent lamp fixture including a conventional ballast, the illumination device comprising:
    means for receiving a current signal from the conventional ballast;
    means for protecting the illumination device from the received current signal;
    means for rectifying the received current signal to produce a rectified voltage output;
    means for sensing the current through the LEDs;
    means for generating a pulse width modulated (PWM) control signal from a current control circuit based on the sensed current;
    means for supplying current to the LEDs in response to the PWM control signal so that the LED current reaches an average LED current.

11. The illumination device of claim 13, further comprising:
    means for filtering the rectified current signal.

12. The illumination device of claim 13, wherein the means for protecting the illumination device comprises:
    an inrush protection circuit configured to limit inrush current from the ballast.

13. The illumination device of claim 13, wherein the means for protecting the illumination device comprises:
    an inrush protection circuit configured to limit inrush current from the ballast.

14. The illumination device of claim 13, wherein the means for protecting the illumination device comprises:
    a surge suppressor configured to suppress ballast voltage from the ballast.