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(54) PULSE-GENERATING CIRCUIT

(71) We, MITSUBISHI DENKI KABUSHIKI KAISHA, a Japanese Company, of 2-3, Marunouchi 2-chome, Chiyoda-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a Patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The present invention relates to a pulse-generating circuit and in particular is concerned with the generation of steep output pulses by the rapid discharge of a capacitor.

Simple capacitive discharge pulse-generating circuits have been used for generating sparks for photographic flash equipment or the ignition of a gas lighter or a stove, for example.

Reference will now be made to Figures 1 and 2 of the accompanying drawings, of which:-

Figure 1 is a circuit diagram of a conventional pulse-generating circuit; and

Figure 2 is a waveform diagram illustrating the operation of the circuit of Figure 1.

In Figure 1, the reference numeral 1 designates a DC power source such as a dry battery giving 9 to 12V; 2 designates a starting switch; 3 designates a charging resistor; 4 designates a capacitor; 5 designates a trigger element; 6 designates a thyristor; 7 designates a load (load resistor); and 8 and 9 respectively designate output terminals.

When the starting switch 2 is turned on, the capacitor 4 is charged from the DC power source 1 through the switch 2 and the resistor 3. The charging time-constant depends upon the resistance of the resistor 3 and the capacitance of the capacitor 4. When the charged voltage of the capacitor 4 reaches the switching voltage E_s of the trigger element 5, the trigger element 5 is turned on to feed a trigger signal to the gate of the thyristor 6 to turn on the thyristor 6. As a result, the charge of the capacitor 4 is discharged through the load resistor 7 and the thyristor 6. A pulse output is thus generated across the output terminals 8, 9.

Figure 2 shows the waveform of the voltage across the capacitor 4. The charging operation is initiated by turning on the starting switch 2. When the voltage reaches the switching voltage E_s of the trigger element 5 at the time t_1, the charge is immediately discharged to zero. After the discharge, the thyristor 6 is immediately turned off and re-charging of the capacitor is initiated to repeat the operation. Accordingly, as shown in Figure 2, the charging and discharging operation is repeated with a period of t_1 to give repetitive pulses at the output terminals 8, 9.

In such a circuit, the initiation of the discharge depends upon the specific switching voltage E_s of the trigger element 5. If the voltage of the DC power source 1 drops to a level to be insufficient to charge to the switching voltage E_s, it is impossible to obtain the pulse output. Accordingly, when the voltage of the DC power source 1 is subject to variation, the switching voltage E_s of the trigger element 5 may be set at a relatively low level to provide output pulses for a wide range of voltages of the DC power source. Accordingly, the voltage of the pulse output is lowered and the output voltage is not proportional to the voltage of the DC power source 1. When the voltage of the DC power source 1 falls to lower than the switching voltage E_s, no output is generated. In this case, it is difficult to discriminate this situation from failure of the circuit.

It is an object of the present invention to provide an improved pulse-generating circuit.

According to the invention there is provided a pulse generating circuit which comprises a DC power source; a capacitor connected in series through a charging resistor to said DC power source; a series connection of a load and a main thyristor which is connected across said capacitor; a shunt circuit for generating a predetermined shunt potential at a shunt point, said shunt circuit being connected directly across said DC power source; and a three-terminal triggering element for triggering the thyristor, the triggering element having a first main terminal connected to the junction of the charging resistor and the said capacitor, a second main terminal connected to the gate terminal of said main thyristor and a control terminal directly or indirectly connected to the shunt point of said shunt circuit.

The invention will further be described with reference to Figures 3 to 14 of the accompanying drawings, which are respectively circuit diagrams of various embodiments of the pulse-generating circuits according to the present invention.

Figure 3 is a circuit diagram of one embodiment of the pulse-generating circuit of the present invention wherein the DC power source 1 is connected in series with the starting switch 2, the charging resistor 3 and the capacitor 4 to form the charging circuit. On the other hand, a series connection of a main thyristor 6 and the load resistance 7 is connected across the capacitor 4. The output terminals 8, 9 are connected across the load resistor 7.

Between the gate terminal G of the main thyristor 6 and the positive pole terminal P of the capacitor 4, there is connected a three-terminal trigger element 5 whose cathode is connected to the gate terminal G and whose anode is connected to the positive pole terminal P.

Between the contact point M of the starting switch 2 and the charging resistor 3 and the negative terminal of the DC power source 1, there is connected a shunt circuit of a series combination of a diode 10 and a resistor 11. The gate terminal of the trigger element 5 is connected to a middle contact point N of the shunt circuit.

When the starting switch 2 is turned on, the capacitor 4 is charged from the DC power source 1 through the starting switch 2, the charging resistor and the capacitor 4. On the other hand, the gate potential of the trigger element 5 is always maintained at the difference between the voltage of the DC power source 1 and the barrier voltage of the diode 10 (about 0.5 to 0.7V). The operation of the circuit has different modes when the voltage of the DC power source 1 is higher or lower than the switching voltage E_s of the trigger element 5.

When the voltage of the DC power source 1 is higher than the switching voltage E_s of the trigger element 5, the voltage at the anode terminal of the trigger element 5 connected to the positive terminal of the capacitor 4 is lower than the gate potential when charging begins. Thus, current is not fed to the gate of the trigger element 5 and the trigger element 5 is not turned on. However, when the capacitor 4 is charged to reach the switching voltage E_s of the trigger element 5, the trigger element 5 is turned on whereby the gate trigger current of the thyristor 6 is fed through the trigger element 5 to trigger the thyristor 6 and the charge of the capacitor 4 is discharged through the load resistor 7 to generate the output voltage across the output terminals 8, 9.

On the other hand, when the voltage of the DC power source 1 is lower than the switching voltage E_s of the trigger element 5, the trigger element 5 is not self-triggered. Thus, when the capacitor 4 is charged to the voltage of the DC power source 1, current is fed from the anode terminal of the trigger element 5 to the gate terminal to turn on the trigger element 5 because the gate potential of the trigger element 5 is lower than the potential at the anode terminal for the barrier voltage of the diode 10. As a result, the thyristor 6 is triggered to generate the output voltage across the output terminals 8, 9.

Gate current is fed to the trigger element 5 and the thyristor 6 is triggered to generate the pulse output because of the self-triggering action of the trigger element 5 when the voltage of the DC power source 1 is higher than the switching voltage of the trigger element 5. Also, pulses are generated by detecting the fact that the charged voltage substantially reaches the voltage of the DC power source when the voltage of the DC power source 1 is lower than the switching voltage of the trigger element 5.

Figure 4 shows another embodiment of the present invention wherein the diode 10 is replaced by a resistor 12 in the embodiment of Figure 3. The same operation can be attained by selecting a suitable resistance for the resistor 12.

In the embodiments of Figures 3 and 4, a silicon unilateral switch SUS or a silicon bilateral switch SBS can be used as the trigger element 5.

Figure 5 shows another embodiment of the present invention wherein the trigger element 5 is replaced by an N gate thyristor 12N in the embodiment of Figure 3. The gate of the N gate thyristor 12N is connected to the shunt point N of the shunt circuit. The operation of the circuit of Figure 5 will be described.

When the switch 2 is turned on, the capacitor 4 is charged from the DC power source 1 through the starting switch 2 and the charging resistor 3. The gate potential of the N gate thyristor 12N is maintained to the voltage given by subtracting the barrier voltage of the diode (about 0.5 to 0.7V) from the voltage of the DC power source 1. At the initiation of the charging operation, the voltage at the anode terminal connected to the positive terminal of the capacitor 4 is lower than the gate potential whereby current is not fed to the gate of the N gate thyristor and the N gate thyristor is not turned on. Thus, when the voltage at the anode terminal of the N gate thyristor 12N reaches a level substantially equal to the voltage of the DC power source by charging the capacitor 4, the gate current is fed from the anode of the N gate thyristor 12N to the gate to turn on the N gate thyristor. As a result, the gate trigger current is fed to the gate of the thyristor 6 to trigger the thyristor 6 whereby the charge of the capacitor 4 is discharged through the load resistor 7 to generate a voltage between the output terminals 8, 9 which is substantially equal to the voltage of the DC power source 1. That is, the thyristor 6 is turned on to generate the pulse output across the load resistor 7 when the charged voltage of the capacitor 4 becomes substantially equal to the voltage of the DC power source 1.

Incidentally, two or more diodes 10 can be connected in series to compensate for the effects of temperature changes on the diode 10.

Figure 6 shows another embodiment of the pulse-generating circuit of the present invention, wherein the reference numeral 13 designates a PNP transistor; 14 to 16 designate resistors and 17 designates a diode.

The collector of the transistor 11 is connected to the control terminal of the thyristor 6, and the emitter of the transistor 11 is connected between the resistor 3 and the capacitor 4. The cathode of the rectifier 17 is connected to the base of the transistor 11 and the anode of the rectifier 17 is connected through the resistor 16 to the positive terminal of the DC power source 1. The resistor 14 is connected between the emitter and base of the transistor 13. The resistor 15 is connected between the base of the transistor 13 and the negative terminal of the DC power source 1.

The capacitor 4 is charged through the resistor 3 and also through the resistor 16, the diode 17, and the resistor 14. As a result, a voltage drop is caused in the resistor 14. The polarity of the voltage drop is in the direction for the reverse-bias of the emitter-base of the transistor 13 whereby the transistor 13 is turned off and the current is not fed to the gate of the thyristor 6.

On the other hand, when the charged voltage of the capacitor 4 becomes substantially equal to the voltage of the DC power source 1, the current fed to the diode 17 becomes zero whereby the charge of the capacitor 4 is discharged through the resistor 14 and the resistor 15. The polarity of the voltage drop in the resistor 14 is opposite to that in the charging operation and the transistor 13 is turned on. Accordingly, the collector current of the transistor 13 is fed to turn on the thyristor 6. At that time, the charged voltage of the capacitor 4 is the value given by subtracting the voltage drop of the rectifier 17 (about 0.7V) from the voltage of the DC power source 1 whereby a large output voltage is applied to the load resistor 7. The output voltage does not depend on the switching voltage E_s of the trigger element 5.

In circuits for firing a gas lighter, for example, a high spark voltage is required.

Figures 7 and 8 respectively show modifications of the pulse-generating circuit of Figure 6. In the embodiment of Figure 7, the diode 17 and the resistor 16 of Figure 6 are replaced by a series connection of a PNP transistor 18 and a resistor 16 which is connected to the DC power source 1. The base of the transistor 18 is connected to the base of the transistor 13.

In the embodiment of Figure 8, the transistor 13 of Figure 6 is replaced by an N gate thyristor 19.

The operation of the circuits is analogous with the operation of the circuit of Figure 6.

Figures 9 and 10 respectively show other embodiments of the invention. In Figures 9 and 10, a trigger element 20 such as an SUS or SBS is connected between the anode and gate of the thyristor 6 and a pulse transformer 21 is used instead of the load resistor 7.

In the circuits of Figures 6 and 7, when the charged voltage of the capacitor 4 reaches the voltage of the DC power source 1, the charge of the capacitor 4 is discharged. Accordingly, when the voltage of the DC power source 1 is high, excess energy, for example, more than twice the minimum energy needed for generating an output pulse is given. When a dry battery is used, this considerably shortens the life of the battery.

Moreover, the discharge always follows charging of the capacitor 4 to the voltage of the DC power source. If the power source voltage is high this results in a disadvantageously long pulse repetition period.

In the circuits of Figures 9 and 10, the switching voltage of the trigger element 20 is preset at a desired value whereby the capacitor 4 is discharged when the charged voltage of the capacitor 4 reaches a predetermined constant minimum voltage needed for spark discharge.

When the voltage of the battery 1 is higher than the switching voltage V_2 of the trigger element 20, the capacitor 4 is charged to a voltage equal to the switching voltage V_s. At this time, the trigger element 20 is turned on whereby the thyristor 6 is triggered. The charge of the capacitor 4 is discharged through the primary winding of the transformer 21 to cause a spark at terminals across the secondary winding of the transformer 21.

On the other hand, when the voltage of the battery 1 is lower than the switching voltage V_s of the trigger element 20, the trigger element 20 is not turned on. Accordingly, the circuits operate in a similar manner to those of the embodiments of Figures 6 and 7. Sparks are capable of being generated until the voltage of the battery falls below a limit governed by the discharge gap. With these arrangements energy loss can be reduced and battery life prolonged.

When the circuit is designed to trigger the trigger element 20 during most of the life of the battery, the charging resistor can be relatively high even though the repetition frequency is relatively high. Accordingly, a thyristor 6 having relatively a small holding current can be used. Even though a battery 1 is used having a voltage lower than the switching voltage of the trigger element 20, the discharge is initiated when the charged voltage of the capacitor 4 is substantially equal to the voltage of the battery. Accordingly, spark discharges can be obtained for relatively low voltage of the battery even though the discharge period is long. The life of the battery can be prolonged advantageously.

Figures 11 and 12 show the other embodiments of the present invention for preventing needless consumption of energy of the DC power source.

In the embodiment of Figure 11, a Zener diode 22 is connected between the gate terminal of the N gate thyristor 12N and the negative terminal of the capacitor 4 and a resistor 23 is connected between the gate of the N gate thyristor 12N and the shunt point N of the shunt circuit.

The capacitor 4 is charged by turning on the starting switch 2. When the charged voltage becomes higher than the Zener voltage of the Zener diode 22, a completed circuit is formed comprising capacitor 4, anode of N gate thyristor 12N, gate of N gate thyristor 12N, Zener diode 22 and capacitor 4. Thus, current is fed to the gate of the N gate thyristor 12N to turn on the thyristor and gate trigger current is fed to the thyristor 6 to turn on the thyristor 6. A pulse output is generated.

On the other hand, when the voltage of the DC power source 1 is lower than the Zener voltage of the Zener diode 22, the charge of the capacitor 4 is discharged when the charged voltage of the capacitor 4 becomes to be substantially equal to the voltage of the DC power source 1.

Consumption of unnecessary energy of the DC power source can be prevented without generating unnecessarily large output pulses.

Figures 13 and 14 show other embodiments of the present invention whereby a pulse output may be generated at the time the starting switch is turned on.

In the previous circuits, the capacitor 4 has substantially no charge when the starting switch 2 is turned on. When the switch 2 is turned on, the charging operation is initiated and the spark discharge is generated when the charge voltage reaches the predetermined voltage. If there is initial failure of firing of the gas lighter (to which the invention is applied), the switch 2 is kept ON whereby the spark discharge is repeatedly generated. The repetition period is selected to be O.5 to 1 second in order to prevent rapid run-down of the battery 1.

Accordingly, it takes 0.5 to 1 second to generate the first spark discharge after turning on the starting switch 2, whereby there is loss of gas and some irritation to the user.

In accordance with the circuit of the embodiments of Figures 13 and 14, the position of the starting switch 2 is modified whereby the capacitor 4 is charged before turning on the starting switch 2 and the charge of the capacitor 4 is discharged as the switch 2 is turned on.

In the embodiment of Figure 13, the starting switch 2 is connected between the resistor 11 of the shunt circuit and the negative terminal of the DC power source 1.

In the embodiment of Figure 14, the starting switch 2 is connected between the shunt point N of the shunt circuit and the gate terminal of the N gate thyristor 12N.

The operation of the embodiment of Figure 13 will be described. The capacitor 4 is charged to be substantially equal to the voltage of the DC power source 1 from the DC power source 1 through the charging resistor 3, before turning on the starting switch 2.

When the starting switch 2 is turned on the capacitor 4 is discharged through the circuit comprising positive terminal of capacitor 4, transformer 21, anode of N gate thyristor 12N, gate of N gate thyristor, resistor 11, switch 2 and negative terminal of capacitor 4 whereby the N gate thyristor 12N is triggered to turn on the thyristor.

The operation of the embodiment of Figure 14 is substantially the same as that of Figure 13.

The starting switch 2 can be connected between the cathode of the N gate thyristor 12N and the gate of the thyristor 6.

In the embodiments of Figures 13 and 14, the charge of the capacitor 4 with the potential substantially equal to the voltage of the

DC power source 1 is discharged when the starting switch 2 is switched on. Thus, the pulse output for the transformer 21 can be generated immediately on operation of the switch and the effective range of the voltage of the DC power source 1 can be broadened and the consumption of the battery can be minimised to prolong the life of the battery.

WHAT WE CLAIM IS:-

1. A pulse-generating circuit which comprises a DC power source; a capacitor connected in series through a charging resistor to said DC power source; a series connection of a load and a main thyristor which is connected across said capacitor; a shunt circuit for generating a predetermined shunt potential at a shunt point, said shunt circuit being connected directly across said DC power source; and a three-terminal triggering element for triggering the thyristor, the triggering element having a first main terminal connected to the junction of the charging resistor and the said capacitor, a second main terminal connected to the gate terminal of said main thyristor and a control terminal directly or indirectly connected to the shunt point of said shunt circuit.

2. A pulse-generating circuit according to Claim 1 wherein said shunt circuit is a series connection of a diode and a resistor.

3. A pulse-generating circuit according to either of the preceding claims wherein said three-terminal triggering element is a silicon unilateral switch SUS.

4. A pulse-generating circuit according to Claims 1 or 2 wherein said three-terminal triggering element is an N gate thyristor.

5. A pulse-generating circuit according to Claim 4 wherein a Zener diode is connected between the gate terminal of said N gate thyristor and the negative terminal of said capacitor, and a resistor is connected between the gate terminal of said N gate thyristor and the shunt point of said shunt circuit.

6. A pulse-generating circuit according to Claim 4 or Claim 5 wherein said starting switch is connected in a circuit for discharging said capacitor which connects the anode-gate of said N gate thyristor and said shunt circuit.

7. A pulse-generating circuit according to Claim 1 wherein said shunt circuit is a series connection of two resistors.

8. A pulse-generating circuit according to Claim 7 wherein said three-terminal triggering element is a silicon unilateral switch SUS.

9. A pulse-generating circuit according to Claim 7 wherein said three-terminal triggering element is an N gate thyristor.

10. A pulse-generating circuit according to Claim 9 wherein one end of said shunt circuit is connected to the contact of said charging resistor and said capacitor and a series connection of a resistor and a diode is connected between the shunt point of said shunt circuit and the other side of said charging resistor.

11. A pulse-generating circuit according to Claim 9 wherein a Zener diode is connected between the gate terminal of said N gate thyristor and the negative terminal of said capacitor and a resistor is connected between the gate terminal of said N gate thyristor and the shunt point of said shunt circuit.

12. A pulse-generating circuit according to Claim 9 wherein said starting switch is connected in a circuit for discharging said capacitor which connects the anode gate of said N gate thyristor and said shunt circuit.

13. A pulse-generating circuit according to Claim 7 wherein said three-terminal triggering element is a transistor.

14. A pulse-generating circuit according to Claim 13 wherein one end of said shunt circuit is connected between said charging resistor and the contact point of said capacitor and a series connection of a resistor and a diode is connected between the shunt point of said shunt circuit and the other side of said charging resistor.

15. A pulse-generating circuit according to Claim 14 wherein said triggering element is connected between the anode and gate of said thyristor.

16. A pulse-generating circuit according to Claim 13 wherein one end of said shunt circuit is connected to the contact point of said charging resistor and said capacitor and a base of a PNP transistor is connected to the shunt point of said shunt circuit, an emitter of said PNP transistor is connected to the other side of said charging resistor and a collector of said PNP transistor is connected through a resistor to the negative terminal of said DC power source.

17. A pulse-generating circuit according to Claim 15 wherein said triggering element is connected between the anode-gate of said thyristor.

18. A pulse-generating circuit according to any of the preceding claims wherein a pulse transformer is used as said load and a dry battery is used as said DC power source.

19. A pulse-generating circuit substantially as hereinbefore described with reference to any of Figures 3 to 14 of the accompanying drawings.

Agents for the Applicants
STEVENS, HEWLETT & PERKINS
Chartered Patent Agents
5, Quality Court
Chancery Lane
London WC2

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4 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1

FIG. 1

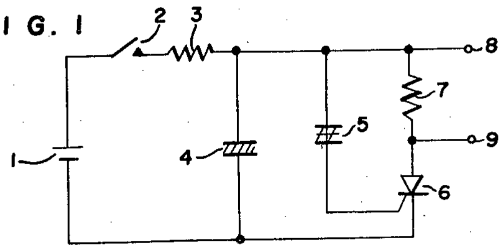


FIG. 2

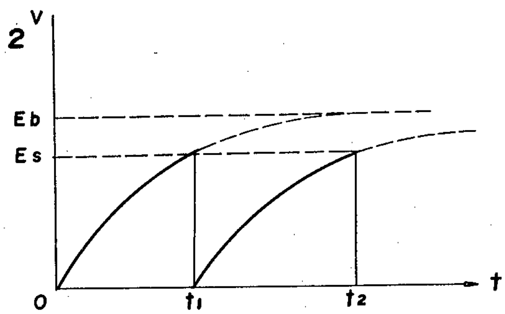


FIG. 3

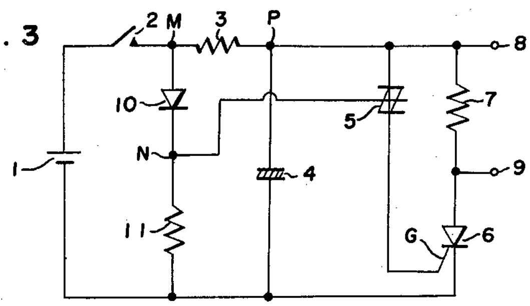


FIG. 4

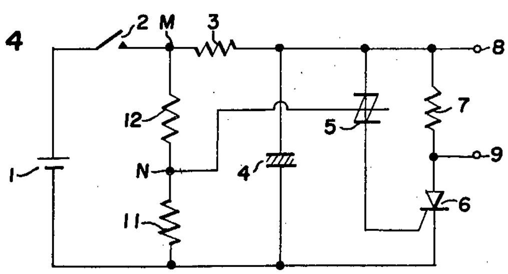


FIG. 5

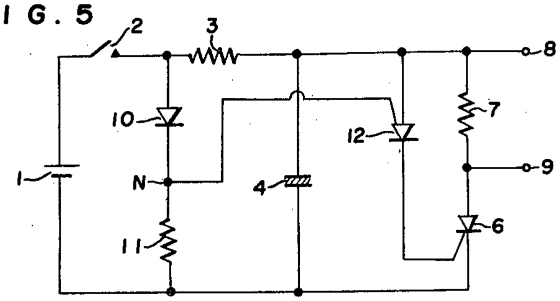


FIG. 6

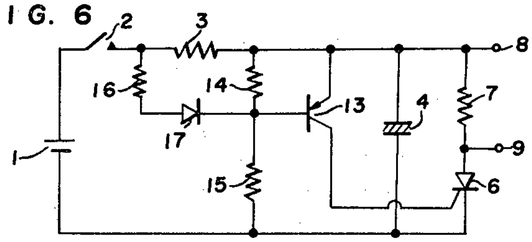


FIG. 7

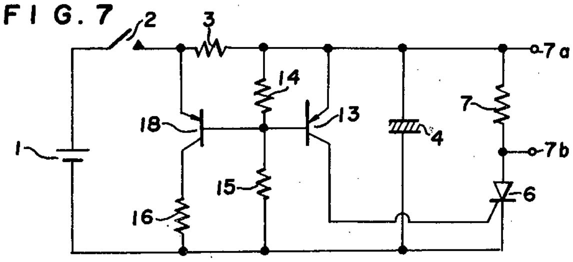


FIG. 8

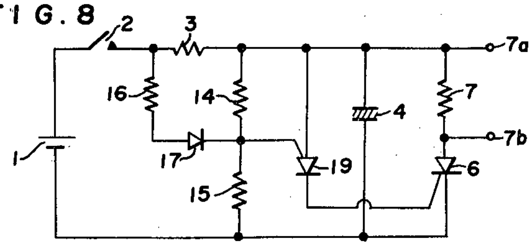


FIG. 9

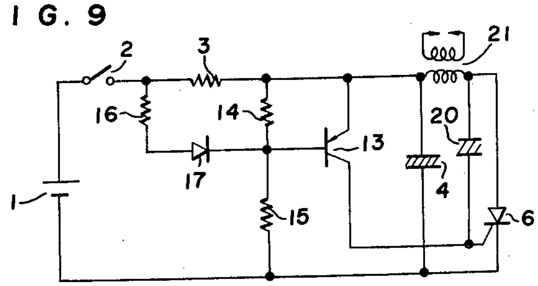


FIG. 10

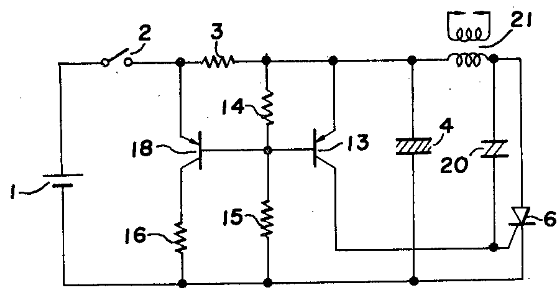
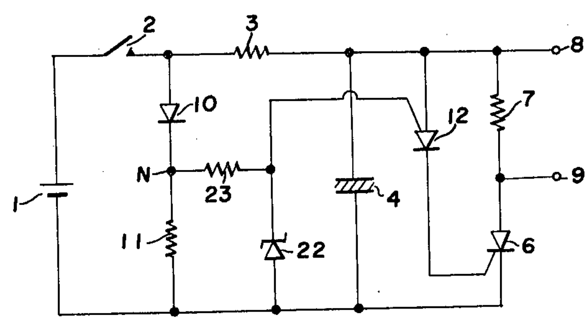


FIG. 11



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Sheet 4

FIG. 12

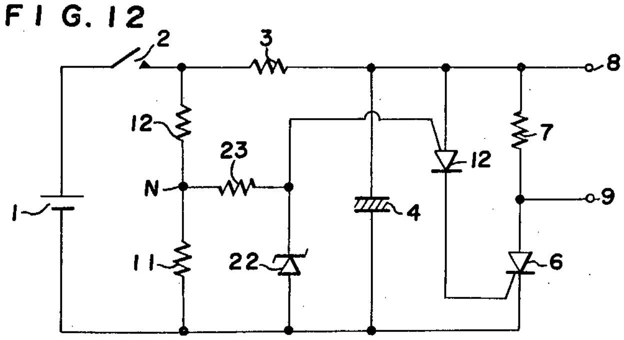

FIG. 13

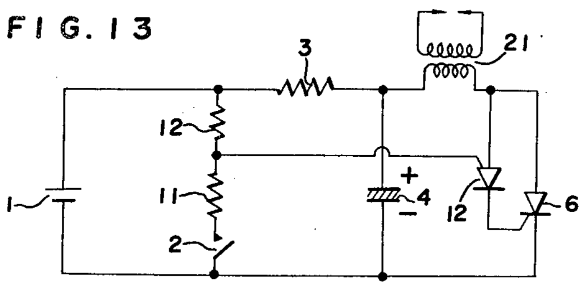

FIG. 14