**(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)**

**(19) World Intellectual Property Organization**
International Bureau

**(43) International Publication Date**
**10 May 2012 (10.05.2012)**

**PCT**

**(10) International Publication Number**
**WO 2012/061130 A2**

**(51) International Patent Classification**:
***H01L 21/328*** (2006.01) ***H01L 21/331*** (2006.01)
***H01L 21/265*** (2006.01) ***H01L 21/336*** (2006.01)

**(21) International Application Number**:
PCT/US2011/057679

**(22) International Filing Date**:
25 October 2011 (25.10.2011)

**(25) Filing Language**: English

**(26) Publication Language**: English

**(30) Priority Data**:
61/406,364 25 October 2010 (25.10.2010) US
13/246,362 27 September 2011 (27.09.2011) US

**(63) Related by continuation (CON) or continuation-in-part (CIP) to earlier applications**:
US 61/406,364 (CON)
Filed on 25 October 2010 (25.10.2010)
US 13/246,362 (CON)
Filed on 27 September 2011 (27.09.2011)

**(71) Applicant** *(for all designated States except US)*: **TEXAS INSTRUMENTS INCORPORATED** [US/US]; P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

**(71) Applicant** *(for JP only)*: **TEXAS INSTRUMENTS JAPAN LIMITED** [JP/JP]; 24-1, Nishi-shinjuku 6-chome, Shinjuku-ku, Tokyo, 160-8366 (JP).

**(72) Inventor; and**
**(75) Inventor/Applicant** *(for US only)*: **CHUANG, Ming-yeh** [US/US]; 8308 Beech Lane, Mckinney, TX 75070 (US).

**(74) Agents**: **FRANZ, Warren, L.** et al.; Texas Instruments Incorporated, P.O. Box 655474, Mail Station 3999, Dallas, TX 75265-5474 (US).

**(81) Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

**(84) Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

*[Continued on next page]*

**(54) Title**: LOW TEMPERATURE IMPLANT TO IMPROVE BJT CURRENT GAIN

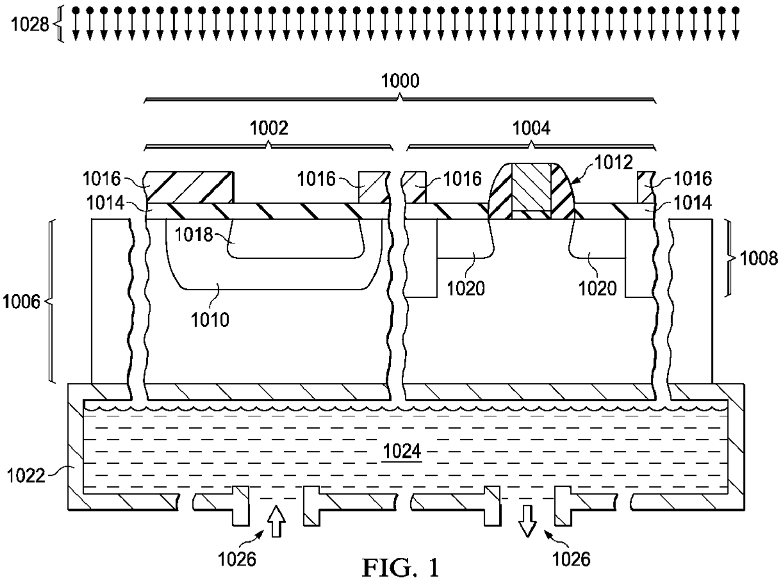


FIG. 1

**(57) Abstract**: A process of forming an integrated circuit containing a bipolar junction transistor (BJT) (1002) and a metal oxide semiconductor (MOS) (1004) transistor by cooling the integrated circuit substrate to 5 °C or colder and concurrently implanting dopants, at a specified minimum dose according to species, into the emitter region of the BJT and into the source and drain regions of the MOS transistor.

WO 2012/061130 A2

**Declarations under Rule 4.17**:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

**Published**:

— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

# LOW TEMPERATURE IMPLANT TO IMPROVE BJT CURRENT GAIN

**[0001]** This relates to the field of integrated circuits, and, more particularly, this invention relates to ion implanted layers in integrated circuits.

## BACKGROUND

**[0002]** An integrated circuit may contain an npn bipolar junction transistor (BJT) and an n-channel metal oxide semiconductor (NMOS) transistor, for example to provide analog functions and logic functions, respectively. Source and drain regions of the NMOS transistor and the emitter region of the npn BJT may be formed concurrently to reduce fabrication costs. Process steps for forming the source and drain regions and the emitter region may include ion implanting arsenic at a dose above $6\times10^{13}$ atoms/cm$^2$, for example to attain a desired resistance in the NMOS transistor. The ion implanted arsenic may form end-of-range defects, sometimes referred to as dislocation loops, at a density higher than $1\times10^7$ defects/cm$^2$, in the emitter region. The end-of-range defects may adversely affect performance of the npn bipolar junction transistor, for example by reducing current gain, also referred to as $h_{fe}$. Subsequent thermal anneals may not be sufficient to reduce the end-of-range defects to a desired level, because attaining desired levels of performance and yield in instances of the NMOS transistor may be achieved by limiting the total thermal profile of the integrated circuit after the arsenic ion implant step. Other devices in an integrated circuit which receives an ion implant at a dose which produces more than $1\times10^7$ end-of-range defects/cm$^2$, for example to provide electrically active dopants or to amorphize the substrate of the integrated circuit, may experience degradation of performance parameters due to the end-of-range defects.

## SUMMARY

**[0003]** An integrated circuit containing an npn bipolar junction transistor (BJT) and an NMOS transistor may be formed by cooling the substrate of the integrated circuit to 5 °C or colder and ion implanting arsenic concurrently into the emitter region of the npn BJT and the source and drain regions of the NMOS transistor through an implant screen dielectric layer, at a dose of at least $6\times10^{13}$ atoms/cm$^2$. An integrated circuit containing a pnp BJT and a p-channel metal oxide semiconductor (PMOS) transistor may be formed by cooling the substrate of the integrated circuit to 5 °C or colder and ion implanting gallium and/or indium concurrently into the emitter region of the pnp BJT and the source and drain regions of the PMOS transistor through an implant screen dielectric layer, at a dose of at least $6\times10^{13}$ atoms/cm$^2$. An integrated circuit containing an ion implanted region may be formed by cooling the substrate of the integrated circuit to 5 °C or colder and ion implanting a species into the implanted region through an implant screen dielectric layer, at a dose which would produce at least $1\times10^{7}$ end-of-range defects/cm$^2$ in a substrate cooled between 20 and 25 °C.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0004]** FIG. 1 depicts a process of forming an integrated circuit according to an example embodiment of implementation of principles of the invention.

**[0005]** FIG. 2 is a chart showing improvement of $h_{fe}$ in a bipolar junction transistor (BJT) as a function of substrate temperature.

**[0006]** FIG. 3 depicts a process of forming an integrated circuit according to a modifed embodiment.

## DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0007]** An integrated circuit may be formed by cooling a substrate of the integrated circuit to 5 °C or colder, and ion implanting a species through an implant screen dielectric layer into a region of the substrate at a dose which would produce at least at least $1\times10^{7}$ end-of-range defects/cm$^2$ in a substrate cooled between 20 and 25 °C.

**[0008]** In an embodiment, the ion implant step may include implanting boron at a dose of at least $1\times10^{16}$ atoms/cm$^2$. In another embodiment, the ion implant step may include implanting phosphorus at a dose of at least $8\times10^{14}$ atoms/cm$^2$. In a further embodiment, the ion implant step may include implanting gallium at a dose of at least $7\times10^{13}$ atoms/cm$^2$. In yet another embodiment, the ion implant step may include implanting germanium at a dose of at least $6\times10^{13}$ atoms/cm$^2$. In a further embodiment, the ion implant step may include implanting arsenic at a dose of at least $6\times10^{13}$

atoms/cm$^2$. In another embodiment, the ion implant step may include implanting indium at a dose of at least $6\times10^{13}$ atoms/cm$^2$. In a further embodiment, the ion implant step may include implanting antimony at a dose of at least $6\times10^{13}$ atoms/cm$^2$.

**[0009]** In a first embodiment, an integrated circuit containing an npn BJT and an NMOS transistor may be formed by cooling the substrate of the integrated circuit to 5 °C or colder and ion implanting phosphorus, arsenic and/or antimony, at the doses listed above, concurrently into the emitter region of the npn BJT and the source and drain regions of the NMOS transistor through an implant screen dielectric layer.

**[0010]** In a second embodiment, an integrated circuit containing a pnp BJT and a p-channel metal oxide semiconductor (PMOS) transistor may be formed by cooling the substrate of the integrated circuit to 5 °C or colder and ion implanting boron, gallium and/or indium, at the doses listed above, concurrently into the emitter region of the pnp BJT and the source and drain regions of the PMOS transistor through an implant screen dielectric layer.

**[0011]** In a third embodiment, an integrated circuit containing an implant region may be formed by cooling the substrate of the integrated circuit to 5 °C or colder and ion implanting boron, phosphorus, gallium, germanium, arsenic, indium and/or antimony, st the doses listed above, into the implant region through an implant screen dielectric layer.

**[0012]** FIG. 1 depicts a process of forming an integrated circuit according to either of the first or second embodiments. An integrated circuit 1000 includes a region defined for a BJT 1002 and a region defined for a metal oxide semiconductor (MOS) transistor 1004. In the first embodiment, the BJT 1002 is an npn BJT and the MOS transistor 1004 is an NMOS transistor. In the second embodiment, the BJT 1002 is a pnp BJT and the MOS transistor 1004 is a PMOS transistor. The integrated circuit 1000 is formed in and on a substrate 1006 which includes a silicon top region 1008. The substrate 1006 may be a single crystal silicon wafer, a silicon-on-insulator (SOI) wafer, a hybrid orientation technology (HOT) wafer with silicon regions of different crystal orientations, or other structure with a silicon top region 1008 appropriate for fabrication of the integrated circuit 1000.

**[0013]** The BJT 1002 includes a base diffused region 1010 in the silicon top region 1008. In the first embodiment, the base diffused region 1010 is p-type. In the second embodiment, the base diffused region 1010 is n-type. The MOS transistor 1004 includes a gate structure 1012, which contains a gate and a gate dielectric layer, and possibly gate sidewall spacers. Lightly doped drain (LDD) regions, not shown, may be formed at a top surface of the substrate 1006 adjacent to the gate. An implant screen dielectric layer 1014 is formed over the top surface of the substrate 1006. The implant screen dielectric layer 1014 is at least 5 nanometers thick. In one embodiment, the implant screen dielectric layer 1014 may be at least 15 nanometers thick. The implant screen dielectric layer 1014 may or may not extend to lateral edges of the substrate 1006. In one embodiment, the implant screen dielectric layer 1014 may include at least 80 percent silicon dioxide. The silicon dioxide may be formed by thermal oxidation of silicon at the top surface of the substrate 1006, may be deposited on the substrate 1006 for example by decomposition of tetraethyl orthosilicate, also known as tetraethoxysilane or TEOS, or may be formed by another process.

**[0014]** An implant mask 1016 is formed over the implant screen dielectric layer 1014 so as to expose an emitter region 1018 in the BJT 1002 and to expose source and drain regions 1020 in the MOS transistor 1004. The implant mask 1016 may be formed of photoresist or other photosensitive polymer using photolithographic processes, or may me formed of other dielectric material, for example by masking and etching processes.

**[0015]** A back surface of the substrate 1006 contacts a substrate chuck 1022. The substrate chuck 1022 is cooled to 5 °C or colder, for example by flowing a coolant fluid 1024 through the substrate chuck 1022, as indicated in FIG. 1 by coolant flow arrows 1026, until the substrate 1006 is cooled to 5 °C or colder. Other means of cooling the substrate chuck 1022 are within the scope of the instant embodiments.

**[0016]** While the substrate 1006 is cooled to 5 °C or colder, an ion implant process 1028 is performed which implants dopant species into the emitter region 1018 and the source and drain regions 1020. In the first embodiment, the ion implant process 1028 may implant phosphorus at a dose of at least $8\times10^{14}$ atoms/cm$^2$, and/or may implant arsenic at a dose of at least $6\times10^{13}$ atoms/cm$^2$, and/or may implant antimony at a dose of at least $6\times10^{13}$ atoms/cm$^2$. In one version of the first embodiment, the ion implant process 1028 may implant arsenic at a dose of at least $4\times10^{14}$ atoms/cm$^2$. In another version of the first embodiment, the ion implant process 1028 may implant arsenic at a dose of at least $1\times10^{15}$ atoms/cm$^2$. In the second embodiment, the ion implant process 1028 may implant boron at a dose of at least $1\times10^{16}$ atoms/cm$^2$ and/or may implant gallium at a dose of at least $7\times10^{13}$ atoms/cm$^2$ and/or may implant indium at a dose of at least $6\times10^{13}$ atoms/cm$^2$. In one version of the first and second embodiments, silicon substrate material in the silicon top region 1008 in into the emitter region 1018 and the source and drain regions 1020 may be amorphized at the top surface of the substrate 1006 to a depth of at least 15 nanometers. Forming the emitter region 1018 as described in reference to FIG. 1 may provide a BJT 1002 with an improved $h_{fe}$ compared to a similar BJT formed using an emitter implant process with a same dose and energy during which the substrate is cooled to 20 °C to 25 °C.

**[0017]** FIG. 2 shows improvement of $h_{fe}$ in an npn BJT as a function of substrate temperature, noted in FIG. 2 as “Implanter Chiller Temperature.” Average data points 2000 depict average values of $h_{fe}$ of a set of npn BJTs formed with emitter implants as described in reference to FIG. 1. Range bars 2002 depict limits of +/- 3 standard deviations of $h_{fe}$ values at each substrate temperature value. Trend line 2004 is provided as a guide to estimating $h_{fe}$ values by interpolation.

**[0018]** FIG. 3 depicts a process of forming an integrated circuit according to the third embodiment. An integrated circuit 3000 is formed in and on a substrate 3002 which includes a silicon top region 3004. The substrate 3002 and silicon top region 3004 have properties of the substrate 1006 and silicon top region 1008 as described in reference to FIG. 1. An implant screen dielectric layer 3006 is formed over a top surface of the substrate 3002. The implant screen dielectric layer 3006 has properties of the implant screen dielectric layer 1014 as described in reference to FIG. 1. An implant mask 3008 is formed over the implant screen dielectric layer 3006 so as to expose an implant region 3010 in the integrated circuit 3000. The implant mask 3008 has properties of the implant mask 1016 as described in reference to FIG. 1.

**[0019]** A back surface of the substrate 3002 contacts a substrate chuck 3012. The substrate chuck 3012 is cooled to 5 °C or colder, for example by flowing a coolant fluid 3014 through the substrate chuck 3012, as indicated in FIG. 3 by coolant flow arrows 3016, until the substrate 3002 is cooled to 5 °C or colder. Other means of cooling the substrate chuck 3012 are within the scope of the instant embodiments.

**[0020]** While the substrate 3002 is cooled to 5 °C or colder, an ion implant process 3018 is performed which implants one or more dopant and/or amorphizing atom species into the implant region 3010. In the instant (third) embodiment, the ion implant process 3018 may implant boron at a dose of at least $1\times10^{16}$ atoms/cm$^2$, and/or may implant phosphorus at a dose of at least $8\times10^{14}$ atoms/cm$^2$, and/or may implant gallium at a dose of at least $7\times10^{13}$ atoms/cm$^2$, and/or may implant germanium at a dose of at least $6\times10^{13}$ atoms/cm$^2$, and/or may implant arsenic at a dose of at least $6\times10^{13}$ atoms/cm$^2$, and/or may implant indium at a dose of at least $6\times10^{13}$ atoms/cm$^2$, and/or may implant antimony at a dose of at least $6\times10^{13}$ atoms/cm$^2$. In one version of the instant (third) embodiment, silicon substrate material in the silicon top region 3004 in the implant region 3010 may be amorphized at the top surface of the substrate 3002 to a depth of at least 15 nanometers. Forming the implant region 3010 as described in reference to FIG. 3 may result in less than $1\times10^{7}$ defects/cm$^2$, compared to a similar implant region formed using an implant process with a same dose and energy during which the substrate is cooled to 20 °C to 25 °C which results in greater than $1\times10^{7}$ defects/cm$^2$.

**[0021]** Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described example embodiments and other embodiments realized within the scope of the claimed invention.

What is claimed is:

1. A process of forming an integrated circuit containing an npn bipolar junction transistor (BJT) and an n-channel metal oxide semiconductor (NMOS) transistor, comprising:

forming a implant screen dielectric layer over a top surface of a silicon top region of a substrate of the integrated circuit, over an emitter region of the npn BJT and source and drain regions of the NMOS transistor;

forming an implant mask over the implant screen dielectric layer so as to expose the emitter region and the source and drain regions;

bringing the substrate of the integrated circuit in contact with a substrate chuck;

cooling the substrate chuck so that the substrate of the integrated circuit is cooled to a temperature of 5 °C or colder; and

while the substrate is cooled to 5 °C or cooler, ion implanting n-type dopants concurrently into the emitter region and the source and drain regions, in which the n-type dopants and a dose of the n-type dopants are selected from the group consisting of

phosphorus at a dose of at least $8\times10^{14}$ atoms/cm$^2$,
arsenic at a dose of at least $6\times10^{13}$ atoms/cm$^2$,
antimony at a dose of at least $6\times10^{13}$ atoms/cm$^2$, and
any combination thereof.

2. The process of claim 1, in which the n-type dopants include arsenic at a dose of at least $4\times10^{14}$ atoms/cm$^2$.

3. The process of claim 1, in which the n-type dopants include arsenic at a dose of at least $1\times10^{15}$ atoms/cm$^2$.

4. The process of claim 1, in which the implant screen dielectric layer includes at least 80 percent silicon dioxide.

5. The process of claim 1, in which the step of ion implanting the n-type dopants amorphizes silicon material at the top surface of the silicon top region in the emitter region and the source and drain regions to a depth of at least 15 nanometers.

6. A process of forming an integrated circuit containing a pnp BJT and a p-channel metal oxide semiconductor (PMOS) transistor, comprising:

forming a implant screen dielectric layer over a top surface of a silicon top region of a substrate of the integrated circuit, over an emitter region of the pnp BJT and source and drain regions of the PMOS transistor;

forming an implant mask over the implant screen dielectric layer so as to expose the emitter region and the source and drain regions;

bringing the substrate of the integrated circuit in contact with a substrate chuck;

cooling the substrate chuck so that the substrate of the integrated circuit is cooled to a temperature of 5 °C or colder; and

while the substrate is cooled to 5 °C or cooler, ion implanting p-type dopants concurrently into the emitter region and the source and drain regions, in which the p-type dopants and a dose of the p-type dopants are selected from the group consisting of boron at a dose of at least $1\times10^{16}$ atoms/cm$^2$, gallium at a dose of at least $7\times10^{13}$ atoms/cm$^2$, indium at a dose of at least $6\times10^{13}$ atoms/cm$^2$, and any combination thereof.

7. The process of claim 6, in which the implant screen dielectric layer includes at least 80 percent silicon dioxide.

8. The process of claim 6, in which the step of ion implanting the p-type dopants amorphizes silicon material at the top surface of the silicon top region in the emitter region and the source and drain regions to a depth of at least 15 nanometers.

9. A process of forming an integrated circuit containing an implant region, comprising:

forming a implant screen dielectric layer over a top surface of a silicon top region of a substrate of the integrated circuit, over the implant region;

forming an implant mask over the implant screen dielectric layer so as to expose the implant region;

bringing the substrate of the integrated circuit in contact with a substrate chuck;

cooling the substrate chuck so that the substrate of the integrated circuit is cooled to a temperature of 5 °C or colder; and

while the substrate is cooled to 5 °C or cooler, ion implanting atoms into the implant region, in which the atoms and a dose of the atoms are selected from the group consisting of

boron at a dose of at least $1\times10^{16}$ atoms/cm$^2$,

phosphorus at a dose of at least $8\times10^{14}$ atoms/cm$^2$,

gallium at a dose of at least $7\times10^{13}$ atoms/cm$^2$,

germanium at a dose of at least $6\times10^{13}$ atoms/cm$^2$,

arsenic at a dose of at least $6\times10^{13}$ atoms/cm$^2$,

indium at a dose of at least $6\times10^{13}$ atoms/cm$^2$,

antimony at a dose of at least $6\times10^{13}$ atoms/cm$^2$, and

any combination thereof.

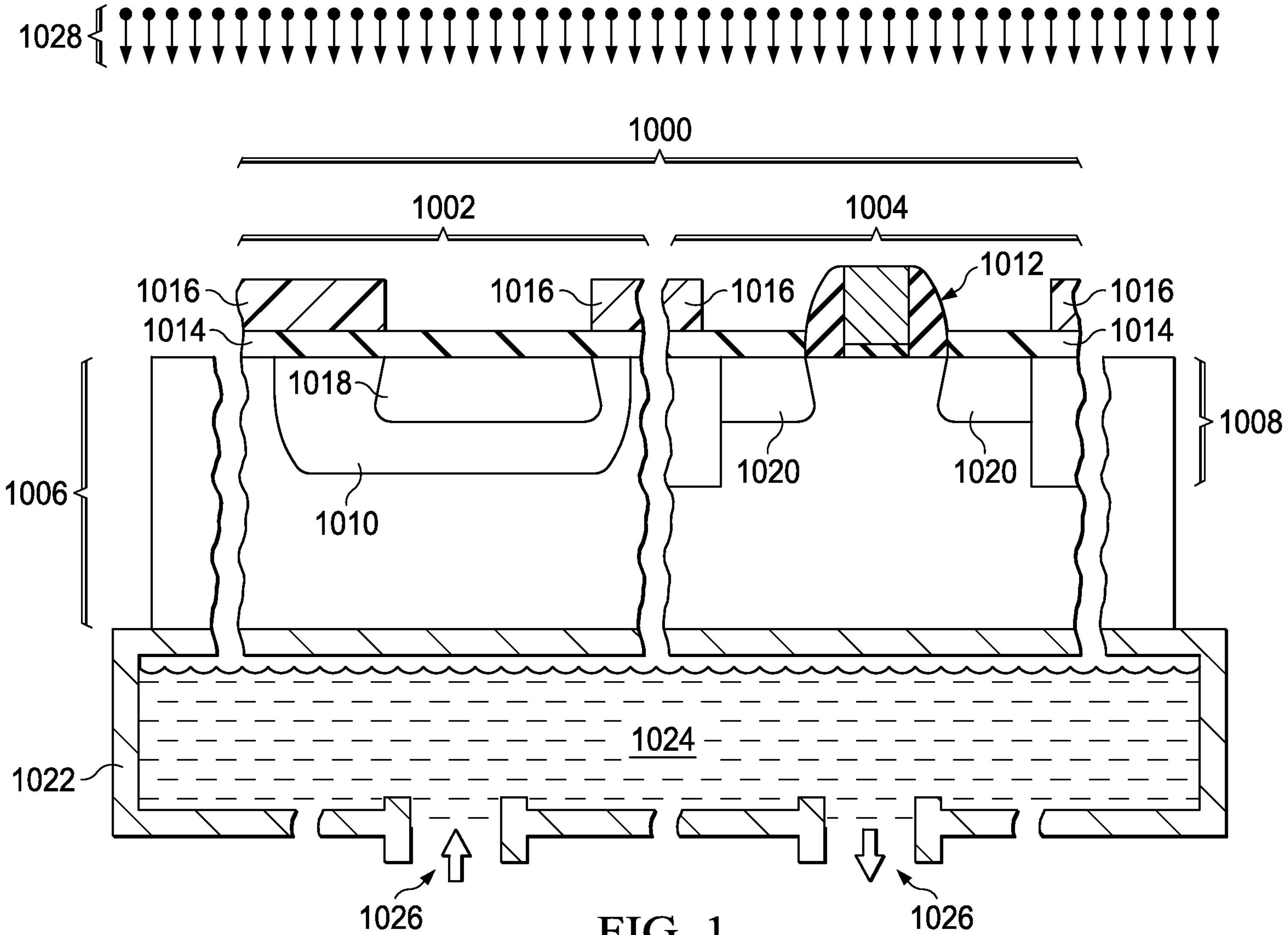
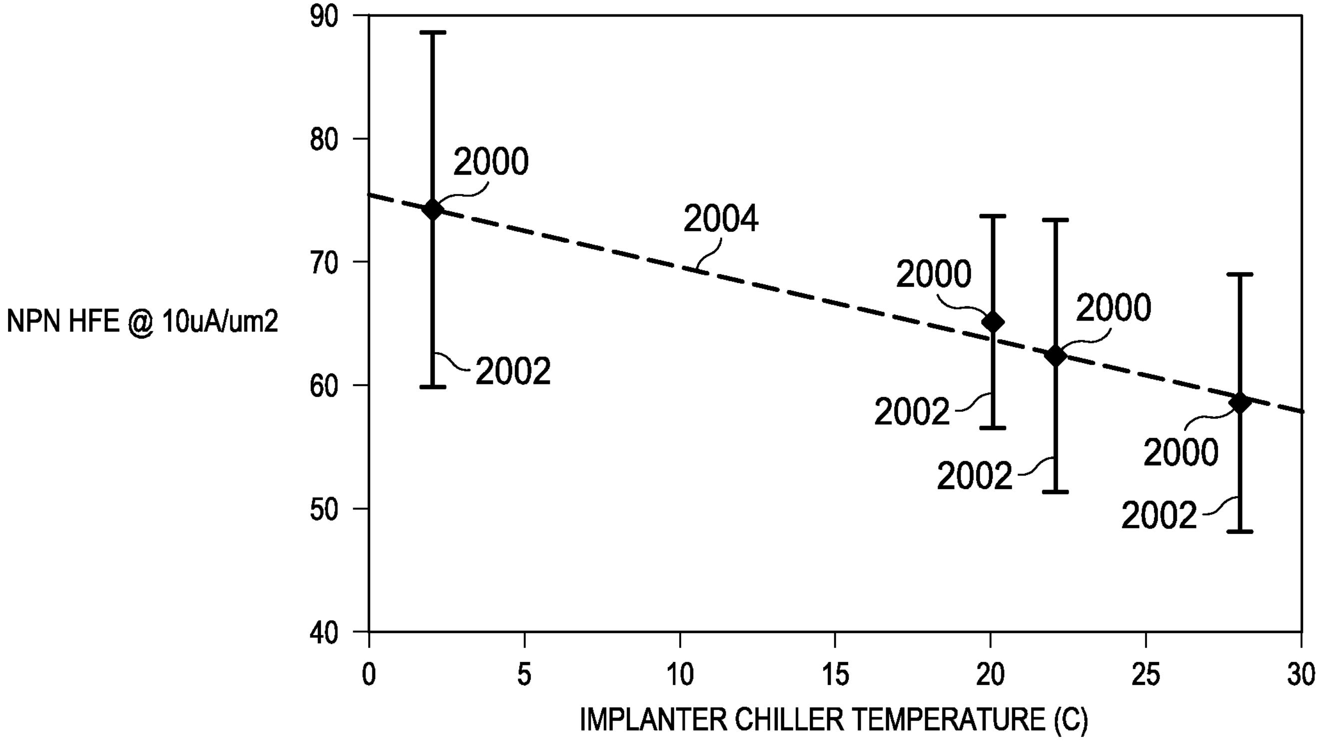

1028
1000
1002
1004
1016
1016
1016
1012
1016
1014
1014
1018
1006
1020
1020
1008
1010
1024
1022
1026
1026

FIG. 1

FIG. 2


NPN HFE @ 10uA/um2
90
80
70
60
50
40
0
5
10
15
20
25
30
IMPLANTER CHILLER TEMPERATURE (C)
2000
2002
2004
2000
2002
2000
2002
2000
2002

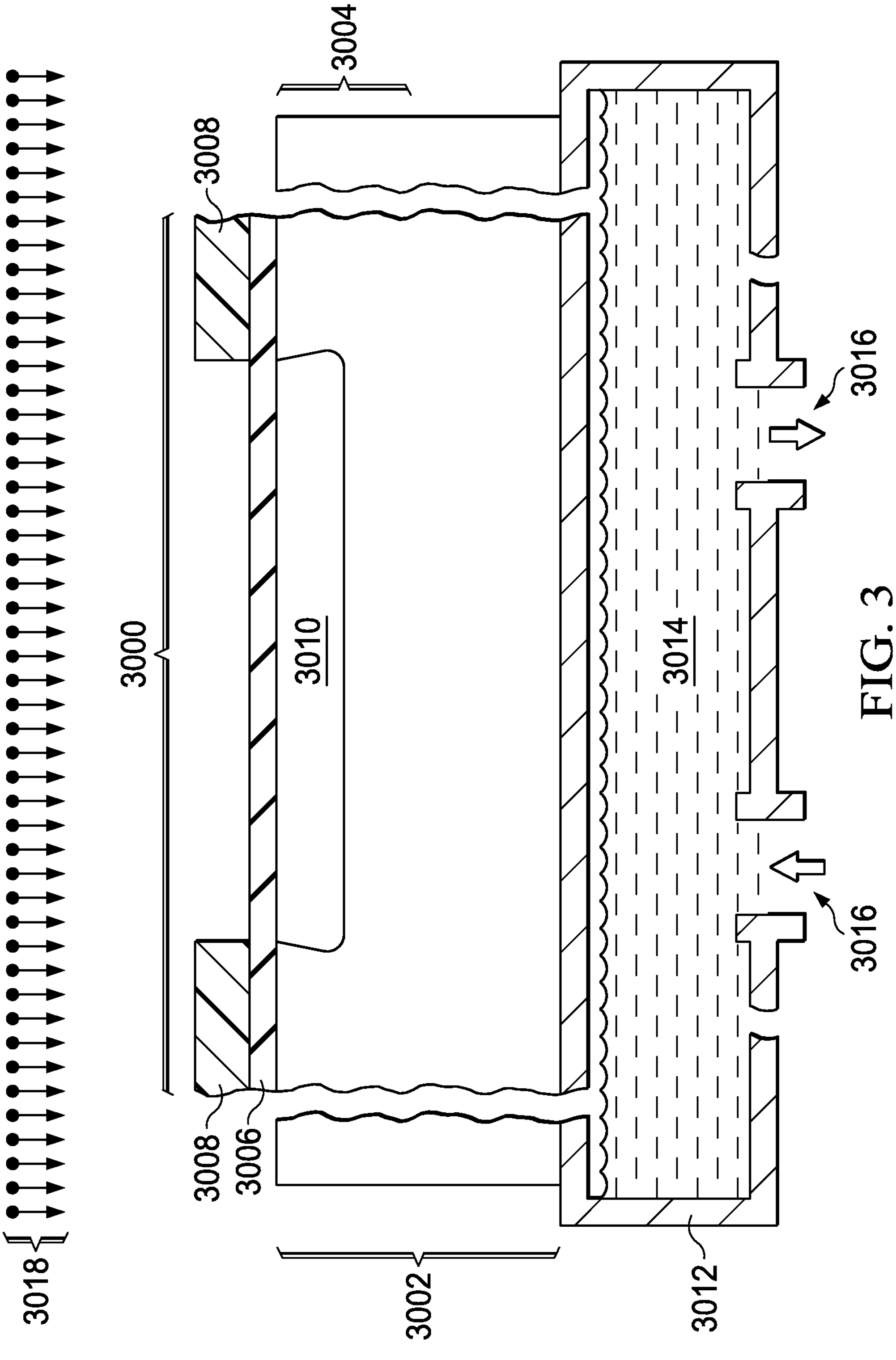


FIG. 3