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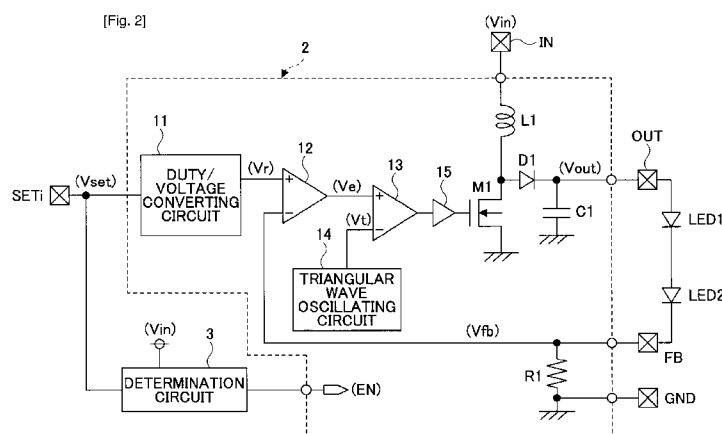
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(54) Title: SEMICONDUCTOR APPARATUS AND METHOD OF CONTROLLING OPERATION THEREOF



(57) Abstract: A semiconductor apparatus includes an input terminal to which an input voltage is applied; an output terminal at which an output voltage is obtained; a power supply circuit unit configured to generate the output voltage from the input voltage, the output voltage having a value corresponding to a duty cycle of a voltage setting signal that is externally applied to the semiconductor apparatus; and a determination circuit unit determining whether the voltage setting signal has a predetermined signal level for the duration of a first predetermined time or longer. The determination circuit unit activates the power supply circuit unit when the voltage setting signal does not have the predetermined signal level for the duration of the first predetermined time or longer. The power supply circuit unit is deactivated when the voltage setting signal has the predetermined signal level for the duration of the first predetermined time or longer.

Description

Title of Invention: SEMICONDUCTOR APPARATUS AND METHOD OF CONTROLLING OPERATION THEREOF

Technical Field

[0001] The present invention relates to semiconductor apparatuses having a power supply circuit whose output voltage is varied depending on the duty cycle of a voltage setting signal.

Background Art

[0002] In a semiconductor apparatus with a built-in power supply circuit for LEDs used as a backlight of an LCD panel of a cellular phone, for example, the size of IC packaging should be minimized in order to reduce the size of the apparatus. Thus, it is important to reduce the number of terminals used in an IC package. In one method, the number of such terminals may be reduced by assigning multiple functions to a single IC terminal.

[0003] For example, in a conventional semiconductor apparatus, a clock signal is supplied to a triangular wave oscillating circuit via a clock signal input terminal, which is an external terminal of the semiconductor apparatus, to generate a triangular wave voltage used for the PWM (pulse wave modulation) control of a switching regulator (see Japanese Laid-Open Patent Application No. 2006-101663, for example). The clock signal is also supplied to a clock pulse detection circuit. The clock pulse detection circuit generates a standby signal if the clock signal remains at a low level for a certain duration of time, thereby terminating the operation of the switching regulator. Thus, the clock signal input terminal doubles as a standby signal input terminal of the switching regulator. However, such a system cannot be utilized when the clock signal of the triangular wave oscillating circuit is generated within the semiconductor apparatus.

[0004] Thus, there is a need for a semiconductor apparatus including a power supply circuit, such as a switching regulator, having a reduced number of terminals, wherein a clock signal of a triangular wave oscillating circuit is generated within the semiconductor apparatus. There is also a need for a method of controlling an operation of such a semiconductor apparatus.

[0005] In one aspect of the present invention, a semiconductor apparatus includes an input terminal to which an input voltage is applied; an output terminal at which an output voltage is obtained; a power supply circuit unit configured to generate the output voltage from the input voltage, the output voltage having a value corresponding to a duty cycle of a voltage setting signal that is externally applied to the semiconductor apparatus; and a determination circuit unit configured to determine whether the voltage

setting signal has a predetermined signal level for the duration of a first predetermined time or longer. The determination circuit unit, when it determines that the voltage setting signal does not have the predetermined signal level for the duration of the first predetermined time or longer, activates the power supply circuit unit, and deactivates the power supply circuit unit when it determines that the voltage setting signal has the predetermined signal level for the duration of the first predetermined time or longer.

[0006] In another aspect of the present invention, a method of controlling an operation of a semiconductor apparatus includes generating an output voltage at an output terminal of the semiconductor apparatus from an input voltage applied to an input terminal of the semiconductor apparatus, the output voltage having a value corresponding to a duty cycle of a voltage setting signal externally applied to the semiconductor apparatus; determining whether the voltage setting signal has a predetermined signal level for the duration of a first predetermined time or longer; supplying the output voltage to the output terminal of the semiconductor apparatus when the determining step determines that the voltage setting signal does not have the predetermined signal level for the duration of the first predetermined time or longer; and not supplying the output voltage to the output terminal when the determining step determines that the voltage setting signal has the predetermined signal level for the duration of the first predetermined time or longer.

Brief Description of Drawings

[0007] Other objects, features and advantages of the present invention will become apparent upon consideration of the specification and the appendant drawings, in which:

[fig.1]FIG. 1 is a block diagram of a semiconductor apparatus according to a first embodiment of the present invention;

[fig.2]FIG. 2 is a diagram of an example of a power supply circuit in the semiconductor apparatus of FIG. 1;

[fig.3]FIG. 3 is a diagram of an internal circuit structure of a duty/voltage converting circuit in the power supply circuit of FIG. 2;

[fig.4]FIG. 4 is a timing chart of an operation of the duty/voltage converting circuit of FIG. 3;

[fig.5]FIG. 5 is a diagram of an example of a determination circuit in the semiconductor apparatus of FIG. 1;

[fig.6]FIG. 6 is a timing chart of an operation of the determination circuit of FIG. 5; and

[fig.7]FIG. 7 is a diagram of another example of the determination circuit in the semiconductor apparatus of FIG. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

- [0008] Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, embodiments of the present invention are described. FIG. 1 is a block diagram of a semiconductor apparatus 1 according to a first embodiment of the present invention. The semiconductor apparatus 1 includes a power supply circuit 2, a determination circuit 3, and various terminals. The terminals include a power supply input terminal IN, a voltage setting signal (clock) input terminal SETi, an output terminal OUT, and a ground terminal GND. The power supply input terminal IN receives an input voltage V_{in} . The voltage setting signal input terminal SETi receives a voltage setting signal V_{set} , which is a clock signal. Ground GND is connected to ground potential.
- [0009] The power supply circuit 2 produces an output voltage V_{out} in accordance with the duty cycle of the voltage setting signal V_{set} , and outputs the output voltage V_{out} via the output terminal OUT. The determination circuit 3 determines whether a period of the voltage setting signal V_{set} at a low level or a high level exceeds a first predetermined time. If the determination circuit 3 determines that the period is less than the first predetermined time, it outputs a high-level enable signal EN, thereby activating the power supply circuit 2. If it determines that the period of the voltage setting signal V_{set} at either the low level or the high level is equal to or more than the first predetermined time, the determination circuit 3 outputs a low-level enable signal EN, which functions as a disable signal, thereby terminating the operation of the power supply circuit 2.
- [0010] FIG. 2 is a circuit diagram of an example of the power supply circuit 2. In this example, the power supply circuit 2 supplies power to LEDs 1 and 2, where the semiconductor apparatus 1 of FIG. 1 includes a feedback terminal FB. The power supply circuit 2 forms a step-up switching regulator of the asynchronous rectification type configured to step up the input voltage V_{in} applied to the power supply input terminal IN to a predetermined voltage that is obtained at the output terminal OUT as the output voltage V_{out} . The power supply circuit 2 includes a duty/voltage converting circuit 11; an error amplifying circuit 12; a PWM comparator 13; a triangular wave oscillating circuit 14 for generating a predetermined triangular wave voltage V_t ; a buffer circuit 15; a switching transistor M1; an inductor L1; a diode D1 as a rectifier element; an output capacitor C1; and a resistor R1. The error amplifying circuit 12, the PWM comparator 13, the triangular wave oscillating circuit 14, the buffer circuit 15, and the resistor R1 form a control circuit unit.
- [0011] The input end of the duty/voltage converting circuit 11 is connected to the voltage setting signal input terminal SETi. The output end of the duty/voltage converting circuit 11 is connected to a non-inverting input end of the error amplifying circuit 12. An inverting input end of the error amplifying circuit 12 is connected to the feedback

terminal FB so that a feedback voltage V_{fb} is applied to the inverting input end of the error amplifying circuit 12. The resistor R1 is connected between the feedback terminal FB and ground GND. The output end of the error amplifying circuit 12 is connected to a non-inverting input end of the PWM comparator 13. An inverting input end of the PWM comparator 13 receives the triangular wave voltage V_t from the triangular wave oscillating circuit 14. The output end of the PWM comparator 13 is connected to the gate of the switching transistor M1 via the buffer circuit 15.

[0012] The source of the switching transistor M1 is connected to ground GND. The inductor L1 is connected between the input voltage V_{in} and the drain of the switching transistor M1. The anode of the diode D1 is connected to the drain of the switching transistor M1. The cathode of the diode D1 is connected to the output terminal OUT. Between the output terminal OUT and ground GND, the output capacitor C1 is connected. Between the output terminal OUT and the feedback terminal FB, the LEDs 1 and 2 are connected in series.

[0013] The duty/voltage converting circuit 11 converts the duty cycle of the input voltage setting signal V_{set} into a voltage and outputs it as a reference voltage V_r . FIG. 3 illustrates an example of the internal circuit structure of the duty/voltage converting circuit 11. The example includes an inverter circuit 16, resistors R2 and R3, and capacitors C2 and C3. The input end of the inverter circuit 16 receives a voltage setting signal V_{set} . The output end of the inverter circuit 16 is connected to one end of the resistor R2. The other end of the resistor R2 is connected to one end of the capacitor C2 and one end of the resistor R3. The other end of the capacitor C2 is connected to ground GND. The capacitor C3 is connected between the other end of the resistor R3 and ground GND. The connecting portion of the resistor R3 and the capacitor C3 is continuous with the output end of the duty/voltage converting circuit 11, at which the reference voltage V_r is obtained.

[0014] The combination of the resistor R2 and the capacitor C2 and the combination of the resistor R3 and the capacitor C3 each form a low-pass filter. Thus, the output signal of the inverter circuit 16 is fed to the two stages of low-pass filters connected in series to generate the reference voltage V_r at the output.

[0015] FIG. 4 is a timing chart illustrating an operation of the duty/voltage converting circuit 11 depicted in FIG. 3. "VA" in FIG. 4 indicates a voltage waveform at a connecting portion A of the resistor R2, the capacitor C2, and the resistor R3 of FIG. 3. The connecting portion A is an output end of the first-stage low-pass filter. As seen from FIG. 4, the reference voltage V_r increases as the time durations in which the voltage setting signal V_{set} is at the high level increase, as indicated by periods P1 through P8 of V_{set} . In period P8, the duty cycle of the high level becomes 100% and the reference voltage V_r has a maximum value. In period P10, the duty cycle of the voltage setting

signal V_{set} at the high level becomes less than 100% and the reference voltage V_r decreases. The circuit depicted in FIG. 3 is merely an example; the duty/voltage converting circuit 11 may be provided by any circuit capable of converting the duty cycle of the voltage setting signal V_{set} as a clock signal into a voltage.

- [0016] Referring back to FIG. 2, the reference voltage V_r from the duty/voltage converting circuit 11 is applied to the non-inverting input end of the error amplifying circuit 12, to the inverting input end of which the feedback voltage V_{fb} is applied. The feedback voltage V_{fb} is obtained by converting a current supplied to the LEDs 1 and 2, which are connected across external terminals of the semiconductor apparatus 1, into a voltage using the resistor R_1 . The error amplifying circuit 12 amplifies a differential voltage between the reference voltage V_r and the feedback voltage V_{fb} to produce an error voltage V_e , which is applied to the non-inverting input end of the PWM comparator 13.
- [0017] The inverting input end of the PWM comparator 13 receives the triangular wave voltage V_t from the triangular wave oscillating circuit 14. The PWM comparator 13 outputs a high level signal in a period in which the triangular wave voltage V_t is lower than the error voltage V_e . The high-level signal is applied via the buffer circuit 15 to the gate of the switching transistor M_1 , thereby turning on the switching transistor M_1 . In response, a current flows from the power supply input terminal IN via the inductor L_1 and the switching transistor M_1 to ground GND , whereby energy is stored in the inductor L_1 .
- [0018] When the triangular wave voltage V_t is equal to or higher than the error voltage V_e , the PWM comparator 13 outputs a low level signal, so that the switching transistor M_1 turns off. As a result, the current supply to the inductor L_1 is blocked, and a back electromotive force is produced in the inductor L_1 . Consequently, the voltage at the connecting portion between the inductor L_1 and the drain of the switching transistor M_1 becomes higher than the input voltage V_{in} . The output capacitor C_1 is charged by the higher voltage at the connecting portion via the diode D_1 , and the output voltage V_{out} is stepped up to a voltage higher than the input voltage V_{in} .
- [0019] Thus, because the power supply circuit 2 controls the output voltage V_{out} such that the feedback voltage V_{fb} is substantially equal to the reference voltage V_r , the current supplied to the LEDs 1 and 2 can be changed by varying the reference voltage V_r . Thus, the illuminance of the LEDs 1 and 2 can be adjusted by the reference voltage V_r . Although not shown in FIG. 2, the enable signal EN is applied to the error amplifying circuit 12, the triangular wave oscillating circuit 14, and the PWM comparator 13. Thus, when the enable signal EN assumes the low level, the error amplifying circuit 12, the triangular wave oscillating circuit 14, and the PWM comparator 13 cease operation, whereby the power supply circuit 2 is disabled and its current output to the

output terminal OUT is terminated.

- [0020] FIG. 5 illustrates an example of the determination circuit 3. In this example, the determination circuit 3 includes PMOS transistors M21 and M23 through M25; a depletion-type NMOS transistor M22; inverter circuits 21 through 24; resistors R21 and R22; and capacitors C21 and C22. The capacitor C21 may be referred to as a first capacitor. The PMOS transistor M21, the depletion-type NMOS transistor M22, and the resistor R21 form a first charge/discharge circuit. The capacitor C22 may be referred to as a second capacitor. The PMOS transistor M23, the resistor R22, and the inverter circuit 21 form a second charge/discharge circuit. The inverters 22 through 24 form a binarizing circuit. The PMOS transistors M24 and M25 form a retaining circuit.
- [0021] The source of the PMOS transistor M21 is connected to the input voltage V_{in} . The depletion-type NMOS transistor M22 is connected between the drain of the PMOS transistor M21 and ground GND. The gate of the PMOS transistor M21 is connected to the gate of the depletion-type NMOS transistor M22, and the connecting portion of the gates is connected to ground GND. The resistor R21 is connected between the drain of the PMOS transistor M21 and the gate of the PMOS transistor M23. The capacitor C21 is connected between the gate of the PMOS transistor M23 and ground GND.
- [0022] The PMOS transistor M23 and the resistor R22 are connected in parallel between the input voltage V_{in} and a positive power supply input end of the inverter circuit 21. The input end of the inverter circuit 21 receives the voltage setting signal V_{set} . The capacitor C22 is connected between the output end of the inverter circuit 21 and ground GND. The output end of the inverter circuit 21 is connected to the input end of the inverter circuit 22. Between the input voltage V_{in} and the input end of the inverter circuit 22, the PMOS transistors M24 and M25 are connected in series. The gate of the PMOS transistor M24 receives the voltage setting signal V_{set} . The gate of the PMOS transistor M25 is connected to the output end of the inverter circuit 22. The output end of the inverter circuit 22 is connected to the input end of the inverter circuit 23. The output end of the inverter circuit 23 is connected to the input end of the inverter circuit 24. The output end of the inverter circuit 24 constitutes the output end of the determination circuit 3, where the enable signal EN is obtained.
- [0023] FIG. 6 is a timing chart of an operation of the determination circuit 3. "VB" in FIG. 6 indicates a voltage at a connecting portion B where the gate of the PMOS transistor M23, the resistor R21, and the capacitor C21 are connected, as depicted in FIG. 5. "VC" indicates a voltage at a connecting portion C where the output end of the inverter circuit 21, the input end of the inverter circuit 22, the PMOS transistor M25, and the capacitor C22 are connected, as depicted in FIG. 5.
- [0024] Referring to the timing chart of FIG. 6, the input voltage V_{in} is applied to the power supply input terminal IN at time t_0 , whereby the PMOS transistor M21, whose gate is

grounded, immediately turns on. Then, current flows via the PMOS transistor M21 to the depletion-type NMOS transistor M22, which is zero-biased, and the resistor R21. The current supplied to the resistor R21 charges the capacitor C21, so that the voltage VB at the connecting portion B gradually increases. Because the PMOS transistor M23 is on until the voltage VB reaches a threshold voltage V1 of the PMOS transistor M23, the input voltage Vin is applied to the inverter circuit 21 as a power supply voltage, via the PMOS transistor M23.

[0025] The voltage setting signal Vset remains at the low level for a while following the input of the input voltage Vin, as depicted in FIG. 6. Thus, the inverter circuit 21 outputs a high-level signal, and the capacitor C22 is charged by this high-level output voltage. At this time, the PMOS transistor M23 that supplies power to the inverter circuit 21 is on, so that the capacitor C22 is charged quickly, and the voltage VC at the connecting portion C increases, substantially equaling the input voltage Vin.

[0026] Because the input voltage to the inverter circuit 22 is the voltage VC at the connecting portion C, a high level signal is applied to the input end of the inverter circuit 22. Thus, the inverter circuit 22 outputs a low level signal, which is applied to the gate of the PMOS transistor M25. As a result, the PMOS transistor M25 turns on. Because the gate of the PMOS transistor M24 is supplied with the voltage setting signal Vset, the PMOS transistor M24 is also on. Thus, the connecting portion C is connected to the input voltage Vin via the PMOS transistors M24 and M25. As a result, the connecting portion C has the high level simultaneously with the input of the input voltage Vin due to the output signal of the inverter circuit 21 and the PMOS transistors M24 and M25.

[0027] The inverter circuit 22 outputs a low level signal as mentioned above, so that the inverter circuit 23 outputs a high level signal and the inverter circuit 24 outputs a low level signal. Thus, the enable signal EN as the output signal of the determination circuit 3 is at the low level. The low-level enable signal EN acts as a disable signal and as such disables the power supply circuit 2. In other words, immediately after the input of the input voltage Vin, the determination circuit 3 outputs a disable signal and the power supply circuit 2 does not operate. Then, at time t1, the voltage VB at the connecting portion B exceeds the threshold voltage V1 of the PMOS transistor M23 to turn off the PMOS transistor M23. Consequently, only the resistor R22 is connected between the power supply input end of the inverter circuit 21 and the power supply input terminal IN.

[0028] At time t2, the voltage setting signal Vset assumes the high level and the PMOS transistor M24 turns off, thereby terminating the connection between the connecting portion C and the input voltage Vin. Further, the inverter circuit 21 outputs a low level signal via the output end of the inverter circuit 21, so that the capacitor C22 is quickly

discharged, resulting in the connecting portion C having the low level. The low level signal is output via the inverter circuits 22 through 24, and therefore the enable signal EN as the output signal of the determination circuit 3 assumes the high level. As a result, the power supply circuit 2 starts operating. In this case, the PMOS transistor M25 is turned off because the inverter circuit 22 outputs a high level signal.

[0029] At time t_3 , the voltage setting signal Vset returns to the low level, and the output signal of the inverter circuit 21 tends to reach the high level. However, the rate of increase of the voltage VC is extremely low because the PMOS transistor M23 is off and the capacitor C22 is charged through the resistor R22. At this time, although the PMOS transistor M24 turns on, the output signal of the inverter circuit 22 remains at the high level. Thus, the PMOS transistor M25 is off so that it does not provide connection between the input voltage Vin and the connecting portion C. As a result, the voltage VC does not reach the input threshold voltage V2 of the inverter circuit 22 before the voltage setting signal Vset next assumes the high level, and therefore the enable signal EN remains at the high level. Thereafter, the high-level enable signal EN is continuously output as long as the voltage setting signal Vset repeats between the high and low levels or remains at the high level.

[0030] Next, at time t_4 , as the voltage setting signal Vset assumes the low level and remains at the low level, the voltage VC begins to increase. At time t_5 , the voltage VC exceeds the input threshold voltage V2 of the inverter circuit 22, and the output signal of the inverter circuit 22 is inverted to the low level. Then, the enable signal EN returns to the low level and becomes a disable signal, terminating the operation of the power supply circuit 2. Further, the PMOS transistor M25 turns on. The PMOS transistor M24 had already turned on when the voltage setting signal Vset assumed the low level. Thus, both the PMOS transistors M24 and M25 are on to connect the connecting portion C to the input voltage Vin and the voltage VC immediately rises to the input voltage Vin.

[0031] The status after time t_5 is the same as that between time t_1 and time t_2 . Namely, when the voltage setting signal Vset assumes the high level again, the same operation as described above with reference to time t_2 is performed, whereby the enable signal EN is output and the power supply circuit 2 is activated. The depletion-type NMOS transistor M22 functions to quickly discharge the capacitor C21 through the resistor R21 upon termination of application of the input voltage Vin.

[0032] In the foregoing description, the output voltage Vout is varied depending on the duty cycle of the high level of the voltage setting signal Vset. Alternatively, the output voltage Vout may be varied depending on the duty cycle of the low level of the voltage setting signal Vset. In this case, the operation of the power supply circuit 2 may be terminated by the enable signal EN that is output when the voltage setting signal Vset has the high level for a predetermined time.

- [0033] It has also been described with reference to FIG. 5 that the capacitor C21 is charged when it is connected via the PMOS transistor M21 and the resistor R21 to the input voltage V_{in} . Alternatively, the capacitor C21 may be charged only through the PMOS transistor M21, as depicted in FIG. 7. In FIG. 7, similar elements to those of FIG. 5 are designated with similar reference numerals or signs and their description is omitted. The circuit structure of FIG. 7 differs from that of FIG. 5 in that the PMOS transistor M21 is connected between the input voltage V_{in} and the connecting portion B, and the gate of the PMOS transistor M21 is supplied with the output signal of the inverter circuit 23, i.e., a signal ENB which is the enable signal EN with an inverted signal level.
- [0034] Referring to FIG. 7, when the input voltage V_{in} is not applied to the power supply input terminal IN, the capacitor C21 is discharged and the connecting portion B is at the low level. Upon application of the input voltage V_{in} , the PMOS transistor M23 immediately turns on, and the output signal of the inverter circuit 21 immediately rises to the high level because the voltage setting signal V_{set} is at the low level upon application of the input voltage V_{in} , as in the case of FIG. 5. Then, the signal ENB has the high level and the enable signal EN has the low level, whereby the operation of the power supply circuit 2 is terminated.
- [0035] When the voltage setting signal V_{set} has the high level, the capacitor C22 is quickly discharged, so that the voltage V_C at the connecting portion C quickly decreases to the low level. As a result, the signal ENB has the low level and the PMOS transistor M21 turns on. The capacitor C21 is then quickly charged and the connecting portion B has the high level, so that the PMOS transistor M23 turns off. Because the enable signal EN has the high level, the power supply circuit 2 starts operating.
- [0036] When the voltage setting signal V_{set} has the low level, because the PMOS transistor M23 is off, the inverter circuit 21 is supplied with power via the resistor R22, and the charge time of the capacitor C22 is extended. Unless the connecting portion C has the high level within the period in which the voltage setting signal V_{set} has the low level, the signal ENB maintains the low level and the enable signal EN maintains the high level, so that the power supply circuit 2 keeps operating.
- [0037] In the circuit of FIG. 7, when the enable signal EN is at the low level and the operation of the power supply circuit 2 is stopped, the signal ENB has the high level and the PMOS transistor M21 is turned off. Thus, the current that keeps flowing through the PMOS transistor M21 and the depletion-type NMOS transistor M22 in the case of FIG. 5 can be terminated in the circuit of FIG. 7. Thus, current consumption during a standby period can be reduced.
- [0038] Thus, in accordance with the first embodiment of the present invention, the determination circuit 3 of the semiconductor apparatus determines whether the voltage

setting signal V_{set} is applied. If it determines the presence of the voltage setting signal V_{set} , the determination circuit 3 outputs a high-level enable signal EN to activate the power supply circuit 2. On the other hand, if it determines that the voltage setting signal V_{set} is not present, the determination circuit 3 outputs a low-level enable signal EN to disable the operation of the power supply circuit 2. In this way, the need for providing a separate external terminal to the semiconductor apparatus for the input of the enable signal can be eliminated, thus reducing the number of terminals of the semiconductor apparatus.

[0039] The determination circuit 3 outputs a disable signal to the power supply circuit 2 in a second predetermined time between time t_0 immediately after the input of the input voltage V_{in} and time t_1 . Therefore, activation of the power supply circuit 2 before the output of the voltage setting signal V_{set} can be prevented, thereby preventing the output of an erroneous output voltage V_{out} . Furthermore, up to 100% of the duty cycle of the voltage setting signal V_{set} can be utilized.

[0040] In the foregoing description of the first embodiment, the power supply circuit 2 has been described as being a step-up switching regulator of the asynchronous rectification type. However, this is merely an example; alternatively, the power supply circuit 2 may be a step-up switching regulator of the synchronous rectification type. In this case, the diode D_1 may be replaced with a PMOS transistor for synchronous rectification, and the gate of the synchronous rectification transistor may be supplied with a gate signal of the switching transistor M_1 having an inverted signal level, so that the synchronous rectification transistor performs an opposite switching operation to the switching transistor M_1 .

[0041] In an embodiment, the power supply circuit 2 may be a step-down switching regulator or an inverting switching regulator, rather than a step-up switching regulator as in the first embodiment. In another embodiment, the power supply circuit 2 may include a linear regulator, such as a series regulator. In this case, the power supply circuit 2 may include an output transistor for controlling the output voltage V_{out} by performing an operation in accordance with a control signal applied to a control electrode, wherein the error amplifying circuit 12 is configured to amplify a voltage difference between the reference voltage V_r from the duty/voltage converting circuit 11 and the feedback voltage V_{fb} that is in proportion to the output voltage V_{out} . Based on the error voltage V_e produced by the error amplifying circuit 12, the current output of the output transistor may be controlled so that the output voltage V_{out} remains at a predetermined voltage.

[0042] Although this invention has been described in detail with reference to certain embodiments, variations and modifications exist within the scope and spirit of the invention as described and defined in the following claims.

[0043] The present application is based on the Japanese Priority Application No. 2009-064448 filed March 17, 2009, the entire contents of which are hereby incorporated by reference.

Claims

- [Claim 1] A semiconductor apparatus comprising:
an input terminal to which an input voltage is applied;
an output terminal at which an output voltage is obtained;
a power supply circuit unit configured to generate the output voltage from the input voltage, the output voltage having a value corresponding to a duty cycle of a voltage setting signal that is externally applied to the semiconductor apparatus; and
a determination circuit unit configured to determine whether the voltage setting signal has a predetermined signal level for the duration of a first predetermined time or longer,
wherein the determination circuit unit, when it determines that the voltage setting signal does not have the predetermined signal level for the duration of the first predetermined time or longer, activates the power supply circuit unit, and deactivates the power supply circuit unit when it determines that the voltage setting signal has the predetermined signal level for the duration of the first predetermined time or longer.
- [Claim 2] The semiconductor apparatus according to claim 1, wherein the determination circuit unit deactivates the power supply circuit unit during a second predetermined time following the start of application of the input voltage to the input terminal.
- [Claim 3] The semiconductor apparatus according to claim 1 or 2, wherein the power supply circuit unit includes:
an output transistor configured to control the output voltage in accordance with a control signal applied to a control electrode of the output transistor;
a duty/voltage converting circuit unit configured to generate a reference voltage by converting the duty cycle of the voltage setting signal into a voltage; and
a control circuit unit configured to control the output transistor so that a feedback voltage which is proportional to the output voltage at the output terminal becomes equal to the reference voltage.
- [Claim 4] The semiconductor apparatus according to claim 3, wherein the output transistor performs a switching operation in accordance with the control signal applied to the control electrode,
wherein the power supply circuit unit includes an inductor that is charged with the input voltage by the switching operation of the output

transistor, and a rectifier element configured to discharge the inductor when the output transistor is turned off,

wherein the control circuit unit includes a switching regulator configured to control the switching operation of the output transistor so that the feedback voltage becomes equal to the reference voltage.

[Claim 5] The semiconductor apparatus according to claim 3, wherein the duty/voltage converting circuit unit includes a low-pass filter to which the voltage setting signal is applied.

[Claim 6] The semiconductor apparatus according to claim 1 or 2, wherein the output voltage is applied to a light-emitting diode via the output terminal.

[Claim 7] The semiconductor apparatus according to claim 6, wherein the power supply circuit unit is configured to adjust the illuminance of the light-emitting diode depending on the duty cycle of the voltage setting signal.

[Claim 8] The semiconductor apparatus according to claim 1 or 2, wherein the determination circuit unit includes:

a first capacitor;

a first charge/discharge circuit configured to charge the first capacitor with the input voltage applied to the input terminal, and configured to discharge the first capacitor when the input voltage is not applied to the input terminal;

a second capacitor;

a second charge/discharge circuit configured to charge or discharge the second capacitor in accordance with a signal level of the voltage setting signal, and configured to change the rate of charging of the second capacitor depending on a terminal voltage of the first capacitor;

a binarizing circuit configured to generate a signal for controlling the activation of the power supply circuit unit by binarizing a terminal voltage of the second capacitor; and

a retaining circuit configured to retain a signal level of an output signal of the binarizing circuit upon inversion of the signal level of the output signal of the binarizing circuit as a result of the discharge of the second capacitor, the retaining circuit retaining the signal level of the output signal of the binarizing circuit by charging the second capacitor with the input voltage in accordance with the signal level of the voltage setting signal,

wherein the second charge/discharge circuit is configured to decrease

the rate of charging of the second capacitor when the terminal voltage of the first capacitor exceeds a predetermined value.

[Claim 9]

A method of controlling an operation of a semiconductor apparatus, the method comprising:

generating an output voltage at an output terminal of the semiconductor apparatus from an input voltage applied to an input terminal of the semiconductor apparatus, the output voltage having a value corresponding to a duty cycle of a voltage setting signal externally applied to the semiconductor apparatus;

determining whether the voltage setting signal has a predetermined signal level for the duration of a first predetermined time or longer;

supplying the output voltage to the output terminal of the semiconductor apparatus when the determining step determines that the voltage setting signal does not have the predetermined signal level for the duration of the first predetermined time or longer; and

not supplying the output voltage to the output terminal when the determining step determines that the voltage setting signal has the predetermined signal level for the duration of the first predetermined time or longer.

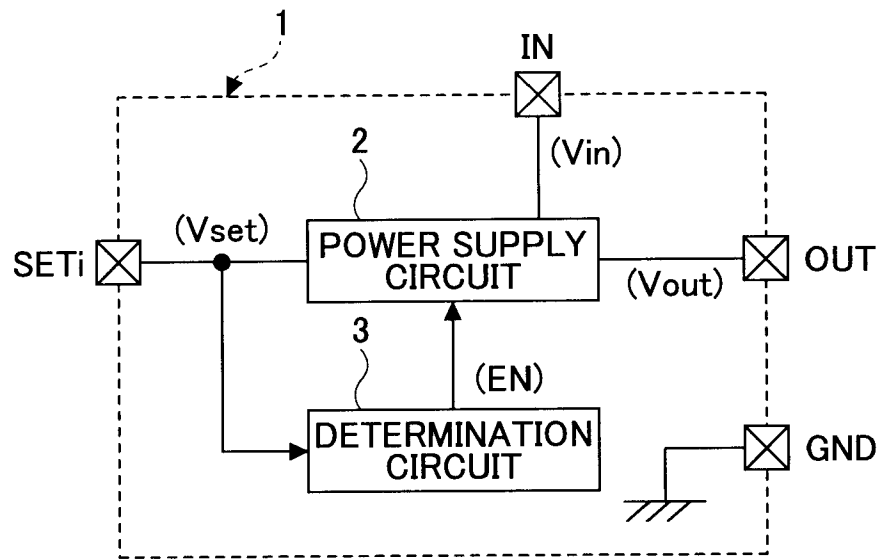
[Claim 10]

The method of controlling an operation of a semiconductor apparatus according to claim 9, further comprising not supplying the output voltage to the output terminal during a second predetermined time following the start of application of the input voltage to the input terminal.

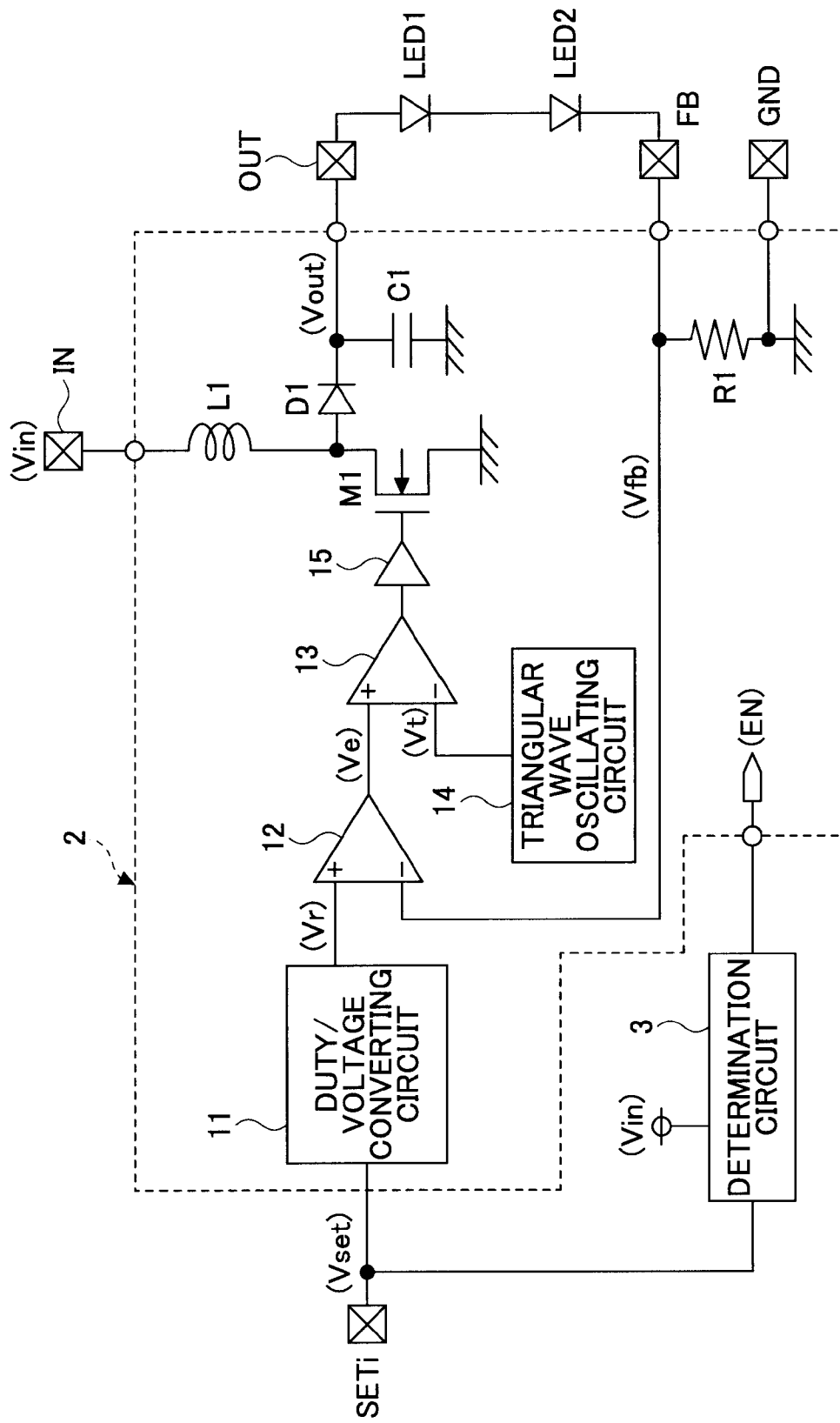
[Claim 11]

The method of controlling an operation of a semiconductor apparatus according to claim 9 or 10, further comprising applying the output voltage to a light-emitting diode via the output terminal, wherein the illuminance of the light-emitting diode is adjusted depending on the duty cycle of the voltage setting signal.

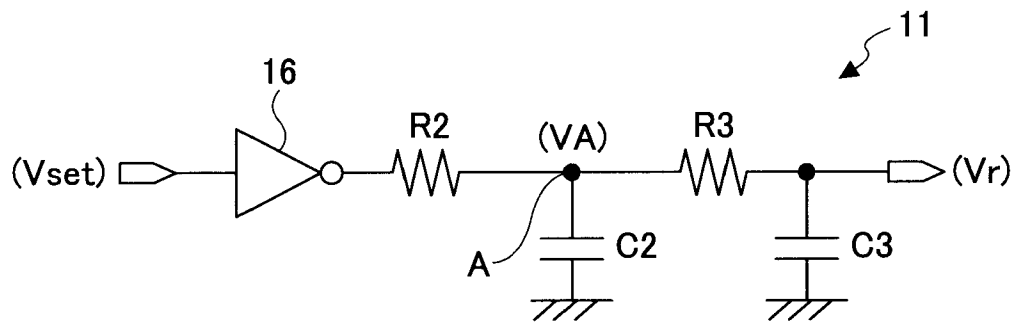
[Fig. 1]



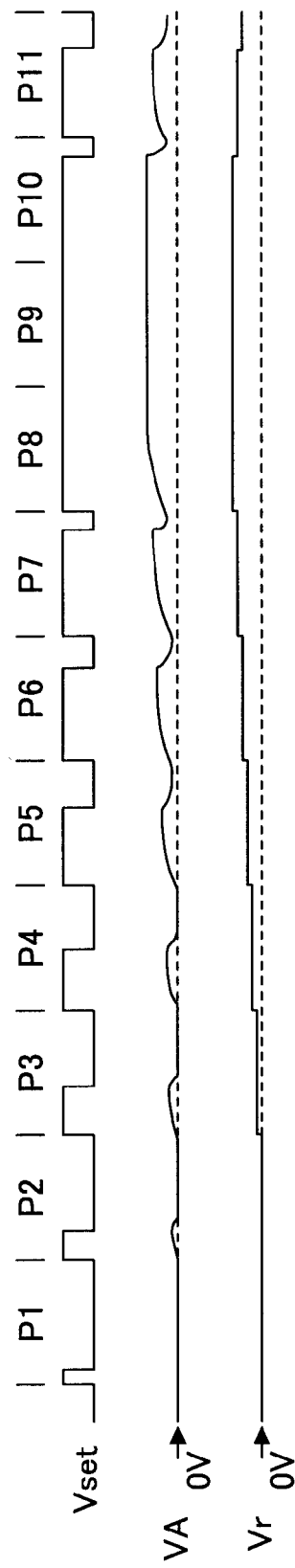
[Fig. 2]



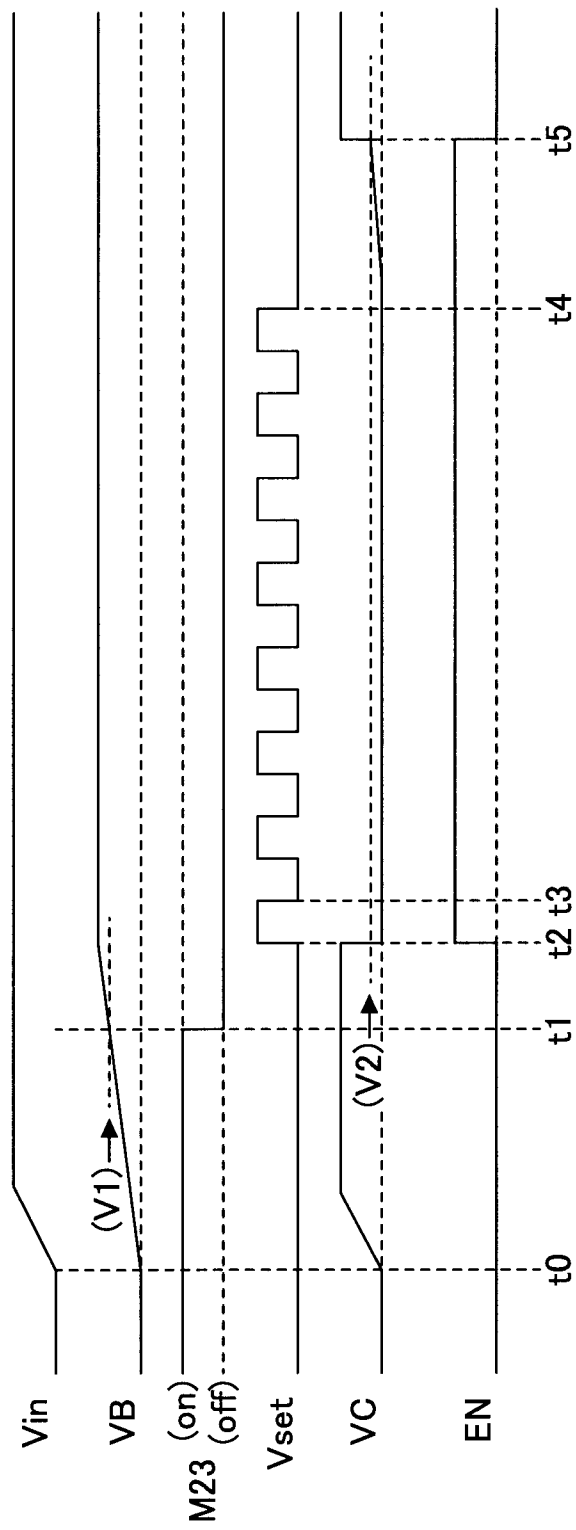
[Fig. 3]



[Fig. 4]



[Fig. 6]



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2010/000129

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H02M3/155 (2006.01) i, H01L33/00 (2010.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H02M3/155, H01L33/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2010
 Registered utility model specifications of Japan 1996-2010
 Published registered utility model applications of Japan 1994-2010

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2006-101663 A (RICOH CAMPANY, LTD.) 2006.04.13, the whole document & US 2007/0114986 A1 & EP 1702403 A & WO 2006/036001 A2	1-11
A	JP 07-170726 A (Hitachi, LTD) 1995.07.04, the whole document (Family-none)	1-11
A	JP 05-335853 A (American Telephone & Telegraph Company) 1993.12.17, [0013] & US 5010306 A & EP 443251 A2	1-11
A	JP 2006-158038 A (RICOH CAMPANY, LTD) 2006.06.15, [0042] & US 2007/0159151 A1 & WO 2006/057431 A1	1-11



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