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(71) Applicant: **SHENZHEN GOODIX TECHNOLOGY CO., LTD.** [CN/CN]; Floor 13, Phase B Tengfei Industrial Building, Futian Free Trade Zone, Shenzhen, Guangdong 518045 (CN).

(72) Inventors: **YAZDI, Siavash**; Floor 13, Phase B Tengfei Industrial Building, Futian Free Trade Zone, Shenzhen, Guangdong 518045 (CN). **HUSSIEN, Faisal**; Floor 13, Phase B Tengfei Industrial Building, Futian Free Trade Zone, Shenzhen, Guangdong 518045 (CN).

(74) Agent: **LONGSUN LEAD IP LTD.**; Rm. 101, Building 3, No. 68 Beiqing Road, Haidian District, Beijing 100094 (CN).

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(54) Title: VOLTAGE-BASED AUTO-CORRECTION OF SWITCHING TIME

(57) Abstract: A control device for a switching voltage regulator having a high-side switch and a low-side switch to supply a switching voltage to a load includes a comparator configured to compare the switching voltage with a reference voltage to provide an enable signal to the low-side switch, and a spike detection circuit configured to receive the switching voltage and output an offset control signal to execute a time shift to the enable signal.

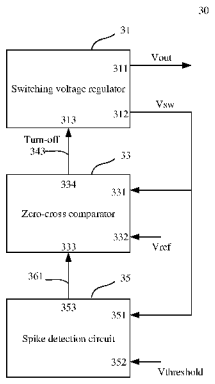

FIG. 3

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VOLTAGE-BASED AUTO-CORRECTION OF SWITCHING TIME

[0001] This patent document claims the benefits and priority of U.S. Non-Provisional Patent Application No. 15/957,900 entitled "VOLTAGE-BASED AUTO-CORRECTION OF SWITCHING TIME" filed April 19, 2018 by Shenzhen Goodix Technology Co., Ltd. The entire content of the before-mentioned patent application is incorporated by reference as part of the disclosure of this patent document.

FIELD OF THE INVENTION

[0002] The present invention relates generally to switching regulators. More particularly, embodiments of the present invention relate to control circuits, devices, and methods of detecting and eliminating the presence of spikes at a switching node of the switching regulators and optimizing a dead time in a switching module of the switching regulators.

BACKGROUND OF THE INVENTION

[0003] Voltage regulators have been employed for providing stable supply voltages to a large variety of electronic products. FIG. 1 schematically shows a switching voltage regulator 100, which includes a high-side switch 102 and a low-side switch 104 connected between an input voltage Vin and ground GND to be alternatively switched by a controller 106, a current sense circuit 108 senses an output current Iout flowing through an inductor L to charge a capacitor C to produce an output voltage Vout. Current sense circuit 108 senses the output current Iout to provide a current Isense to controller 106, which then turns on and off high-side switch 102 and low-side switch 104 to maintain a desired voltage level of the output voltage Vout.

[0004] However, improper turn-on and/or turn-off times of high-side switch 102 and low-side switch 104 may cause a large shoot-current flowing through the switches when the turn-on time of both switches overlaps, or overshoot current/voltage and undershoot current/voltage when the ideal switching time of both switches is not well controlled.

[0005] Thus, there is a need for solutions to overcome the above-described drawbacks.

BRIEF SUMMARY OF THE INVENTION

[0006] Embodiments of the present invention provides circuits, devices, and methods for correcting systematic offset or delay of a low-side switch in a switching voltage regulator. The offset or delay may cause glitches at the switching node of the switching voltage regulator. The glitches may cause additional power loss to the switching voltage regulator and reduce its life expectancy.

[0007] In accordance with some embodiments of the present invention, a control device for a switching voltage regulator having a high-side switch and a low-side switch to supply a switching voltage to a load may include a comparator configured to compare the switching voltage with a reference voltage to provide a disable (turn-off) signal to the low-side switch, and a spike detection circuit configured to receive the switching voltage and output an offset control signal to execute a time shift to the disable signal.

[0008] In one embodiment, the spike detection circuit includes a first input coupled to the switching voltage, a second input coupled to a threshold voltage, and an output for providing the offset control signal to the comparator.

[0009] In one embodiment, the comparator is a differential operational amplifier having a first input coupled to the switching voltage, a second input coupled to the reference voltage, and an output for providing the disable (turn-off) signal to the low-side switch. In one embodiment, the differential operational amplifier includes a variable resistive element.

[0010] In one embodiment, the spike detection circuit includes a first differential operational amplifier for detecting a positive glitch associated with a late off time of the disable signal, a second differential operational amplifier for detecting a negative glitch associated with an early off time of the disable signal, and a logic circuit coupled to the first and second differential operational amplifiers and configured to provide an indication signal indicating the presence of a glitch and whether the glitch is a positive glitch or a negative glitch. In one embodiment, the spike detection circuit further includes a digital-to-analog converter configured to convert the indication signal to an analog delay through adjusting a resistive value of the variable resistive element array.

[0011] In one embodiment, the high-side switch is a p-channel transistor, and the low-side switch is an n-channel transistor.

[0012] Embodiments of the present invention also provide a switching regulator including a controller for providing a first driver signal and a second driver signal, a dead-time control circuit having a first input terminal connected to the first driver signal, a second input terminal connected to the second driver signal, a first output terminal, and a second output terminal, a switching module coupled to the first and second out terminals and configured to supply a switching voltage to an LC network; and a spike detection circuit configured to receive the switching voltage and provide a control signal to the dead-time control circuit.

[0013] In one embodiment, the dead-time control circuit may comprise two cross-coupled logic gates including a first logic gate having a first input connected to the first input terminal, a second input, and a first output, a second logic gate having a third input connected to the second input terminal, a fourth input, and a second output; a first delay element having a fifth input connected to the second output of the second logic gate and a third output connected to the second input of the first logic gate; and a second delay element having a sixth input connected to the first output of the first logic gate and a fourth output connected to the second input of the second logic gate. In one embodiment, the first and second logic gates are not a same type logic gate.

[0014] In one embodiment, the first delay element and the second delay element each comprise RC elements. The RC elements may include a variable resistive element. In one embodiment, the variable resistive element includes a metal oxide semiconductor (MOS) transistor or a field effect transistor.

[0015] In one embodiment, the switching module includes a p-channel transistor and an n-channel transistor connected in series between an input voltage signal and ground.

[0016] In one embodiment, the spike detection circuit includes a differential operational amplifier having a first input for receiving the switching voltage, a second input for receiving a reference voltage, and configured to provide the control signal in response to a difference between the switching voltage and the reference voltage.

[0017] In one embodiment, the spike detection circuit further includes an analog-to-digital converter configured to convert the control signal to an analog delay through for adjusting a resistance value of the variable resistive element array.

[0018] Embodiments further provide a method for controlling a turn-off time of a low-side switch in a switching voltage regulator having a high-side switch and the low-side switch connected in series between an input voltage supply and ground. The method may include providing a spike detection circuit coupled to the switching voltage regulator. The method also includes determining a glitch at a switching node of the switching voltage regulator. In one embodiment, the glitch may be a positive glitch caused by a late turn-off of the low-side switch. In another embodiment, the glitch may be a negative glitch caused by an early turn-off of the low-side switch. In yet another embodiment, the glitch may not be present when the low-side switch is turned at the correct instant.

[0019] In one embodiment, the method may further include varying a slew rate of an output signal of a comparator in response to the glitch. In one embodiment, after determining that a glitch is present, the method may also provide a control signal to the comparator to vary the slew rate of the output signal according to the determined glitch. In one embodiment, the method may also include buffering the output signal, and providing the buffered output signal to turn off the low-side switch.

[0020] Embodiments of the present invention also provide a method for controlling a dead time of a switching regulator comprising a switching module and a controller providing first and second driver signals to the switching module. The method may include providing a dead-time control circuit between the controller and the switching module and a spike detection circuit between the switching module and the dead-time control circuit; monitoring a switching voltage at a switching node of the switching module by the spike detection circuit; and determining whether the switching voltage exceeds a threshold voltage. In one embodiment, if the method determines that the switching voltage exceeds the threshold voltage, the method includes generating a control signal to the dead-time control circuit to adjust a dead time between the first driver signal and the second driver signal; and if the method determines that the switching voltage does not exceed the threshold voltage, the method includes maintaining the dead time between the first driver signal and the second driver signal.

[0021] In one embodiment, the dead-time control circuit may include two cross-coupled logic gates including a first logic gate having a first input for receiving the first driver signal, a second input, and a first output, a second logic gate having a third input for receiving the second driver signal, a fourth input, and a second output, a first delay element having a fifth input connected to the second output of the second logic gate and a third output connected to the second input of the first logic gate, and a second delay element having a sixth input connected to the first output of the first logic gate and a fourth output connected to the second input of the second logic gate.

[0022] In one embodiment, determining whether the switching voltage exceeds a threshold voltage includes comparing the switching voltage with a threshold voltage to obtain the control signal, and converting the control signal to an analog signal for adjusting the dead time.

[0023] In one embodiment, the method further includes iteratively monitoring the switching voltage, comparing the switching voltage with the threshold voltage, and adjusting the dead time until the switching voltage is lower than first threshold voltage.

[0024] The following detailed description together with the accompanying drawings will provide a better understanding of the nature and advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] The accompanying drawings, referred to herein and constituting a part hereof, illustrate embodiments of the disclosure. The drawings together with the description serve to explain the principles of the invention.

[0026] FIG. 1 is a schematic diagram of a conventional switching voltage regulator, as known in the art.

[0027] FIG. 2A is a graph illustrating the switching voltage LX and the output current Iout of the voltage regulator in FIG. 1 for the case where the turn-off time of the low-side switch is at ideal timing.

[0028] FIG. 2B is a graph illustrating the switching voltage LX, the output current Iout of the voltage regulator in FIG. 1 for the case where the low-side switch is turned off late.

[0029] FIG. 2C is a graph illustrating the switching voltage LX and the output current Iout of the voltage regulator in FIG. 1 for the case where the low-side switch is turned off early.

[0030] FIG. 3 is a simplified block diagram of a switching regulator according to an embodiment of the present invention.

[0031] FIG. 3A is a circuit diagram of a switching voltage regulator according to an exemplary embodiment of the present invention.

[0032] FIG. 4 is a circuit diagram illustrating a spike detection circuit according to an embodiment of the present invention.

[0033] FIG. 5A is a graph illustrating the turn-off signal for the low-side switch in response to an offset control signal according to an embodiment of the present invention.

[0034] FIG. 5B is a graph illustrating adjusted slew rates shown in FIG. 5A being converted to a digital turn-off signal for the low-side switch after the output signal with adjusted slew rates passes through an inverter buffer according to an embodiment of the present invention.

[0035] FIG. 6 is a simplified flow chart of a method for controlling a turn-off time of a low-side switch in a switching voltage regulator according to an embodiment of the present invention.

[0036] FIG. 7 is a simplified block diagram of a switching voltage regulator for minimizing power loss during a dead time according to an embodiment of the present invention.

[0037] FIG. 8 is a simplified circuit diagram of a switching voltage regulator for minimizing a dead time according an embodiment of the present invention.

[0038] FIG. 9 is a schematic circuit diagram of an RC delay element according to an embodiment of the present invention.

[0039] FIG. 10 is a graph illustrating waveforms of driver signals for the respective high-side switch and the low-side switch according to an embodiment of the present invention.

[0040] FIG. 11 is a simplified flow chart of a method for controlling a dead time of a switching voltage regulator according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0041] In the following description, numerous specific details are provided for a thorough understanding of the present invention. However, it should be appreciated by those of skill in the art that the present invention may be realized without one or more of these details. In other examples, features and techniques known in the art will not be described for purposes of brevity.

[0042] It will be understood that the drawings are not drawn to scale, and similar reference numbers are used for representing similar elements. Embodiments of the invention are described herein with reference to functional block diagrams that are schematic illustrations of idealized embodiments (and intermediate structures) of the invention.

[0043] It will be understood that, when an element or component is referred to as "connected to" or "coupled to" another element or component, it can be connected or coupled to the other element or component, or intervening elements or components may also be present. In contrast, when an element or component is referred to as being "directly connected to" or "directly coupled to" another element or component, there are no intervening elements or components present between them. It will be understood that, although the terms "first" ,"second" ,"third" etc. may be used herein to describe various elements, components, these elements, components, regions, should not be limited by these terms. These terms are only used to distinguish one element, component, from another element, component. Thus, a first element, component, discussed below could be termed a second element, component, without departing from the teachings of the present invention. As used herein, the terms "logic low", "low state", "low level" ,"logic low level", "low" or "0" are used interchangeably. The terms "logic high", "high state" ,"high level", "logic high level", "high" or "1" are used interchangeably.

[0044] As used herein, the terms "a", "an" and "the" may include singular and plural references. It will be further understood that the terms "comprising", "including", having" and variants thereof, when used in this specification, specify the presence of stated features, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, steps, operations, elements, components, and/or groups thereof. In contrast, the term "consisting of" when used in this specification, specifies the stated features, steps, operations, elements, and/or components, and precludes additional features, steps, operations, elements and/or components. Furthermore, as used herein, the words "and/or" may refer to and

encompass any possible combinations of one or more of the associated listed items. The terms "Vsw" and "LX" are used interchangeably herein.

[0045] Referring back to FIG. 1, controller 106 receives feedback signal carrying Isenseinformation to control the turn-on and turn-off times of high-side and low-side switches 102, 104 through respective gate driver signal Pgate 112 and Ngate 114. When Pgate signal 112 transitions from a high state to a low state (e.g., from Vin to 0V), high-side switch 102 is turned on, and when Pgate signal 112 transitions to a high state, high-side switch 102 is turned off. Conversely, when Ngate signal 114 transitions from a low state to a high state (e.g., from 0V to Vin), low-side switch 104 is turned on, and when Pgate signal 112 transitions to a low state, low-side switch 104 is turned off. High-side and low-side switches 102, 104 are alternatively turned on, so that they are not turned on at the same time to avoid a shoot-through current. The turning on of high-side switch sends a current Iout through the inductor L to charge the capacitor C to provide the output voltage Vout to a load.

[0046] FIG. 2A is a graph illustrating the switching voltage LX and the output current Iout for the case where the low-side switch is turned off at the ideal time. Referring to FIG. 2A, at time < t0, both the high-side switch and the low-side switch are turned off. When controller 106 turns on high-side switch 102 at time t0, the input voltage Vin is supplied to the inductor L at node LX 124, the current Iout rises with a constant slope 201 and starts charging the capacitor C. At time t1, controller 106 turns off high-side switch 102 and turns on low-side switch 104, the current Iout begins to fall with a constant slope 202. At t2, when Iout crosses the zero threshold, controller 106 turns off low-side switch 104. The capacitor C smooths out the triangular current Iout to deliver a DC current to the load.

[0047] FIG. 2B is a graph illustrating the switching voltage LX and the output current Iout for the case where the low-side switch is turned off late. Referring to FIG. 2B, instead of turning off low-side switch 104 at t2, controller 106 turns off low-side switch 104 late, the current Iout will undershoot the zero crossing before low-side switch 104 is turned off (at time t3). Then, the inductor L operates as a current source that continues to deliver the undershoot current value and cause the voltage LX to rise from 0V to a peak voltage Vpeak Vd102 that is above Vin by an amount equivalent to the voltage drop across the body diode D102 (e.g., 07V). The negative current 213 will continue to flow through the body diode D102, and peak voltage Vpeak Vd102

will remain until the negative current 223 decreases back to zero at t4. At this time, the switching voltage LX at node 124 is back to the desired output voltage Vout.

[0048] FIG. 2C is a graph illustrating the switching voltage LX, the output voltage Vout, and the output current Iout for the case where the low-side switch is turned off early. Referring to FIG. 2C, instead of turning off low-side switch 104 when Iout crosses the zero crossing, controller 106 turns off low-side switch 104 early, the current Iout is still positive at t2. Both the high-side and low-side switches are now turned off, the inductor will keep the current Iout to continue to flow through the body diode D104 of the low-side switch into the inductor, so that the switching voltage LX is below ground (indicated by Vd104) while the positive current decreases to zero. The current flowing through body diodes D102 (FIG. 2B) and body diode D104 causes additional power consumption and heat dissipation in the switching regulator. Besides, the overshoot and undershoot values, Vd102 and Vd104, can cause reliability issues for the pass devices 102 and 104. Accordingly, the present inventors provide novel technical solutions to avoid these drawbacks.

[0049] FIG. 3 is a simplified block diagram of a switching regulator 30 that can correct systematic offsets causing an early or late switching of the low-side switch according to an embodiment of the present invention. Switching regulator 30 includes a switching voltage regulator 31, a zero-cross comparator 33, a spike detection circuit 35. Switching voltage regulator 31 may include a first output terminal 311 for providing a desired output voltage Vout to a load, a second output terminal 312 for providing a switching voltage Vsw, and a first input terminal 313. Zero-cross comparator 33 may include a second input terminal 331 for receiving the switching voltage Vsw, a third input terminal 332 for receiving a reference voltage Vref, a fourth input terminal 333, and a second output terminal 334 for providing a turn-off signal (disable) 343 to switching voltage regulator 31 through first input terminal 313. Spike detection circuit 35 may include a fifth input terminal 351 for receiving the switching voltage Vsw, a sixth input terminal 352 for receiving a threshold voltage Vthreshold, and a third output terminal 353 for providing an offset control signal 361 to zero-cross comparator 303. The terms “turn-off signal” and “disable signal” are used interchangeably herein.

[0050] FIG. 3A is a circuit diagram of a switching voltage regulator 30A according to an exemplary embodiment of the present invention. Referring to FIG. 3A, switching voltage

regulator 31A includes logic circuit 305 for driving a switching module including a high-side switch 302 and a low-side switch 304, a zero-cross comparator 33A, and a spike detection circuit 35A. In some embodiments, high-side switch 302 may be a P-channel transistor, low-side switch may be an N-channel transistor. High-side switch 302 is turned on by a Pgate signal at a low state (e.g., 0V) and turned off by the Pgate signal at a high state (e.g., Vin). When high-side switch 302 is turned on, the voltage Vsw at node 324 will have substantially the voltage Vin. Low-side switch 302 is turned on by an Ngate signal at the high state (e.g., Vin) and turned off by the Ngate signal at the low state (e.g., 0V). When low-side switch 304 is turned on, the voltage Vsw at node 324 will have substantially the voltage GND.

[0051] Referring back to FIG. 2A, the current Iout flowing through the inductor L increases linearly from 0A to a certain value when high-side switch 302 is turned on and low-side switch 304 is turned off (e.g., between the time period t0-t1). The current Iout decreases linearly from the certain value to 0A when high-side switch 302 is turned off and low-side switch 304 is turned on (e.g., time period t1-t2). The capacitor C is charged by the current Iout to provide a desired output voltage Vout. The turn-on and turn-off times of high-side and low-side switches are controlled by logic circuit 305 of the switching voltage regulator. There is no undershoot or overshoot in the switching voltage Vsw at node 324 if logic circuit 305 turns off low-side switch 304 at the ideal time when the current Iout crosses zero (e.g., at time t2).

[0052] Referring back to FIG. 2B, in the case where logic circuit 305 turns off low-side switch 304 too late, the current Iout will overshoot the zero crossing before low-side switch is turned off. The negative current will flow to ground through low-side switch 304. When low-side switch 304 is eventually turned off at time t3, the switching voltage Vsw at node 324 will rises from 0V to above the supply voltage Vin by an amount equivalent to the body diode D302. The current continues to flow across the body diode D302 of high-side switch 302, the switching voltage Vsw remains at its peak value Vpeak until the current Iout decreases to 0A at time t4. After that, the switching voltage Vsw returns back to the desired output voltage value Vout.

[0053] Referring back to FIG. 2C, in the case where logic circuit 305 turns off low-side switch 304 too early, i.e., the current Iout has not reached the zero crossing at time t2, the inductor L will maintain the continuous current flow so that the current Iout will flow across the body diode

D304 of low-side switch 304. The switching voltage Vsw will remain below the ground level (denoted by Vnegative) while the current Iout decreases to 0A at time t3.

[0054] The voltage overshoot and undershoot can be detected by spike detection circuit 35A. In one example embodiment, spike detection circuit 35A includes a differential operational amplifier 350 having a first input 351 for receiving the switching voltage, a second input 352 for receiving a first threshold voltage Vthreshold1, and a third input for receiving a second threshold voltage Vthreshold2. Spike detection circuit 35A is configured to compare the switching voltage Vsw with the first and second threshold voltages and provide a decision result. For example, the first threshold voltage may be Vin or a percentage of Vin, and the second threshold voltage may be 0V. When the switching voltage Vsw is greater than the first threshold voltage, spike detection circuit 35A determines that low-side switch 304 is turned off too late. Similarly, when the switching voltage Vsw is lower than the the second threshold voltage, spike detection circuit 35A determines that low-side switch 304 is turned off too early. When the switching voltage Vsw is within the range between 0V and Vout, spike detection circuit 35A determines that low-side switch 304 is turned off at the exact time. In one embodiment, spike detection circuit 35A may also include a decision result storage 360 that stores the decision result whether the turn-off time of low-side switch is at the exact time, too late, or too early and provides the stores decision result as an offset control signal 361 to zero-cross comparator 33A.

[0055] FIG. 4 is a circuit diagram illustrating a spike detection circuit 40 according to an embodiment of the present invention. Referring to FIG. 4, spike detection circuit 40 may include a first differential operational amplifier 41 having a first input 411 for receiving the switching voltage Vsw and a second input 412 for receiving a first threshold voltage Vth1, a second differential operational amplifier 42 having a third input 421 for receiving the switching voltage Vsw and a fourth input 422 for receiving a second threshold voltage Vth2, and decision making logic 43 for making control decision. For example, the first threshold voltage Vth1 may have a voltage level about the voltage level of Vin, and the second threshold voltage Vth2 may have a voltage level about 0V. In one embodiment, first differential operational amplifier 41 is configured to operate as a comparator to compare the difference between Vsw and Vth1 and outputs a comparison result “Late” 413 when it determines that Vsw > Vth1. In one embodiment, the second differential operational amplifier 42 is configured to operate as a

comparator to compare the difference between Vsw and Vth2 and outputs a comparison result "Early" 423 when it determines that Vsw < Vth2. Decision making logic 43 includes a first input 431 for receiving Late signal 413 and a second input for receiving Early signal 423. Decision making logic 43 also includes logic gates (e.g., NAND, NOR), latches, flipflops to make decisions whether the switching voltage Vsw includes a glitch (i.e., a positive voltage above Vin or negative voltage below 0V) at the node 324. In one embodiment, spike detection circuit 40 may further include a digital-to-analog circuit for converting the decision result (i.e., whether low-side switch 304 is turned off at the right time, too early, or too late) to a corresponding analog offset control signal for controlling the zero-cross comparator 33A. It is understood that the spike detection circuit and the zero-cross comparator are only operative when the high-side switch is in the turn-off state.

[0056] Referring back to FIG. 3A, zero-cross comparator 33A includes a first input 331 for receiving the switching signal Vsw, a second input 332 for receiving a reference voltage Vref, and a third input 333 for receiving an offset control signal 361 provided by spike detection circuit 35A. The reference voltage Vref may be a value in the range between 0V and Vout. In one embodiment, zero-cross comparator 33A may include a differential operational amplifier 330 and a variable resistive element 315 having a resistance value that can be varied under the control of the analog offset control signal 361 receiving at third input 333. In one embodiment, variable resistive element 315 may include an array of resistors whose equivalent resistance value determined by a digital control word. In some embodiments, a capacitor may be connected in parallel to variable resistance element 315. In an example embodiment, variable resistance element 315 may a MOS transistor, a bipolar transistor, a field effect transistor, whose resistive value can be adjusted linearly with respect to the control voltage at its gate (base).

[0057] FIG. 5A is a graph illustrating the turn-off signal for the low-side switch in response to an offset control signal according to an embodiment of the present invention. Referring to FIG. 5A, the slew rate of turn-off signal 343 at output 334 of zero-cross comparator 33A may be adjusted in response to offset control signal 361. For example, line 511 represents a slew rate of the output signal at a nominal value of variable resistance element 335, which corresponds to the correct turn-off time of low-side switch 304; line 512 represents a slew rate when the resistive value of variable resistance element 335 increases; and line 513 represents a slew rate when the

resistive value of variable resistance element 335 decreases. FIG. 5B is a graph illustrating the adjusted slew rates shown in FIG. 5A being converted to a digital turn-off signal for the low-side switch after the output signal with adjusted slew rates passes through an inverter buffer (not shown). For example, the turn-off signal for the low-side switch may be delayed by an amount $\Delta t1$ or advanced by an amount $\Delta t2$ in relation to a nominal time t by adjusting the resistive value of variable resistance element 335. It is understood that the inverter buffer (not shown) can be implemented in the zero-cross comparator or in the switching voltage regulator.

[0058] In another embodiment, zero-cross comparator 331 may include a series-string of delay elements, e.g., a resistor array whose equivalent resistance value can be determined by a digital code word. In this case, digital-to-analog converter 44 of spike detection circuit 35A shown in FIG. 4 is omitted. Logic circuit 43 will output control signals (i.e., digital code words) for controlling the series-string of delay elements (i.e., determining the equivalent resistance value of the series-string of delay elements or resistor array) to adjust the turn-off signal timing of low-side switch 304. In yet another embodiment, zero-cross comparator 331 may include an internal offset shift to Vref (332) value. In this case, digital-to-analog converter 44 of spike detection circuit 35A shown in FIG. 4 is omitted. Logic circuit 43 will output control signals for controlling the value of the offset affecting the comparator output switching with a delay corresponding to the offset value added. This adjusts the turn-off signal timing of low-side switch 304.

[0059] FIG. 6 is a simplified flow chart of a method 600 for controlling a turn-off time of a low-side switch in a switching voltage regulator having a high-side switch and the low-side switch connected in series between an input voltage supply and ground. Method 600 may include:

[0060] At 601: providing a spike detection circuit coupled to the switching voltage regulator. In one embodiment, the spike detection circuit may be spike detection circuit 35A shown in FIG. 3A or spike detection circuit 40 shown in FIG. 4 and described in sections above.

[0061] At 603: determining a glitch at an output terminal of the switching voltage regulator. The glitch may be a positive glitch caused by a late turn-off of the low-side switch. The glitch may be a negative switch caused by an early turn-off of the low-side switch. The glitch may not be present when the low-side switch is turned at the ideal time.

[0062] At 605: varying a slew rate of an output signal of a comparator in response to the glitch. After determining that a glitch is present, the method may also provide a control signal to the comparator to vary the slew rate of the output signal according to the determined glitch. For example, the output signal slew rate curve of the comparator can be made steeper if the glitch is determined to be a positive glitch, i.e., the low-side switch was turned off to late, or the output signal slew rate curve of the comparator can be made slower than the nominal value if the glitch is determined to be a negative glitch, i.e., the low-side switch was turned off to early.

[0063] At 607: buffering the output signal. The output signal is then buffered to drive the low-side switch. In one embodiment, the buffer may be integrated in the comparator. In another embodiment, the buffer may be integrated in the switching voltage regulator. In some embodiments, the buffer, the comparator, and the switching voltage regulator are integrated within the same integrated circuit.

[0064] At 609: providing the buffered output signal to turn off the low-side switch.

[0065] As described above, a late or early turn-off of the low-side switch causes the inductor current Iout to flow across the body diode of the high-side switch or the low-side switch, thereby increasing power loss in the switching voltage regulator. Another cause of power loss is associated with the non-overlap period of the high-side and low-side switches. As used herein, a dead time is defined as a time when neither the high-side switch nor the low-side switch is turned on. When both high-side and low-side switches are only momentarily on at the same time, a large shoot-through current will flow between the input supply voltage and ground. However, when a dead time is selected to exceed an optical time period, the inductor current Iout flows through the body diode of the low-side switch and causes voltage ringing at the switching node LX. Also, it causes power loss through the body diode. Embodiments of the present invention provide a circuit and method for reducing power loss associated with the dead time.

[0066] FIG. 7 is a simplified block diagram of a switching voltage regulator 70 for minimizing power loss during a dead time according to an embodiment of the present invention. Referring to FIG. 7, switching voltage regulator 70 include a logic circuit 71 for providing driver signals Pdrive and Ndrive, a dead-time control circuit 72, a high-side switch 702, a low-side switch 704, and a spike detection circuit 75. Switching voltage regulator 70 further includes an inductor L and a capacitor C. The inductor L and the capacitor C may be integrated with switching voltage

regulator 70 in the same integrated circuit, or the inductor L and the capacitor may be external to switching voltage regulator 70. In one embodiment, dead-time control circuit 72 may include two cross-coupled gates and a pair of delay elements each of which having one terminal coupled to an output of one of the two cross-coupled gates and another terminal coupled to an input of one of the two cross-coupled gates. Spike detection circuit 75 may include a differential operational amplifier operative to compare the switching voltage Vsw with a threshold voltage and provides a dead-time control signal 752 to dead-time control circuit 72.

[0067] FIG. 8 is a simplified circuit diagram of a switching voltage regulator 80 according an embodiment of the present invention. Referring to FIG. 8, dead-time control circuit 82 includes a first gate 801, a second gate 802, a first delay element 803, and a second delay element 804. First gate 801 has a first input coupled to the Pdrive signal, a second input coupled to an output of first delay element 803, and a first output coupled to an input of second delay element 804. Second gate 802 has a third input coupled to an output of second delay element 804, a fourth input coupled to the Ndrive signal, and a second output coupled to an input of first delay element 803. Switching voltage regulator 80 may further include a first buffer 805 having an input coupled to the first output of first gate 801 and an output coupled to high-side switch 702, and a second buffer 806 having an input coupled to the second output of second gate 802 and an output coupled to low-side switch 704. Spike detection circuit 85 may include a differential operational amplifier configured to compare the switching output voltage Vsw with a threshold voltage for determining the presence of a glitch. The threshold voltage may have a level ranging around 0V. Spike detection circuit 85 may also include a logic circuitry for providing a dead-time control signal 752 to first and second delay elements 803, 804. In one embodiment, spike detection circuit 85 may be similar to spike detection circuit 35A shown in FIG. 3A. In another embodiment, spike detection circuit 85 may be similar to spike detection circuit 40 shown in FIG. 4.

[0068] In one embodiment, the first and second delay elements may be RC delay elements. FIG. 9 is a schematic circuit diagram of RC delay elements 90 according to an embodiment of the present invention. RC delay elements 90 may include a variable resistive element 91 and a capacitor C 92. Variable resistive element 91 may an MOS transistor, a field effect transistor, and the like having a resistive value that can be adjusted under the control of a voltage applied at

its gate. In one embodiment, the voltage applied to variable resistive element 91 is the analog dead-time control signal 752 provided by spike detection circuit 85 (e.g., provided by the analog-to-digital converter 44 shown in FIG. 4). In one embodiment, the first and second delay elements may be a current-starved delay cell, where the delay is controlled through a current supplied to the delay cell. This can vary under the control of a voltage applied to a gate of an MOS transistor.

[0069] In one embodiment, first gate may be an OR gate, and second gate may be an AND gate. In another embodiment, first gate may be an AND gate, and second gate may be an OR gate. In yet another embodiment, first gate may be a NOR gate, and second gate may be a NAND gate. In still another embodiment, first gate may be a NAND gate, and second gate may be a NOR gate. One of skill in the art will appreciate that a NAND gate in the positive logic system may be expressed by a NOR gate in the negative system.

[0070] FIG. 10 is a graph illustrating waveforms of driver signals 807 and 808 for the respective high-side switch and the low-side switch according to an embodiment of the present invention. As shown in FIG. 10, the dead time is variable, thereby enabling the control of the turn-on or turn-off time of the high-side switch and the low-side switch. One of skill in the art will appreciate that the delay elements provide the delay only when the gate outputs change from a high level to a low level in the case of an OR gate, alternatively, the delay elements provide the delay only when the gate outputs change from a low level to a high level in the case of an AND gate. By having different types of logic gates for the first and second gates, the dead time can be controlled both in the high-to-low and low-to-high transitions.

[0071] FIG. 11 is a simplified flow chart of a method 1100 for controlling a dead time of a switching voltage regulator according to an embodiment of the present invention. Referring to FIG. 11, method 1100 may include:

[0072] At 1101: providing a dead-time control circuit between a logic circuit of the switching voltage regulator and the high-side and low-side switches.

[0073] At 1103: monitoring a switching voltage at an output terminal of the switching voltage regulator by a spike detection circuit.

[0074] At 1105: determining whether the switching voltage exceeds a threshold voltage by the spike detection circuit.

[0075] At 1107: if the switching voltage is determined to exceed the threshold voltage, generating a control signal and provide the control signal to the dead-time control circuit to adjust a dead time between a first driver signal and a second driver signal and go back to 1103. If the switching voltage is determined not to exceed the threshold voltage, maintaining the dead time between the first driver signal and the second driver signal and go back to 1103.

[0076] While the present invention is described herein with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Rather, the purpose of the illustrative embodiments is to make the spirit of the present invention be better understood by those skilled in the art. In order not to obscure the scope of the invention, many details of well-known processes and manufacturing techniques are omitted. Various modifications of the illustrative embodiments, as well as other embodiments, will be apparent to those of skill in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications.

[0077] Furthermore, some of the features of the preferred embodiments of the present invention could be used to advantage without the corresponding use of other features. As such, the foregoing description should be considered as merely illustrative of the principles of the invention, and not in limitation thereof. Those of skill in the art will appreciate variations of the above-described embodiments that fall within the scope of the invention. As a result, the invention is not limited to the specific embodiments and illustrations discussed above, but by the following claims and their equivalents.

CLAIMS

WHAT IS CLAIMED IS:

1. A control device for a switching voltage regulator having a switching module to supply a switching voltage to a load, the control device comprising:

a comparator configured to compare the switching voltage with a reference voltage to provide a disable signal to the switching module; and

a spike detection circuit configured to receive the switching voltage and output an offset control signal to execute a time shift to the disable signal.

2. The control device of claim 1, wherein the spike detection circuit comprises a first input coupled to the switching voltage, a second input coupled to a threshold voltage, and an output for providing the offset control signal to the comparator.

3. The control device of claim 1, wherein the comparator is a differential operational amplifier having a first input coupled to the switching voltage, a second input coupled to the reference voltage, a third input coupled to the offset control signal of the spike detection circuit, and an output for providing the disable signal to the switching module.

4. The control device of claim 3, wherein the differential operational amplifier comprises:

a variable resistive element with an equivalent resistance determined by an analog control signal; or

a resistor array with an equivalent resistance determined by a digital word.

5. The control device of claim 4, wherein the spike detection circuit comprises:

a first differential operational amplifier for detecting a positive glitch associated with a first off time of the disable signal;

a second differential operational amplifier for detecting a negative glitch associated with a second off time of the disable signal;

a logic circuit coupled to the first and second differential operational amplifiers and configured to provide an indication signal indicating a presence of a glitch and whether the glitch is a positive glitch or a negative glitch.

6. The control device of claim 5, wherein the spike detection circuit further comprises a digital-to-analog converter configured to convert the indication signal to an analog signal for adjusting a resistive value of the variable resistive element.

7. The control device of claim 1, wherein the switching module comprises a high-side switch being a p-channel transistor, and a low-side switch being an n-channel transistor.

8. A switching regulator comprising:

a controller for providing a first driver signal and a second driver signal;

a dead-time control circuit comprising a first input terminal connected to the first driver signal, a second input terminal connected to the second driver signal, a first output terminal, and a second output terminal;

a switching module coupled to the first and second out terminals and configured to supply a switching voltage to an LC network; and

a spike detection circuit configured to receive the switching voltage and provide a control signal to the dead-time control circuit.

9. The switching regulator of claim 8, wherein the dead-time control circuit comprises:

two cross-coupled logic gates including a first logic gate having a first input connected to the first input terminal, a second input, and a first output, a second logic gate having a third input connected to the second input terminal, a fourth input, and a second output;

a first delay element having a fifth input connected to the second output of the second logic gate and a third output connected to the second input of the first logic gate;

a second delay element having a sixth input connected to the first output of the first logic gate and a fourth output connected to the second input of the second logic gate.

10. The switching regulator of claim 9, wherein the switching module comprises:

one or more p-channel transistor and one or more n-channel transistor connected in series between an input voltage signal and ground.

11. The switching regulator of claim 9, wherein the first and second logic gates are not a same type logic gate.

12. The switching regulator of claim 9, wherein the first delay element and the second delay element each comprise an RC element or a cascaded delay stage having a plurality of variable delay units.

13. The switching regulator of claim 12, wherein the RC element comprises a variable resistive element.

14. The switching regulator of claim 13, wherein the variable resistive element comprises a metal oxide semiconductor (MOS) transistor or a field effect transistor.

15. The switching regulator of claim 13, wherein the spike detection circuit comprises:

a differential operational amplifier having a first input for receiving the switching voltage, a second input for receiving a reference voltage, and configured to provide the control signal in response to a difference between the switching voltage and the reference voltage.

16. The switching regulator of claim 15, wherein the spike detection circuit further comprises an analog-to-digital converter configured to convert the control signal to an analog signal for adjusting a resistance value of the variable resistive element.

17. The switching regulator of claim 12, wherein the plurality of variable delay units comprises:

an array of switchable capacitor elements; or

current controlled delay cells.

18. A method for controlling a dead time of a switching regulator comprising a switching module and a controller providing first and second driver signals to the switching module, the method comprising:

providing a dead-time control circuit between the controller and the switching module and a spike detection circuit between the switching module and the dead-time control circuit;

monitoring a switching voltage at an output terminal of the switching module by the spike detection circuit;

determining whether the switching voltage exceeds a threshold voltage; and

if the switching voltage exceeds the threshold voltage, generating a control signal to the dead-time control circuit to adjust a dead time between the first driver signal and the second driver signal; and

if the switching voltage does not exceed the threshold voltage, maintaining the dead time between the first driver signal and the second driver signal.

19. The method of claim 18, wherein the dead-time control circuit comprises:

two cross-coupled logic gates including a first logic gate having a first input for receiving the first driver signal, a second input, and a first output, a second logic gate having a third input for receiving the second driver signal, a fourth input, and a second output;

a first delay element having a fifth input connected to the second output of the second logic gate and a third output connected to the second input of the first logic gate; and

a second delay element having a sixth input connected to the first output of the first logic gate and a fourth output connected t the second input of the second logic gate.

20. The method of claim 18, wherein determining whether the switching voltage exceeds a threshold voltage comprises:

comparing the switching voltage with a threshold voltage to obtain the control signal; and

converting the control signal to an analog signal for adjusting the dead time.

21. The method of claim 20, further comprising:

iteratively monitoring the switching voltage, comparing the switching voltage with the threshold voltage, and adjusting the dead time until the switching voltage is lower than first threshold voltage.

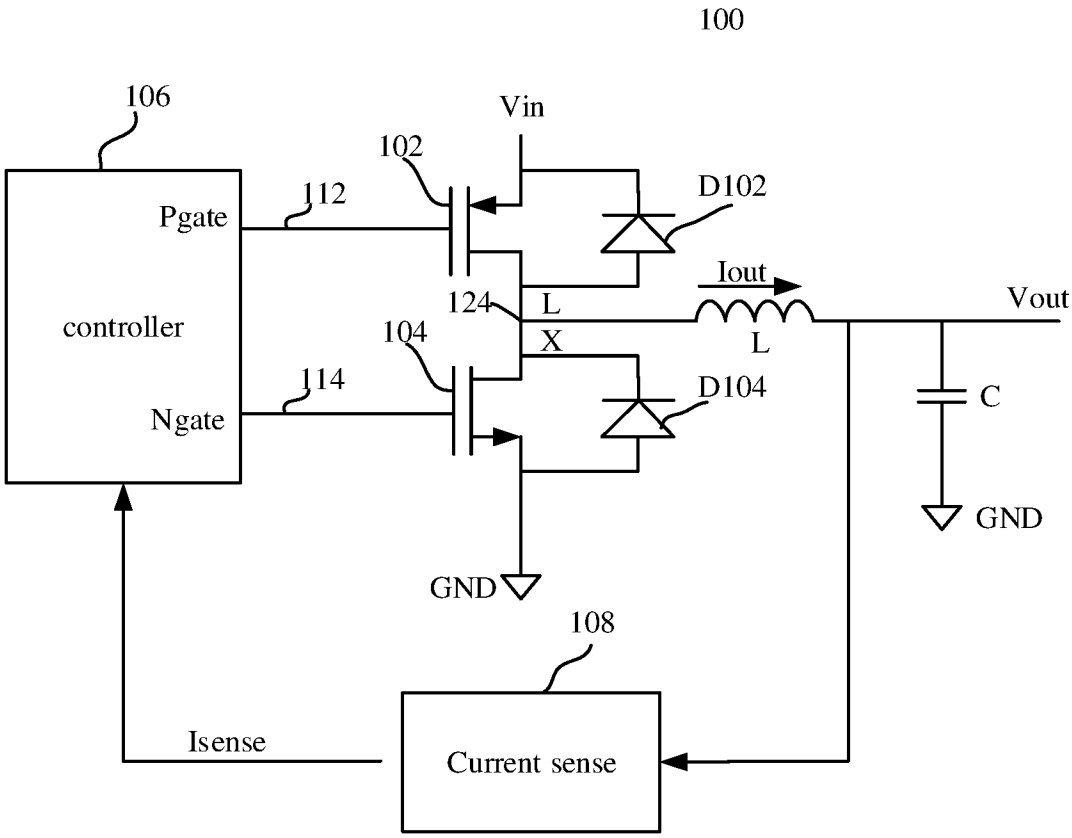
100
106
Vin
102
D102
112
Pgate
Iout
124
L
Vout
controller
104
X
L
114
D104
C
Ngate
GND
GND
108
Isense
Current sense

FIG. 1

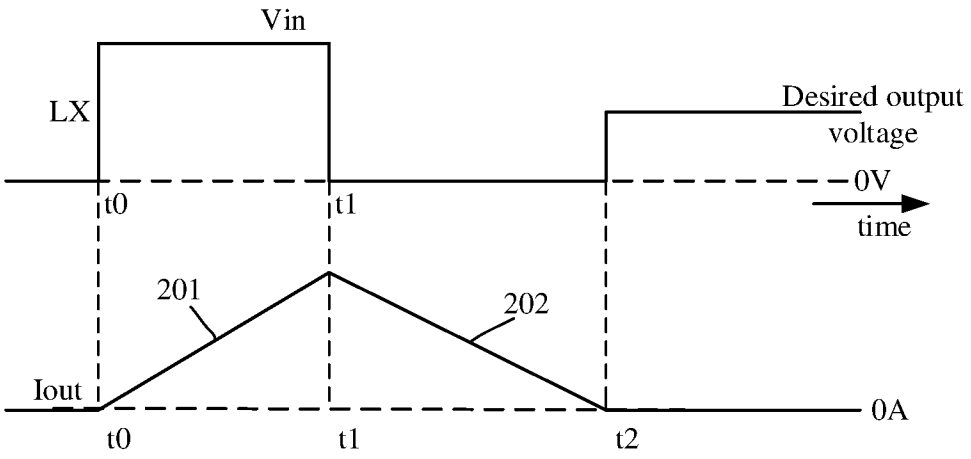

FIG. 2A

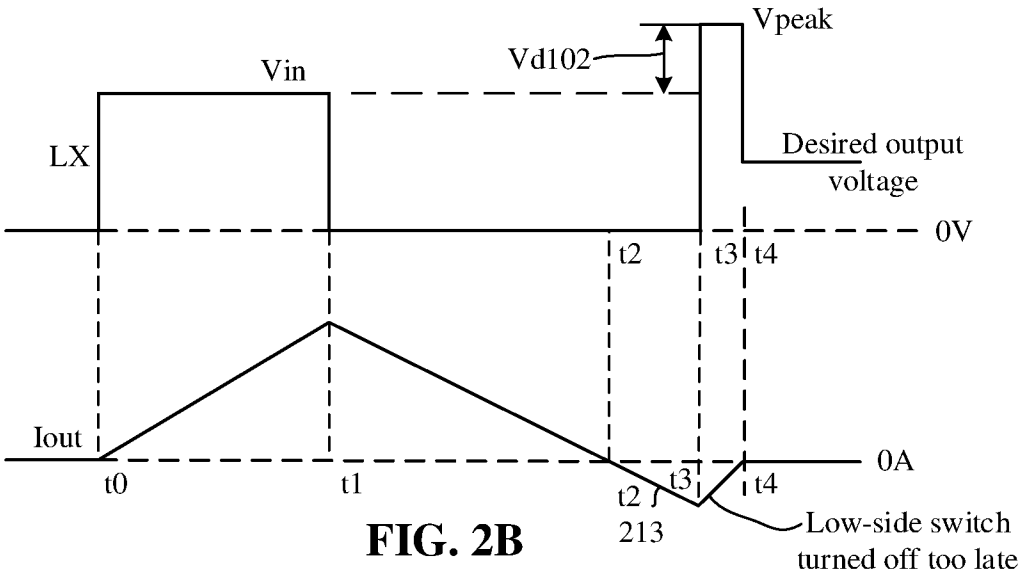

FIG. 2B

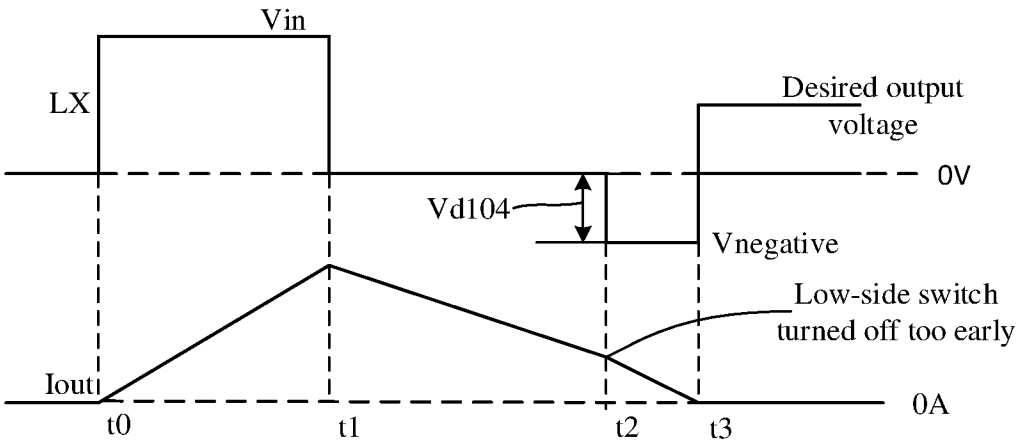

FIG. 2C

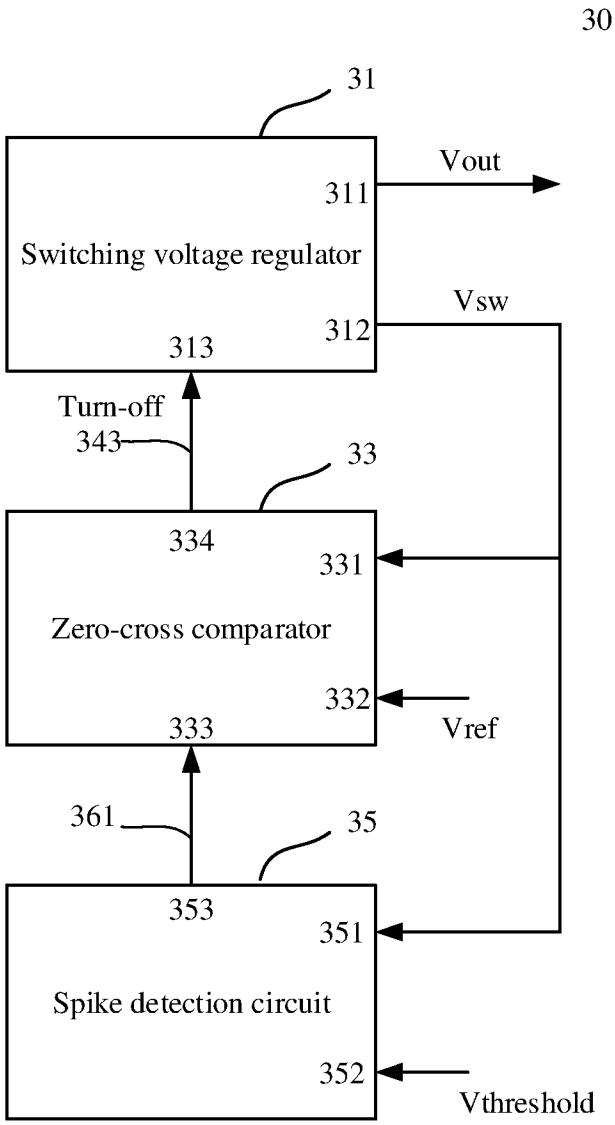
30
31
Vout
311
Switching voltage regulator
Vsw
312
313
Turn-off
343
33
334
331
Zero-cross comparator
332
Vref
333
361
35
353
351
Spike detection circuit
352
Vthreshold

FIG. 3

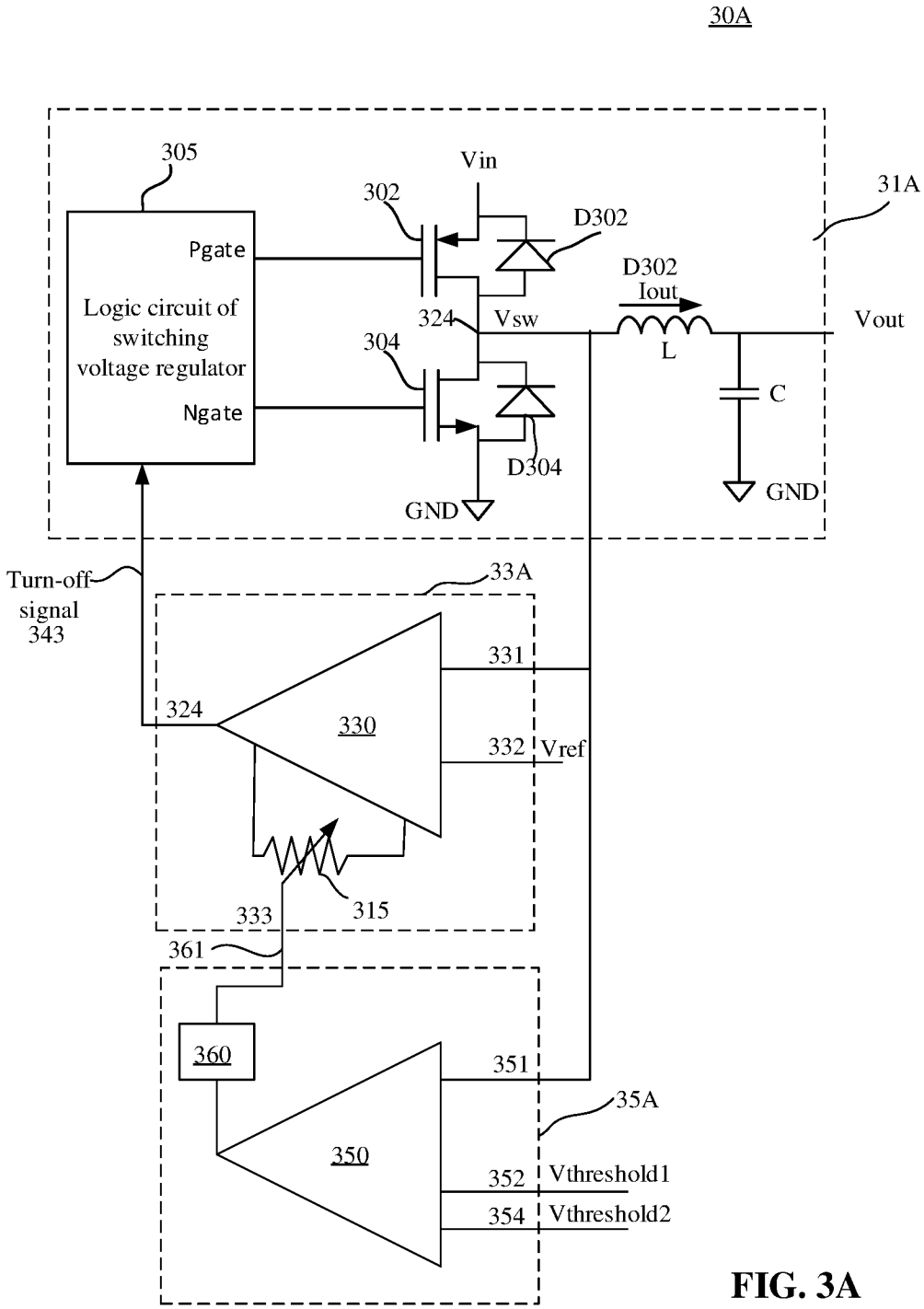
30A
305
Vin
302
D302
31A
Pgate
D302
Iout
Logic circuit of switching voltage regulator
324
Vsw
Vout
304
L
C
Ngate
D304
GND
GND
Turn-off signal 343
33A
331
324
330
332
Vref
315
333
361
360
351
35A
350
352
Vthreshold1
354
Vthreshold2

FIG. 3A

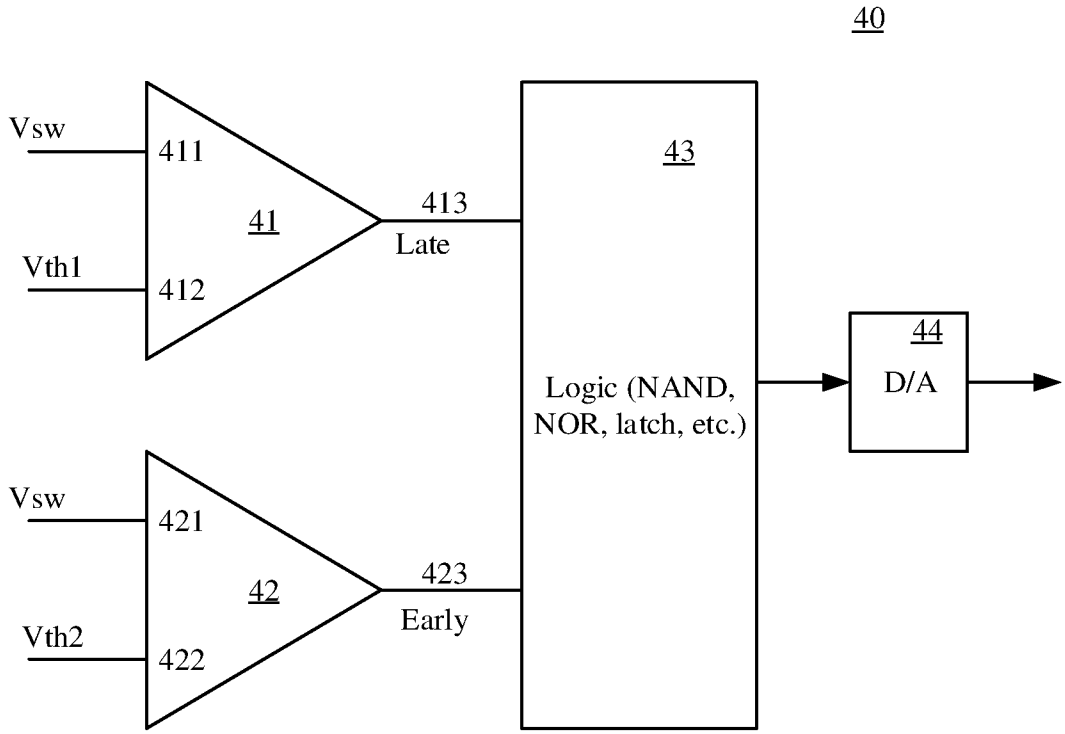
40
Vsw
411
41
Vth1
412
413
Late
43
Logic (NAND, NOR, latch, etc.)
44
D/A
Vsw
421
42
Vth2
422
423
Early

FIG. 4

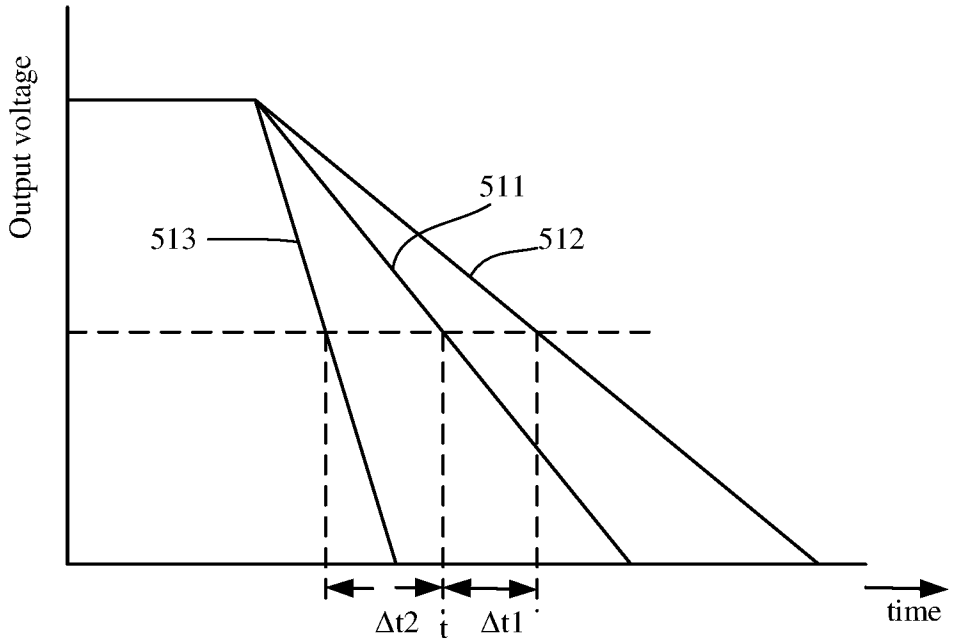
Output voltage
511
513
512
Δt2
t
Δt1
time

FIG. 5A

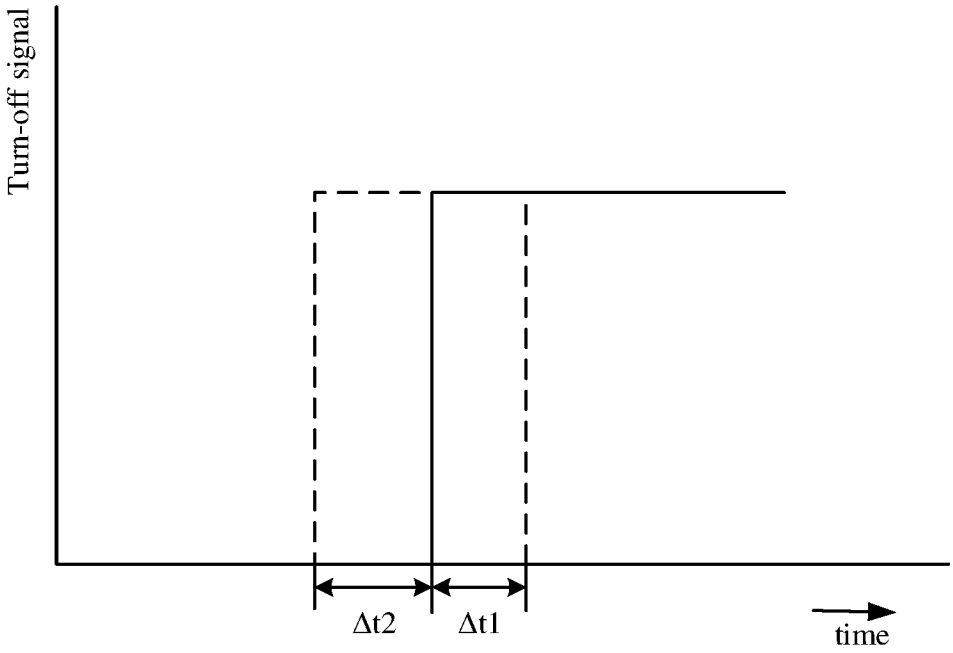
Turn-off signal
Δt2
Δt1
time

FIG. 5B

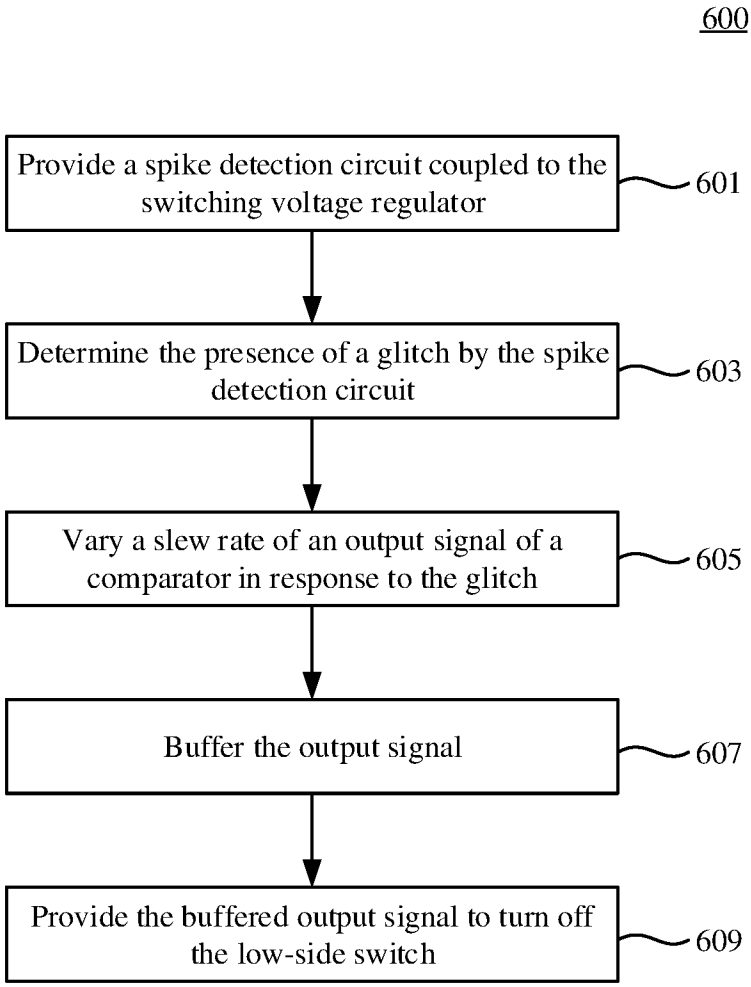
600
Provide a spike detection circuit coupled to the switching voltage regulator
601
Determine the presence of a glitch by the spike detection circuit
603
Vary a slew rate of an output signal of a comparator in response to the glitch
605
Buffer the output signal
607
Provide the buffered output signal to turn off the low-side switch
609

FIG. 6

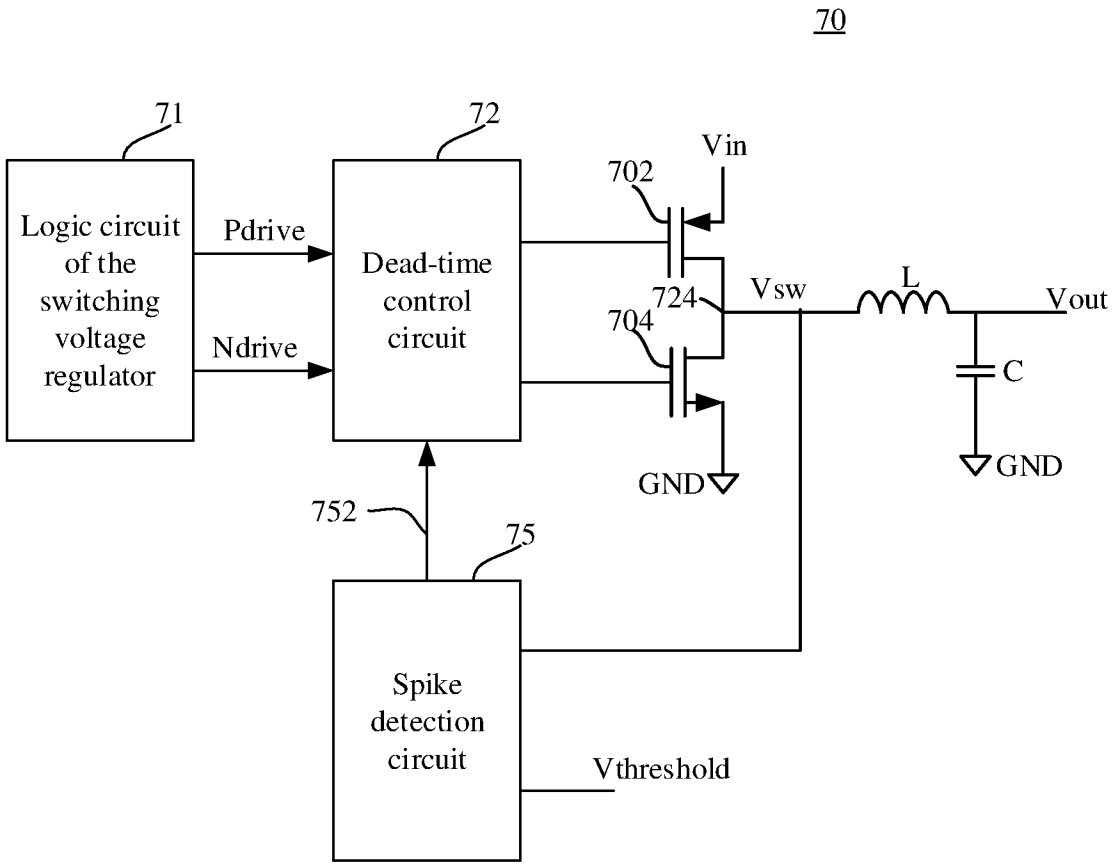
70
71
72
Logic circuit of the switching voltage regulator
Pdrive
Ndrive
Dead-time control circuit
Vin
702
724
704
Vsw
L
Vout
C
GND
GND
752
75
Spike detection circuit
Vthreshold

FIG. 7

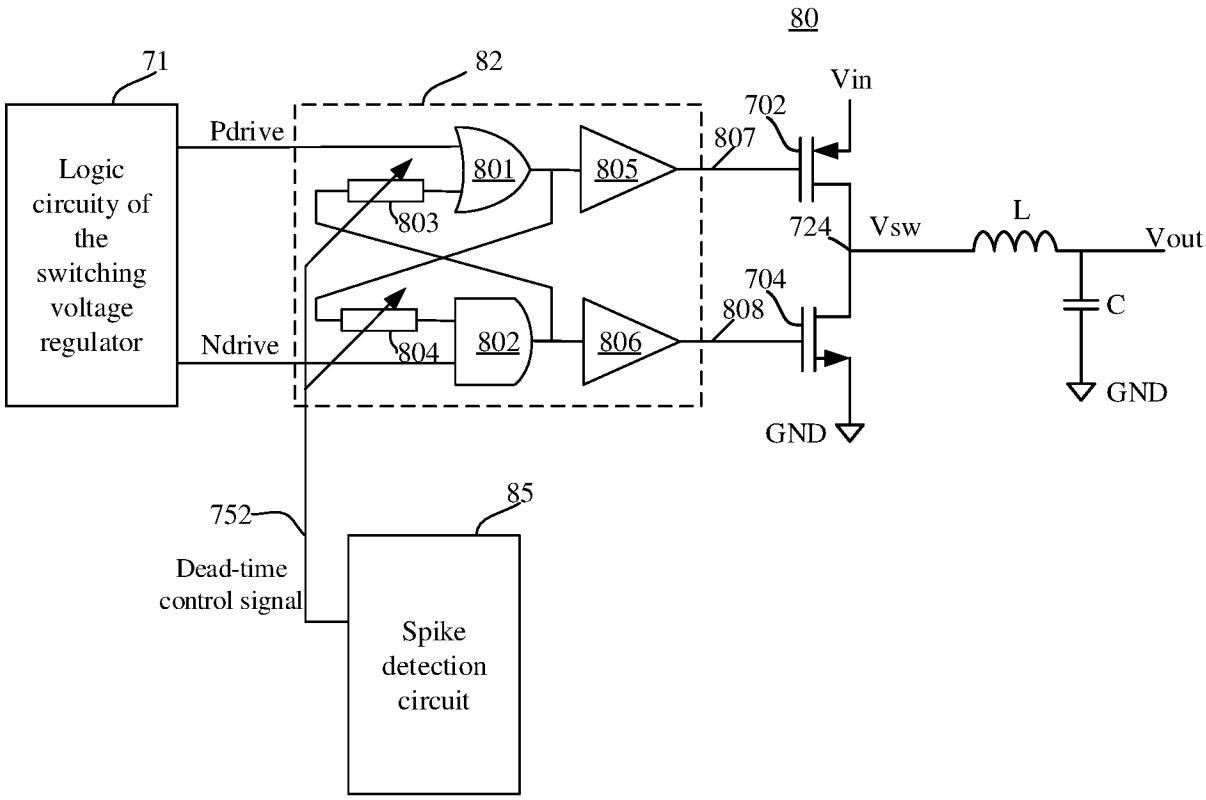
80
71
82
Logic circuity of the switching voltage regulator
Pdrive
Ndrive
801
802
803
804
805
806
807
808
702
704
724
Vin
Vsw
L
Vout
C
GND
GND
752
Dead-time control signal
85
Spike detection circuit

FIG. 8

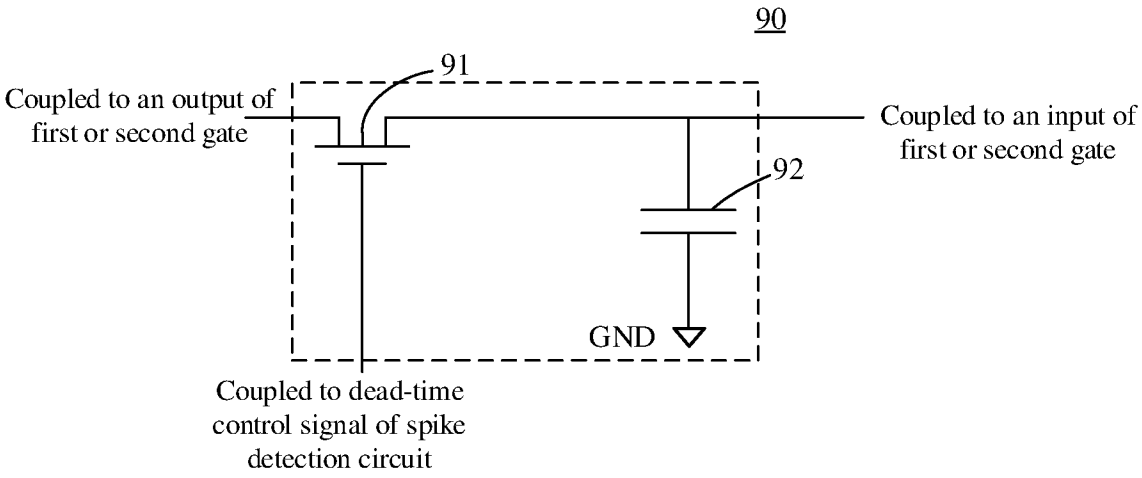
90
91
Coupled to an output of first or second gate
Coupled to an input of first or second gate
92
GND
Coupled to dead-time control signal of spike detection circuit

FIG. 9

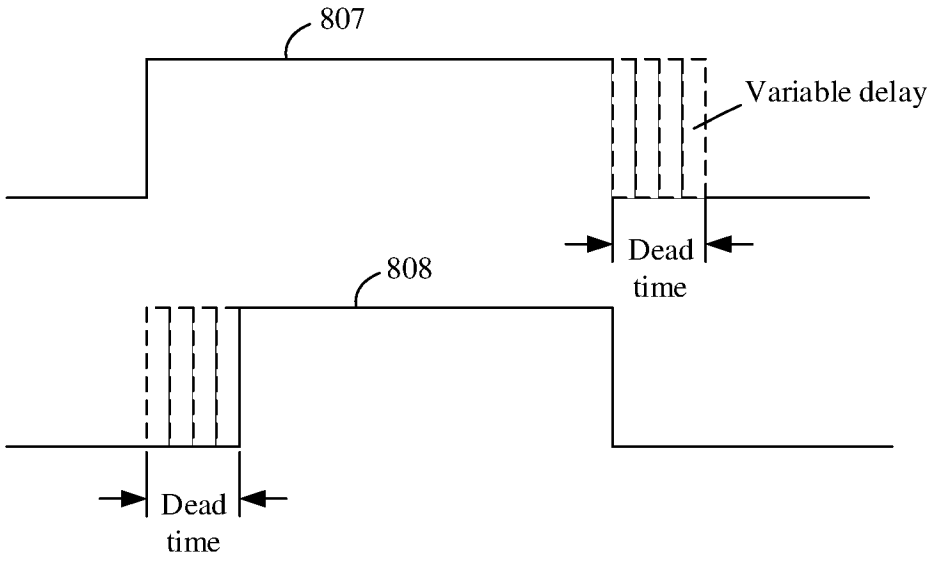
807
Variable delay
Dead time
808
Dead time

FIG. 10

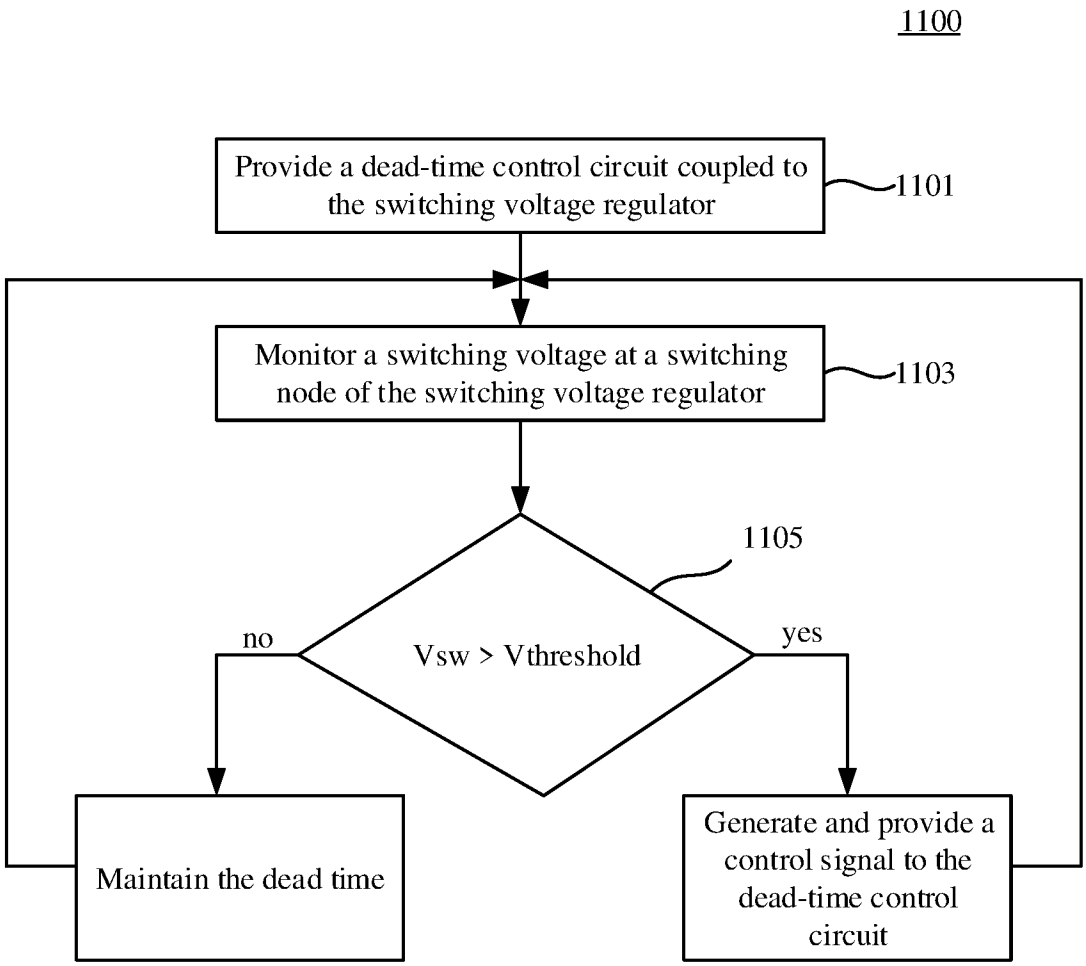
1100
Provide a dead-time control circuit coupled to the switching voltage regulator
1101
Monitor a switching voltage at a switching node of the switching voltage regulator
1103
1105
Vsw > Vthreshold
no
yes
Maintain the dead time
Generate and provide a control signal to the dead-time control circuit

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/104420

A. CLASSIFICATION OF SUBJECT MATTER

H02M 3/155(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC,WPI,CNPAT,USTXT,CNKI,IEEE: switch+ 2w voltage, spik+ 2w detect+, comparator, dead 2w time

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	TW 201230681 A (ANPEC ELECTRONICS CORP.) 16 July 2012 (2012-07-16) description, page 8, line 9-page 13, line 6, figures 6-7	1-7
Y	CN 107735932 A (QUALCOMM INCORPORATED) 23 February 2018 (2018-02-23) description, paragraphs [0085]-[0090], figures 5-6	8-21
A	CN 103616556 A (SILERGY SEMICONDUCTOR TECHNOLOGY HANGZHOU CO., LTD.) 05 March 2014 (2014-03-05) the whole document	1-21
A	US 2017294839 A1 (DIALOG SEMICONDUCTOR UK LIMITED) 12 October 2017 (2017-10-12) the whole document	1-21
Y	TW 201230681 A (ANPEC ELECTRONICS CORP.) 16 July 2012 (2012-07-16) description, page 8, line 9-page 13, line 6, figures 6-7	8-21

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 January 2019	**18 January 2019**
Name and mailing address of the ISA/CN **National Intellectual Property Administration, PRC** **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing** **100088** **China** Facsimile No. **(86-10)62019451**	Authorized officer **WANG,Xun** Telephone No. **86-(10)-53961265**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2018/104420

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
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CN	107735932	A	23 February 2018	US	9729061	B2	08 August 2017
				US	2017012526	A1	12 January 2017
				WO	2017007619	A1	12 January 2017
CN	103616556	A	05 March 2014	CN	103616556	B	18 January 2017
				US	9444441	B2	13 September 2016
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US	2017294839	A1	12 October 2017	US	2016233768	A1	11 August 2016
				US	9685868	B2	20 June 2017
				DE	102015224873	A1	11 August 2016