PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
G11C 5/02

A1

(11) International Publication Number: **WO 96/36050**

(43) International Publication Date: 14 November 1996 (14.11.96)

(21) International Application Number: PCT/US96/04253

(22) International Filing Date: 27 March 1996 (27.03.96)

(30) Priority Data:
08/440,169 12 May 1995 (12.05.95) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: BILL, Colin; 1384 Rosegarden Lane, Cupertino, CA 95014 (US). GUTALA, Ravi; 655 S. Fair Oaks Avenue, Sunnyvale, CA 94086 (US). CHANG, Chung; 627 San Juan Drive, Sunnyvale, CA 94086 (US). VAN BUSKIRK, Michael; 1742 Fabian Drive, San Jose, CA 95124 (US).

(74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

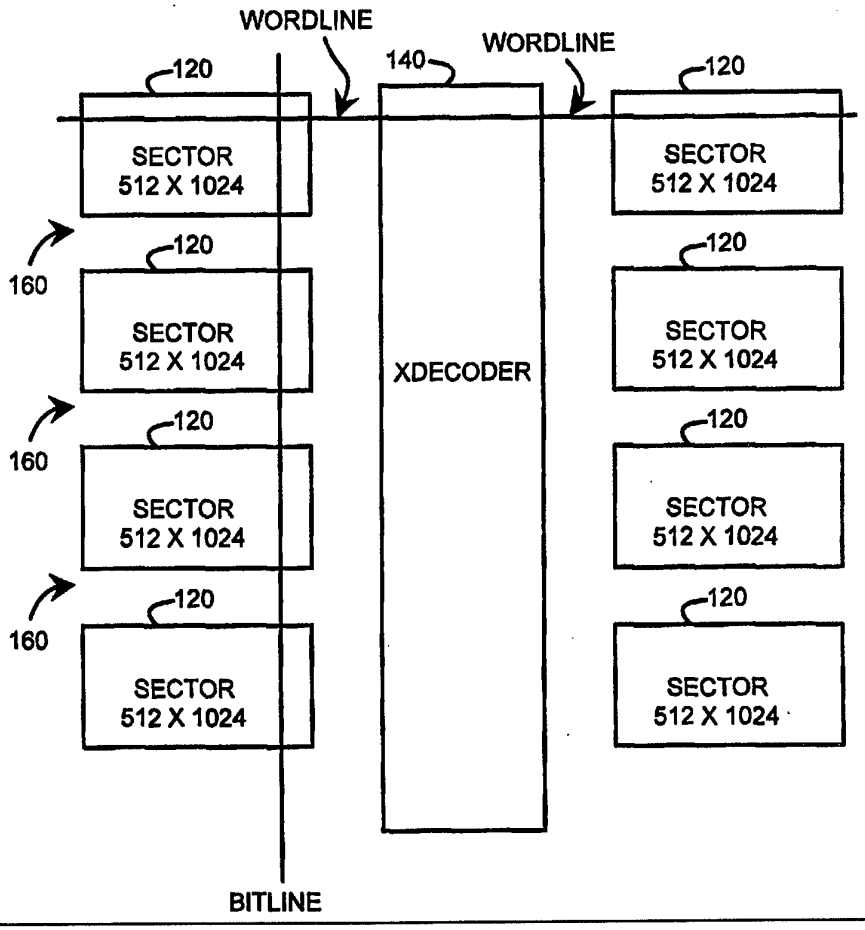
(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: SECTOR ARCHITECTURE FOR FLASH MEMORY DEVICE

(57) Abstract

A sector architecture for a FLASH EPROM in accordance with the present invention includes a wordline decoder and a plurality of sectors, the sectors having a wordline to bitline ratio such that all of the sectors are on one side of the decoder. In so doing, the number of boundaries in the architecture are significantly reduced compared to the conventional architecture. Therefore, through this sector architecture arrangement, a FLASH memory product die area can be significantly reduced given the same size memory.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	**GB**	United Kingdom	**MW**	Malawi
AT	Austria	**GE**	Georgia	**MX**	Mexico
AU	Australia	**GN**	Guinea	**NE**	Niger
BB	Barbados	**GR**	Greece	**NL**	Netherlands
BE	Belgium	**HU**	Hungary	**NO**	Norway
BF	Burkina Faso	**IE**	Ireland	**NZ**	New Zealand
BG	Bulgaria	**IT**	Italy	**PL**	Poland
BJ	Benin	**JP**	Japan	**PT**	Portugal
BR	Brazil	**KE**	Kenya	**RO**	Romania
BY	Belarus	**KG**	Kyrgystan	**RU**	Russian Federation
CA	Canada	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SG**	Singapore
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovakia
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LR**	Liberia	**SZ**	Swaziland
CS	Czechoslovakia	**LT**	Lithuania	**TD**	Chad
CZ	Czech Republic	**LU**	Luxembourg	**TG**	Togo
DE	Germany	**LV**	Latvia	**TJ**	Tajikistan
DK	Denmark	**MC**	Monaco	**TT**	Trinidad and Tobago
EE	Estonia	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**UG**	Uganda
FI	Finland	**ML**	Mali	**US**	United States of America
FR	France	**MN**	Mongolia	**UZ**	Uzbekistan
GA	Gabon	**MR**	Mauritania	**VN**	Viet Nam

SECTOR ARCHITECTURE FOR FLASH MEMORY DEVICE

FIELD OF THE INVENTION

The present invention is related to flash memories of the type implemented on semiconductor chips and in particular to a sector architecture arrangement for use in such memory chips.

BACKGROUND OF THE INVENTION

Large Scale Integration (LSI) techniques have made possible the construction of memory devices having large arrays of binary storage elements on a single chip of silicon. The advantages for such arrangements are the high cell density and low power requirements. A typical flash memory chip includes a plurality of sectors. A sector in the context of this application is a section of the core of the memory array that can be independently erased. Previously, in known flash memory architectures, a central wordline decoder is utilized. The central decoder therefore divides each sector in half. This type of sector arrangement has worked effectively in known memory cell arrays until up to approximately a four (4) megabit (Mb) cell level.

As the number of memory cells for a particular device has become larger, e.g., 16 and 32 megabit cells, this type of array requires significantly more die area. The reason for this in the prior art is that the number of sector boundaries along the direction of the bit line

increases one extra sector boundary for each additional sector added to the array. As is well known, select transistors are typically located on the boundaries between sectors. In a 4 megabit array, only eight of these boundaries are required between the sectors, for 64 Kbyte sector storage.

However, as the number of memory cells is increased, for example, 8 Mb and greater, the number of required boundaries becomes greater, one extra boundary for each sector added. Typically a sector boundary is between 55 and 70 microns in size. Accordingly, these additional boundaries significantly increase the die size of the semiconductor device.

Accordingly, in such a memory device, as the number of bits increases, the number of boundaries increases. It is well understood that to ensure that the die is as densely packed and compact as possible, any means that could be used to reduce the size of the die would be upgraded utility. What is desired therefore is a sector architecture which is more compact and utilizes less surface area than previously known sector architectures. The sector architecture at the same time should be one which is easily implemented using existing processes. It should also be economically feasible while at the same time significantly reducing the overall die size of the integrated circuit. The present invention address such a need.

SUMMARY OF THE INVENTION

A sector architecture for a Flash memory core cell array arrangement in accordance with the present invention includes an wordline decoder and a plurality of sectors, the sectors having a wordline to bitline ratio such that all of each sector is on one side of the wordline decoder. In so doing, the number of sector boundaries in the bit line direction are significantly reduced compared to the conventional architecture. Therefore, through this sector architecture arrangement, a FLASH memory product die area can be significantly reduced given the same size memory.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a chip layout diagram illustrating how the conventional sector layout of a semiconductor integrated circuit is positioned relative to a central wordline decoder. The case of a 4 megabit device is shown.

Figure 2 is a chip layout diagram illustrating how the sector layout in accordance with the present invention of a semiconductor integrated circuit is positioned relative to an wordline decoder. The use of a 4 megabit device is shown.

Figure 3 is a 16 megabit implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates to an improvement in

the FLASH memory array architecture. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred embodiment and the generic principles and features described herein will be readily apparent to those skilled in the art.

Referring now in detail to the drawings, there is illustrated in Figure 1 a chip layout of how a conventional 64Kbyte sector 12 lies relative to an wordline decoder 14, all formed as a part of a single semiconductor integrated circuit chip (not shown).

The semiconductor integrated circuit chip also contains an array (not shown) having a large number of FLASH EPROM memory cells arranged in an N x M matrix. An external or off-chip power supply potential V_{cc} (also not shown) which is typically at +5.0 V, or +3.0V is supplied to the integrated circuit chip and is fed to the input of the distributed power supply (not shown). The array of the FLASH EPROM memory cells is formed on a substrate to define columns and rows, where the substrate includes a common source line extending along at least one of the rows and a plurality of bit lines extending along respective columns. Each of the memory cells includes an N-type source region coupled to the common source line, a control gate, a floating gate, a channel region and an N-

type drain region coupled to a respective one of the bit lines. Further, each of the memory cells is programmable predominately by transferring hot electrons into its floating gate and is erasable predominantly by tunneling electrons from its floating gate to its source region.

It should be noted that where the memory array is, for example, physically arranged in a matrix of 2048 rows by 2048 columns, a predetermined number of rows may be grouped together so as to form a sector defining a page-selectable erase block. For instance, the 2048 rows may be divided into 8 sectors with each sector being composed of an equal number of rows (256 each). However, it should be apparent to those skilled in the art that each sector could be formed with an unequal number of rows. Further, the columns may be broken into segments so that each sector has a left side and a right side (half-sectors).

As is seen in Figure 1, each sector 12 is essentially spread across the chip architecture (12L and 12R). One half of each sector 12 is on one side of the wordline decoder 14 and the other half of the sector 12 is on the other side of the wordline decoder 14. Hence in this embodiment, for a 4 megabit chip there are 8 sectors. In this embodiment, each of the sectors 12 are 256 wordlines wide and 2,048 bitlines long. The area 16 between each of the sectors is referred to as the boundary. These boundaries 16 are necessary to separate

the sectors from each other. A 16 Megabit device, using prior art architecture, would need 32 sectors and have 32 sector boundaries in the bit line direction. Each sector would be 4096 bit lines wide by 128 wordlines long.

For higher density Flash memories, i.e., 8 Mb and higher, these boundaries can take up significantly more area. As is seen in this type of architecture, with these long and thin sectors, the number of boundaries 16 in the bit line direction can increase significantly as the memory becomes larger. These boundaries 16 significantly increase the overall size of the chip architecture.

As above noted, previous examples of Flash memory products use a sector which is spread uniformly and horizontally across the chip on both sides of the wordline decoder. Had this method been used, there would be 32 sector boundaries along the bit line direction of the chip resulting in a significantly larger die. What is needed therefore is an improvement that would limit the number of boundary areas and still allow for the same or greater memory capability in the architecture to allow for a reduced die size.

The present invention substantially reduces the number of boundaries on the integrated circuit by confining the area of one sector to one side of the wordline decoder 14. The present invention changes the aspect ratio of the sector. In other words, a sector has

a higher wordline to bitline ratio. In so doing, each sector can be made such that it is all on one side of the wordline decoder.

To more particularly understand the present invention, refer now to Figure 2. Figure 2 shows a plurality of eight sectors 120 which would be the equivalent of the 16 sector architecture shown in Figure 1. As is seen, each sector 120 is confined to one side of wordline decoder 145. In this embodiment, to produce the 16 Mb device, each sector is 512 wordlines wide and 1024 bitlines long rather than being 128 wordlines wide by 4096 bitlines long as would be required by the architecture used in in Figure 1. (Also, for 16 meg device, four times the architecture shown in Figure 2 is needed). Figure 3 shows the 16 Mb implementation. A total of 8 boundaries in the bit line direction are needed compared with 32 needed in the prior art.

Although the present invention has been described in relationship to 16 Mb FLASH memory device, one of ordinary skill in the art will readily recognize that it can be utilized in a variety of sizes of memories and that use would be within the spirit and scope of the present invention. Accordingly, Applicants have discovered that by making the sectors, wordline to bitline ratio greater than 0.25, the number of boundaries therebetween can be significantly reduced. In so doing, the overall size of the architecture can be significantly

reduced. It has been found for example that on the 16 Mb Flash product approximately 13 $Kmil^2$ of die area was saved (representing 10% die area) using the technique.

Although the present invention has been described in accordance with the embodiments shown in the figures, one of ordinary skill in the art recognizes there could be variations to the embodiments and those variations would be within the spirit and scope of the present invention. Accordingly, many modifications may be made by one of ordinary skills in the art without departing from the spirit and scope of present invention, the scope of which is defined solely by the appended claims.

CLAIMS

1. A sector architecture for a FLASH memory core cell array comprising:

a wordline decoder means; and

a plurality of sectors, each of the sectors having a wordline to bitline ratio such that all of each sector is confined to one side of the wordline decoder means.

2. The sector architecture arrangement of claim 1 in which the wordline to bitline ratio of the sector is greater than 0.25.

3. The sector architecture arrangement of claim 1 in which the FLASH memory is 8 megabit (Mb) or greater.

4. The sector architecture of claim 1 in which each of the sectors comprises 512 wordlines by 1024 bitlines.

5. The sector architecture of claim 1 in which the decoder means comprises a wordline decoder.

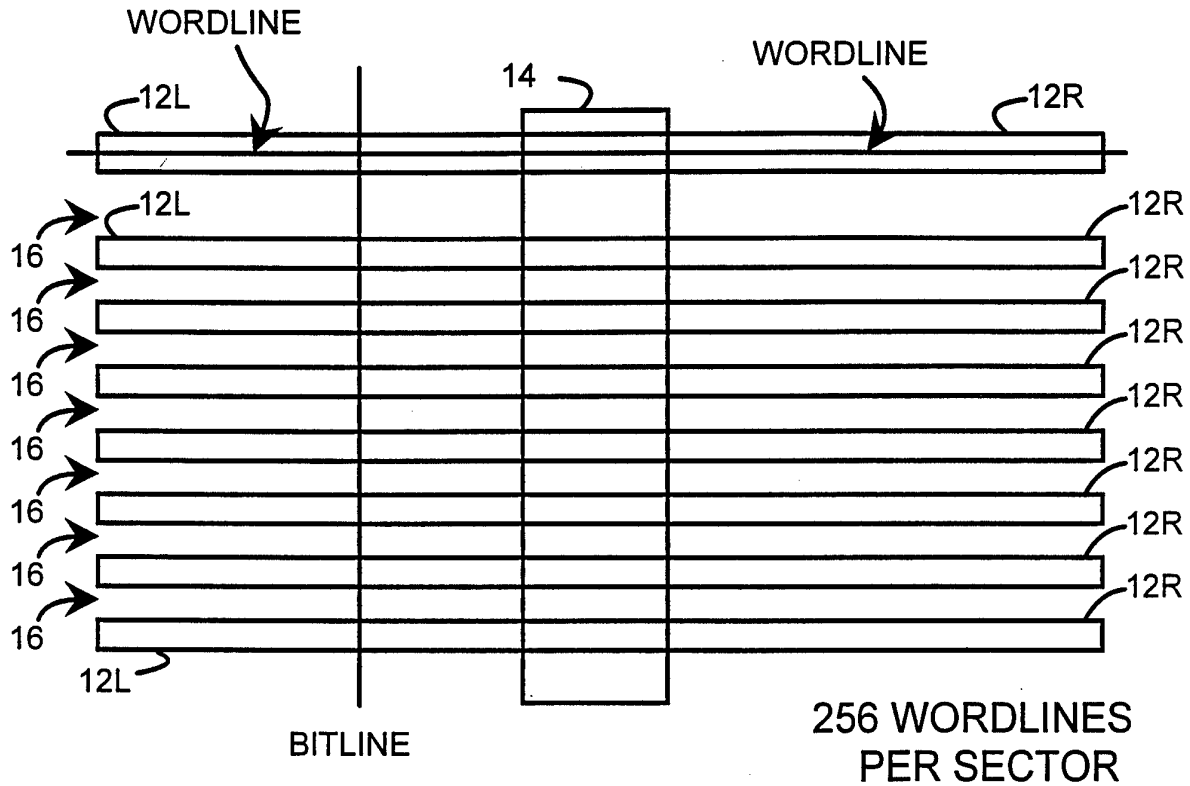
6. A sector architecture for a FLASH memory core cell array, the FLASH memory cell having a memory capacity of greater than 8 megabits, comprising:

a decoder means; and

a plurality of sectors, each of the sectors having a wordline to bitline ratio such that all of each sector are confined to one side of the decoder means, each sector having a wordline to bitline ratio of greater than 0.25.

7. The sector architecture of claim 6 in which each of the sectors comprises 512 wordlines by 1024 bitlines.

8. The sector architecture of claim 6 in which the wordline decoder means comprises a wordline decoder.



PRIOR-ART

10

FIGURE 1

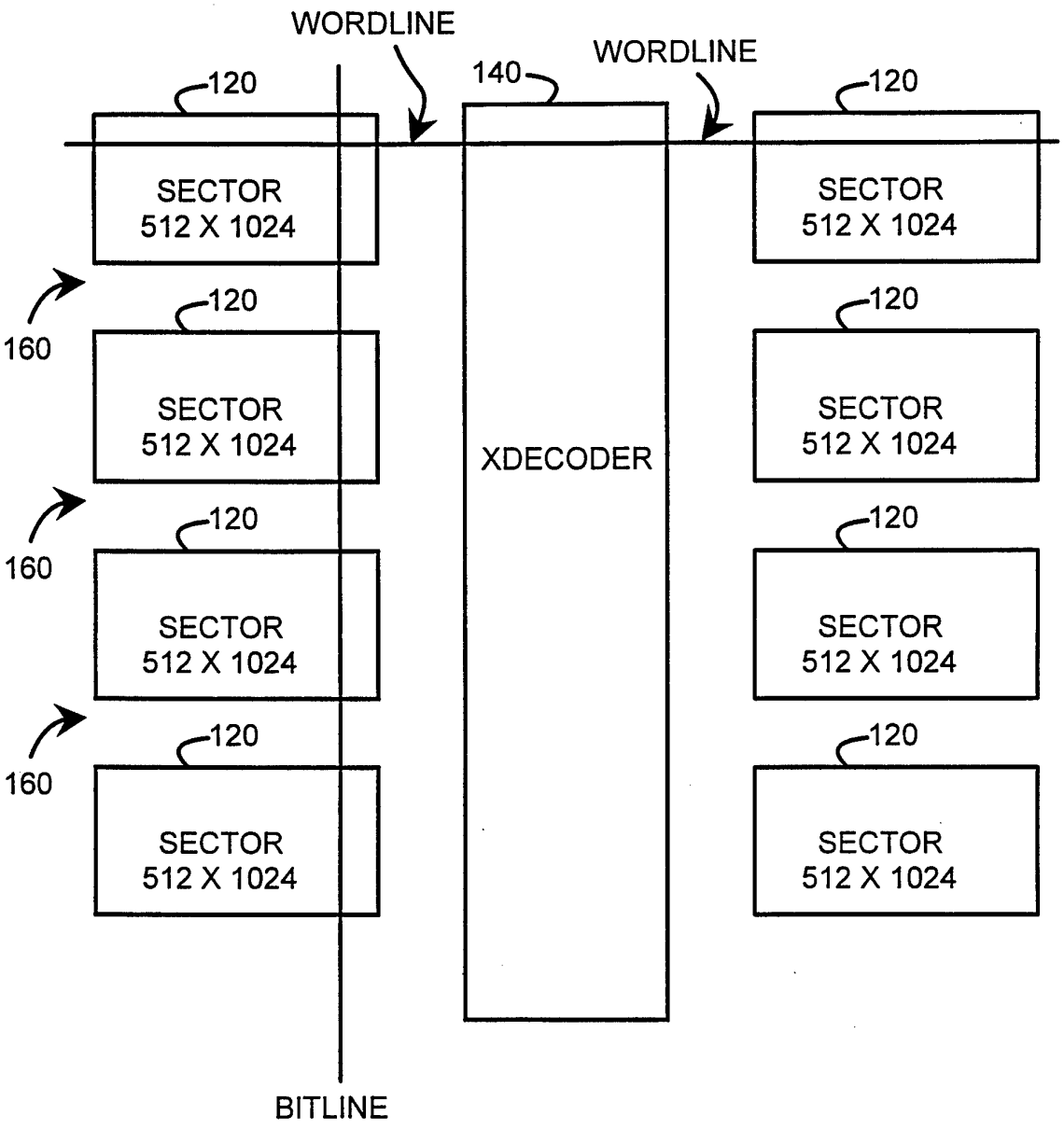
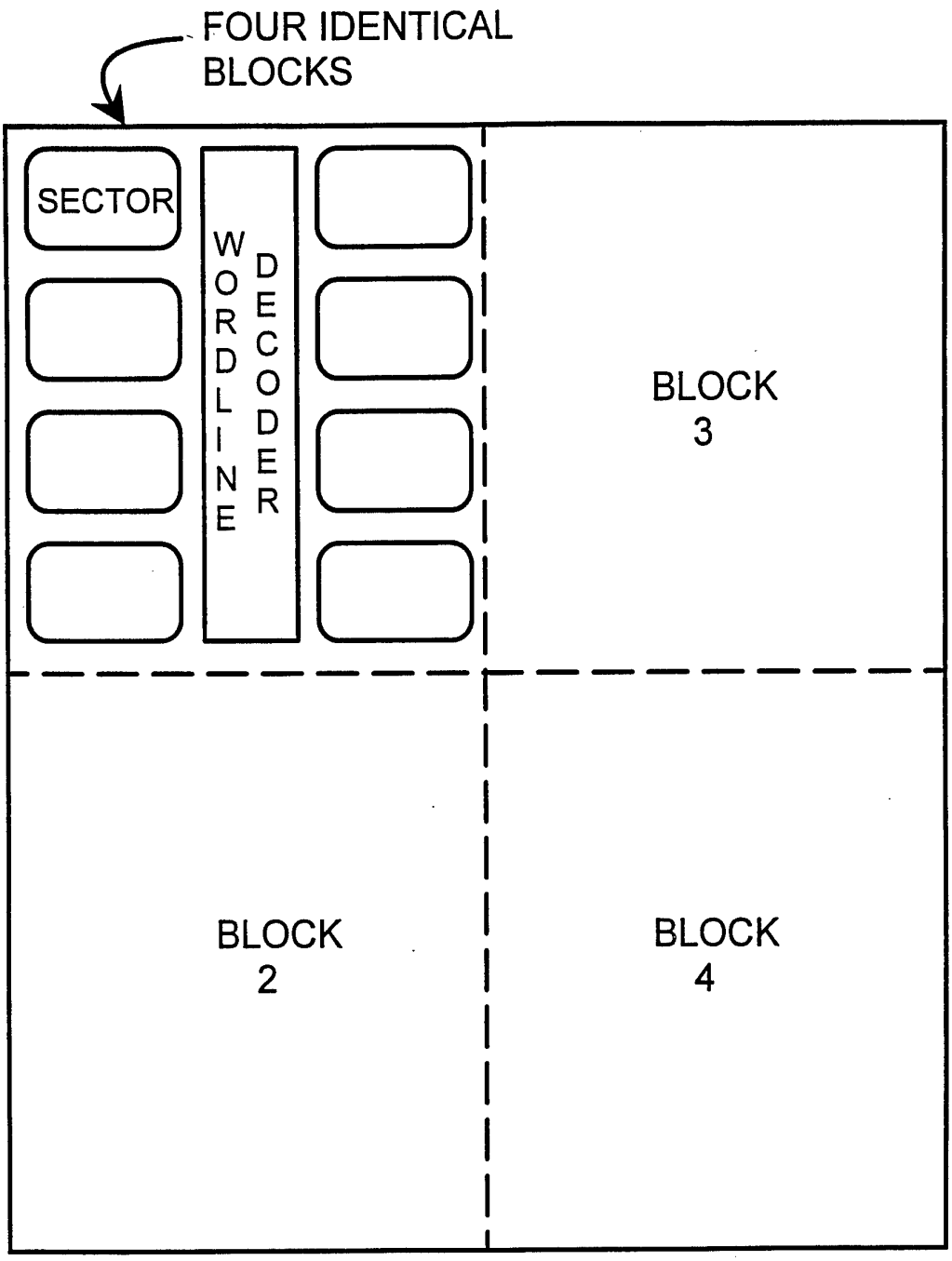

WORDLINE
WORDLINE
140
120
120
SECTOR
512 X 1024
SECTOR
512 X 1024
160
120
120
SECTOR
512 X 1024
XDECODER
SECTOR
512 X 1024
160
120
120
SECTOR
512 X 1024
SECTOR
512 X 1024
160
120
120
SECTOR
512 X 1024
SECTOR
512 X 1024
BITLINE

FIGURE 2



16 MEGABIT IMPLEMENTATION

FIGURE 3

INTERNATIONAL SEARCH REPORT

In' tional Application No
PCT/US 96/04253

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11C5/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, vol. 34, February 1991, NEW YORK US, pages 260-261, XP000238331 TAKESHI NAKAYAMA ET AL: "A 60ns 16Mb flash EEPROM with program and erase sequence controller"	1-3,5,6, 8
A	see figure 1	4,7

X	EP,A,0 550 751 (KABUSHIKI KAISHA TOSHIBA) 14 July 1993	1,5
A	see page 6, line 50 - page 7, line 6; figures 1,28,11	2-4,6-8

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 August 1996	05. 09. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Cummings, A

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 96/04253

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO,A,94 11880 (SILICON STORAGE TECHNOLOGY) 26 May 1994 see page 5, line 5 - page 7, line 2; figure 1A see page 13, line 15 - page 14, line 21; figure 2	1,5
A	EP,A,0 040 377 (TOKYO SHIBAURA DENKI KK) 25 November 1981 see page 8, line 26 - page 10, line 12; figure 1	1,5,6

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter ɔnal Application No
PCT/US 96/04253

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-550751	14-07-93	WO-A- 9205560	02-04-92
		JP-A- 5274894	22-10-93
		US-A- 5384742	24-01-95
WO-A-9411880	26-05-94	US-A- 5369609	29-11-94
		US-A- 5475634	12-12-95
EP-A-40377	25-11-81	JP-A- 56162860	15-12-81
		US-A- 4692785	08-09-87