United States Patent

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[31] **49,036/68**

[54] **ANALOG COMPUTING APPARATUS FOR PERFORMING SQUARE ROOTING, MULTIPLICATION AND LOGARITHMIC CALCULATION**
4 Claims, 3 Drawing Figs.

[52] **U.S. Cl.** **235/193,** 235/193.5, 235/194, 307/229, 320/1, 328/145
[51] **Int. Cl.** **G06g 7/20,** G06g 7/24
[50] **Field of Search** 235/193, 194, 195, 196, 193.5; 328/151, 160, 161, 145, 146; 307/246, 229; 320/1

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ABSTRACT: There is disclosed herein analogue computing apparatus comprising storage means so adapted that the value of a signal in the storage means may change as a function of time, an input to the storage means by means of which a first input signal may be applied to the storage means to determine a starting level for a stored signal therein, comparison means for comparing the stored signal with a second input signal, as the value of the stored signal changes with time, and providing a response when the compared signals have predetermined relationship, which will be after a time interval dependent (in a manner determined by the stored signal value/time characteristics of the storage means) on the first and second input signals, and converting means coupled to the comparison means and operable by said response to produce a signal related to the said time interval, which signal will thereby also be dependent on the first and second input signals.

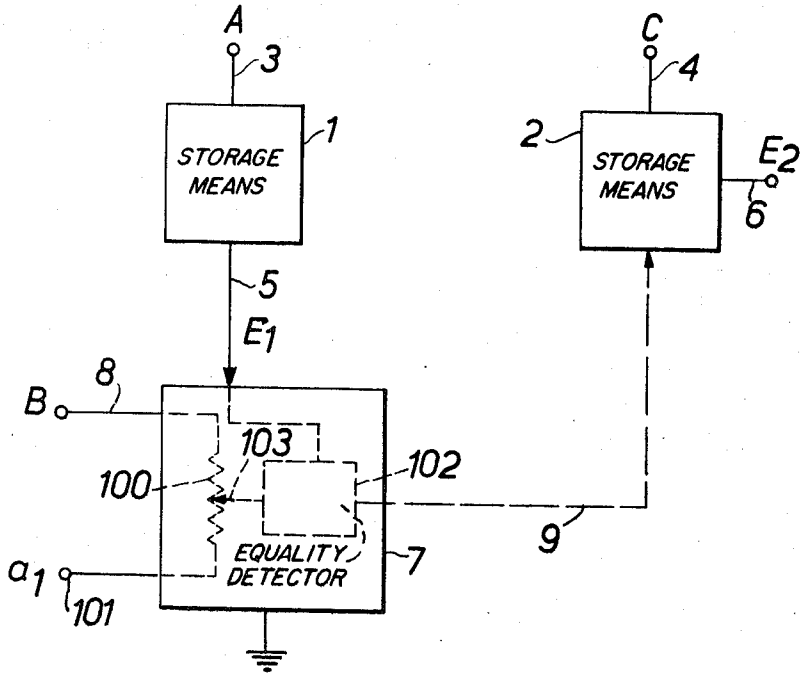
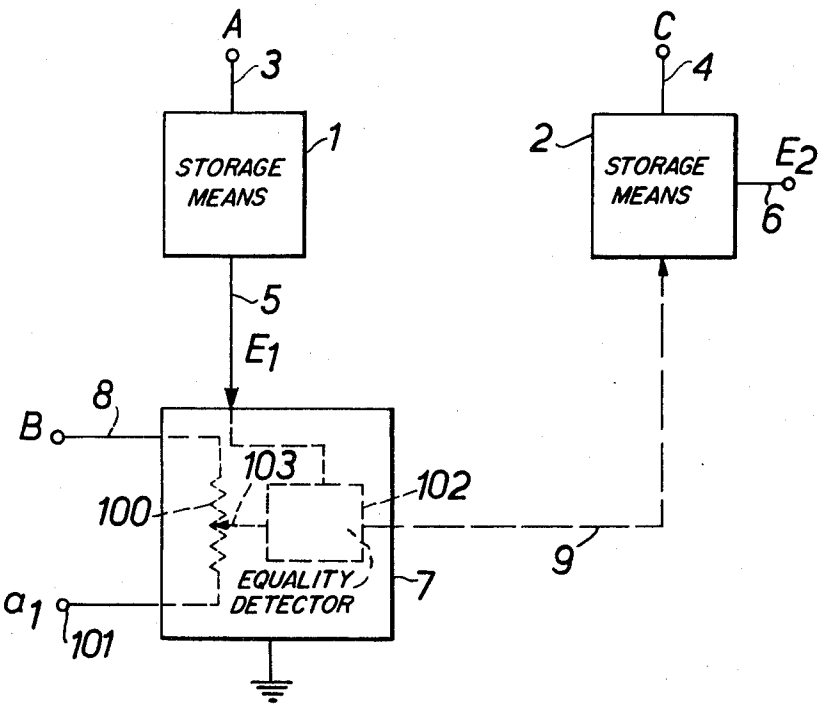


FIG.1.



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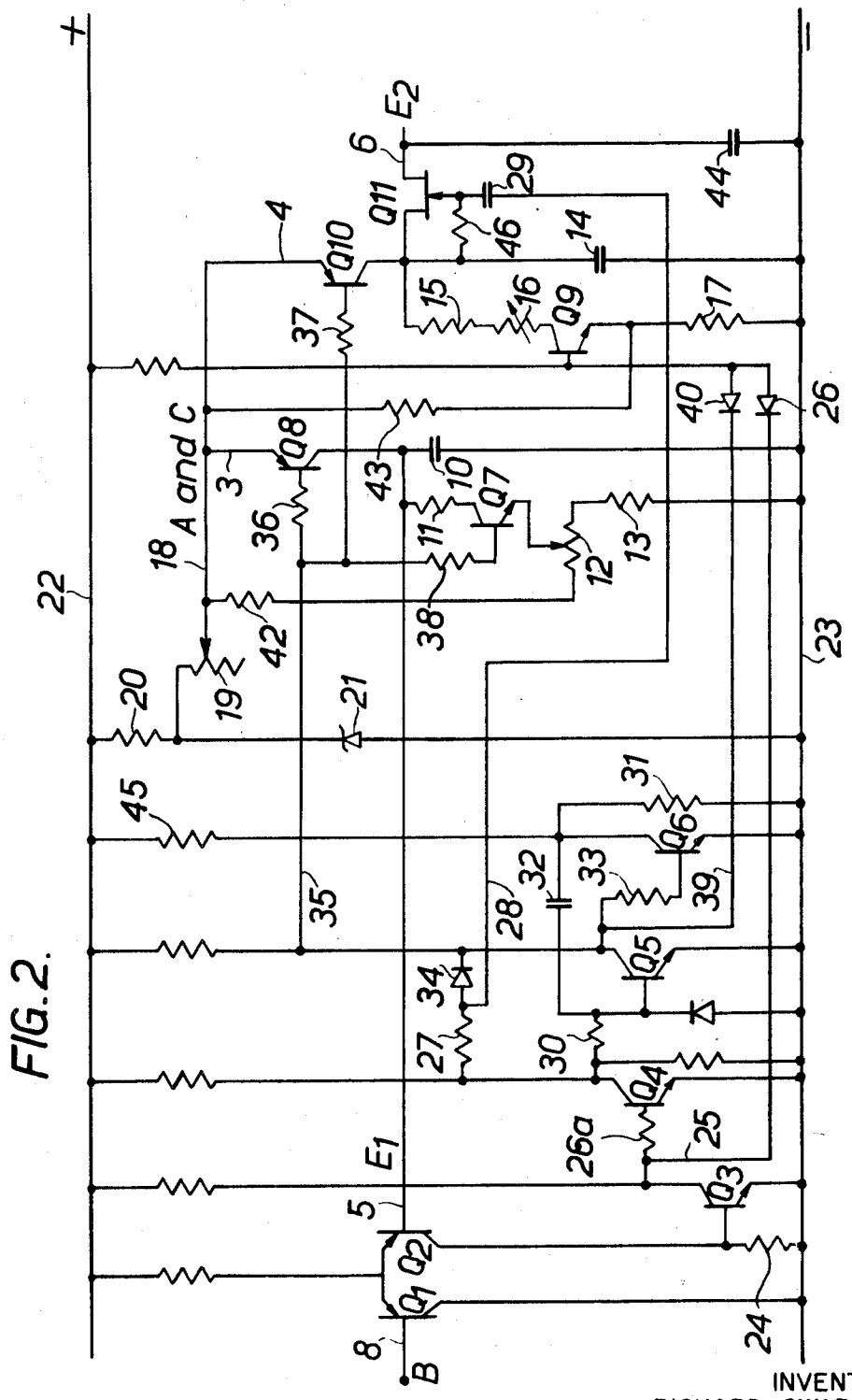

FIG. 2.

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FIG. 3.

INPUT(S) FIXED AT I_U	VARIABLE INPUTS	OUTPUT SIGNAL (E_2)	FUNCTION OF $\bar{A}$, $\bar{B}$, $\bar{C}$, REPRESENTED BY E_2	FUNCTION REPRESENTED WHEN N=1
A	C and B	$\frac{K(C-I_L)(B-I_L)^{1/N}}{(I_U-I_L)^{1/N}} + I_L$	$\bar{C} \cdot \bar{B}^{1/N}$	$\bar{C}\ \bar{B}$
C	A and B	$\frac{K(I_U-I_L)(B-I_L)^{1/N}}{(A-I_L)^{1/N}} + I_L$	$\frac{\bar{B}^{1/N}}{\bar{A}^{1/N}}$	$\frac{\bar{B}}{\bar{A}}$
A and C	B	$\frac{K(I_U-I_L)(B-I_L)^{1/N}}{(I_U-I_L)^{1/N}} + I_L$	$\bar{B}^{1/N}$	$\bar{B}$
A and B	C	$\frac{K(C-I_L)(I_U-I_L)^{1/N}}{(I_U-I_L)^{1/N}} + I_L$	$\bar{C}$	$\bar{C}$

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ANALOG COMPUTING APPARATUS FOR PERFORMING SQUARE ROOTING, MULTIPLICATION AND LOGARITHMIC CALCULATION

This invention relates to analogue computing apparatus.

Such apparatus is frequently required in systems, such as process control systems, where the values of one or more variables (which may be, for example, pressure or temperature), hereinafter referred to as data values, are converted into signals whose values represent the data values, and computations have to be performed on one ore more of the signals in order to derive a particular function which involves one or more of the data values.

According to the present invention analogue computing apparatus comprises storage means so adapted that the value of a signal in the storage means may change as a function of time, an input to the storage means by means of which a first input signal may be applied to the storage means to determine a starting level for a stored signal therein, comparison means for comparing the stored signal with a second input signal, as the value of the stored signal changes with time, and providing a response when the compared signals have a predetermined relationship, which will be after a time interval dependent (in a manner determined by the stored signal value/time characteristics of the storage means) on the first and second input signals, and converting means coupled to the comparison means and operable by said response to produce a signal related to the said time interval, which signal will thereby also be dependent on the first and second input signals.

The converting means may comprise second storage means, so adapted that the value of a signal in the second storage means may change as a function of time, and an input to the second storage means by means of which a third input signal may be applied to the second storage means to determine the starting level of a stored signal therein, the comparison means being coupled to the second storage means and the second storage means being operable by said response of the comparison means to terminate the change of the stored signal therein, whereby the resultant signal then in the second storage means will be dependent on all three input signals.

A preferred feature, which is incorporated in the particular embodiment described in detail below, is that the first and second storage means are such that their stored signals will change exponentially with time.

The first storage means may, however be such that its stored signal will change linearly with time and the second storage means may be such that its stored signal will change exponentially with time, such an arrangement allowing computation of the antilogarithm of the data value represented by the second input signal.

On the other hand, the first storage means may be such that its stored signal will change exponentially with time and the second storage means may be such that its stored signal will change linearly with time, such an arrangement allowing computation of the logarithm of the data value represented by the second input signal.

Where both storage means have exponential characteristics, the apparatus may also include:

(a) means for providing a first input signal having a predetermined value. In this case the resultant signal will represent the function $\bar{C}\cdot\bar{B}^{\frac{1}{N}}$ where $\bar{B}$ and $\bar{C}$ are data values represented by the second and third input signals respectively, and N is a number which is not necessarily a whole number.

or (b) means for providing a third input signal having a predetermined value. The resultant signal will represent the function

$$\frac{\bar{B}^{\frac{1}{N}}}{\bar{A}^{\frac{1}{N}}}$$

where $\bar{A}$ is a data value represented by the first input signal.

or (c) means for providing first and third input signals having predetermined values. The resultant signal will represent the function $\bar{B}^{\frac{1}{N}}$

or (d) means for providing first and second input signals having predetermined values. Resultant signal representing the function $\bar{C}$.

The manner is which these functions arise in the output signal will be explained in detail below.

N arises from having the time constant of the second storage means N times that of the first storage means (N not necessarily being a whole number nor necessarily greater than one).

Conveniently, the predetermined relationship between the third input signal and the decaying signal in the first storage means is equality.

In a particular embodiment of the invention, which is described below and which computes the square root of the second input signal, this simple relationship allows the resultant signal automatically to be produced on the same "live zero" signal scale as the second input signal. A "live zero" scale is one where the lower limit of the input signal, which represents a data value of zero, is not zero but a finite value, and systems using such a scale are commonly preferred for the transmission of analogue data signals. A scale commonly used is one where a current range of 4–20 milliamperes is used to represent the full range of data values from zero up to a selected maximum. In this scale, the current may be passed through a 250-ohm resistance to derive a corresponding 1–5 volt signal wherever a voltage signal may be required in the system.

The above distinction between data values (say $\bar{A}$, $\bar{B}$ and $\bar{C}$) and the respective signal values (which we may refer to as A, B and C) by which they are represented, should be recognized. It arises from the "live zero" system, in which a portion of the actual signal value is not in any way dependent on the data value but merely exists to bias the whole signal scale away from zero.

In general, a scaling factor must be introduced in order to automatically produce the resultant signal on the same "live zero" scale as the input signal or signals, where a "live zero" scale is being used, and in such a case preferably the said predetermined relationship is such as to introduce a scaling factor required to produce a resultant signal on the same signal scale as the variable input signal or signals.

In a particularly advantageous form of apparatus according to the invention, the means for providing the input signal or signals having a predetermined value provide said signal or signals having a value equal to the upper limit value of a "live zero" signal scale on which scale the variable input signal or signals may represent data values, and the apparatus may comprise means for setting equal datum levels for the changing stored signals in the two storage means, the datum levels having a value equal to the lower limit value of said "live zero" signal scale.

Alternatively, the means for providing the input signal or signals having a predetermined value provide said signal or signals having a value equal to the upper limit value of a "dead zero" signal scale on which scale the variable input signal or signals may represent data values, and the apparatus may comprise means for ensuring that the datum levels for the changing stored signals in the two storage means are zero. A "dead zero" scale is one where a zero data value is actually represented by zero signal.

Preferably the apparatus is electrical apparatus, in which the first and second storage means each comprise capacitance, coupled to the storage means input so as to be able to receive an input signal therefrom, and also resistance through which the capacitance may discharge thereby changing any voltage signal stored on it.

The comparison means may include two transistors in a long-tailed pair configuration.

In an embodiment described in detail hereinafter, a switching device is so connected into the resistance/capacitance circuit of the second storage means as to prevent or terminate decay of the voltage on the capacitance when the switching device is rendered nonconductive.

The comparison means may be adapted to provide an output signal when the compared signals have said predetermined relationship, and the apparatus may comprise means for rendering the switching device associated with the second storage means nonconductive in response to said output signal.

Preferably a switching device is similarly connected into the resistance/capacitance circuit of the first storage means.

The described embodiment also comprises respective input switching means through which the respective storage means are connected to their inputs, whereby the first and third input signals will be applied to the respective storage means when said input switching means are conductive.

A further feature which is preferably incorporated in apparatus in accordance with the invention, in any of the forms referred to above, is cycling means for repeatedly

a. applying the first and second input signals to the first and second storage means to set their starting levels.
b. then initiating the change of the signals in both storage means, and
c. after termination of the change of the signal in the second storage means reapplying the first and second input signals to the first and second storage means to initiate another cycle.

This enables the function to be computed repetitively so that as the variable input signal or signals varies the resultant signal is virtually continuously varied also so as to continuously represent the appropriate function of the varying input signal or signals.

In the described embodiment, the cycling means comprises a two-state circuit which is connected to the input switching means of both storage means and to the switching devices of both storage means in such manner that when in one state it provides signals to render the input switching means nonconductive and the switching devices conductive, whereby the first and third input signals are not applied to the storage means while the signals in the latter decay, the two-state circuit having an input connected to the output of the comparison means whereby the output signal of the comparison means will place the two-state circuit in its other state, wherein it provides output signals to render the input switching means conductive and the switching devices nonconductive, so that the signals in the storage means are not able to decay while the first and third input signals are being applied to them to set their starting levels.

The two-state circuit may also be further provided with means for delaying its response to the output signal of the comparison means.

Preferably also, gating means is provided for gating the said resultant signal from the second storage means to an output of the apparatus, the gating means and the switching device of the second storage means being connected to respond immediately to the output signal from the comparison means, whereby the delaying means of the two-state circuit allows the decay of the signal in the second storage means to be terminated and the resultant signal to be gated to the apparatus output before the input switching means are rendered conductive.

In order that the invention may be more clearly understood, embodiments in accordance with it will now be described, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram of one form of computing apparatus in accordance with the present invention,

FIG. 2 is a circuit diagram of a practical embodiment for continuously computing a root or power function, and

FIG. 3 is a table which shows how a selection of other functions may be computed.

It is convenient first to consider in general the requirements of any form of analogue computing apparatus which is to do a computation of the form

$$\frac{\overline{C}\times\overline{B}^{\frac{\cdot}{\overline{N}}}}{\overline{A}^{\frac{\cdot}{\overline{N}}}}$$

where $\overline{A}$, $\overline{B}$ and $\overline{C}$ are "data values" (for example, pressure or temperature values) which are represented by respective signals having values A, B and C on a "live zero" scale (and n is not necessarily a whole number and so may be a fraction), and to produce an output signal representing the function on the same "live zero" scale.

In general, take the upper and lower limits of the "live zero" scale to be I_U and I_L respectively. The logical sequence of operations then required in order to derive the required output signal is:

(a) Subtract I_L from each input signal—giving $(A-I_L)$, $(B-I_L)$ and $(C-I_L)$

(b) Take the required function—giving

$$\frac{(C-I_L)\ (B-I_L)^{\frac{\cdot}{\overline{n}}}}{(A-I_L)^{\frac{\cdot}{\overline{n}}}}$$

(c) Multiply by a scaling factor K—giving

$$\frac{K(C-I_L)\ (B-I_L)^{\frac{\cdot}{\overline{n}}}}{(A-I_L)^{\frac{\cdot}{\overline{n}}}}$$

(d) Add I_L to the result—giving

$$\frac{K(C-I_L)\ (B-I_L)^{\frac{\cdot}{\overline{n}}}}{(A-I_L)^{\frac{\cdot}{\overline{n}}}}+I_L \qquad (1)$$

which is a signal representing $\frac{\overline{C}\times\overline{B}^{\frac{\cdot}{\overline{n}}}}{\overline{A}^{\frac{\cdot}{\overline{n}}}}$ on the same "live zero" scale.

We will revert to the above derivation after considering the apparatus shown in FIG. 1. Referring to FIG. 1, first and second storage means are shown at 1 and 2, respectively the storage means having respective inputs 3 and 4 by means of which input signals A and C can respectively be applied to them to set the storage means at starting levels A and C respectively. The storage means are passive components and are so adapted that the value of a signal in either of them may change, from its starting level, as a function of time. The changing signals, E_1 and E_2, are provided on output connections 5 and 6.

Comparison means 7 is connected to the output connection 5 of the first storage means 1 and also has an input 8 to which an input signal B is applied. Comparison means 7 operates to compare the level of the changing signal E_1 in the first storage means 1 with the input signal B. The input signals A, C and B are respectively the first, third and second input signals hereinbefore referred to.

An operative coupling 9 is shown in broken lines, through which the comparison means 7 operates to terminate the change of the signal E_2 in the second storage means 2 when the compared signals E_1 and B have a predetermined relationship. Most simply, this occurs when the compared signals are equal. The resultant signal E_2 then present in the second storage means 2 will then be dependent on all three input signals A, B and C, in a manner which will shortly be explained.

Preferably, as in the embodiment which will be described in detail with reference to FIG. 2, the storage means 1 and 2 have exponential characteristics.

By the expression "exponential characteristic," we mean a characteristic having the general form

$$E=(E_o-a)\ e^{-t/T}+a$$

where E is the value of the stored signal in the storage means at time t.

E_o is the starting level of the stored signal

a is a datum level of the stored signal, beyond which it will not change further owing, for instance, to the application of a bias signal to the storage means (as in the practical embodiment to be described).

e is the base of the natural logarithms, and

T is a time constant for the storage means.

The changing stored signals in the two storage means at time t may then be written as

$$E_1=(A-a_1)e^{-t}/T_1+a_1$$

and

$$E_2=(C-a_2)e^{-t}/t_2+a_2$$

where the suffixes **1** and **2** relate to the first and second storage means, respectively, and provided of course that the changes are started simultaneously.

We can consider that T_2 is equal to $N\,T_1$ (where N may be, but is not necessarily, a whole number, and so could be a fraction). Assuming that the comparison means **7** terminates the change of the signal (E_2) in the second storage means **2** when the signal (E_1) in the first storage means **1** is actually equal to the third input signal (C), then at that time

$$B=(A-a_1)e^{-t}/T_1+a_1$$

and

$$E_2=(C-a_2)e^{-t}/NT_1+a_2$$

Taking the Nth root of the first of the above equations, and eliminating e^{-t}/NT_1, we have

$$E_2=\frac{(C-a_2)(B-a_1)^{\frac{1}{N}}}{(A-a_1)^{\frac{1}{N}}}+a_2 \qquad (2)$$

The similarity of equations (1) and (2) should be noted. In fact, it can be seen that if, in the apparatus of FIG. **1**, N is made equal to n of the required function, the datum levels a_1 and a_2 are both made equal to the lower scale limit I_L, and the signals A, B and C are applied to the apparatus as the first, second and third input signals, respectively only the factor K remains to prevent the equations becoming identical. This may be achieved by arranging the comparator so that, instead of producing its output signal when its two input signals (E_1 and B) are equal, this occurs when $E_1=K^N(B-a_1)+a_1$. This may be arranged by giving the comparator an input circuit (as shown in broken lines in FIG. **1**) which comprises a potentiometer **100** connected at one end to the B input terminal and at the other to a terminal **101** held at the voltage a_1, and an equality detecting circuit **102** which has one input connected to receive the signal E_1 from the first storage means, and an other input connected to a slider **103** on the potentiometer. The slider position may then be adjusted to produce the factor K^N in the signal tapped off by the slider.

With such an arrangement, correspondence has been established between the resultant signal E_2 and the ideal signal represented in equation (1), so that the apparatus will automatically compute a signal E_2 which represents, on the same "live zero" scale as the input signals, the function

$$\frac{D\times B^{\frac{1}{n}}}{A^{\frac{1}{n}}}$$

It has been assumed above that A, B and C are all variable signals and that the output is to be a function of all of them. In fact, any one or two of these input signals may be made constant, so that the output signal will only vary with the remaining two, or one, of the input signals. It can be shown that, in order to then preserve the desirable feature of producing the output signal automatically on the same "live zero" scale as the input signals, it is necessary to set any input signals, which are to be constant, at a value of I_t, the upper scale limit.

FIG. **3** is a table which shows the form of the function computed when a selection of single ones of combinations of the input signals A, B and C are given the fixed value I_t. It is assumed, as before, that the input signals A, B, C, where they are not fixed, represent, on a live zero system, data values $\overline{A}$, $\overline{B}$ and $\overline{C}$ respectively.

It can be seen from FIG. **3** that the apparatus will compute a signal representing, for example, the product (col. 5 row 1), or quotient (col. 5 row 2) of two variables. Referring to column 4, row 3, of FIG. **3**, it can be seen that with a single variable if $N>1$ the Nth root is computed, or if $N<1$ the Nth power is computed. In addition, of course, if all three inputs are variable, and N is made equal to unity, the function

$$\frac{D\times B}{A}$$

is computed.

It should here be mentioned that the apparatus described above with reference to FIG. **1** is subject to the limitation that A should be greater than B, so that the quotient computation (row 2 in FIG. **3**), which involves variation of both A and B, will only be performed effectively so long as $A>B$. For the same reason, if B alone, or both C and B, are fixed and the other(s) allowed to vary, operation on a consistent "live zero" scale is precluded.

The above examples are among the most commonly required forms of function, and the apparatus will (subject to the limitation referred to above) compute signals which represent any one of them on the same "live zero" scale as the input signals, provided the variable input signal or signals is or are applied to the appropriate inputs, the fixed input signals are set at the value I_t, and the base levels are set at the value I_L.

It will be apparent from the foregoing description that for a "dead zero" system, i.e., where a zero data value is actually represented by a zero value signal (that is to say $I_L=0$) the datum levels a_1 and a_2 may be set to zero. In that case the output signal E_2 will have a simpler form, as can be seen by setting I_L equal to zero in the third column of FIG. **3**, but the functions represented will still be as indicated in the fourth and fifth columns and will be on the same "dead zero" scale ($0-I_t$) as the input signals. With $a_1=0$ the comparator should operate, in general, when $E_1=K^NB$. This can be achieved simply by having a comparator with an input circuit which multiplies B by K^N.

If, instead of setting any nonvariable input signal to a value I_t, which was said to be necessary in order to produce an output signal on the right scale, they are set to a different constant value, then the effect is to produce an output signal which is on a scale related to, but not identical with, the scale of the variable input signals.

Referring now to FIG. **2** of the drawings, which shows a circuit, in accordance with the invention, which includes means for internally providing input signals A and C which have equal predetermined values, and for setting the datum levels also to equal predetermined values. The circuit thus performs the Nth root function, to which the third row of FIG. **3** relates, and in fact the circuit components which determine the storage means time constants have been chosen to make N equal 2, so as to compute the square root. The circuit is intended to operate in a 4–20 milliamperes (or 1–5 volts) "live zero" system so the first and second input signals are set at 5 volts while the datum levels are set at 1 volt.

In this particular instance, then $N=2$, $I_t=5$ volts, and $I_L=1$ volt. Substituting these values in the equation of the fourth row of FIG. **3** gives

$$E_2=\frac{4K(B-1)^{\frac{1}{2}}}{2}+1$$

It is known that when $B=5$ volts, E_2 must equal 5 volts. Substituting these values in the above equation, it is found that K must be unity. Consequently the comparator **7** can in this case merely be an equality detector, thus making $K=1$, yet the apparatus will still compute an output signal on the same "live zero" scale as the input signal.

Now, relating FIG. **2** to FIG. **1**, the first storage means **1** comprises a capacitor **10** in parallel with resistors **11**, **12** and **13**. The voltage signal on capacitor **10** can decay when a transistor Q_7, between resistors **11** and **12**, is conductive,

thereby allowing the capacitor **10** to discharge exponentially through the resistors.

The second storage means comprises a capacitor **14** in parallel with resistors **15**, **16** and **17**. A transistor Q_9 is connected between resistors **16** and **17** and, when conductive, allows the voltage on capacitor **14** to decay in a similar manner.

The input connections **3** and **4** to the respective storage means are connected in common to a line **18** which derives a voltage from a tapped resistor **19** which is connected to the junction between a resistor **20** and a Zener diode **21**. The latter two components are connected in series between power supply lines **22**, **23** so that Zener diode **21** (which nominally provides 6.6 volts) establishes a stable voltage from which a 5 volt signal can be applied to connections **3** and **4** by suitably adjusting the tapping on resistor **19**. The 5 volt signals on connections **3** and **4** are *A* and *C* respectively, so that these two input signals are internally provided in this instance. These signals are applied to the capacitors **10** and **14** of the respective storage means when transistors Q_8 and Q_{10}, connected into connections **3** and **4** respectively, are rendered conductive.

The comparator **7** comprises two transistors Q_1 and Q_2 connected as a long-tailed pair in a generally known manner so as to form an equality detector. Input connection **8**, to which the second, and variable, input signal *B* is to be applied, is connected to the base of Q_1, while a line **5** connects the base of Q_2 to the capacitor **10** in the first storage means. Hence Q_2 will be cut off so long as E_1, the voltage on capacitor **10**, is greater than *B*, but will conduct as soon as E_1 decays to a level equal to *B*.

The remainder of the circuit can conveniently be described in conjunction with a description of one cycle of operation of the circuit. Since the operation is cyclic it is convenient to assume arbitrarily a starting point where both capacitors **10** and **14** have been charged to their starting level of 5 volts. They then start to discharge (transistors Q_7 and Q_9 being at this time conductive, while transistors Q_8 and Q_{10} are nonconductive) at rates which depend on the time constants of the RC combinations mainly consisting of components **10**, **11**, **12**, **13** and **14**, **15**, **16**, **17**. The values of components **42**, **43**, **19**, **20** and **21** also have an effect on these time constants which is very small owing to their very small values in relation to resistors **11** and **15**. In this circuit, which is intended to compute a square root function, *N* should be equal to 2, i.e., if the capacitors **10**, **14** are equal, the total value of resistors **15**, **16** and **17** should be twice that of resistors **11** and **13** and the operative portion of resistor **12**. The capacitor values could, of course, be varied also, or instead, to obtain the desired value of *N*.

As soon as E_1, the decaying voltage on capacitor **10**, becomes equal to *B*, Q_2 conducts, hence producing an output signal from the comparator across a resistor **24** in the collector circuit of Q_2.

This output signal is applied to the base of transistor Q_3 in a switching circuit. Q_3 therefore conducts and its collector voltage drops to the negative supply voltage on line **23**. This voltage drop is applied by line **25** through a diode **26** to the base of Q_9, which immediately stops conducting thus terminating the decay of the voltage on capacitor **14** of the second storage means. The same voltage drop is applied through a resistor **26***a* to the base of Q_4 and cuts it off so that a voltage rise occurs at the collector of Q_4. This voltage rise is applied through a resistor **27**, line **28** and capacitor **29** to the base of Q_{11}, which then conducts to allow the resultant voltage signal E_2 on capacitor **14** to be provided on output connection **6**.

Transistors Q_5 and Q_6 in the switching circuit form the active elements of two-state circuit which has one state in which Q_6 is conductive and Q_5 nonconductive. However, the aforementioned voltage rise at the collector of Q_4 is applied also through a resistor **30** to the base of Q_5, which switches the two-state circuit to its other state in which Q_5 conducts and Q_6 does not, because of the voltage drop then applied to the base of Q_6 through resistor **33**. As Q_5 conducts, the line **28** is put back to the negative supply voltage on line **23** by conduction of a diode **34**, so that conduction of Q_{11} is terminated. However, a delay occurs between the initiation and termination of conduction of Q_{11} owing to the provision of a RC delay circuit which includes a capacitor **32** and also the resistor **30**, which delays the application of the voltage rise through resistor **30** to the base of Q_5. This delay allows the output signal E_2 to be provided on connection **6** for a sufficient time for it to be transferred to an output capacitor **44** which will provide a continuous output voltage which will represent the desired function (in this case the square root) of the data value ($\overline{B}$) represented by the variable input signal B.

As Q_5 conducts, not only does it cut off Q_{11}, but it also applies a voltage drop through a line **35** and respective resistors **36**, **37** and **38** to the bases of Q_8, Q_{10} and Q_7, causing Q_8 and Q_{10} to conduct, so that capacitors **10** and **14** start being charged up to their starting level of 5 volts again, and causing Q_7 to become nonconductive so that capacitor **10** cannot discharge through it.

Q_9 would be rendered conductive again as capacitor **14** charges to a voltage above *B*, since the comparator output would then cease. In order to avoid this, which would prevent proper recharging of capacitor **14**, a line **39** is connected from the collector of Q_5 through a diode **40** to the base of Q_9. Thus, even when the comparator output ceases Q_5 will be maintained in conduction by capacitor **32** for sufficient time to keep Q_9 nonconductive throughout the full recharging of capacitor **14**.

After capacitors **10** and **14** have recharged to 5 volts, in a time determined by capacitor **32** and resistors **45** and **31**, Q_5 will revert to its normal nonconductive state, Q_6 becoming conductive, and hence Q_8 and Q_{10} will be rendered nonconductive, and Q_7 rendered conductive, by the resultant positive signal on line **35**, while Q_9 will be rendered conductive by the resultant positive signal on line **39**. Thus both capacitors start to discharge again, this being the beginning of the next computing cycle. A resistor **46** is shown, which has a very high value and is intended to prevent buildup of charge on the gate of Q_{11}.

Referring to the earlier part of this description, datum levels a_1 and a_2 were there referred to. In the circuit of FIG. **2**, the resistors **12** and **13** of the first storage means form part of a resistor chain **42**, **12**, **13** between the 5-volt line **18** and the negative supply line **23**. Similarly a resistor **43** is connected in series with resistor **17** of the second storage means to form a chain between lines **18** and **23**. The resistance values in these chains are selected and adjusted so that the capacitor voltages cannot decay below 1 volt. In this way the datum levels a_1 and a_2 are both made equal to I_L, the lower limit of the "live zero" scale, as already discussed with reference to FIG. **1**.

It will be appreciated that the storage means in this particular circuit have been given exponential decay characteristics so related that *N* is equal to 2, *A* and *C* have both been made equal to $I_{L'}$ (5 volts), and a_1 and a_2 have both been made equal to I_L (1 volt). Referring to the third row of FIG. **3**, it is evident that the resultant signal E_2, provided intermittently at output connection **6** and across capacitor **44**, represents on the 1–5 volt "live zero" scale the square root of the data value represented by the third input signal B applied at input **8**, if the latter is also on the 1–5 volt "live zero" scale.

Substantially the same circuitry as is shown in FIG. **2** may be used to derive any others of the functions shown in FIG. **3**.

If, for instance, *A* or *C* are to be variable signals, the appropriate storage means input connection **3** or **4** will be detached from the line **18** and connected instead to a source of the variable voltage signal (*A* or *B*) which is to contribute to the output function. As this voltage signal varies, so the capacitor in the respective storage means will become charged to slightly different starting levels in successive cycles of operation, and hence the variable voltage will have its effect on the output signal E_2 in accordance with the above equations and the table of FIG. **3**.

If *B* is to be nonvariable (equal to 5 volts, for example, if

operating on the 1–5 volt scale) it will be connected to a constant voltage source, such as line **18**.

The datum levels of the storage means can be made equal to zero, for operation on a "dead zero" scale, by having an open circuit in place of resistors **42** and **43**, so that no bias voltage will be applied to the capacitors **10** and **14**.

It will be appreciated that a more complex form of constant voltage supply may be provided if the accuracy of the circuit is required to be greater.

It can be seen from FIG. **3** that if N is made less than 1, the power of the data values, instead of their roots, will appear in the output function. For example, with $N=\frac{1}{2}$, the arrangement referred to in the third row of the table, which is the same arrangement as shown in detail in FIG. **2**, will produce a signal representing the square of B.

It will now be appreciated that in the apparatus described with reference to FIGS. **1** and **2**, the first storage means and the comparison means act in conjunction to delineate a time interval which is dependent on both the first and second input signals A and B, and also on the stored signal value/time characteristics of the first storage means. The second storage means then operates to convert this time interval into an output signal which is related to the value of the time interval, and hence is also dependent on A and B.

When the second storage means has an exponential stored signal value/time characteristic, as described, then it itself introduces a further factor to the function computed. The second storage means may, however, to be given a linear characteristic, by providing a constant-current discharge path for the storage capacitor **10**. Constant-current arrangements are well known, and it is not considered necessary to describe any in detail here.

The effect then is, assuming that the comparator gives its output signal when equality is detected and the datum level is set to zero, that the comparator produces an output signal when

$$B=Ae^{\frac{-t}{T_1}}$$

so that

$$\log_e \frac{B}{A}=\frac{-t}{T_1}$$

If also the second storage means is arranged to start from the zero datum level and charge towards, C, then $E_2=k\ C\ t$, where k is a constant.

Consequently, when the change in E_2 is terminated,

$$E_2=-kCT_1 \log_e \frac{B}{A}=kCT_1 \log_e \frac{A}{B}$$

Thus in this form, assuming C and B are held constant the apparatus will compute a voltage representing the natural logarithm of A. Here the conversion of time interval to output signal is done linearly. Other logarithms to any base can be computed by appropriate choice of k and T_1.

An antilogarithm computation may be done by giving the first storage means a linear characteristic and the second storage means an exponential one.

Then $E_1=A-k'At$ (k' being a constant) so that when the change in E_2 is terminated,

$$B=A(1-k't) \text{ or } t=\frac{A-B}{k'A}$$

Now

$$E_2=Ce^{-t/T_2}$$

$$=Ce\left(\frac{B-A}{k'AT_2}\right)$$

or

$$E_2=C \text{ antilog}_e \left(\frac{B-A}{k'AT_2}\right)$$

Hence, keeping A and C constant, this arrangement will compute a signal representing the natural antilogarithm of B.

Other antilogarithms to any base can be computed by appropriate choice of k' and T_2.

We claim:

1. Analog computing apparatus comprising storage means so adapted that the value of a signal in said storage means may change of the function of time, said storage means having an input by means of which a first input signal may be applied to said storage means to determine a starting level for a stored signal therein, comparison means coupled to said storage means for comparing said storage signal with a second input signal, as the value of the said stored signal changes with time, and providing a response when the compared signals have a predetermined relationship, which will be after a time interval dependent (in a matter determined by the stored signal value/time characteristics of said storage means) on said first and second input signals, and converting means coupled to said comparison means and operable by said response to produce a signal related to the said time interval, which signal will thereby also be dependent on said first and second input signals, said converting means including second storage means, so adapted that the value of a signal in said second storage means may change as a function of time, and an input to said second storage means by means of which a third input signal may be applied to said second storage means to determine the starting level of a stored signal therein, said comparison means being coupled to said second storage means and said second storage means being operable by said response of said comparison means to terminate the change of the stored signal therein, whereby the resultant signal then in said second storage means will be dependent on all three input signals, said first and second storage means are such that their stored signals will change exponentially with time, means for providing a first input signal having a predetermined value, said predetermined relationship between said second input signal and the stored signal in said first storage means is equality, said means for providing the input signal or signals having a predetermined value provide said signal or signals having a value equal to the upper limit value of a "live zero" signal scale on which scale the variable input signal or signals may represent data values, and including means for setting equal datum levels for the changing stored signals in the two storage means, the datum levels having a value equal to the lower limit value of said "live zero" signal scale.

2. Analog computing apparatus comprising storage means so adapted that the value of a signal in said storage means may change of the function of time, said storage means having an input by means of which a first input signal may be applied to said storage means to determine a starting level for a stored signal therein, comparison means coupled to said storage means for comparing said storage signal with a second input signal, as the value of the said stored signal changes with time, and providing a response when the compared signals have a predetermined relationship, which will be after a time interval dependent (in a matter determined by the stored signal value/time characteristics of said storage means) on said first and second input signals, and converting means coupled to said comparison means and operable by said response to produce a signal related to the said time interval, which signal will thereby also be dependent on said first and second input signals, said converting means including second storage means, so adapted that the value of a signal in said second storage means may change as a function of time, and an input to said second storage means by means of which a third input signal may be applied to said second storage means to determine the starting level of a stored signal therein, said comparison means being coupled to said second storage means and said second storage means being operable by said response of said comparison means to terminate the change of the stored signal therein, whereby the resultant signal then in said second storage means will be dependent on all three input signals, said first and second storage means are such that their

stored signals will change exponentially with time, means for providing a first input signal having a predetermined value, said predetermined relationship between said second input signal and the stored signal in said first storage means is equality, said means for providing the input signal or signals having a predetermined value provides said signal or signals having a value equal to the upper limit value of a "dead zero" signal scale on which scale the variable input signal or signals may represent data values, and comprising means for ensuring that the datum levels for the changing stored signals in the two storage means are zero.

3. Apparatus according to claim 1 including cycling means for repeatedly

a. applying the first and second input signals respectively to the first and second storage means to set their starting levels,

b. then initiating said change of the stored signals in both storage means, and

c. after termination of the change of the stored signal in the second storage means reapplying the first and second input signals respectively to the first and second storage means to initiate another cycle.

4. Apparatus according to claim 2 including cycling means for repeatedly

a. applying the first and second input signals respectively to the first and second storage means to set their starting levels,

b. then initiating said change of the stored signals in both storage means, and

c. after termination of the change of the stored signal in the second storage means reapplying the first and second input signals respectively to the first and second storage means to initiate another cycle.