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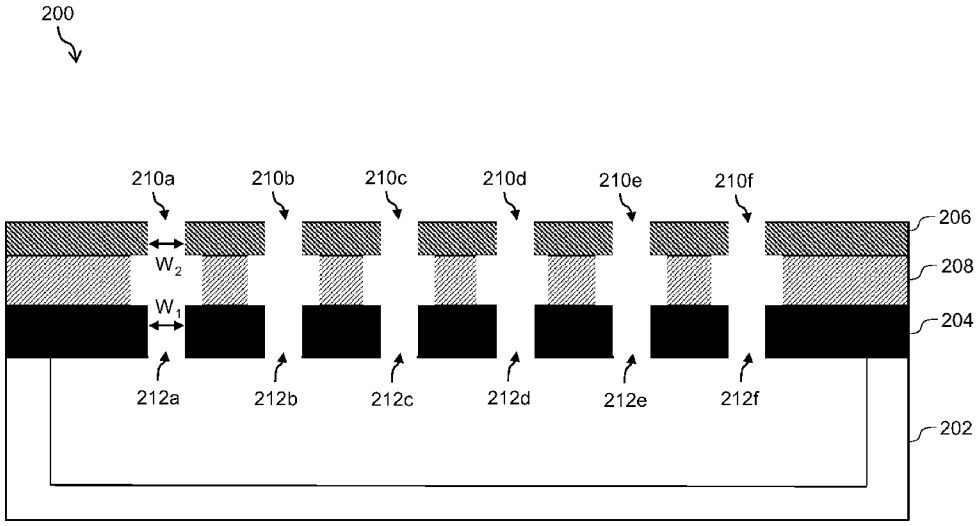

FIG. 2

(57) **Abstract:** In some embodiments, a self-aligned electrospray device can include a silicon wafer, a fluid reservoir, and a circuit. The silicon wafer can have a layer of electrically insulating material deposited on a top surface and a deposited layer of electrically conducting material. The silicon wafer and the deposited layers can have through holes. The electrically insulating layer may be undercut. The fluid reservoir can be mounted to a bottom surface of the silicon wafer for containing fluid. The circuit can provide an electric potential difference and be coupled between the layer of electrically conducting material and the fluid reservoir.

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[Continued on next page]

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SELF-ALIGNED ELECTROSPRAY DEVICE AND RELATED MANUFACTURING TECHNIQUES

BACKGROUND

[0001] Electrosprays are aerosols of charged particles (droplets, or ions) that are electrostatically extracted from an electrically conductive liquid. As shown in Figure 1, an electrospray device 100 can include an array of emitters 110a, 110b, etc. (110 generally) and an extractor 106. Emitters 110 provide the source of the ions, generally as holes in a fluid reservoir or tank 102, and are electrically isolated from the extractor 106. The extractor 106 is electrically conductive and contains holes or apertures 112a, 112b, etc. For proper operation of the device 100, each emitters 110a, 110b, etc. must be aligned with a respective one of the apertures 112a, 112b, etc. Applying an electric potential between the extractor 106 and a conductive fluid 120 in the reservoir 102 causes a Taylor cone 122 to form in the space between the extractor 106 and each emitter 110 so that ions exit each aperture 112 as an aerosol.

[0002] Microfabricated electrospray devices are used in many fields, including, among others: chemical and biochemical analysis for mass spectrometry, focused ion beam instruments (as a liquid metal ion source), low thrust electric propulsion (e.g. satellite propulsion), deposition instruments for nanoscale structures (e.g. textiles, highly porous drug carriers, and nebulizers), and ambient atmospheric charge neutralizers.

[0003] Existing microfabricated electrospray devices are formed as microelectromechanical systems (MEMS) using appropriate techniques known in the art. These systems include the fluid reservoir and emitters on one wafer, and the extractor with apertures on another wafer, where the two wafers are carefully bonded, so the emitters and apertures align.

SUMMARY OF DISCLOSED EMBODIMENTS

[0004] As shown in Figure 1, with existing electrospray devices 100 and manufacturing techniques, it is common for misalignment of apertures 112 and

emitters 110 to occur causing aerosol to be physically intercepted by the device, reducing the efficiency of the device or even rendering it inoperable. For example, misalignment between a first aperture 112a and a corresponding first emitter 110a can cause aerosol 122 to be physically intercepted by an underside of extractor 106, as illustrated in Figure 1.

[0005] Disclosed embodiments avoid misalignment by providing self-aligning electrospray devices, in which the fabrication technique ensures that emitters are precisely aligned with extractor apertures.

[0006] Thus, a first embodiment is a self-aligned electrospray device. The device includes a silicon wafer that provides the emitters. The silicon waver has, deposited on a top surface thereof, a layer of electrically insulating material the provides a physical gap between the emitters and the extractor. Deposited thereon is a layer of electrically conducting material, which provides the extractor. The silicon wafer and the deposited layers have openings or through-holes provided therein to permit passage of the aerosol, and the electrically insulating layer is undercut to promote formation of a Taylor cone. The device further includes a fluid reservoir, coupled to a bottom surface of the silicon wafer, for containing fluid. The device also includes a circuit, for providing an electric potential difference, coupled between the layer of electrically conducting material and the fluid reservoir.

[0007] A second embodiment is a method of making a self-aligned electrospray device. The method includes forming a silicon wafer having deposited or otherwise disposed on a first or top surface thereof a layer of electrically insulating material. A layer of electrically conducting material is deposited or otherwise disposed on the electrically insulating material. The silicon wafer and the deposited layers have through holes. The method next includes undercutting the electrically insulating material. The method then includes mounting or otherwise coupling a bottom surface of the silicon wafer to a fluid reservoir for containing fluid. The method further includes providing a circuit, for providing an electric potential difference, between the layer of electrically conducting material and the fluid reservoir.

[0008] In some embodiments, forming the silicon wafer and the deposited layers comprises using a Bosch (or Bosch-like) technique. Such embodiments include depositing, on the top surface of the silicon wafer, the layer of electrically insulating material; depositing, on the electrically insulating material, the layer of electrically conducting material; depositing, on the layer of electrically conducting material, a layer of photoresist having an aperture pattern; etching the aperture pattern through the deposited layers; etching the silicon wafer using a Bosch process to expose emitters that are each self-aligned with a corresponding aperture in the pattern; and thinning the silicon wafer to expose the emitters as the bottom surface of the silicon wafer.

[0009] In some embodiments, forming the silicon wafer and the deposited layers comprises using a metal-assisted chemical etching (MACE) technique. Such embodiments include depositing, on the top surface of the silicon wafer, the layer of electrically insulating material; depositing, on the layer of electrically insulating material, a layer of photoresist having an aperture pattern; etching the aperture pattern through the deposited layer; depositing the layer of electrically conducting material on the etched surface; etching through the etched pattern using metal-assisted chemical etching; and thinning the silicon wafer through any residual electrically conducting material to expose the emitters as the bottom surface of the silicon wafer.

[0010] Some embodiments include, before thinning the silicon wafer, reducing diameters of one or more emitter holes using thermal oxidation or selective silicon-based epitaxy.

[0011] It is appreciated that other embodiments may form the required silicon wafer, electrically insulating layer, and electrically conducting layer using other techniques known in the art.

DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0012] The manner and process of making and using the disclosed embodiments may be appreciated by reference to the drawings.

[0013] Figure 1 is a cross-sectional view of a prior art electrospray device having misaligned extractor apertures.

[0014] Figure 2 is a cross-sectional view of a self-aligned electrospray device, according to some embodiments.

[0015] Figure 2A is a cross-sectional view of a self-aligned electrospray device including a circuit for providing an electric potential difference between the extractor and fluid in the fluid reservoir, according to some embodiments.

[0016] Figure 3 is a series of cross-sectional views illustrating a process of making a self-aligned electrospray device which may be the same as or similar to the device illustrated in Figure 2, according to some embodiments.

[0017] Figure 3A is a series of cross-sectional views illustrating another process of making a self-aligned electrospray device which may be the same as or similar to the device illustrated in Figure 2, according to some embodiments.

[0018] Figure 4 is a series of cross-sectional views illustrating another process of making a self-aligned electrospray device which may be the same as or similar to the device illustrated in Figure 2, according to some embodiments.

DETAILED DESCRIPTION

[0019] Before proceeding with a discussion of the concepts, systems, device, circuits and techniques described herein, some introductory concepts and terminology are first provided.

[0020] Various embodiments of the concepts systems and techniques are described herein with reference to the related drawings. Alternative embodiments can be devised without departing from the scope of the described concepts. It is noted that various connections and positional relationships (e.g., over, below, adjacent, etc.) are set forth between elements in the following description and in the drawings. These connections and/or positional relationships, unless specified otherwise, can be direct or indirect, and

the present invention is not intended to be limiting in this respect. Accordingly, a coupling of entities can refer to either a direct or an indirect coupling, and a positional relationship between entities can be a direct or indirect positional relationship. As an example of an indirect positional relationship, references in the present description to element or structure "A" over element or structure "B" include situations in which one or more intermediate elements or structures (e.g., element "C") is between element "A" and element "B" regardless of whether the characteristics and functionalities of element "A" and element "B" are substantially changed by the intermediate element(s).

[0021] The following definitions and abbreviations are to be used for the interpretation of the claims and the specification.

[0022] As used herein, the terms "comprises," "comprising," "includes," "including," "has," "having," "contains" or "containing," or any other variation thereof, are intended to cover a non-exclusive inclusion. For example, a method, article, or apparatus that comprises a list of elements is not necessarily limited to only those elements but can include other elements not expressly listed or inherent to such method, article, or apparatus.

[0023] Additionally, the term "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any embodiment or design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments or designs. The terms "one or more" and "one or more" are understood to include any integer number greater than or equal to one, i.e. one, two, three, four, etc. The terms "a plurality" are understood to include any integer number greater than or equal to two, i.e. two, three, four, five, etc. The term "connection" can include an indirect "connection" and a direct "connection".

[0024] References in the specification to "one embodiment," "an embodiment," "an example embodiment," or variants of such phrases indicate that the embodiment described can include a particular feature, structure, or characteristic, but every embodiment can include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a

particular feature, structure, or characteristic is described in connection knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0025] Furthermore, it should be appreciated that relative, directional or reference terms (e.g. such as “above,” “below,” “left,” “right,” “top,” “bottom,” “vertical,” “horizontal,” “front,” “back,” “rearward,” “forward,” etc.) and derivatives thereof are used only to promote clarity in the description of the figures. Such terms are not intended as, and should not be construed as, limiting. Such terms may simply be used to facilitate discussion of the drawings and may be used, where applicable, to promote clarity of description when dealing with relative relationships, particularly with respect to the illustrated embodiments. Such terms are not, however, intended to imply absolute relationships, positions, and/or orientations. For example, with respect to an object or structure, an "upper" surface can become a "lower" surface simply by turning the object over. Nevertheless, it is still the same surface and the object remains the same. Also, as used herein, "and/or" means "and" or "or", as well as "and" and "or." Moreover, all patent and non-patent literature cited herein is hereby incorporated by references in their entirety.

[0026] The terms “disposed over,” "overlying," "atop," "on top," "positioned on" or "positioned atop" mean that a first element, such as a first structure, is present on a second element, such as a second structure, where intervening elements or structures (such as an interface structure) may or may not be present between the first element and the second element. The term "direct contact" means that a first element, such as a first structure, and a second element, such as a second structure, are connected without any intermediary elements or structures between the interface of the two elements.

[0027] Figure 2 shows a self-aligned electrospray device, according to some embodiments. The illustrative self-aligned electrospray device 200 includes a fluid reservoir 202, an emitter substrate 204 disposed over the reservoir 202, an extractor 206, and an insulation layer 208 disposed between the substrate 204 and the

extractor 206. An array of emitters 212a, 212b, etc. (212 generally) provide a pathway for fluid to exit the fluid reservoir 202. An array of apertures 210a, 210b, etc. (210 generally) may be formed in the extractor 206, providing a pathway for fluid to exit the device. Insulation layer 208 provides electrical isolation between each emitter 212 the extractor 206. While five emitters 212a–212f are shown in the example of Figure 2, the disclosed subject matter can be applied to devices having an arbitrary number of emitters 212.

[0028] In embodiments, the array of emitters 212 may be formed from a silicon wafer. That is, emitter substrate 204 in Figure 2 may be provided as a silicon wafer. The insulation layer 208 may be formed from an electrically insulating material that is deposited on a top surface of the silicon wafer. Such insulating materials may include, for example, oxides such as SiO_2, nitrides such as SiN, and polymers such as Teflon or Kapton. The extractor 206 may be formed from an electrically conducting material that is deposited on a top surface of the insulation layer 208. Such electrically conducting material may include, for example, metals such as Aluminium (Al), Tungsten (W), Gold (Au), Chromium (Cr), Molybdenum (Mo), or Copper (Cu); heavy doped semiconductors such as p++ or n++ type Silicon (Si); or conducting oxides such as indium tin oxide.

[0029] In some embodiments, an emitter 212 can have a diameter or width W_1 of approximately 500 nm. In some embodiments, an aperture 210 can have a diameter or width W_2 of approximately 600 nm. In some embodiments, W_2 can be about 20% larger than W_1 (e.g., W_2 can be between 15% and 25% larger than W_1).

[0030] Referring to Figure 2A in which like elements of Figure 2 are shown using like reference numbers, the self-aligned electrospray device 200 can include a circuit 230 for providing an electric potential difference between the extractor 206 and electrically conductive fluid 220 in fluid reservoir 202. The circuit 230 can be any voltage source in the range of approximately 1 kilovolt (kV) to tens of kV. The electric potential applied by circuit 230 can cause Taylor cones to form in the spaces between the extractor 206 and each emitter 212 (e.g., between extractor 206 and emitter 212a) so

that ions exit each aperture as an aerosol (e.g., so that ions 222 exit aperture 210a as an aerosol).

[0031] Figure 3 shows a process, using the Bosch technique, of making a self-aligned electrospray device which may be the same as or similar to device 200 of Figure 2.

[0032] Step 300 includes providing a silicon wafer 302 having a full thickness. The array of emitters of the device will be formed from a portion of this wafer. As used herein, “full thickness” refers to the thickness of wafer as manufactured. For example, if a 200mm Si wafer is manufactured to be around 725um thick, then its full thickness is 725um. In some embodiments, wafer 302 has a full thickness in the range of 300 microns to 1 millimeter.

[0033] Step 310 includes depositing, on the top surface of a silicon wafer 302, a layer of electrically insulating material 304, which can include any of the electrically insulating materials described in connection with Figure 2. In some embodiments, the insulating layer 304 can have a thickness that is sufficient to withstand an applied electric potential of 1000 kV without significant degradation. Step 310 can further include depositing, on a top surface of the electrically insulating material 304, a layer of electrically conducting material 306, which can include any of the electrically insulating materials described in connection with Figure 2. The layer of electrically conducting material 306 will form the extractor. The materials 304 and 306 may be deposited or otherwise disposed on the insulating material using any technique known to those of ordinary skill in the art including but not limited to any additive or subtractive technique including but not limited to any sputtering or vapor deposition technique.

[0034] Step 320 includes depositing, on a top surface of the layer of electrically conducting material 306, a layer of photoresist 308 having an aperture pattern. The aperture pattern is indicated as holes (e.g., hole 309) in the layer of photoresist 308 that expose a top surface of the underlying electrode layer 306 for use in etching. Thus, in this illustrative embodiment, the apertures are formed using a patterning technique.

Those of ordinary skill in the art will appreciate, of course, that any additive or subtractive technique may be used to form or otherwise provide the apertures.

[0035] Step 330 includes etching the aperture pattern through the deposited layers 306 and 304. The processing of step 330 may be performed, for example, using “dry” reactive ion etching (RIE) or using “wet” chemical etching.

[0036] Step 340 includes etching the silicon wafer 302 using a Bosch, or Bosch-like, process to expose emitters that are each self-aligned with a corresponding aperture in the pattern. As used herein, “Bosch-like process” refers to an etching that creates features having a relatively high aspect ratio; that is, a relatively high ratio between the depth of a hole and its diameter.

[0037] Step 350 includes thinning the silicon wafer 302 to expose the emitters as the bottom surface of the silicon wafer. The thinning processing step 350 is complete when the emitters are exposed. Any thinning technique known in the art may be employed.

[0038] In some embodiments, the bottom surface thus exposed may be coupled to a fluid reservoir (e.g. reservoir 202 of Figure 2), so that the exposed bottom surface becomes the array of emitters (e.g., emitters 212 in Figure 2). Such coupling may be accomplished via a bonding process or via any other process well known to those of ordinary skill in the art.

[0039] In some embodiments, prior to coupling the structure to a fluid reservoir, a processing step 360 can include undercutting the insulation layer 304 to provide space for the Taylor cone to form in the gap between each emitter and its corresponding extractor aperture. Undercutting may be performed, for example, by isotropically etching the insulation layer 304.

[0040] Figure 3A shows another process making a self-aligned electrospray device which may be the same as or similar to device 200 of Figure 2. The process shown in Figure 3A is similar to that of Figure 3 but for an optional, extra processing step 345.

[0041] Step 345 includes growing or otherwise providing a structure on the inside of the apertures to reduce the diameter of the eventual emitters. For example, as shown in Figure 3A, a structure 347 may be provided along the bottom and insides of aperture 346. Structure 347 can be comprised of, for example, an oxide or a silicon-based epitaxy. To make the structure 347, a selective thermal oxidation process or a selective Si epitaxial process can be used to grow Si in the exposed Si in the emitters on the wafer. With both processes, the metal may be selected to be compatible with high temperature processing, such as W. In an embodiment using the extra processing step 345, the emitters may be narrower, so the aspect ratios of the through-holes in the self-aligned electrospray device are thereby increased. Aspect ratio here refers to the emitter length divided by diameter. In some embodiments, emitters can have an aspect ratios in the range of 300 to 400.

[0042] Figure 4 shows another process, using a metal-assisted chemical etching (MACE) technique, of making a self-aligned electrospray device which may be the same as or similar to device 200 of Figure 2.

[0043] Step 400 includes providing a silicon wafer 402 having a full thickness and may be substantially the same as processing step 300 of Figure 3. The array of emitters of the device will be formed or otherwise provided from a portion of this wafer 402.

[0044] Step 410 includes disposing (e.g. depositing or otherwise providing), on the top surface of the silicon wafer 402, a layer of electrically insulating material 404, e.g. any of the electrically insulating materials described in connection with Figure 2. Processing step 410 may be the same as or similar to processing step 310 describe above in conjunction with Figure 3. However, in the embodiment of FIG. 4, no electrically conducting material is deposited at this time. In particular, the extractor is formed later, as described below.

[0045] Step 420 includes depositing, on the layer of electrically insulating material, a layer of photoresist 406 having an aperture pattern. Step 420 may be the same as or similar to step 320 described above in conjunction with Figure 3.

[0046] Step 430 includes etching the aperture pattern through the deposited layers 406 and 404. This step produces the capillaries through which fluid will eventually traverse, and guarantees self-alignment of the emitters and the extractor apertures.

[0047] Step 440 includes depositing a layer of electrically conducting material 408 on the etched surface. This processing can include a non-conformal metal deposition. The extractor is formed on a top surface of the insulation layer 404 as a result of performing step 440, in manner which may be the same as or similar to the process described above in conjunction with Figure 3. However, in contrast to Figure 3, in the embodiment of Figure 4 metal 409 is deposited at the bottom of each capillary.

[0048] Step 450 includes etching through the pattern substrate using a metal-assisted chemical etching (MACE) technique. The MACE technique requires that metal be deposited in each capillary and is enabled by processing step 440. Thus, the process of Figure 4 includes two etching steps, similar to Figure 3, however the second etching step differs between the two processes. The process used in any particular embodiment therefore may be chosen on the basis of cost, manufacturing processes available, or other external design factor.

[0049] Step 460 includes thinning the silicon wafer 402 through any residual electrically conducting material 411 to expose the emitters as the bottom surface of the silicon wafer 402. The thinning step 460 is complete when the emitters are exposed. Any thinning technique known in the art may be employed. However, unlike the thinning step 350 of Figure 3, step 460 may first reveal residual electrical conducting material at the bottom of each capillary, and may be required to remove this material as well.

[0050] Step 470 includes undercutting the insulation layer to provide space for the Taylor cone to form in the gap between each emitter and its corresponding extractor aperture. Undercutting may be performed, for example, by oxidizing the insulation layer 404 and may use substantially the same techniques as processing step 360 of Figure 3.

[0051] It is also appreciated that the processes of both Figures 3 and 4 define automatically align the extractor apertures with the emitters without the need for a separate two-wafer alignment process that is prone to misalignment errors. It is further appreciated that in both of these processes, the insulation layer is undercut only after the aforementioned self-alignment, ensuring that the alignment is not thereby affected. It is appreciated that in either case, the flow rate of embodiments may be controlled by varying the size of the extractor apertures.

[0052] In the foregoing detailed description, various features of embodiments are grouped together in one or more individual embodiments for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the claimed invention requires more features than are expressly recited in each claim. Rather, inventive aspects may lie in less than all features of each disclosed embodiment. It should also be appreciated that Elements of different embodiments described herein may be combined to form other embodiments not specifically set forth above. Various elements, which are described in the context of a single embodiment, may also be provided separately or in any suitable subcombination. Other embodiments not specifically described herein are also within the scope of the following claims.

[0053] Having described implementations which serve to illustrate various concepts, structures, and techniques which are the subject of this disclosure, it will now become apparent to those of ordinary skill in the art that other implementations incorporating these concepts, structures, and techniques may be used. Accordingly, it is submitted that that scope of the patent should not be limited to the described implementations but rather should be limited only by the spirit and scope of the following claims.

CLAIMS

1. A self-aligned electrospray device comprising:
   a silicon wafer having deposited on a top surface thereof a layer of electrically insulating material, and having deposited thereon a layer of electrically conducting material, wherein the silicon wafer and the deposited layers have through holes and the electrically insulating layer is undercut;
   a fluid reservoir, mounted to a bottom surface of the silicon wafer, for containing fluid; and
   a circuit, for providing an electric potential difference, coupled between the layer of electrically conducting material and the fluid reservoir.

2. The device of claim 1, wherein the insulating material comprises an oxide.

3. The device of claim 1, wherein the electrically conducting material comprises Tungsten (W).

4. The device of claim 1, wherein the electrically conducting material comprises a doped semiconductor material.

5. The device of claim 1, wherein the electrically conducting material comprises a conducting oxide.

6. The device of claim 1, wherein the through holes in the deposited layer have a diameter that is 15% to 25% larger than a dimeter of the through holes in the silicon wafer.

7. A method of making a self-aligned electrospray device, the method comprising:

forming a silicon wafer having deposited on a top surface thereof a layer of electrically insulating material, and having deposited thereon a layer of electrically conducting material, wherein the silicon wafer and the deposited layers have through holes;

undercutting the electrically insulating material;

mounting a bottom surface of the silicon wafer to a fluid reservoir for containing fluid; and

coupling a circuit, for providing an electric potential difference, between the layer of electrically conducting material and the fluid reservoir.

8. The method of claim 7, wherein forming the silicon wafer and the deposited layers comprises:

depositing, on the top surface of the silicon wafer, the layer of electrically insulating material;

depositing, on the electrically insulating material, the layer of electrically conducting material;

depositing, on the layer of electrically conducting material, a layer of photoresist having an aperture pattern;

etching the aperture pattern through the deposited layers;

etching the silicon wafer using a Bosch process to expose emitters that are each self-aligned with a corresponding aperture in the pattern; and

thinning the silicon wafer to expose the emitters as the bottom surface of the silicon wafer.

9. The method of claim 8, further comprising, before thinning the silicon wafer, reducing diameters of one or more emitter holes using thermal oxidation or selective silicon-based epitaxy.

10. The method of claim 7, wherein forming the silicon wafer and the deposited layers comprises:

depositing, on the top surface of the silicon wafer, the layer of electrically insulating material;

depositing, on the layer of electrically insulating material, a layer of photoresist having an aperture pattern;

etching the aperture pattern through the deposited layer;

depositing the layer of electrically conducting material on the etched surface;

etching through the etched pattern using metal-assisted chemical etching; and

thinning the silicon wafer through any residual electrically conducting material to expose the emitters as the bottom surface of the silicon wafer.

11. The method of claim 10, further comprising, before thinning the silicon wafer, reducing diameters of one or more emitter holes using thermal oxidation or selective silicon-based epitaxy.

12. The method of claim 7, wherein the insulating material comprises an oxide.

13. The method of claim 7, wherein the electrically conducting material comprises Tungsten (W).

14. The method of claim 7, wherein the electrically conducting material comprises a doped semiconductor material.

15. The method of claim 7, wherein the electrically conducting material comprises a conducting oxide.

16. The method of claim 7, wherein the through holes in the deposited layer have a diameter that is 15% to 25% larger than a dimeter of the through holes in the silicon wafer.

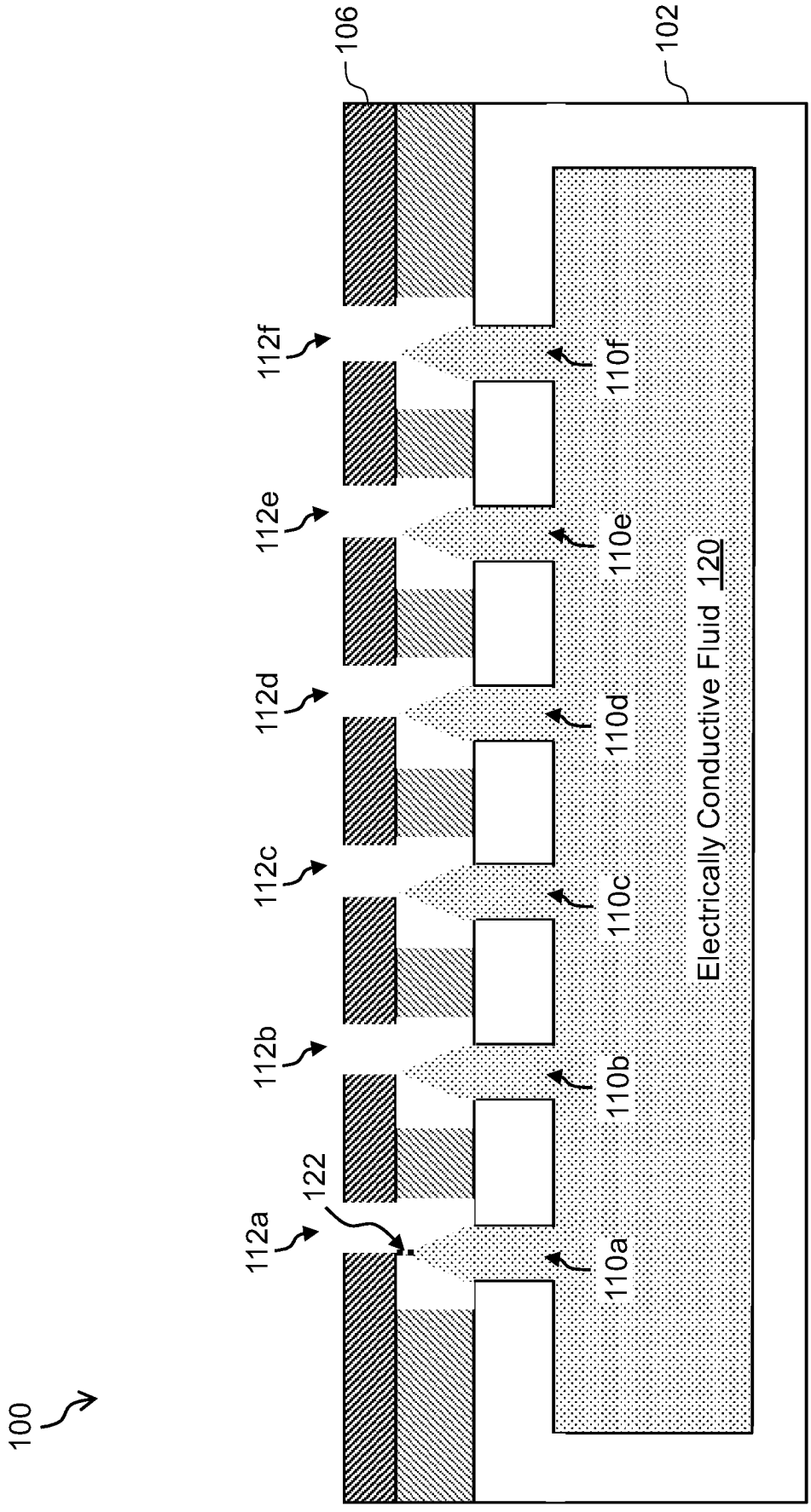

FIG. 1
(Prior Art)

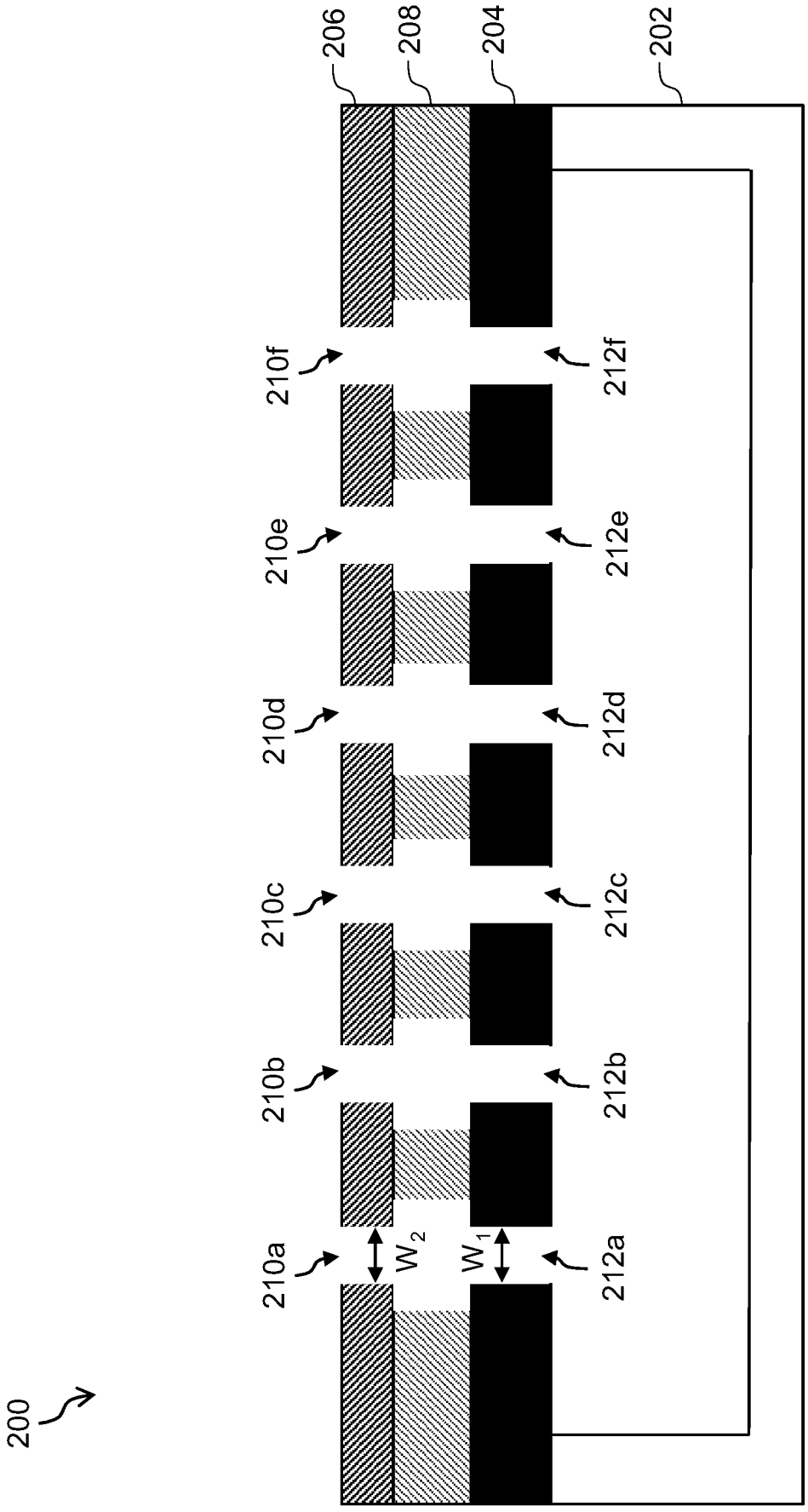
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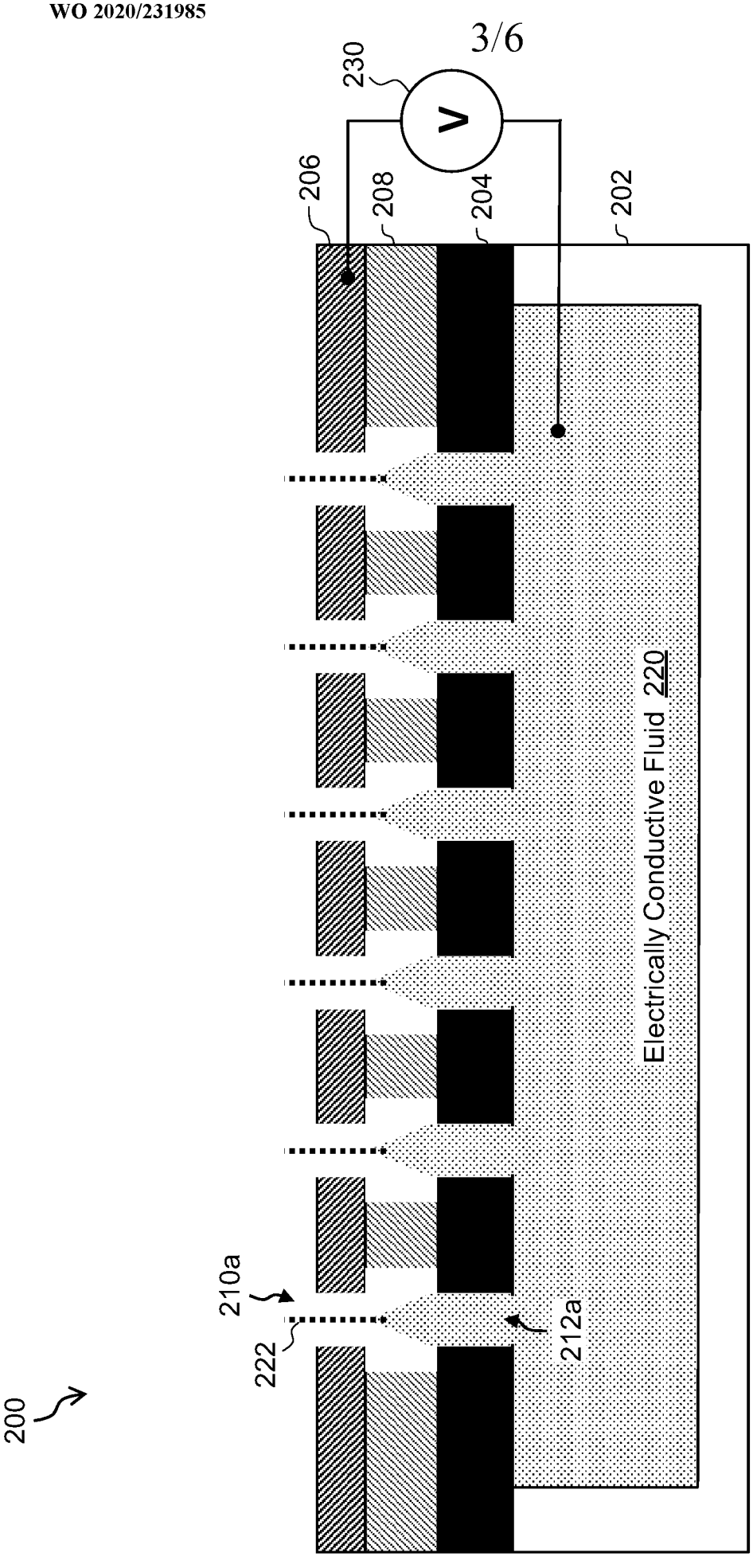
FIG. 2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Electrically Conductive Fluid 220

FIG. 2A

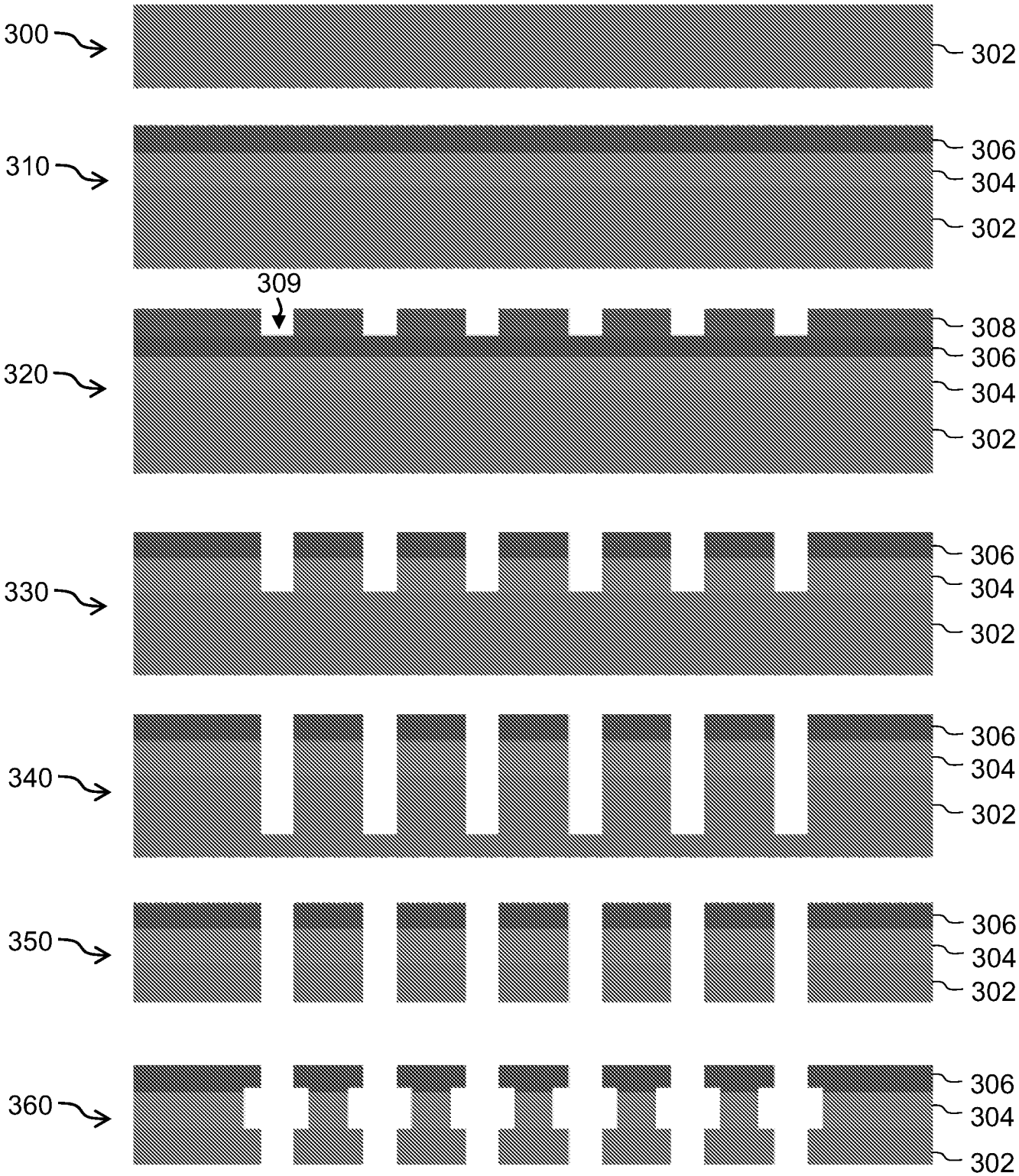
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FIG. 3

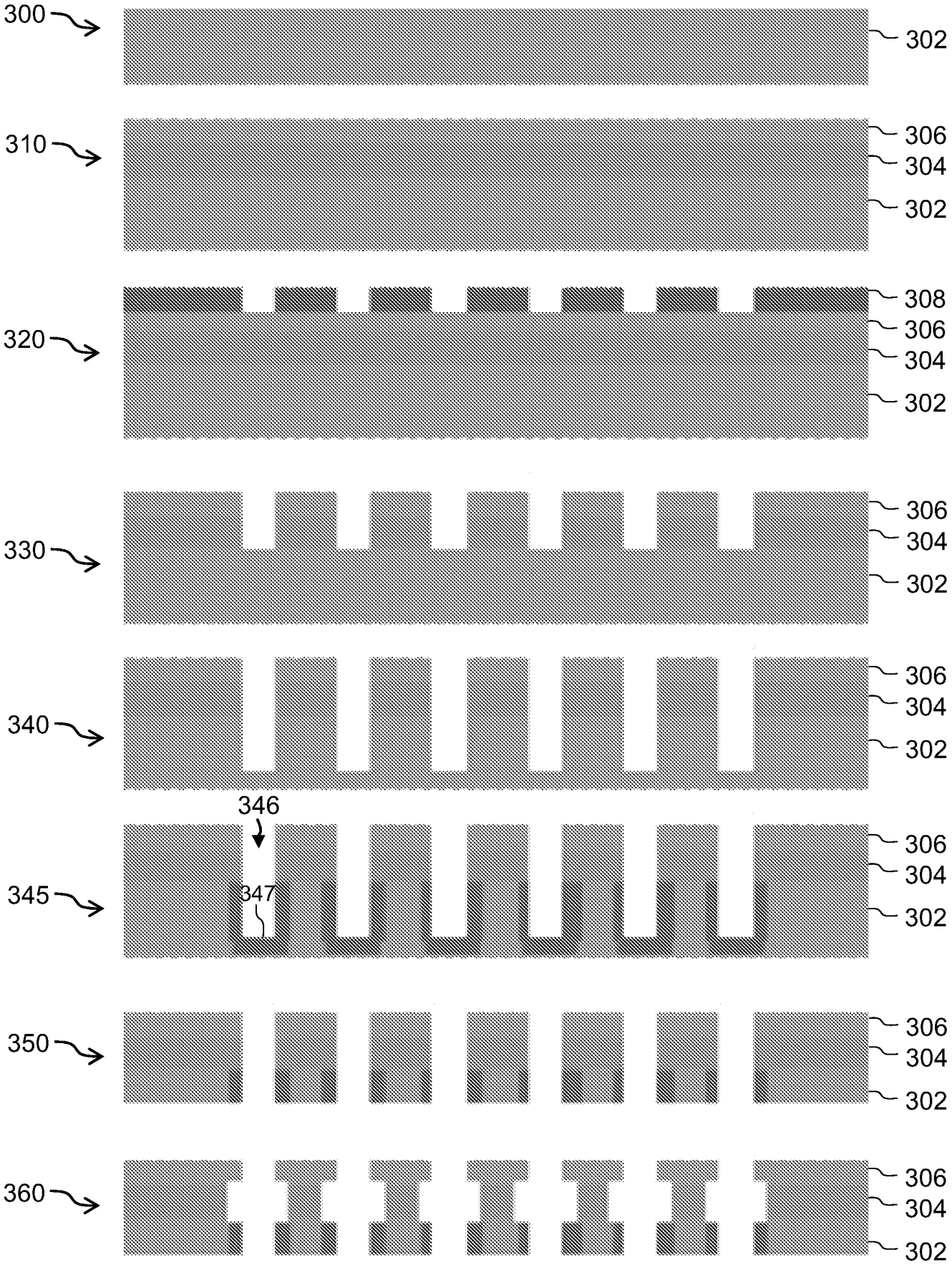
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FIG. 3A

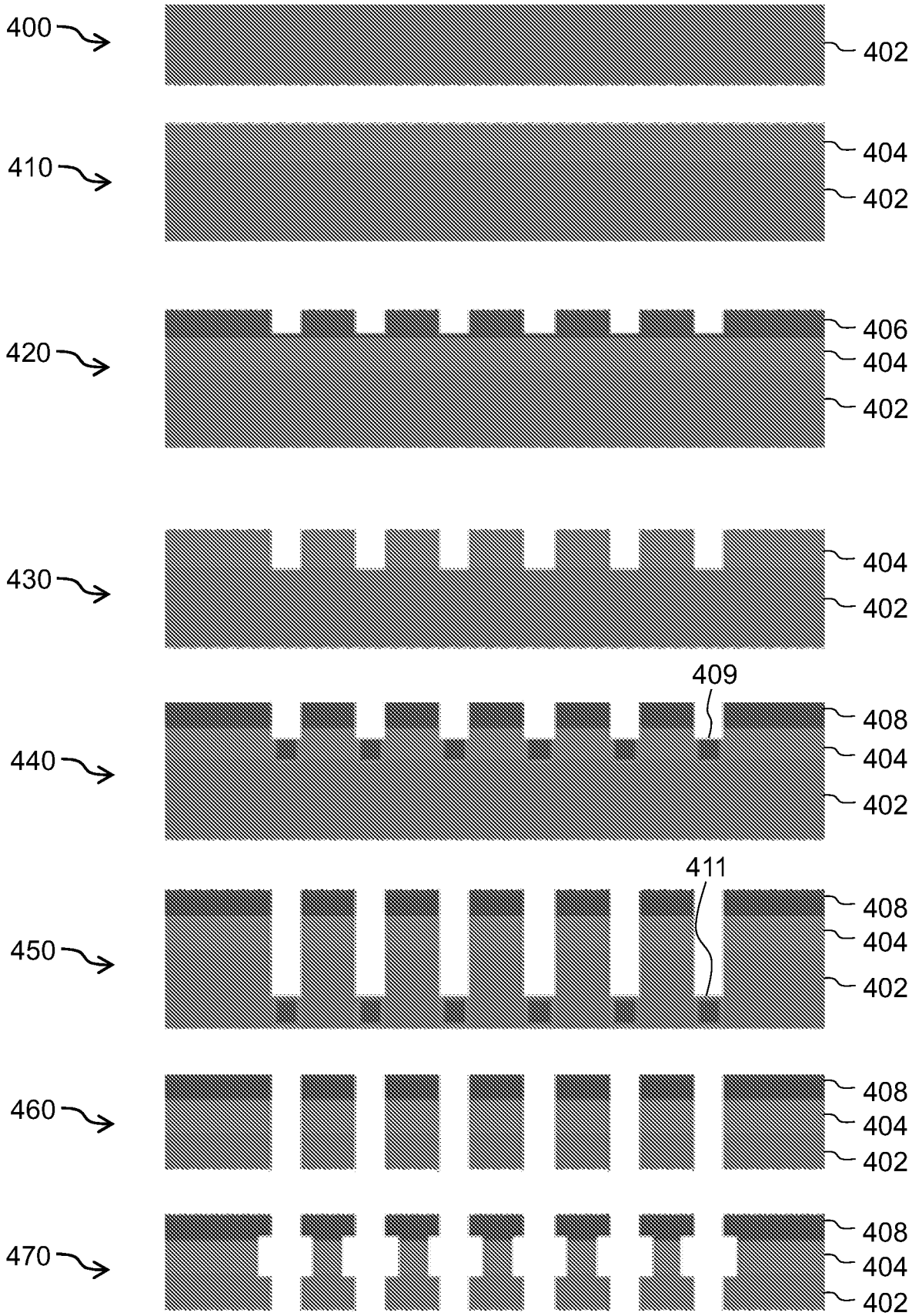
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FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 20/32465

A. CLASSIFICATION OF SUBJECT MATTER

IPC - B01D 15/10; B05B 1/02 (2020.01)

CPC - B01D 15/10; B01L 3/502715; B01L 3/502753; B01L 3/563

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009/0056133 A1 (Waits et al.) 05 March 2009 (05.03.2009) para [0003], [0012], [0021], [0024], [0027], [0028], [0030]	1-6
Y	Kim et al., 'Miniaturized multichannel electrospray ionization emitters on poly(dimethylsiloxane) microfluidic devices' Electrophoresis. 2001; 22(18): 3993-3999. doi:10.1002/1522-2683(200110)22:18<3993::AID-ELPS3993>3.0.CO;2-X, Abstract	1-6
Y	US 2011/0192968 A1 (Makarov et al.) 11 August 2011 (11.08.2011) Abstract, para [0031]	4
A	'Pyrex', Wikipedia, 08 September 2016 (08.09.2016) [retrieved from the internet on 24 July 2020 (24.07.2020) at <https://en.wikipedia.org/wiki/Pyrex>] pg 2 para 7	2
A	US 2002/0123153 A1 (Moon et al.) 05 September 2002 (05.09.2002) entire document	1-6
A	US 2002/0000516 A1 (Schultz et al.) 03 January 2002 (03.01.2002) entire document	1-6

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 July 2020	06 OCT 2020
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Lee Young Telephone No. PCT Helpdesk: 571-272-4300

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 20/32465

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
(see supplemental box)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-6

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Continuation of Box III

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I: Claims 1-6 is directed towards a self-aligned electrospray device comprising: a silicon wafer having deposited on a top surface thereof a layer of electrically insulating material, and having deposited thereon a layer of electrically conducting material, wherein the silicon wafer and the deposited layers have through holes and the electrically insulating layer is undercut; a fluid reservoir, mounted to a bottom surface of the silicon wafer, for containing fluid; and a circuit, for providing an electric potential difference, coupled between the layer of electrically conducting material and the fluid reservoir.

Group II: Claims 7-16 is directed towards a method of making a self-aligned electrospray device, the method comprising: forming a silicon wafer having deposited on a top surface thereof a layer of electrically insulating material, and having deposited thereon a layer of electrically conducting material, wherein the silicon wafer and the deposited layers have through holes; undercutting the electrically insulating material; mounting a bottom surface of the silicon wafer to a fluid reservoir for containing fluid; and coupling a circuit, for providing an electric potential difference, between the layer of electrically conducting material and the fluid reservoir.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features:

Group II requires towards a method of making a self-aligned electrospray device, the method comprising: forming a silicon wafer having deposited on a top surface thereof a layer of electrically insulating material, and having deposited thereon a layer of electrically conducting material, wherein the silicon wafer and the deposited layers have through holes; undercutting the electrically insulating material; mounting a bottom surface of the silicon wafer to a fluid reservoir for containing fluid; and coupling a circuit, for providing an electric potential difference, between the layer of electrically conducting material and the fluid reservoir, not required by group I.

Shared Technical Features:

Groups I -II share the common feature of a self-aligned electrospray device comprising: a silicon wafer having deposited on a top surface thereof a layer of electrically insulating material, and having deposited thereon a layer of electrically conducting material, wherein the silicon wafer and the deposited layers have through holes and the electrically insulating layer is undercut; a fluid reservoir, mounted to a bottom surface of the silicon wafer, for containing fluid; and a circuit, for providing an electric potential difference, coupled between the layer of electrically conducting material and the fluid reservoir.

However, these shared technical features do not represent a contribution over prior art, because the shared technical feature is obvious over US 2009/0056133 A1 to Waits et al. (hereinafter 'Waits') in view of the article 'Miniaturized multichannel electrospray ionization emitters on poly(dimethylsiloxane) microfluidic devices' to Kim et al. (hereinafter 'Kim'). Waits teaches a well aligned electrospray device (Abstract: "an integrated multiplex electrospray..."; para [0003] "...with improved component alignment") comprising: a silicon wafer (para [0024] "In the instance of ring extractor substrate being a silicon wafer..."; para [0027] "a nozzle array layer according to the present invention is readily formed of the materials detailed from which a ring extractor is formed"; therefore, the substrate/nozzle array layer can be a silicon wafer) having deposited on a top surface thereof a layer of electrically insulating material (para [0028] "As shown in FIG.5A, a spacer layer 32 is bonded to a nozzle array layer...provide electrical insulation"), and having deposited thereon a layer of electrically conducting material (para [0024] "In the instance of ring extractor substrate being a silicon wafer..."; see figure 1 that shows the insulating spacer deposited on the nozzle array layer and ring extractor deposited on the spacer), wherein the silicon wafer and the deposited layers have through holes (see fig. 1 that shows through holes through the layers) and the electrically insulating layer is undercut (para [0030] "The mold 42 is then preferentially etched to form a spacer 35 as shown in FIG. 7D and detailed with respect to FIG. 5C"; see fig. 5C that shows this step) a fluid reservoir, mounted to a bottom surface of the silicon wafer, for containing fluid (see fig. 1 that shows the reservoir at the bottom of the nozzle array layer); and a circuit, for providing an electric potential difference, coupled between the layer of electrically conducting material and the fluid reservoir (para [0012] "under a differential potential between the liquid within the reservoir and the ring extractor."; it is understood that a circuit would need to be utilized to provide that differential potential). Waits does not teach that the device is self-aligned. However, in a similar invention for an electrospray device (Abstract: "A multichannel electrospray ionization (ESI) emitter..."), Kim teaches forming the device using self-aligning (Abstract: "produces a self-alignment system to make a bonding between the top and bottom PDMS parts"). It would have been obvious to one skilled in the art to combine these references and form the aligned device taught by Waits using self-alignment taught by Kim for ease of manufacturing and accuracy of alignment.

As the shared technical features were known in the art at the time of the invention, they cannot be considered special technical features that would otherwise unify the groups. Therefore, Groups I-II lack unity under PCT Rule 13.