(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 301 603 B1**

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: **01.12.93**

(51) Int. Cl.[5]: **G11C 7/00**, H03K 19/00

(21) Application number: **88112482.0**

(22) Date of filing: **01.08.88**

(54) **Output circuit of semiconductor integrated circuit device.**

(30) Priority: **31.07.87 JP 191602/87**

(43) Date of publication of application:
01.02.89 Bulletin 89/05

(45) Publication of the grant of the patent:
01.12.93 Bulletin 93/48

(84) Designated Contracting States:
DE FR GB

(56) References cited:
EP-A- 0 121 217
EP-A- 0 164 615
EP-A- 0 238 358
US-A- 4 061 999

PATENT ABSTRACTS OF JAPAN, vol. 10, no. 29 (E-452), 8th November 1986; & JP-A-61 135 223

Electronics, 5 April 1984, pages 125-128, BATEMAN et al.: "C-MOS challenges bipolars in static-RAM race"

(73) Proprietor: **KABUSHIKI KAISHA TOSHIBA**
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi Kanagawa-ken 210(JP)

Proprietor: **Toshiba Micro-Computer Engineering Corporation**
25-1, Ekimaehoncho
Kawasaki-ku
Kawasaki-shi(JP)

(72) Inventor: **Tatsumi, Yuuichi**
1-10-18, Kaminoge
Setagaya-ku
Tokyo(JP)
Inventor: **Minagawa, Hidenobu**
Daini-Taiyo-So, 194
Kariyado
Nakahara-ku
Kawasaki-shi(JP)
Inventor: **Iwahashi, Hiroshi**
c/o Pat. Div.
K.K. Toshiba
1-1 Shibaura 1-chome
Minato-ku Tokyo 105(JP)
Inventor: **Asano, Masamichi**
c/o Pat. Div.
K.K. Toshiba
1-1 Shibaura 1-chome
Minato-ku Tokyo 105(JP)

EP 0 301 603 B1

Inventor: **Imai, Mizuho**
2-7-5, Itahana
Annaka-shi Cunma-ken(JP)

(74) Representative: **Henkel, Feiler, Hänzel & Partner**
Möhlstrasse 37
D-81675 München (DE)

Description

This invention relates to a semiconductor integrated circuit with an output circuit for externally outputting a signal or data, and more particularly to a semiconductor integrated circuit in which a signal or data output speed can be controlled in accordance with a control signal.

In an ordinary semiconductor integrated circuit such as a semiconductor memory device, a signal or data is externally supplied via an output circuit which is generally called an output buffer circuit. In general, a semiconductor memory device is designed to meet the application thereof and at the same time to attain a preset readout speed in a condition that a load capacitance of approx. 100 pF is connected to the data output terminal. For example, address access time t_{ACC} from a time that the address signal starts to vary to a time that data is read out is set to 150 ns at maximum. Further, time t_{OE} from a time that output enable signal $\overline{OE}$ is activated to a time that output data is determined is set to approx. 70 ns at maximum.

Since it is necessary to charge or discharge the load capacitor connected to the output terminal, a large current will flow at this time, and therefore the power source voltage fluctuates, causing noise to be generated. Such a noise may cause the integrated circuit to operate erroneously. Generally, the output circuit includes a buffer amplifier section for directly driving the load, and a pre-amplifier section for driving the buffer amplifier section. In order to suppress generation of noise due to rapid variation in current flowing in the output circuit, transistors constituting the pre-amplifier section or transistors constituting the buffer amplifier section are each formed to have a small channel width in the prior art. In this way, if the channel width of the transistor of the pre-amplifier section is set to be small, the current driving ability of the transistor becomes small, thereby causing the potential of a signal supplied to the gate of the transistor of the buffer amplifier section to rise or fall slowly. Therefore, current flowing in the buffer amplifier section will not vary abruptly, suppressing the noise generation due to the fluctuation in the power source voltage. Also, when the transistor of the buffer amplifier section has a small channel width, a small amount of current flows in the buffer amplifier section. This suppresses the generation of noise due to the fluctuation in the power source voltage, thereby preventing an erroneous circuit operation of the IC. However, with these methods, the operation speed or the data readout speed will be lowered.

With the conventional method, increase in the operation speed and reduction in the noise cannot be attained at the same time. Thus, when a high-speed operation is desired, and suppression of noise is also required, a thick power-source line is used, or a large-capacitance decoupling capacitor is connected between the power source of the semiconductor integrated circuit and the ground. Use of the thick line or the large-capacitance capacitor inevitably raise the cost of the apparatus in which the integrated circuit is incorporated. Further, when the sufficient suppression of the noise is desired and the reduction of the cost of the apparatus is also required, the operation speed is lowered.

As described above, in the conventional semiconductor integrated circuit, increase in the operation speed of the output circuit and reduction in the noise cannot be attained at the same time.

Prior art document EP-A-0 164 615 discloses a circuit for adjusting the rise and fall times of an output signal of a driver circuit to correspond to reference rise and fall times by using a feedback circuit acting on the gates of output MOS transistors.

It is an object of the present invention to provide a semiconductor integrated circuit which makes no operation errors despite noise, without reducing the operation speed of its output section, wherein the rate of changes of an output signal of an output buffer is made selectable so that the rate is relatively low or relatively high.

To solve this object the present invention provides a semiconductor integrated circuit as specified in claim 1 or 2.

With the construction described above, the control circuit is operated to charge or discharge the preset node of the data output circuit for a preset period of time after the control signal has changed in level. Therefore, the preset node can be rapidly charged or discharged, permitting data to be read out at a high speed.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing the entire construction of a semiconductor memory device according to one embodiment of this invention;

Fig. 2 is a circuit diagram showing the detail construction of part of an output circuit section in the device of Fig. 1;

Figs. 3 and 4 are timing charts for illustrating the operation of circuits shown in Figs. 1 and 2;

Figs. 5 and 6 are voltage waveforms at respective portions of the circuit shown in Figs. 1 and 2;

Fig. 7 is a diagram showing the waveforms of the signals which are generated at the various portions of the circuit shown in Figs. 1 and 2 when no output control circuit is used;

Fig. 8 is a circuit diagram showing the detail construction of an output enable/program control circuit and an output control circuit in the device of Fig. 1;

Fig. 9 is a circuit diagram showing another detail construction of the output circuit shown in Fig. 2;

Fig. 10 is a timing chart for illustrating the operation of the output circuit shown in Fig. 9; and

Figs. 11 to 13 are circuit diagrams showing still another construction of the output circuit shown in Fig. 2.

First, the technical idea underlying this invention is explained before explaining the embodiments of this invention.

For example, in the standard of a semiconductor memory device (TC571000D and TC571001D manufactured by TOSHIBA Co., Ltd Japan. are shown as examples), it is generally required as shown in the table-1 to set readout times t_{OE} and t_{PGM} shorter than address access time t_{ACC} and chip-enable access time t_{CE}. Address access time t_{ACC} ranges from variation of the address signal to the data readout time, chip-enable access time t_{CE} ranges from variation of chip enable signal $\overline{CE}$ to the data readout time, and times t_{OE} and t_{PGM} range respectively from variation of output buffer enable signal $\overline{OE}$ and program mode setting signal $\overline{PGM}$ to the data readout time. As shown in the table-1, time t_{ACC} is set at 150 ns or 200 ns at maximum, but times t_{OE} andt_{PGM} are set at 70 ns at maximum.

TABLE-1

A.C. ELECTRICAL CHARACTERISTICS (Ta = -40 ~ 85°C, Vcc = 5V ± 5%, Vpp = Vcc ± 0.6V)

SYMBOL	ITEM	TC 571000D-15/ TC 571001D-15		TC 571000D-20/ TC 571001D-20		UNIT
		MIN	MAX	MIN	MAX	
t_{ACC}	ADDRESS ACCESS TIME	--	150	--	200	ns
t_{CE}	VARIATION OF $\overline{CE}$ TO DATA READOUT	--	150	--	200	ns
t_{OE}	VARIATION OF $\overline{CE}$ TO DATA READOUT	--	70	--	70	ns
t_{PGM}	VARIATION OF $\overline{PGM}$ TO DATA READOUT	--	70	--	70	ns
t_{DF1}	VARIATION OF $\overline{CE}$ TO SET-UP OF HIGH OUTPUT	0	60	0	60	ns
t_{DF2}	IMPEDANCE VARIATION OF OE TO SET-UP OF HIGH OUTPUT IMPEDANCE	0	60	0	60	ns
t_{DF3}	VARIATION OF $\overline{PGM}$ TO SET-UP OF HIGH OUTPUT IMPEDANCE	0	60	0	60	ns
t_{OH}	OUTPUT DATA HOLDING TIME	0	--	0	--	ns

*A.C. test condition:

* output load: 1 TTL Gate and C_L = 100pF
* fall and rise times of input pulse: 10 ns MAX.
* input pulse level: 0.45 V to 2.4 V
* reference level for timing measurement: input 0.8 V and 2.2 V

In general, the address input signal is supplied to the row decoder and column decoder via the address buffer. The row decoder functions to select a memory cell, and the readout data from the selected memory cell is supplied to the column line. The readout data supplied to the column line is further supplied to the data sensing circuit via the column gate which is selectively controlled by means of the column decoder. Data sensed by the data sensing circuit is supplied to the exterior by means of the output circuit.

In this way, address access time t_{ACC} is the sum of delay time in such circuit blocks, so data transmission time in the output circuit section occupies only a small portion of address access time t_{ACC}. Therefore, address access time t_{ACC} will not be influenced even if the charging and discharging speeds in the output buffer section of the output circuit are low. In contrast, since output buffer enable signal $\overline{OE}$ is supplied to the output circuit only via the $\overline{OE}$ buffer circuit, substantially all portion of time t_{OE} is occupied by the delay time in the output circuit. Thus, the charging and discharging speeds in the output circuit become one of the most important factors for determining time t_{OE}.

For the reasons described above, even if address access time t_{ACC} is delayed by 10 to 20 ns, it will not give as much influence to the entire operation speed as times t_{OE} and t_{PGM} is delayed by such time. However, if the charging and discharging speeds are lowered in order to suppress the influence due to noise, times t_{OE} and t_{PGM} are prolonged and will not satisfy the standard. With the fact described above taken into consideration, an output control circuit for delaying address access time t_{ACC} and reducing times t_{OE} and t_{PGM} is used in this invention.

Fig. 1 is a block diagram showing the entire construction of a semiconductor memory device (programmable read only memory) according to one embodiment of this invention. Chip enable control circuit 11 generates internal chip enable signals CE* and $\overline{CE}$* in response to chip enable signal $\overline{CE}$. Output enable/program control circuit 12 generates internal output enable signals OE* and $\overline{OE}$* and internal program signal $\overline{PGM}$* in response to externally supplied output enable signal OE and program signal $\overline{PGM}$. External address signal Add and internal chip enable signals CE* and $\overline{CE}$* are input to address buffer 13 which outputs internal address signal Add* when signals CE* and $\overline{CE}$* are activated.

An internal address signal Add* output from address buffer 13 is supplied to row decoder 14 and column decoder 15. Internal chip enable signals CE* and $\overline{CE}$* are also supplied to row decoder 14 and column decoder 15. Row decoder 14 is operated when chip enable signals CE* and $\overline{CE}$* are activated, and selectively drives row line 17 in memory cell array 16 in response to internal address Add*. In memory cell array 16, data is read out from a plurality of memory cells (not shown) connected to row line 17. Data thus read out is input to column gate circuit 19 via column line 18.

Column decoder 15 is operated when chip enable signals CE* and $\overline{CE}$* are activated, and controls the operation of column gate circuit 19 in response to internal address Add*. As a result of the control operation, column gate circuit 19 will select n bits out of m-bit data (m > n) read out from memory cell array 16. Then, n-bit data selected by column gate circuit 19 is input to data detection circuit 20. Data detection circuit 20 is connected to chip enable signals CE* and $\overline{CE}$* and reference voltage Vref generated from reference potential generating circuit 21. Data detection circuit 20 is operated when signals CE* and $\overline{CE}$* are activated, and determines data by comparing the data from column gate circuit 19 with reference voltage Vref. Data thus determined is input to output circuit 22.

Internal output enable signals OE* and $\overline{OE}$* and internal program signal $\overline{PGM}$* from output enable/program control circuit 12 and signals CE* and $\overline{CE}$* from chip enable control circuit 11 are supplied to output control circuit 23. Output control circuit 23 detects variation in level of external output enable signal $\overline{OE}$ based on internal output enable signals OE* and $\overline{OE}$*, and produces pulses P and $\overline{P}$ with a preset pulse width. Pulse signals P and $\overline{P}$ are supplied together with internal output enable signals OE* and $\overline{OE}$* to output circuit 22. Output circuit 22 is operated in response to pulse signals P and $\overline{P}$ and internal output enable signals OE* and $\overline{OE}$* to supply data Dout of plural bits corresponding to detection data from data detection circuit 20 to the outside of the chip.

The memory device in this embodiment is similar to the conventional memory device except that output control circuit 23 is used and output circuit 22 is controlled by pulse signals P and $\overline{P}$ generated from output control circuit 23 in addition to internal output enable signals OE* and $\overline{OE}$*.

Fig. 2 is a circuit diagram showing the construction of part of output circuit 22 included in the memory device shown in Fig. 1 which processes one-bit data. One-bit data DS detected by data detection circuit 20 is supplied to CMOS inverter 33 which is constituted by P-channel MOS transistor 31 and N-channel MOS transistor 32 having current paths connected in series between power source terminals Vcc and Vss (or ground). An output of inverter 33 is supplied to CMOS inverter 36 which is constituted by P-channel MOS transistor 34 and N-channel MOS transistor 35 having current paths connected in series between power source terminals Vcc and Vss.

Further, the current paths of P-channel MOS transistor 37 and two N-channel MOS transistors 38 and 39 are connected in series between power source terminals Vcc and Vss. The gates of P-channel MOS transistor 37 and N-channel MOS transistor 38 are connected to receive an output of inverter 36, and the gate of N-channel MOS transistor 39 is connected to receive internal output enable signal OE*. The current paths of two N-channel MOS transistors 41 and 42 are connected in series between power source terminal Vss and connection node 40 between P-channel MOS transistor 37 and N-channel MOS transistor 38. The gates of N-channel MOS transistors 41 and 42 are connected to receive an output of inverter 36 and pulse signal P, respectively. In addition, the current path of P-channel MOS transistor 43 whose gate is connected to receive internal output enable signal OE* is connected between node 40 and power source terminal Vcc.

Further, the current paths of two P-channel MOS transistors 44 and 45 and N-channel MOS transistor 46 are connected in series between power source terminals Vcc and Vss. The gates of P-channel MOS transistor 45 and N-channel MOS transistor 46 are connected to receive an output of inverter 36, and the gate of P-channel MOS transistor 44 is connected to receive internal output enable signal $\overline{OE^*}$. The current paths of two P-channel MOS transistors 48 and 49 are connected in series between power source terminal Vcc and connection node 47 between P-channel MOS transistor 45 and N-channel MOS transistor 46. The gates of P-channel MOS transistors 48 and 49 are connected to receive pulse signal $\overline{P}$ and an output of inverter 36, respectively. In addition, the current path of N-channel MOS transistor 50 whose gate is connected to receive internal output enable signal $\overline{OE^*}$ is connected between node 47 and power source terminal Vss.

Further, the current paths of P-channel MOS transistor 51 and N-channel MOS transistor 52 are connected in series between power source terminals Vcc and Vss. The gates of P-channel MOS transistor 51 and N-channel MOS transistor 52 are connected to nodes 40 and 47, respectively. In addition, data output terminal (or pad) 54 is connected to connection node 53 between transistors 51 and 52, and data Dout is supplied from terminal 54 to the exterior.

Two inverters 33 and 36, and transistors 37 to 50 constitute pre-amplifier section PB, and other transistors 51 and 52 constitute buffer amplifier section BA. In order to drive a load which is externally connected to terminal 54 with a sufficiently large current, P-channel MOS transistor 51 and N-channel MOS transistor 52 provided at the buffer amplifier BA are formed to have a conductance larger than that of the other transistors.

The operation mode of the PROM includes a programming mode in which data is programmed and a readout mode in which data is read out. The readout mode includes three modes: an output disable mode in which data is read out from a memory cell array in response to an address signal but is not supplied to the exterior, a standby mode in which data is not read out and an active mode in which readout data is supplied to the exterior.

Now, the operation of the memory device with the construction described above is explained.

In the active mode, externally supplied output enable signal $\overline{OE}$ and chip enable signal $\overline{CE}$ are previously set at "0" level. At this time, as shown by the timing chart of Fig. 3, internal output enable signals OE* and $\overline{OE^*}$ are set at "1" and "0" levels, respectively. Pulse signals P and $\overline{P}$ output from output control circuit 23 are respectively set at "0" and "1" levels. Therefore, in the output circuit shown in Fig. 2, N-channel MOS transistor 39 is turned on, N-channel MOS transistor 42 is turned off, P-channel MOS transistor 43 is turned off, P-channel MOS transistor 44 is turned on, P-channel MOS transistor 48 is turned off, and N-channel MOS transistor 50 is turned off. As a result, an output of inverter 36 is supplied to the gate of P-channel MOS transistor 51 via a CMOS inverter constituted by P-channel MOS transistor 37 and N-channel MOS transistor 38, and to the gate of N-channel MOS transistor 52 via CMOS inverter constituted by P-channel MOS transistor 45 and N-channel MOS transistor 46.

In this case, if detection data DS of data detection circuit 20 is at "0" level, an output of inverter 33 is set to "1" level and an output of succeeding inverter 36 is set to "0" level. At this time, node 40 is charged by means of P-channel MOS transistor 37 and is set to "1" level. Node 47 is charged via the current paths of P-channel MOS transistors 44 and 45 and is set to "1" level. Therefore, N-channel MOS transistor 52 is turned on to set data Dout appearing at node 53 to "0" level.

Next, if address signal Add is changed and detection data DS from data detection circuit 20 is changed from "0" to "1" level, an output from inverter 36 is set from "0" to "1" level. As a result, node 40 which has been charged by means of P-channel MOS transistor 37 is now discharged via the serial current paths of N-channel MOS transistors 38 and 39, and the voltage level thereof is inverted to "0" level. At this time, node 47 which has been charged by means of P-channel MOS transistors 44 and 45 is now discharged via the current path of N-channel MOS transistor 46, and the voltage level thereof is also inverted to "0" level. In this way, after detection data DS is set to "1" level, P-channel MOS transistor 51 is turned on and data Dout of node 53 is inverted from "0" to "1" level. In this case, node 40 is discharged via the current paths of N-

channel MOS transistors 38 and 39 at a relatively low discharging speed, and therefore data Dout rises slowly to "1" level.

Next, if address signal Add is changed again and detection data DS from data detection circuit 20 is set to "0" level, nodes 40 and 47 are set to "1" level. As a result, N-channel MOS transistor 52 is turned on and data Dout of node 53 is inverted to "0" level. In this case, node 47 is charged via the current paths of P-channel MOS transistors 44 and 45 at a relatively low charging speed, and therefore data Dout falls slowly to "0" level.

There will now be described the operation in the output disable mode. In this operation mode, data DS from data detection circuit 20 is previously determined by address signal Add, and data Dout is supplied from output circuit 22 by activating external output enable signal $\overline{OE}$. Assume now that detection data DS is at "1" level as shown in the timing chart of Fig. 4. At this time, an output of inverter 36 in Fig. 2 is at "1" level, P-channel MOS transistors 37 and 45 are set in the nonconductive state and N-channel MOS transistors 38 and 46 are set in the conductive state.

Then, if external output enable signal $\overline{OE}$ is set to "0" level, internal output enable signals OE* and $\overline{OE}$* are respectively set to "1" and "0" levels. As a result, N-channel MOS transistor 39 is turned on and P-channel MOS transistor 43 is turned off, causing node 40 to be discharged via the serial current paths of N-channel MOS transistors 38 and 39.

When it is detected by output control circuit 23 that signal $\overline{OE}$ is changed to "0" level, pulse signals P and $\overline{P}$ from control circuit 23 are respectively set at "1" and "0" levels for a preset period of time. when signal P is at "1" level, N-channel MOS transistor 42 is turned on. Since, at this time, N-channel MOS transistor 41 is set in the conductive state, node 40 will be discharged via the current paths of N-channel MOS transistors 41 and 42 in addition to those of N-channel MOS transistors 38 and 39. Therefore, the discharging speed at which node 40 is discharged to "0" level is enhanced in comparison with the case of the active mode. As a result, P-channel MOS transistor 51 is rapidly turned on, causing data Dout to rise rapidly to "1" level.

When output data DS of data detection circuit 20 is set at "0" level, an output of inverter 36 shown in Fig. 2 is also set at "0" level. Therefore, P-channel transistors 37 and 45 are turned on and N-channel transistors 38 and 46 are turned off. When signal $\overline{OE}$ is set to "0" level, internal output enable signals OE* and $\overline{OE}$* are respectively set to "1" and "0" levels. As a result, P-channel MOS transistor 44 is turned on and N-channel MOS transistor 50 is turned off, thereby causing node 47 to be charged via the current paths of P-channel MOS transistors 44 and 45.

At this time, since signal $\overline{P}$ is set at "0" level for a preset period of time, P-channel MOS transistor 48 is turned on. Since, in this case, P-channel MOS transistor 49 is set in the conductive state, node 47 is charged via the current paths of P-channel MOS transistors 48 and 49 in addition to the case of P-channel MOS transistors 44 and 45. Therefore, the charging speed at which node 47 is charged to "1" level is enhanced in comparison with the case of the active mode. As a result, N-channel MOS transistor 52 is rapidly turned on, causing data Dout to fall rapidly to "0" level.

In the standby mode, internal output enable signals OE* and $\overline{OE}$* are respectively set to "0" and "1" levels in response to signal $\overline{OE}$. At this time, P-channel MOS transistor 43 is turned on and N-channel MOS transistor 39 is turned off so that node 40 can be set to "1" level, unconditionally setting P-channel MOS transistor 51 into the nonconductive state. Further, when N-channel MOS transistor 50 is turned on and P-channel MOS transistor 44 is turned off, node 47 is set to "0" level, unconditionally setting N-channel MOS transistor 52 into the nonconductive state. As a result, node 53 is set into the high impedance (electrically floating) condition.

As described above, in the memory device of the above embodiment, data can be rapidly read out in the output disable mode in which high operation speed is required. In this case, address signal Add has been set and then a certain period of time has passed before signal $\overline{OE}$ is activated to supply data Dout to the exterior. Therefore, even if the power source voltage has varied due to noise generation, there is no possibility of the memory device being erroneously operated.

In the active mode, the discharging operation of node 40 and the charging operation of node 47 are effected at a slower speed than in the case of the output disable mode. Thus, current will not abruptly flow in P-channel MOS transistor 51 or N-channel MOS transistor 52, suppressing the occurrence of noise.

Figs. 5 and 6 show the voltage waveforms at respective points in the memory device according to the above embodiment, Fig. 5 showing the case of the active mode and Fig. 6 showing the case of the output disable mode. Da shown in Figs. 5 and 6 is output data of column gate circuit 19. As is clearly understood from Figs. 5 and 6, output data Dout is rapidly rises to "1" level in the output disable mode than in the active mode.

Fig. 7 shows the waveforms of the signals which are generated in the circuit when the potential of node 40 and the potential of output signal Dout are rapidly lowered and raised, respectively. Data detection circuit 20 compares the data Da read from the memory cells, with the reference potential Vref, thus determining whether the data DS is at the "H" or "L" level. As is shown in Fig. 7, when the output circuit operates at high speed, the potential of node 40 starts falling, and the output node 53 is therefore charged, before the potential of the data Da deviates from the reference voltage Vref. As a result of this, a large current flows from the output buffer to the output terminal, and both the power source potential and the ground potential fluctuate. Consequently, noise is generated. The noise inverts the relationship in level between the reference potential Vref and the potential of data Da, which are not sufficiently different from each other. The data Da becomes erroneous. More specifically, the potential of this data rises above the reference potential Vref since the noise is superposed on the data Da when ΔVD is small immediately the potential of the data Da falls below potential Vref during the discharging of data Da. The sense amplifier detects this potential rise of data Da. Nonetheless, the difference ΔVD between potential Vref and the potential of data Da remains sufficiently great since both the reference potential Vref and that of data Da are fixed during period t_{OE} or period t_{PGM}, as is illustrated in Fig. 6. Hence, even if the reference potential Vref and that of data Da fluctuate because of the noise resulting from a large current flowing in the output circuit, no inversion occurs in their level relationship. This is because internal enable signal $\overline{OE}^*$ changes sufficiently long after the address has changed, as has been described above. Thus, the data Da is read out stably, and does not become erroneous. The output circuit can, therefore, operate at high speed during period t_{OE} and period t_{PMG}. During period t_{ACC}, the output circuit operates at low speed. Thus, the generation of noise is suppressed during this period even if the potential difference ΔVD is small, and the semiconductor integrated circuit makes no errors during period t_{ACC}, too.

Fig. 8 is a circuit diagram showing the detail construction of output enable/program control circuit 12 and output control circuit 23 in the memory device of the above embodiment. Pad or terminal 61 is connected to receive signal $\overline{OE}$. When internal program signal $\overline{PGM}^*$ is at "1" level and signal $\overline{CE}^*$ is at "0" level, P-channel MOS transistor 62 is turned on, N-channel MOS transistor 63 is turned off, N-channel MOS transistor 64 is turned on and P-channel MOS transistor 65 is turned off in output enable/program control circuit 12. Therefore, signal $\overline{OE}$ supplied to terminal 61 is supplied as output enable OE* via CMOS inverters 66 and 67, and output as internal output enable signal $\overline{OE}^*$ via CMOS inverter 69.

When signals CE* and $\overline{CE}^*$ are respectively set at "1" and "0" levels, P-channel MOS transistor 71 and N-channel MOS transistor 72 are turned off and N-channel MOS transistor 73 and P-channel MOS transistor 74 are turned on in output control circuit 23. At this time, an output of CMOS inverter 75 to which signal $\overline{PGM}^*$ is supplied is set to "0" level, and an output of succeeding CMOS inverter 76 is set to "1" level. The output of CMOS inverter 76 is supplied to the gates of P-channel MOS transistor 77 and N-channel MOS transistor 78 to turn off P-channel MOS transistor 77 and turn on N-channel MOS transistor 78. Therefore, an output signal of inverter 68 in circuit 12 is supplied to CMOS NAND circuit 80 including P- and N-channel MOS transistors via CMOS NAND circuit 79 which functions as an inverter. Further, an output signal of NAND circuit 79 is supplied to CMOS NAND circuit 80 via CMOS inverter 81, signal delay circuit 82 including P- and N-channel MOS transistors, CMOS inverter 83, signal delay circuit 84 with the same construction as signal delay circuit 82 and three CMOS inverters 85 to 87. A signal on output node 88 of NAND circuit 79 and that on output node 89 of inverter 87 are generated with a certain time delay from each other and are set in the inverted logic states. Therefore, a pulse signal which is set to "0" level only when signals on nodes 88 and 89 are both set at "1" level is generated from output node 90 of NAND circuit 80. The pulse signal is supplied as pulse signal P via CMOS inverter 91 and as pulse signal $\overline{P}$ via CMOS inverters 91 and 92.

Fig. 9 is a circuit diagram showing the construction of part of output circuit 22 which is provided in the memory device shown in Fig. 1 and which processes one bit of data. This output circuit has two output sections PB1 and PB2, both corresponding to pre-amplifier section PB shown in Fig. 2. The output signal of the PBO, which is equivalent to the input of pre-amplifier section PB, is supplied to output sections PB1 and PB2. The outputs of these sections PB1 and PB2 are input to two buffer amplifier sections BA1 and BA2, respectively. Pre-amplifier sections PB1 and PB2 are formed to have the construction obtained by omitting N-channel MOS transistors 41 and 42 and P-channel MOS transistors 48 and 49 from pre-amplifier section BA shown in Fig. 2. One of pre-amplifier section BA1 is connected to receive signals OE*1 and $\overline{OE^*1}$ instead of internal output enable signals OE* and $\overline{OE}^*$, and the other pre-amplifier section PB2 is connected to receive signals OE*2 and $\overline{OE^*2}$ instead of internal output enable signals OE* and $\overline{OE}^*$. Output nodes 53 of buffer amplifier sections BA1 and BA2 are connected to terminal 54. Two sets of signals OE*1 and OE*1 and signals OE*2 and $\overline{OE^*2}$ are generated at different timings from output control circuit 23.

In the output circuit with the construction described above, as shown by the timing chart of Fig. 10, internal output enable signals OE*1 and $\overline{OE*1}$ are respectively set from "0" and "1" levels to "1" and "0" levels after external output enable signal $\overline{OE}$ is activated and changed to "0" level. Therefore, buffer amplifier section BA1 is continuously operated after signal $\overline{OE}$ has been activated.

Internal output enable signals OE*2 and $\overline{OE*2}$ are set at "1" and "0" levels respectively for a preset period of time after signal $\overline{OE}$ has been activated. Thus, buffer amplifier section BA2 is operated for a preset period of time after signal $\overline{OE}$ has been activated. Then, signals OE*2 and $\overline{OE*2}$ are set to "1" and "0" levels, respectively. As a result, the operation speed of charging or discharging node 54 is enhanced and data can be read out at a higher speed in a period of time in which buffer amplifier section BA2 than in a case in which only buffer amplifier section BA1 is operated. However, in this case, the number of stages of the buffer amplifier sections is increased and therefore the output circuit becomes easily influenced by power source noise in comparison with the output circuit shown in Fig. 2.

In the embodiment shown in Fig. 9, output section PB1 and buffer amplifier section BA1 have a response speed different from that of output section PB2 and buffer amplifier section BA2. Output section PB1 and buffer amplifier section BA1 have the same response speed when transistors 42 and 48 (both shown in Fig. 2) are off. Therefore, nodes 40 and 47 of buffer amplifier section BA1 are slowly discharged and charged, respectively, whereas nodes 40 and 47 of buffer amplifier section BA2 are quickly discharged.

Substantially the same effect and operation of the circuit shown in Fig. 2 can be obtained by the circuit of Fig. 9.

The sway in the power source voltage is caused by the presence of parasitic inductance associated with the wiring layer of the power source line. That is, in a case where the output terminal is charged or discharged from the power source by means of the output buffer transistor, potential fluctuation ΔV in the power source wiring line can be expressed as follows:

$$\Delta V = Lx \cdot di/dt \quad (1)$$

where di/dt denotes variation in the current flowing in the output buffer transistor and power source wiring line and Lx denotes the inductance of the power source wiring line. Potential fluctuation ΔV is the cause of power source noise generation. As is clearly understood from equation (1), ΔV becomes small as di/dt is set to be smaller, reducing the fluctuation in the power source voltage and suppressing noise generation.

Assume now that the output terminal which has been charged to the power source potential is discharged. In this case, after the gate potential of the transistor which has been set at the power source potential is raised to the power source potential by the drain voltage, the output terminal is discharged. Therefore, di/dt is influenced by the current-voltage characteristic of the transistor. After the discharging operation is operated, the output buffer transistor is operated in the saturation region until the drain voltage becomes lower than the gate voltage by the threshold voltage. It is well known in the art that the voltage-current characteristic of the MOS transistor in the saturation region can be expressed by the following equation:

$$ID = \frac{W \cdot Cox \cdot \mu}{L \cdot 2} (VG - Vth)^2 \quad --- (2)$$

where L denotes the channel length, W the channel width, Cox the gate capacitance for each unit area, μ the mobility of electrons, VG the gate voltage, and Vth the threshold voltage.

Assume now that gate voltage VG starts to rise. In this case, in order to simplify the explanation, assume that gate voltage VG rises linearly with respect to time. Thus, if gate voltage VG rises with inclination ΔX with respect to time, gate voltage VG can be expressed as follows:

$$VG = \Delta X \cdot t \quad (3)$$

The following equation can be obtained by substituting equation (3) into equation (2):

$$ID = \frac{W \cdot Cox \cdot \mu}{L \cdot 2} (\Delta X \cdot t - Vth)^2 \quad --- (4)$$

The rate of change in current with time can be obtained by differentiating equation (4) with respect to time t, and dID/dt can be obtained as follows:

$$dID/dt = \frac{W \cdot Cox \cdot \mu}{L} (\Delta X^2 \cdot t - \Delta X \cdot Vth) \quad \text{--- (5)}$$

As is clearly seen from equation (5), the rate of change in current dID/dt varies in proportion to the square of ΔX which is the rising inclination of the gate voltage and varies in proportion to channel width W of the transistor. Therefore, the rate of change in current di/dt at the data output time can be more effectively reduced by making gentle the rising inclination of the gate voltage of the transistor to be turned on as shown in Fig. 2 than by reducing the channel width of the transistor to be turned on. Assume now that the potential of the output terminal is gradually discharged, the drain voltage of the output buffer transistor is gradually lowered and the transistor is operated in the triode operation mode. For brief explanation, assume that the voltage-current characteristic of the MOS transistor operation in the triode operation mode can be approximately expressed in the form of linear function which is attained by resistance R. Then, the relation between drain voltage VD and current ID can be expressed as follows:

$$ID = \frac{1}{R} \cdot VD \quad (6)$$

If the charge stored in capacitor C whose initial voltage is Vo is discharged via resistor R, voltage VD at time t can be expressed as follows:

$$VD = Vo \cdot e^{-\frac{t}{CR}} \quad (7)$$

The following equation can be obtained by substituting equation (7) into equation (6):

$$ID = \frac{1}{R} \cdot VD = \frac{1}{R} \cdot Vo \cdot e^{-\frac{t}{CR}} \quad (8)$$

Further, the following equation can be obtained by differentiating equation (8) with respect to time t:

$$dID/dt = -\frac{1}{CR^2} \cdot Vo \cdot e^{-\frac{t}{CR}} \quad \text{--- (9)}$$

As can be seen from equation (9), di/dt in the triode operation mode varies with the square of resistance R and has a negative value. That is, as shown in equation (1), the power source voltage will fluctuate in a negative direction. The resistance of the MOS transistor becomes larger as the channel width thereof is set to be smaller. That is, in the discharging operation in the triode operation mode after the gate voltage has been raised to the power source voltage, fluctuation in the power source voltage can be suppressed to a small value if the channel width is set to be small. Further, as described above, the effects can be obtained in proportion to the square of the channel width.

In general, the conduction resistance of the MOS transistor is determined by the channel width, and at the same time, depends on the gate voltage thereof. That is, the conduction resistance becomes smaller as the gate voltage becomes higher.

Fig. 11 is a circuit diagram showing the circuit which is constituted by taking the above effect into consideration so as to improve the circuit of Fig. 2. In the circuit of Fig. 11, voltage V1 is used to obtain a voltage lower than power source voltage Vcc by a preset voltage and voltage V2 is used to obtain a voltage higher than power source voltage Vss by a preset voltage. In the operation in the saturation region at the data output time, the rate of change in the gate voltage of the output buffer MOS transistor is reduced to improve di/dt. In the triode mode operation, the gate voltage of the output buffer MOS transistor is set to be lower than Vcc or higher than Vss so as to increase the conduction resistance of the MOS transistor, thus improving di/dt. In this case, it is possible to provide V1 and V2 only in transistors 44 and 39. This is because transistors 42 and 48 are set in the nonconductive state in a period in which it is necessary to reduce di/dt and which ranges from the change of address in the state in which signal $\overline{OE}$ is set at "0" level to the data output time.

Fig. 12 is a circuit diagram showing the circuit of Fig. 11 for generating voltages V1 and V2. Voltage V1 is generated by means of P-channel MOS transistor 101 and 102 whose gate and drain are connected

together respectively, and voltage V2 is generated by means of N-channel MOS transistor 103 and 104 whose gate and drain are connected together respectively. With this construction, a voltage which is lower than power source voltage Vcc by the threshold of the P-channel MOS transistor is supplied to MOS transistors 44 and 48, and a voltage which is higher than ground voltage Vss by the threshold voltage of the N-channel MOS transistor is supplied to MOS transistors 39 and 42.

In the example described above, the output voltage is set to have a potential difference equal to the threshold voltage of the MOS transistor, but it is possible to adjust the potential difference according to required di/dt.

Fig. 13 is a circuit diagram showing another construction of part of output circuit 22 which is provided in the memory device shown in Fig. 1 and which processes one bit of data. This output circuit has two output sections PB11 and PB12, both corresponding to pre-amplifier section PB shown in Fig. 2. The output signal of the PB10, which is equivalent to the input of pre-amplifier section PB, is supplied to output sections PB11 and PB12. The outputs of these sections PB11 and PB12 are input to two buffer amplifier sections BA11 and BA12, respectively. Each of buffer amplifier sections BA11 and BA12 is similar to buffer amplifier section BA of Fig. 2 except that N-channel MOS transistor 52 of buffer amplifier section BA11 is connected to ground terminal Vss1 and N-channel MOS transistor 52 of buffer amplifier section BA12 is connected to ground terminal Vss2. Ground terminal Vss1 or Vss2 can also be used as another ground terminal Vss.

In the circuit of the embodiment shown in Fig. 13, data can be output at a high speed by operating BA11 and BA12 when signal $\overline{OE}$ is set at "0" level to derive out data. When address is changed to output new data with signal $\overline{OE}$ kept at "0" level, BA12 is operated. At this time, signals OE*2 and $\overline{OE*2}$ are respectively set at "0" and "1" levels, and therefore variation in the gate voltage of output transistors 51 and 52 becomes gentle as in the case of the circuit shown in Fig. 2. That is, in the circuit of Fig. 13, in the saturation operation effected before data is output, the rate of change in the gate voltage is set small to suppress di/dt to a small value. Further, in the triode operation mode, only the transistor of BA12 is used to drive the output terminal and therefore the resistance thereof in the charging and discharging operations may be set to be large, suppressing di/dt to a small value. If, for example, data out put speeds attained when signal $\overline{OE}$ is set to "0" level are equal to each other in the circuits of Figs. 2 and 13, di/dt obtained in the triode operation mode when the address is changed with signal $\overline{OE}$ kept at "0" level will be more improved in the circuit of Fig. 13.

In this circuit, two different power source terminals Vss are used to distribute the total amount of current flowing into the power source terminals Vss, and therefore, variation in the power source voltage can be suppressed to a smaller value in comparison with the case where only one power source terminal Vss is used, and erroneous operation can be effectively prevented. Further, if the power source for the circuit section in which noise may be generated is separated from the power source for the circuit section which may be easily influenced by noise, influence by noise can be reduced. Two or more power sources Vcc can be provided, as well as two or more power sources Vss.

In general some of EPROMs (erasable PROM) such as a 1M-bit EPROM with 40 pins which is a sort of PROM includes two ground terminals. In such a case, ground terminals of the buffer amplifier sections in the output circuit may be divided as shown in Fig. 13 so as to suppress noise. One of previously prepared two ground lines is connected to terminals Vss1 and Vss2 which are respectively connected to transistor 52 of buffer amplifier section BA11 and transistor 52 of buffer amplifier section BA12, and the other ground line is connected to terminal Vss of Fig. 13 terminal Vss outside the buffer amplifier section. As a result of this, influence due to variation in the power source voltage caused by the discharging of Dout at the time of changing data will not be given to the circuit which is connected to the other terminal Vss. Therefore, erroneous operation of the circuit can be effectively prevented. Further, in a case where three or more ground lines are used, noise can be more effectively suppressed if the ground terminal of the buffer amplifier section is divided into a plurality of terminals. Further, if the power source for the circuit section in which noise may be generated is separated from the power source for the circuit section which may be easily influenced by noise, erroneous operation caused by noise can be reduced.

As described above, according to the above embodiment, output data can be supplied at a high speed when the high operation speed is required and the output data can be supplied at a low speed when it is required to suppress the noise occurrence.

This invention has been described with reference to the embodiments, but is to limited to the embodiments and can be variously modified. In the embodiments described above, use is made of either the first-type transistor which raises the potential of the output node toward power source Vcc level when it is turned on, or the second-type transistor which lowers the potential of the output node toward power source Vss level when it is turned on. The first-type transistor is used when the semiconductor integrated circuit includes a circuit which is more likely to make errors when power source voltage Vss changes than

when power source voltage Vss changes. The second-type transistor is used when the semiconductor integrated circuit includes a circuit which is more likely to make errors when power source voltage Vss changes than when power source voltage Vcc changes. In the above embodiment, this invention is applied to the semiconductor memory device, but this invention can be applied to any semiconductor integrated circuit having an output circuit. With the use of this invention, it becomes possible to hold the high operation speed in selected circuit sections even if the average operation speed is lowered, and to enhance the reliability by selectively lowering the operation speed of circuit sections which are easily influenced by noise.

Further, if the power source for the circuit section in which noise may be generated is separated from the power source for the circuit section which may be easily influenced by noise, the operation reliability of the circuit section which may be easily influenced by noise can be enhanced. This invention is not limited to the embodiment described above, and can be variously modified.

As described above, according to this invention, a semiconductor integrated circuit can be provided in which the high operation speed and noise reduction in the output circuit can be attained at the same time.

Claims

1. A semiconductor integrated circuit comprising:
- an output circuit (22) including an output transistor (51 or 52), said output transistor having its current path connected between a power supply voltage (Vcc or Vss) and an output node (53);
- precharge means (43 or 50) for precharging (to Vcc) or discharging (to Vss) the control electrode of the output transistor (51 or 52) before data are output so that the output transistor is non-conducting;
- means (38, 39 or 44, 45) for conditionally discharging or charging the control electrode of the output transistor (51 or 52) in accordance with an internal signal (DS) and in response to the activation of an output enable signal ($\overline{OE}$) so that the output transistor (51 or 52) is conditionally rendered conductive, and
- control means (41, 42 or 48, 49) for assisting said conditionally discharging or charging means in discharging or charging the control electrode of the output transistor (51 or 52) for a preset period of time after the output enable signal has been activated, thereby increasing the rate of reduction in the conduction resistance of the output transistor (51 or 52) for said preset period of time.

2. A semiconductor integrated circuit comprising:
- an output circuit (22) including a first (51 or 52) and a second (51' or 52') output transistor, said first and second output transistors having their current paths connected in parallel between a power supply voltage (Vcc or Vss) and an output node (54);
- precharge means (43 and 43' or 50 and 50') for precharging (to Vcc) or discharging (to Vss) the control electrodes of said first and second output transistors before data are output so that said first and second output transistors are non-conducting;
- means (38, 39 or 44, 45) for conditionally discharging or charging the control electrode of said first output transistor in accordance with an internal signal (DS) and in response to the activation of an output enable signal ($\overline{OE}$) so that said first output transistor is conditionally rendered conductive; and
- means (38', 39' or 44', 45') for conditionally discharging or charging the control electrode of said second output transistor in accordance with the internal signal and for a preset period of time after the output enable signal has been activated so that said second output transistor is conditionally rendered conductive for the preset period of time, thereby assisting said first output transistor in switching the voltage on the output node during the preset period of time.

3. A semiconductor integrated circuit according to claim 1, characterized in that said conditionally discharging or charging means (38,39) discharges by applying a voltage (V2), which is higher than the power supply voltage (Vss) by a predetermined value, to the control electrode of said output transistor (51), and said conditionally discharging or charging means (44,45) charges by applying a voltage (V1), which is lower than the power supply voltage (Vcc) by a predetermined value, to the control electrode of said output transistor (52).

4. A semiconductor integrated circuit according to claim 3, characterized in that said control means (41, 42) discharges by applying the voltage (V2) to the control electrode of said output transistor (51) and

said control means (48, 49) charges by applying the voltage (V1) to the control electrode of said output transistor (52).

5. A semiconductor integrated circuit according to claim 3, characterized in that the voltage (V2) is generated by use of a threshold voltage of the MOS transistor (103) located between said conditionally discharging or charging means (38, 39) and the power supply voltage (Vss) and connected in such a manner as to function as a diode, and the voltage (V1) is generated by use of a threshold voltage of the MOS transistor (101) located between said conditionally discharging or charging means (44, 45) and the power supply voltage (Vcc) and connected in such a manner as to function as a diode.

6. A semiconductor integrated circuit according to claim 4, characterized in that the voltage (V2) is generated by use of the threshold voltage of a MOS transistor (104) located between said control means (41, 42) and the power supply voltage (Vss) and connected in such a manner as to function as a diode, and the voltage (V1) is generated by use of a threshold voltage of a MOS transistor (102) located between said control means (48, 49) and the power supply voltage (Vcc) and connected in such a manner as to function as a diode.

7. A semiconductor integrated circuit according to claim 2, characterized by further comprising control means (41, 42, or 48, 49) for assisting said conditionally discharging or charging means in discharging or charging the control electrode of the second output transistor (51' or 52') for a preset period time after the output enable signal have been activated, thereby increasing the rate of reduction in the condition resistance of the second output transistor (51' or 52') for said preset period time, and said first (52) and second (52') output transistors are connected to different power source voltages (Vss1 and Vss2).

8. A semiconductor integrated circuit according to claim 1 or 2, characterized by comprising an array of memory cells (16), a row decoder (14) and a column decoder (15) which cooperate to select the memory cells, and data detecting circuit (20) detecting data (DS) stored in any memory cell selected by the row and column decoders (14 and 15).

9. A semiconductor integrated circuit according to claim 8, characterized in that said control signal is generated from an output enable signal ($\overline{OE}$) externally input to the semiconductor integrated circuit.

10. A semiconductor integrated circuit according to claim 1, characterized in that said control means includes a switching transistor for charging or discharging the gates of said output transistors (51 and 52), and said rate of reduction is changed by changing the effective channel width of the switching transistor.

11. A semiconductor integrated circuit according to claim 10, characterized in that said switching transistor is replaced by a plurality of switching transistors, and the number of said switching transistors which are simultaneously used to charge or discharge the gate of said output transistor (51 or 52), thereby to change said effective channel width.

12. A semiconductor integrated circuit according to claim 10 or 11, characterized in that said control means includes pulse signal generating means for generating a pulse signal (P and $\overline{P}$) when a control signal changes to a high level or a low level, and the pulse signal (P and $\overline{P}$) is used to change said effective channel width.

13. A semiconductor integrated circuit according to claim 12, characterized in that said control means turn off said output transistor (51 or 52) when said control signal is at a first logic level, and turns on said output transistor (51 or 52) when said control signal rises or falls from said first logic level.

Patentansprüche

1. Integrierte Halbleiterschaltung, die folgendes umfaßt:

- eine Ausgangsschaltung (22), die einen Ausgangstransistor (51) enthält, wobei der Strompfad des Ausgangstransistors zwischen einer Versorgungsspannung (Vcc oder Vss) und einem Ausgangsknoten (53) liegt;

- Vorlade-Einrichtungen (43 oder 50) zum Vorladen (auf Vcc) oder Entladen (auf Vss) der Steuerelektrode des Ausgangstransistors (51 oder 52) bevor Daten ausgegeben werden, so daß der Ausgangstransistor nichtleitend ist;
- Einrichtungen (38, 39, oder 44, 45) zum bedingungsweisen Entladen oder Laden der Steuerelektrode des Ausgangstransistors (51 oder 52) gemäß einem internen Signal (DS) und als Antwort auf die Aktivierung eines Ausgabe-Freigabe-Signals ($\overline{OE}$), so daß der Ausgangstransistor (51 oder 52) leitend gemacht wird, und
- Steuereinrichtungen (41, 42, oder 48, 49), die die genannten Einrichtungen zum bedingungsweisen Vorladen oder Entladen beim Vorladen oder Entladen der Steuerelektrode des Ausgangstransistors (51 oder 52) für einen voreingestellten Zeitraum nach der Aktivierung des Ausgabe-Freigabe-Signals unterstützen und dadurch das Verringerungsmaß des Leitungswiderstandes des Ausgangstransistors (51 oder 52) für den voreingestellten Zeitraum erhöhen.

2. Integrierte Kalbleiterschaltung, die folgendes umfaßt:

- eine Ausgangsschaltung (22), die einen ersten (51 oder 52) und einen zweiten (51' oder 52') Ausgangstransistor enthält, wobei die Strompfade der ersten und zweiten Transistoren zwischen einer Versorgungsspannung (Vcc oder Vss) und einem Ausgangsknoten (54) parallel geschaltet sind;
- Vorlade-Einrichtungen (43 und 43' oder 50 und 50') zum Vorladen (auf Vcc) oder Entladen (auf Vss) der Steuerelektroden der ersten und zweiten Ausgangstransistoren bevor Daten ausgegeben werden, so daß die ersten und zweiten Ausgangstransistoren nichtleitend sind;
- Einrichtungen (38, 39, oder 44, 45) zum bedingungsweisen Entladen oder Laden der Steuerelektrode des ersten Ausgangstransistors gemäß einem internen Signal (DS) und als Antwort auf die Aktivierung eines Ausgabe-Freigabe-Signals ($\overline{OE}$), so daß der Ausgangstransistor bedingungsweise leitend gemacht wird; und
- Einrichtungen (38', 39', oder 44', 45') zum bedingungsweisen Entladen oder Laden der Steuerelektrode des zweiten Ausgangstransistors gemäß dem internen Signal und für einen voreingestellten Zeitraum nach der Aktivierung des Ausgabe-Freigabe-Signals, so daß der zweite Ausgangstransistor für den voreingestellten Zeitraum leitend gemacht wird und dadurch den ersten Ausgangstransistor während des voreingestellten Zeitraums beim Schalten der Spannung am Ausgangsknoten unterstützt.

3. Integrierte Halbleiterschaltung gemäß Anspruch 1, dadurch gekennzeichnet, daß die Einrichtung zum Entladen oder Laden (38, 39) durch Anlegen einer Spannung (V2), die um einen vorbestimmten Wert höher als die Versorgungsspannung (Vss) ist, an die Steuerelektrode des genannten Ausgangstransistors (51) entlädt und die Einrichtung zum bedingungsweisen Entladen oder Laden (44, 45) durch Anlegen einer Spannung (V1), die um einen vorbestimmten Wert niedriger als die Versorgungsspannung (Vcc) ist, an die Steuerelektrode des Ausgangstransistors (52), lädt.

4. Integrierte Halbleiterschaltung gemäß Anspruch 3, dadurch gekennzeichnet, daß die Steuereinrichtung (41, 42) durch Anlegen der Spannung (V2) an die Steuerelektrode des Ausgangstransistors (51) entlädt und die Steuereinrichtung (48, 49) durch Anlegen der Spannung (V1) an die Steuerelektrode des Ausgangstransistors (52) lädt.

5. Integrierte Kalbleiterschaltung gemäß Anspruch 3, dadurch gekennzeichnet, daß die Spannung (V2) unter Verwendung einer Schwellenspannung des MOS-Transistors (103), der zwischen der bedingungsweisen Entlade- oder Ladeeinrichtung (38, 39) und der Versorgungsspannung (Vss) liegt und so angeschlossen ist, daß er als Diode arbeitet, erzeugt wird und die Spannung (V1) unter Verwendung einer Schwellenspannung des MOS-Transistors (101), der zwischen der bedingungsweisen Entlade- oder Ladeeinrichtung (44, 45) und der Versorgungsspannung (Vcc) liegt und so angeschlossen ist, daß er als Diode arbeitet, erzeugt wird.

6. Integrierte Halbleiterschaltung gemäß Anspruch 4, dadurch gekennzeichnet, daß die Spannung (V2) unter Verwendung der Schwellenspannung eines MOS-Transistors (104), der zwischen der Steuereinrichtung (41, 42) und der Versorgungsspannung (Vss) liegt und so angeschlossen ist, daß er als Diode arbeitet, erzeugt wird und die Spannung (V1) unter Verwendung der Schwellenspannung des MOS-Transistors (102), der zwischen der Steuereinrichtung (48, 49) und der Versorgungsspannung (Vcc) liegt und so angeschlossen ist, daß er als Diode arbeitet, erzeugt wird.

7. Integrierte Halbleiterschaltung gemäß Anspruch 2, gekennzeichnet durch Steuereinrichtungen (41, 42 oder 48, 49), die die bedingungsweise Entlade- oder Ladeeinrichtung beim Entladen oder Laden der Steuerelektrode des zweiten Ausgangstransistors (51' oder 52') für einen vorbestimmten Zeitraum nach der Aktivierung des Ausgabe-Freigabe-Signals unterstützen und dadurch das Verringerungsmaß des Bedingungs-widerstandes des zweiten Ausgangstransistors (51' oder 52') für den vorbestimmten Zeitraum erhöhen, wobei die ersten (52) und zweiten (52') Ausgangstransistoren mit verschiedenen Versorgungsspannungen (Vss1 und Vss2) verbunden sind.

8. Integrierte Halbleiterschaltung gemäß Anspruch 1 oder 2, gekennzeichnet durch ein Feld von Speicherzellen (16), einen Reihen-Dekodierer (14) und einen Spalten-Dekodierer (15), die bei der Auswahl der Speicherzellen zusammenwirken, und eine Daten-Detektierschaltung (20), die die, in einer beliebigen Speicherzelle abgelegten, von den Reihen- und Spalten-Dekodierern (14 und 15) ausgewählten Daten (DS) ermittelt.

9. Integrierte Halbleiterschaltung gemäß Anspruch 8, dadurch gekennzeichnet, daß das Steuersignal aus einem Ausgabe-Freigabesignal ($\overline{OE}$) erzeugt wird, das von außen in die integrierte Halbleiterschaltung eingegeben wird.

10. Integrierte Halbleiterschaltung gemäß Anspruch 1, dadurch gekennzeichnet, daß die Steuereinrichtung einen Schalt-Transistor zum Laden oder Entladen der Gates der Ausgangstransistoren (51 und 52) enthält und das Verringerungsmaß durch Ändern der effektiven Kanalbreite des Schalt-Transistors verändert wird.

11. Integrierte Halbleiterschaltung gemäß Anspruch 10, dadurch gekennzeichnet, daß der genannte Schalt-Transistor durch mehrere Schalt-Transistoren ersetzt wird und daß die Anzahl der Schalt-Transistoren, die gleichzeitig zum Laden oder Entladen des Gates des Ausgangstransistors (51 oder 52) benutzt werden, verändert wird, um so die effektive Kanalbreite zu verändern.

12. Integrierte Halbleiterschaltung gemäß Anspruch 10 oder 11, dadurch gekennzeichnet, daß die Steuereinrichtung eine Vorrichtung zur Erzeugung von Impulssignalen einschließt, die ein Impulssignal (P und $\overline{P}$) erzeugt, wenn ein Steuersignal zu einem hohen Pegel oder einem niedrigen Pegel wechselt und daß das Impulssignal (P und $\overline{P}$) zum Verändern der effektiven Kanalbreite benutzt wird.

13. Integrierte Halbleiterschaltung gemäß Anspruch 12, dadurch gekennzeichnet, daß die Steuereinrichtung den Ausgangstransistor (51 oder 52) ausschaltet, wenn das Steuersignal auf einem ersten logischen Pegel liegt, und den Ausgangstransistor (51 oder 52) einschaltet, wenn das Steuersignal vom ersten logischen Pegel aus ansteigt oder abfällt.

Revendications

1. Circuit intégré à semiconducteur comprenant :

un circuit de sortie (22) incluant un transistor de sortie (51 ou 52), ledit transistor de sortie ayant sa voie de courant connectée entre une tension d'alimentation (Vcc ou Vss) et un noeud de sortie (53) ;

un moyen de précharge (43 ou 50) pour précharger (à Vcc) ou pour décharger (à Vss) l'électrode de commande du transistor de sortie (51 ou 52) avant que des données ne soient émises en sortie de telle sorte que le transistor de sortie soit non conducteur ;

un moyen (38, 39 ou 44, 45) pour décharger ou charger de façon conditionnelle l'électrode de commande du transistor de sortie (51 ou 52) en relation avec un signal interne (DS) et en réponse à l'activation d'un signal de validation de sortie ($\overline{OE}$) de telle sorte que le transistor de sortie (51 ou 52) soit rendu conducteur de façon conditionnelle ; et

un moyen de commande (41, 42 ou 48, 49) pour assister ledit moyen de décharge ou de charge conditionnelle lors de la décharge ou de la charge de l'électrode de commande du transistor de sortie (51 ou 52) pendant une période temporelle pré-établie après que le signal de validation de sortie a été activé d'où il résulte que le faux de réduction de la valeur de résistance de conduction du transistor de sortie (51 ou 52) est augmenté pour ladite période temporelle pré-établie.

2. Circuit intégré à semiconducteur comprenant :

un circuit de sortie (22) incluant un premier (51 ou 52) et un second (51' ou 52') transistors de

sortie, lesdits premier et second transistors de sortie ayant leurs voies de courant connectées en parallèle entre une tension d'alimentation (Vcc ou Vss) et un noeud de sortie (54);

un moyen de précharge (43 et 43' ou 50 et 50') pour précharger (à Vcc) ou décharger (à Vss) les électrodes de commande desdits premier et second transistors de sortie avant que les données ne soient émises en sortie de telle sorte que lesdits premier et second transistors de sortie soient non conducteurs ;

un moyen (38, 39 ou 44, 45) pour décharger ou charger de façon conditionnelle l'électrode de commande dudit premier transistor de sortie en relation avec un signal interne (DS) et en réponse à l'activation d'un signal de validation de sortie ($\overline{OE}$) de telle sorte que ledit premier transistor de sortie soit rendu conducteur de façon conditionnelle ; et

un moyen (38', 39' ou 44', 45') pour décharger ou charger de façon conditionnelle l'électrode de commande dudit second transistor de sortie en relation avec un signal interne pendant une période temporelle pré-établie après que le signal de validation de sortie a été activé de telle sorte que ledit second transistor de sortie soit rendu conducteur de façon conditionnelle pendant la période temporelle pré-établie, ce qui aide ledit premier transistor de sortie à commuter la tension sur le noeud de sortie pendant la période temporelle pré-établie.

3. Circuit intégré à semiconducteur selon la revendication 1, caractérisé en ce que ledit moyen de décharge ou de charge conditionnelle (38, 39) réalise une décharge en appliquant une tension (V2) qui est supérieure à la tension d'alimentation (Vss) d'une valeur prédéterminée à l'électrode de commande dudit transistor de sortie (51) et ledit moyen de décharge ou de charge conditionnelle (44, 45) réalise une charge en appliquant une tension (V1) qui est inférieure à la tension d'alimentation (Vcc) d'une valeur prédéterminée à l'électrode de commande dudit transistor de sortie (52).

4. Circuit intégré à semiconducteur selon la revendication 3, caractérisé en ce que ledit moyen de commande (41, 42) réalise une décharge en appliquant la tension (V2) à l'électrode de commande dudit transistor de sortie (51) et ledit moyen de commande (48, 49) réalise une charge en appliquant la tension (V1) à l'électrode de commande dudit transistor de sortie (52).

5. Circuit intégré à semiconducteur selon la revendication 3, caractérisé en ce que la tension (V2) est générée au moyen de l'utilisation d'une tension de seuil du transistor métal-oxyde-semiconducteur (MOS) (103) situé entre ledit moyen de décharge ou de charge conditionnelle (38, 39) et la tension d'alimentation (Vss) et connecté de manière à fonctionner en tant que diode et la tension (V1) est générée au moyen de l'utilisation d'une tension de seuil du transistor MOS (101) situé entre ledit moyen de décharge ou de charge conditionnelle (44, 45) et la tension d'alimentation (Vcc) et connecté de manière à fonctionner en tant que diode.

6. Circuit intégré à semiconducteur selon la revendication 4, caractérisé en ce que la tension (V2) est générée au moyen de l'utilisation de la tension de seuil du transistor métal-oxyde-semiconducteur (MOS) (104) situé entre ledit moyen de commande (41, 42) et la tension d'alimentation (Vss) et connecté de manière à fonctionner en tant que diode et la tension (V1) est générée au moyen de l'utilisation d'une tension de seuil d'un transistor MOS (102) situé entre ledit moyen de commande (48, 49) et la tension d'alimentation (Vcc) et connecté de manière à fonctionner en tant que diode.

7. Circuit intégré à semiconducteur selon la revendication 2, caractérisé en ce qu'il comprend en outre un moyen de commande (41, 42 ou 48, 49) pour aider ledit moyen de décharge ou de charge conditionnelle à décharger ou à charger l'électrode de commande du second transistor de sortie (51' ou 52') pendant une période temporelle pré-établie après que le signal de validation de sortie a été activé, ce qui augmente le taux de réduction de la valeur de résistance de conduction du second transistor de sortie (51' ou 52') pendant ladite période temporelle prédéterminée, et lesdits premier (52) et second (52') transistors de sortie sont connectés à des tensions d'alimentation différentes (Vss1 et Vss2).

8. Circuit intégré à semiconducteur selon la revendication 1 ou 2, caractérisé en ce qu'il comprend un réseau de cellules de mémoire (16), un décodeur de rangée (14) et un décodeur de colonne (15) qui coopèrent pour sélectionner les cellules de mémoire et un circuit de détection de données (20) qui détecte les données (DS) stockées dans une quelconque cellule de mémoire sélectionnée par les décodeurs de rangée et de colonne (14 et 15).

9. Circuit intégré à semiconducteur selon la revendication 8, caractérisé en ce que ledit signal de commande est généré à partir d'un signal de validation de sortie ($\overline{OE}$) entré de manière externe sur le circuit intégré à semiconducteur.

10. Circuit intégré à semiconducteur selon la revendication 1, caractérisé en ce que ledit moyen de commande inclut un transistor de commutation pour charger ou décharger les grilles desdits transistors de sortie (51 et 52) et ledit taux de réduction est modifié en modifiant la largeur de canal efficace du transistor de commutation.

11. Circuit intégré à semiconducteur selon la revendication 10, caractérisé en ce que ledit transistor de commutation est remplacé par une pluralité de transistors de commutation et en ce que le nombre desdits transistors de commutation qui sont simultanément utilisés pour charger et décharger la grille dudit transistor de sortie (51 ou 52) est choisi pour ainsi modifier ladite largeur de canal efficace.

12. Circuit intégré à semiconducteur selon la revendication 10 ou 11, caractérisé en ce que ledit moyen de commande inclut un moyen de génération de signal impulsionnel pour générer un signal impulsionnel (P et ($\overline{P}$)) lorsqu'un signal de commande passe d'un niveau haut à un niveau bas et le signal impulsionnel (P et ($\overline{P}$)) est utilisé pour modifier ladite largeur de canal efficace.

13. Circuit intégré à semiconducteur selon la revendication 12, caractérisé en ce que ledit moyen de commande bloque ledit transistor de sortie (51 ou 52) lorsque ledit signal de commande est à un premier niveau logique et rend passant ledit transistor de sortie (51 ou 52) lorsque ledit signal de commande croît ou décroît à partir dudit premier niveau logique.

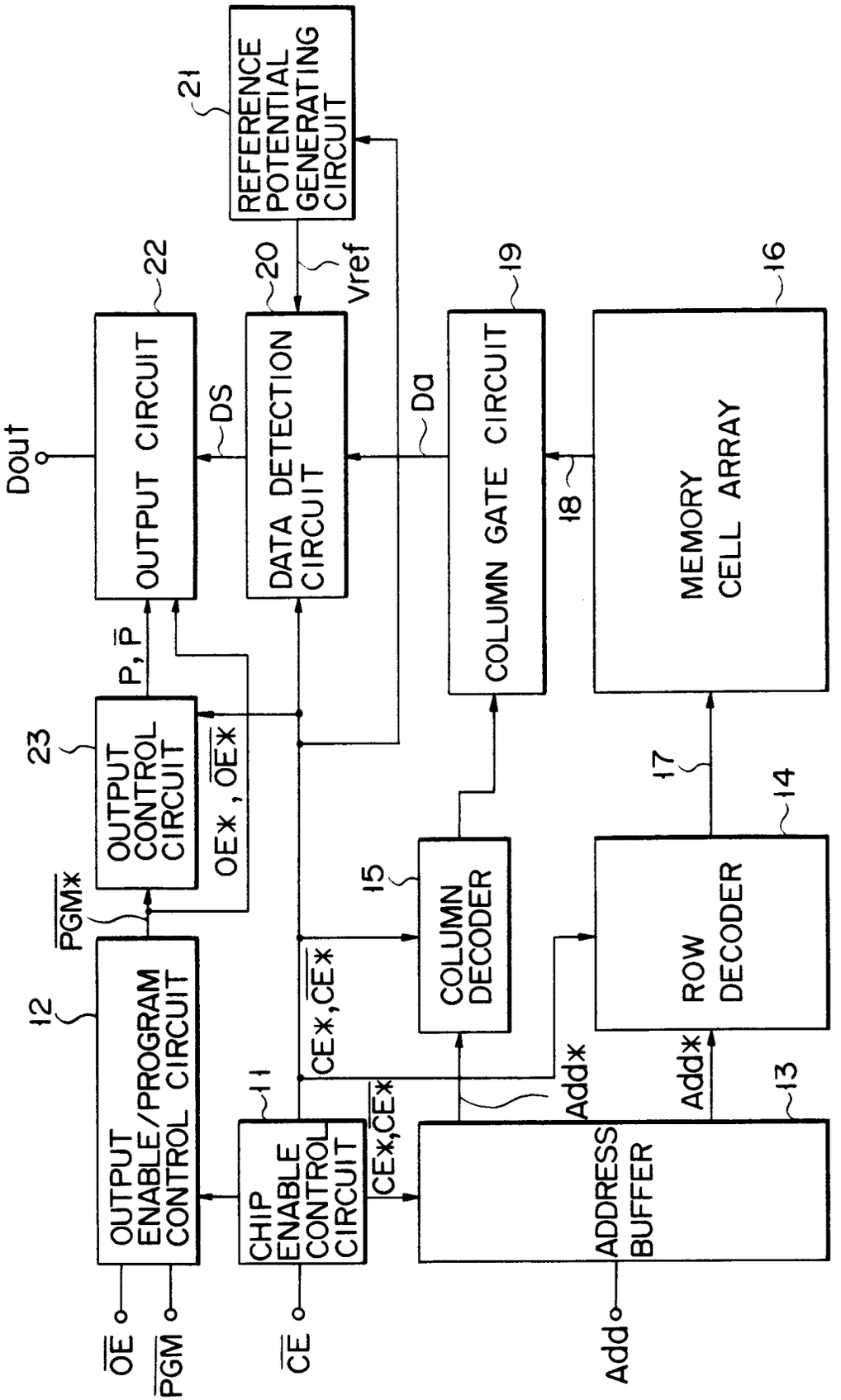

REFERENCE POTENTIAL GENERATING CIRCUIT
21
Vref
DATA DETECTION CIRCUIT
20
OUTPUT CIRCUIT
22
Dout
DS
Da
COLUMN GATE CIRCUIT
19
MEMORY CELL ARRAY
16
18
OUTPUT CONTROL CIRCUIT
23
P, P̄
OEx , OEx
COLUMN DECODER
15
ROW DECODER
14
17
PGMx
OUTPUT ENABLE/PROGRAM CONTROL CIRCUIT
12
CEx,CEx
CHIP ENABLE CONTROL CIRCUIT
11
Addx
Addx
ADDRESS BUFFER
13
OE
PGM
CE
Add

FIG. 1

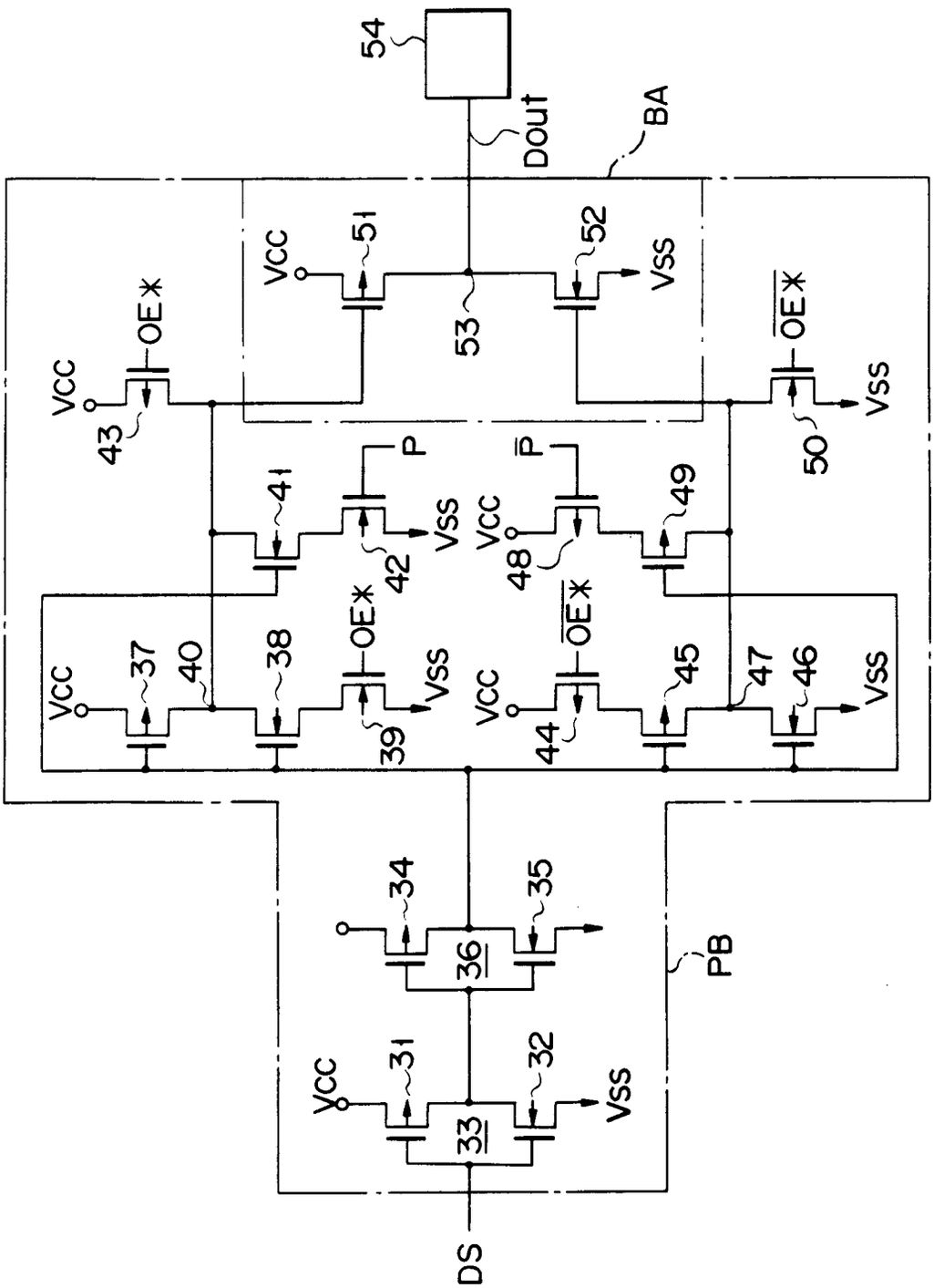

54
Dout
BA
VCC
51
52
Vss
53
OE*
43
50
41
P
42
48
49
37
40
38
39
44
45
47
46
34
35
36
PB
31
32
33
DS

FIG. 2

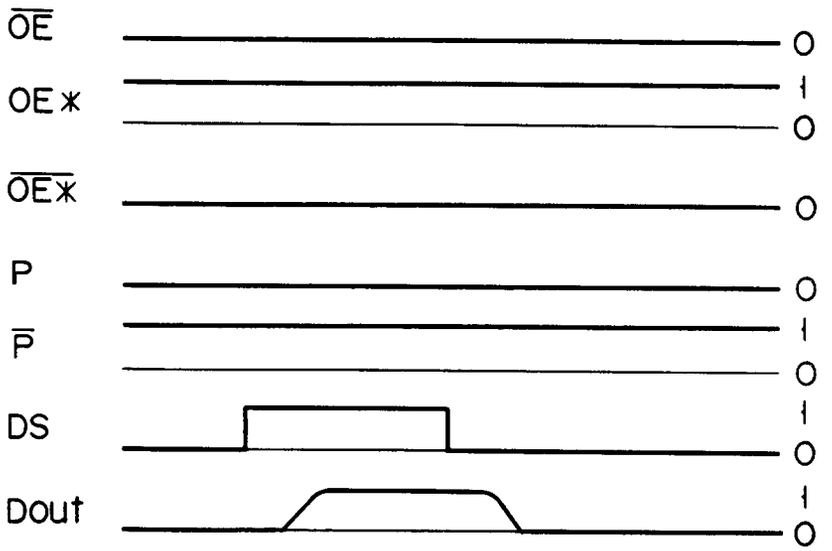

$\overline{OE}$
OE*
$\overline{OE*}$
P
$\overline{P}$
DS
Dout

FIG. 3

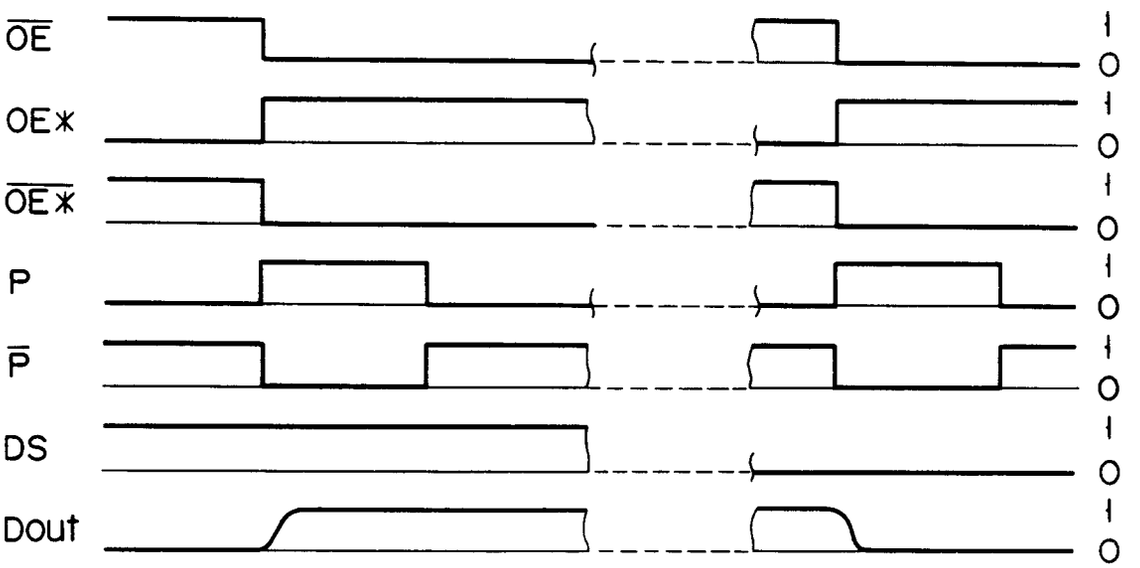

$\overline{OE}$
OE*
$\overline{OE*}$
P
$\overline{P}$
DS
Dout

FIG. 4

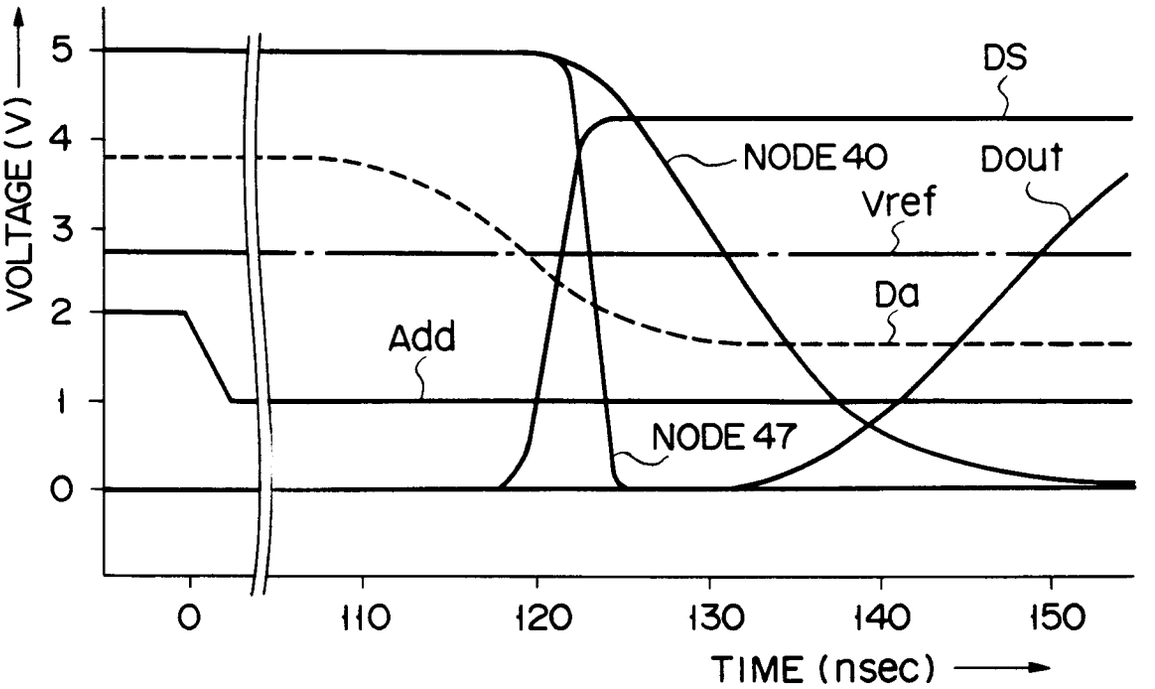

VOLTAGE (V)
5
4
3
2
1
0
DS
NODE 40
Dout
Vref
Da
Add
NODE 47
0
110
120
130
140
150
TIME (nsec)

FIG. 5

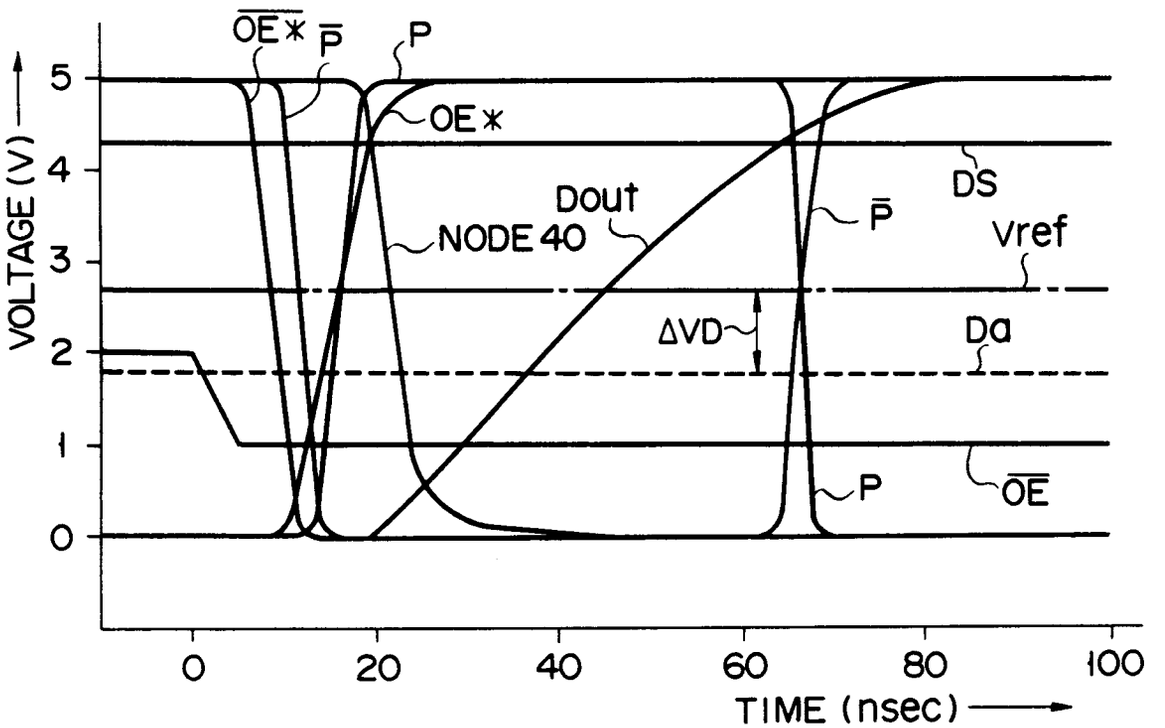

OE*
P
OE*
VOLTAGE (V)
5
4
3
2
1
0
Dout
NODE 40
DS
Vref
ΔVD
Da
OE
0
20
40
60
80
100
TIME (nsec)

FIG. 6

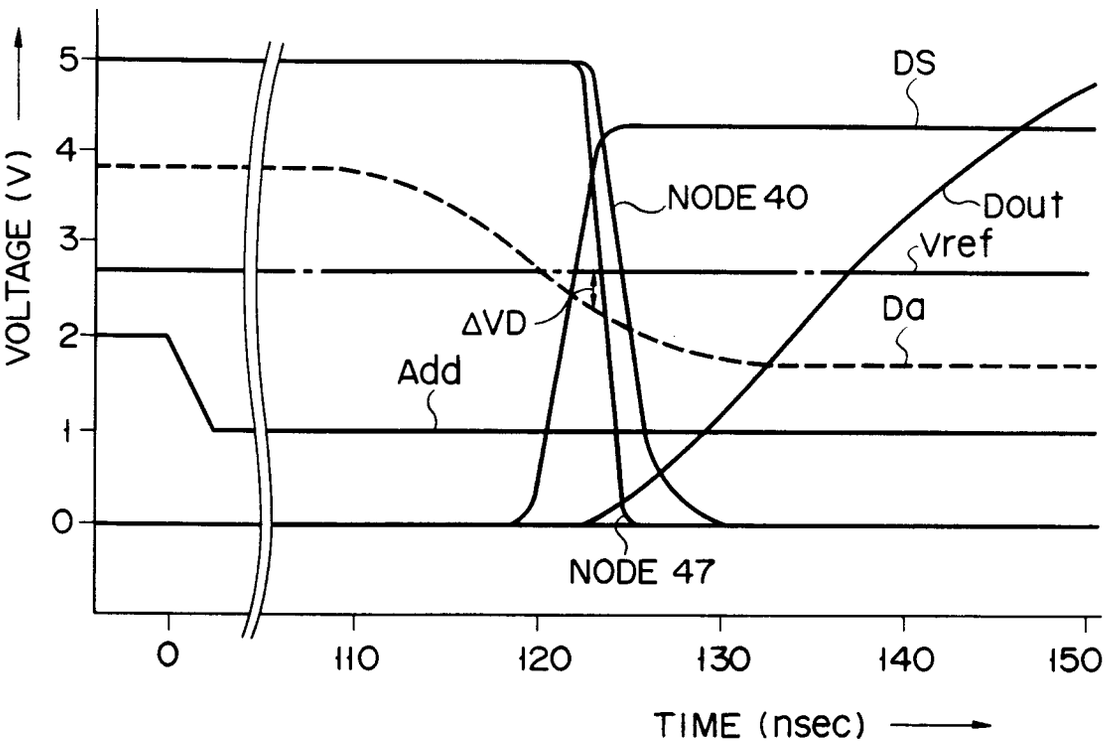
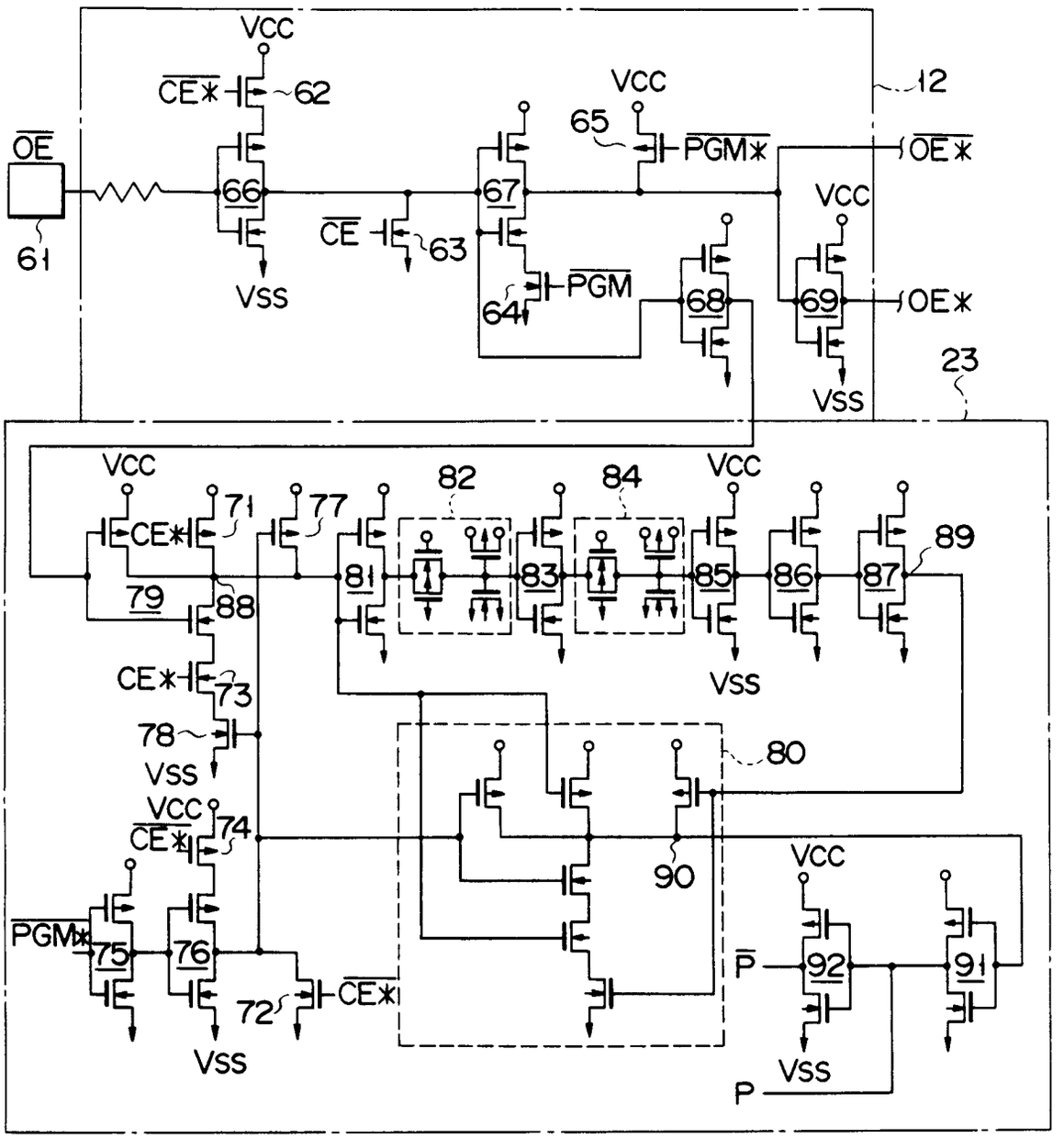

VOLTAGE (V)
5
4
3
2
1
0
DS
NODE 40
Dout
Vref
Da
ΔVD
Add
NODE 47
0
110
120
130
140
150
TIME (nsec)

FIG. 7


VCC
CE*
62
OE
66
61
VSS
CE
63
VCC
65
PGM*
67
OE*
12
64
PGM
68
69
VCC
OE*
VSS
23
VCC
71
77
82
84
VCC
89
CE*
81
83
85
86
87
79
88
VSS
CE*
73
78
VSS
80
VCC
CE*
74
90
VCC
PGM*
75
76
P
92
91
72
CE*
VSS
VSS
P

F I G. 8

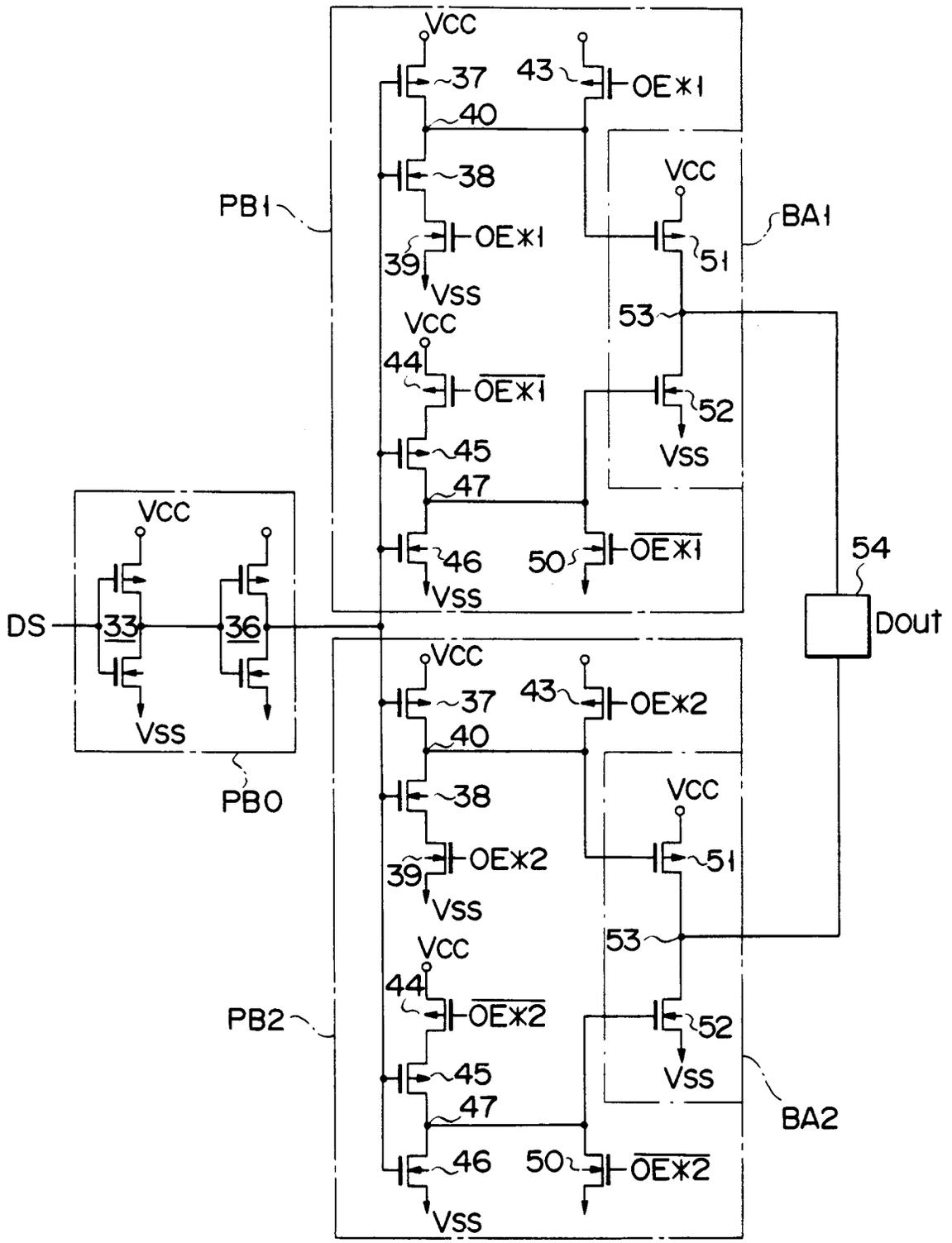

VCC
37
43
OE*1
40
38
VCC
PB1
BA1
OE*1
51
39
VSS
53
VCC
44
OE*1
52
45
VSS
47
VCC
54
46
50
OE*1
VSS
DS
33
36
Dout
VCC
VCC
37
43
OE*2
40
VSS
38
VCC
PB0
OE*2
51
39
VSS
53
VCC
44
PB2
OE*2
52
45
VSS
47
BA2
46
50
OE*2
VSS

FIG. 9

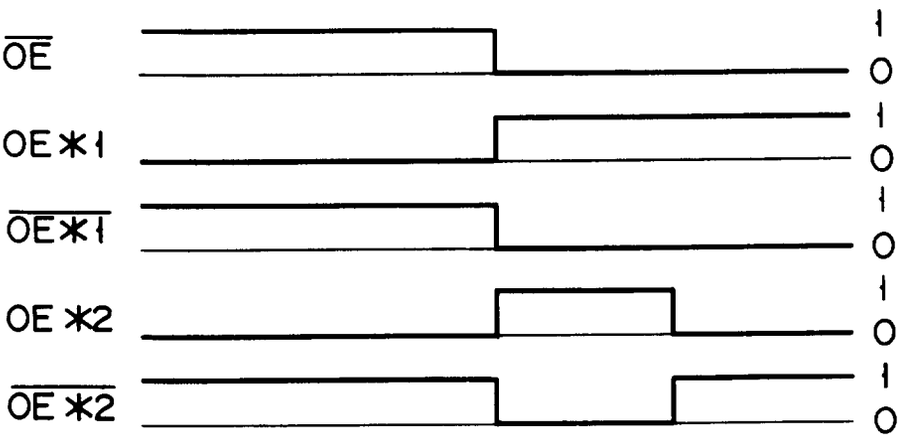


FIG. 10

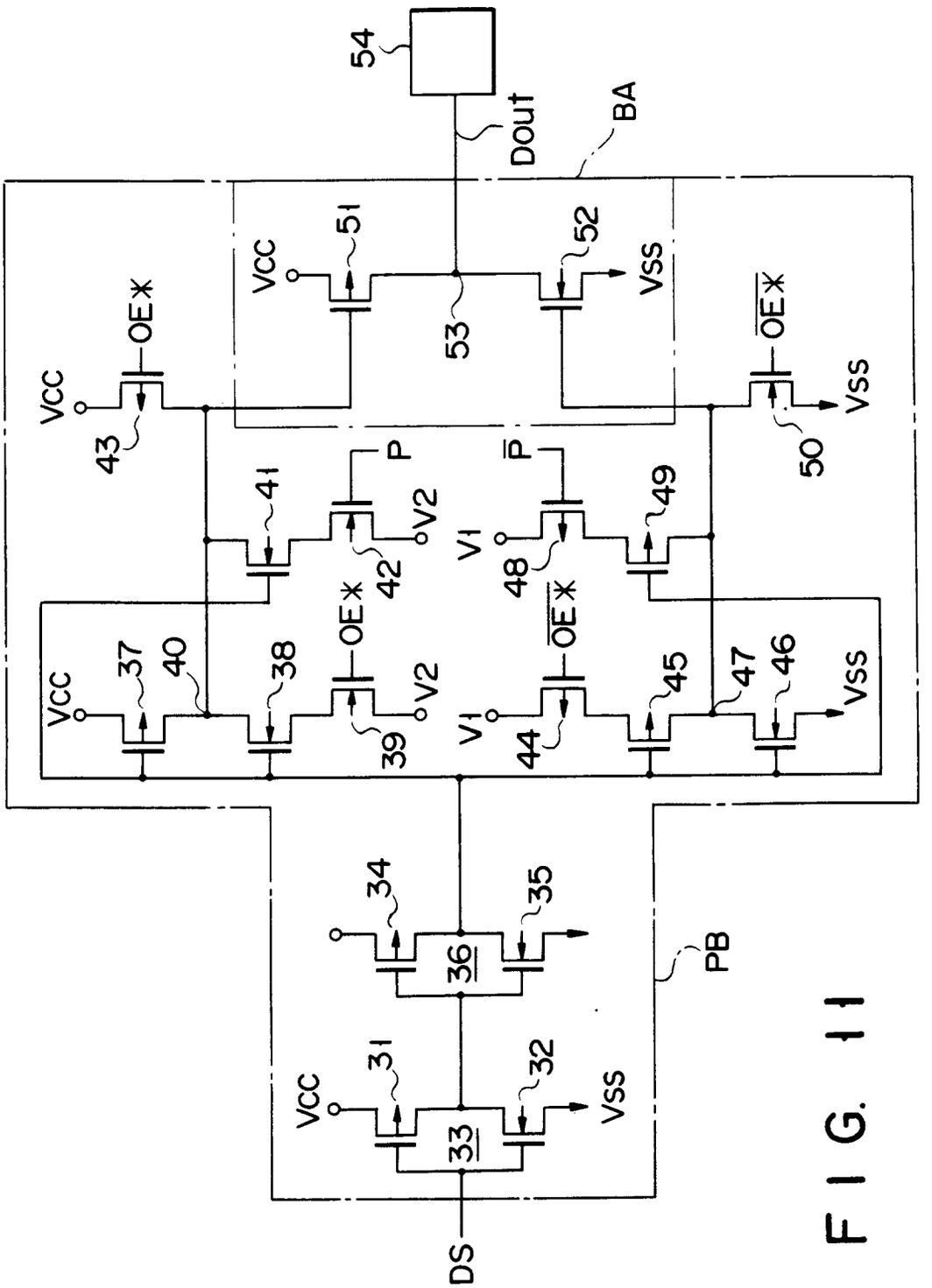

54
DOut
BA
VCC
51
52
VSS
53
OE*
43
41
P
V2
42
V1
48
49
50
37
40
38
39
44
45
47
46
34
35
36
PB
31
32
33
DS

FIG. 11

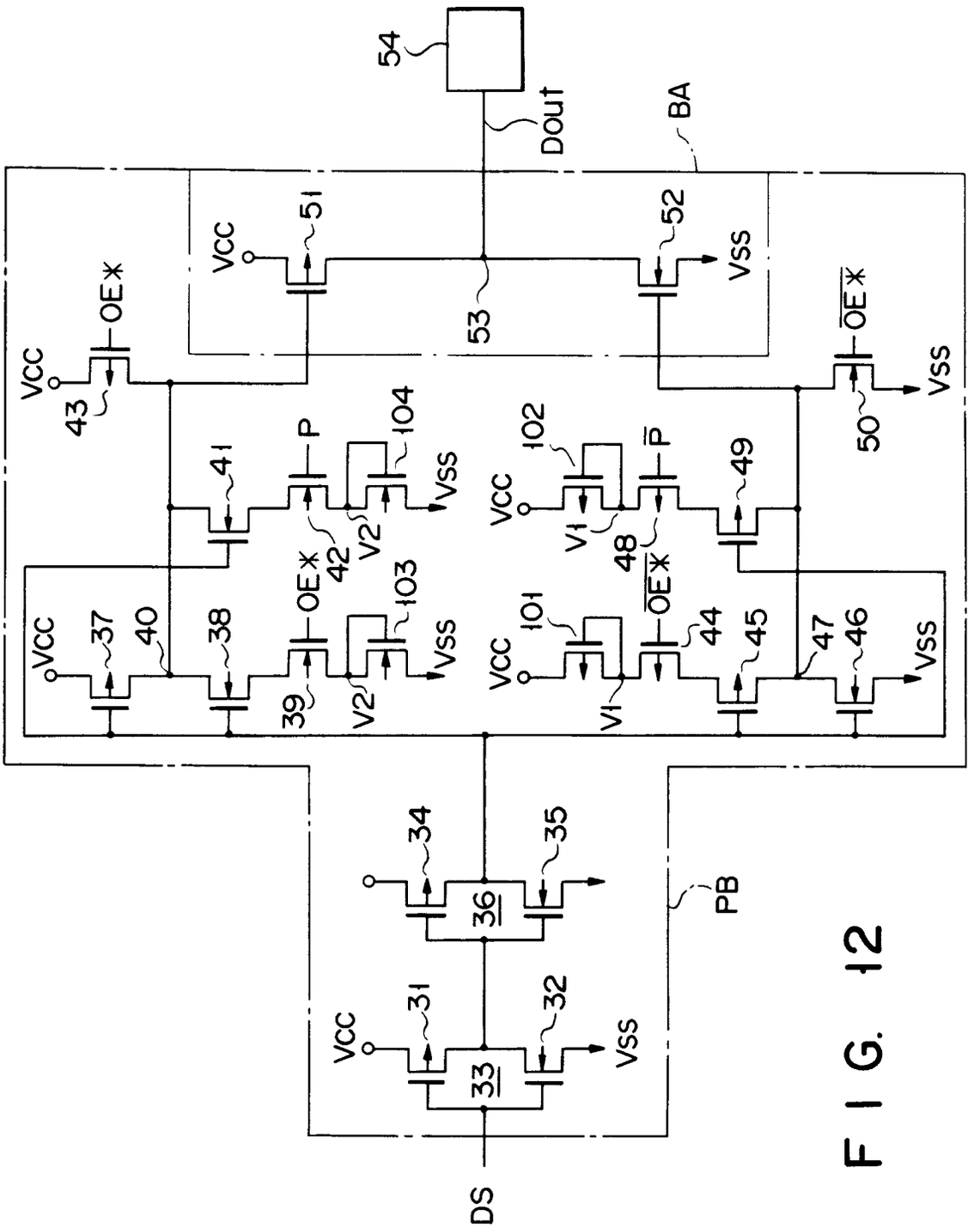

54
DOut
BA
Vcc
51
52
Vss
53
OE*
43
41
P
104
42
V2
102
V1
49
48
37
40
38
103
39
101
44
45
47
46
50
34
35
36
PB
31
32
33
DS

FIG. 12

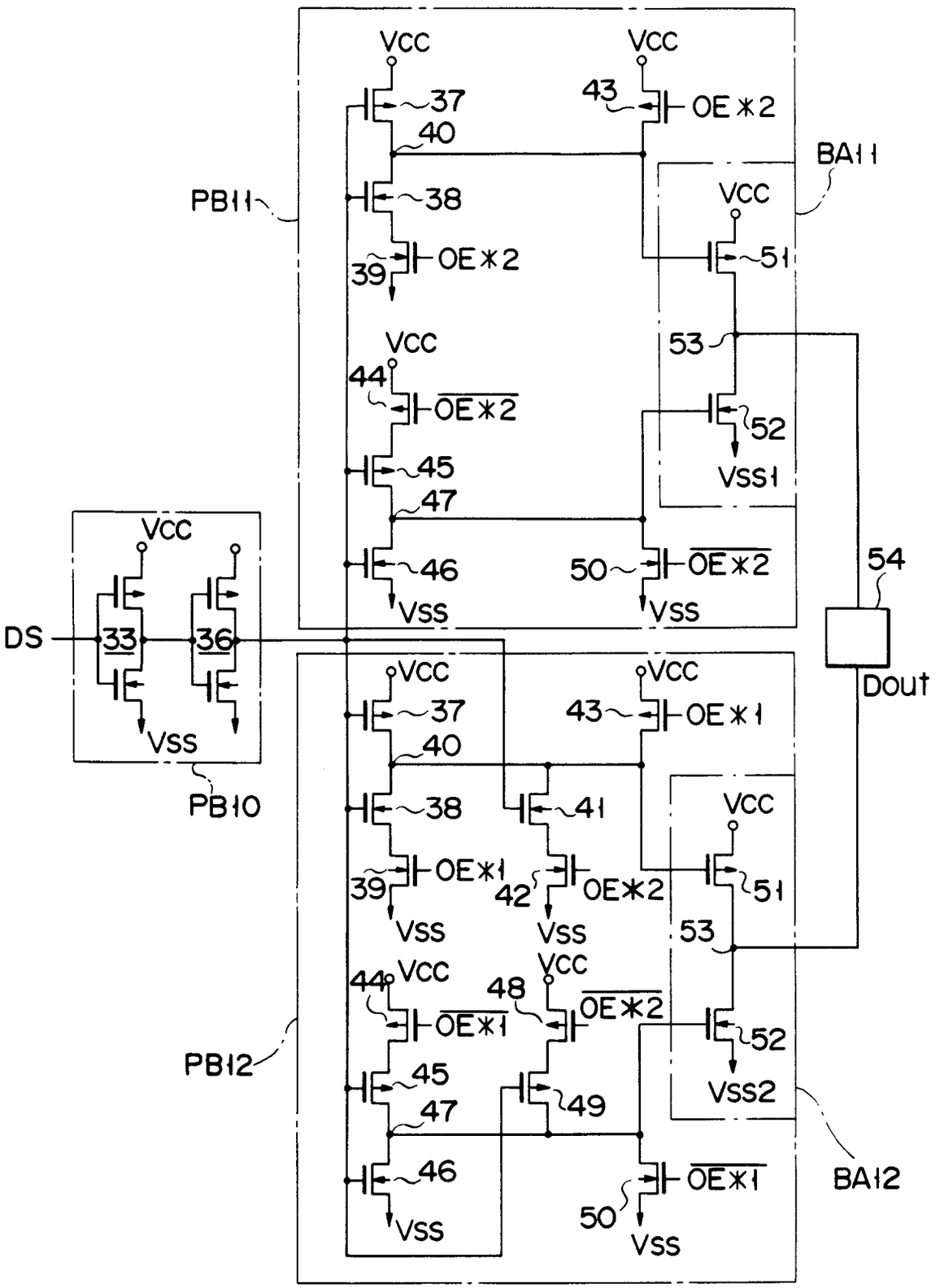

VCC
VCC
37
43
OE*2
40
BA11
PB11
38
VCC
39
OE*2
51
53
VCC
44
OE*2
52
45
Vss1
47
VCC
54
46
50
OE*2
Vss
Vss
DS
33
36
Dout
Vss
PB10
VCC
VCC
37
43
OE*1
40
38
41
VCC
39
OE*1
42
OE*2
51
Vss
Vss
53
VCC
VCC
44
48
OE*1
OE*2
52
PB12
45
Vss2
49
47
46
OE*1
BA12
50
Vss
Vss

FIG. 13