The document describes a power-saving CAM (Content Addressable Memory) circuit. It explains how the memory word of the CAM is subdivided into smaller sub-words, each associated with a match line. The first match line of a memory word is always precharged, but subsequent match lines are pre-charged only if the preceding sub word has been found matching. The speed of operation is increased by time-interlacing the search cycles of successive search operations. The memory cells have a single subword and a command line associated with each memory cell, allowing for arbitrary size searching.
Power Saving CAM

Background of the Invention

In Content Addressable Memories (CAM, or CAM array) of the known type, words of memory storing a given data can be searched, and their position found by presenting this data to the memory. Each CAM Cell, storing one word of memory, comprises a comparator that compares the data stored in it with the searched data. The searched data is set on a number of bit lines, and these bit lines are routed to the CAM Cells of the memory array. Whenever the comparator of a CAM Cell detects equality between the data stored in the word, and the searched data (“Match”), then this comparator outputs a signal which initiates a process that outputs the address of one of the matching words.

In CAMs of the known type, this comparator is implemented by means of a precharged line – Match Line - associated to each CAM Cell. The CAM Cell, being able to store and compare a word of data, is composed of a number of CAM-bit cells, each one able to store 1 bit of data. A logic circuit is then associated with each CAM-bit cell, that discharges the Match Line whenever the data stored in the CAM-bit cell is different from the data set on the bit lines. Examples of such circuit are shown in Hisatada and all, IEEE journal of solid-state circuits, vol. 36 No. 6, June 2001.

This kind of design has been preferred for CAMs because discharging can be done at high speed, and it allows a high speed for the detection of the matching condition. However, a significant drawback of this design is that, in typical applications, match does not occur for the great majority of CAM cells, so that the Match Lines of this great majority of cells are all discharged. This results in a very high power consumption of the CAM device.

In another aspect of CAM applications, it is often required to search strings having a variable number of words and at variable positions in the array. In that case the searching operation may be done in several steps, one word of the string being searched in each step, and logical circuitry may then be used to detect successive matches at contiguous positions, indicating a string match. Similarly in this case, all comparators detecting a mismatch will discharge the associated match lines, thus resulting in a high power consumption.

It is therefore desirable to design a Content Addressable Memory where the power used to charge the match lines is reduced so as to reduce memory power consumption.

In US 6,191,970 to Pereira, a design is shown that reduces the power consumption. In this design, the match line is divided in several sections. The first section is discharged in the same way as for a normal CAM, but the following sections are discharged conditionally, depending on the matching condition of the previous section.

This design reduces power consumption, however it has the following disadvantages:
a) To avoid discharge, a transistor must be added in each CAM bit cell, that prevents the discharge in case previous match line was discharged. These transistors add a very significant delay in the discharge time.

b) One transistor is added in every CAM bit cell, resulting in a large number of transistors, thus adding a significant silicone area to the total CAM area.

c) The state of the match line is by default “Match”, so that if the match line has not been discharged because a previous one was discharged, a logic circuit must be added to discard this false match condition.

It is therefore desirable to design a circuit and a method that can be used in a CAM in order to enable significant reduction of power consumption, without reducing the speed of operation, and with a minimum addition to the circuit area.

Summary of the Invention:

The invention concerns a CAM memory with conditional precharge circuits and a method of searching data in the said CAM memory that enable reduced power consumption. The CAM bit cells of each CAM cell are subdivided in groups, each group constituting a Sub Word and each Sub Word being associated with a Match line. The first Match Line, associated with the first Subword, is always precharged, but consecutive Match Lines are pre-charged only on the condition that the preceding Sub-word has been found matching. The speed of operation is similar to that of CAM’s of the known type, and the number of search operations per second can be increased by time-interlacing the search cycles of successive search operations. In accordance with a further aspect of the invention, each of the CAM cells stores a single subword and a conditional pre-charge circuit is disposed between two consecutive CAM Cells, the conditional pre-charge circuit receiving as input a Command signal to define the starting point of a new comparison unit whereby words of arbitrary size may be searched.

Brief description of the drawings:

Fig 1: Shows a general block diagram of a CAM of the known type.

Fig 2: Shows a more detailed block diagram of one CAM Cell of the known type and the associated circuits.

Fig 3: Shows a block diagram of a preferred embodiment of a CAM Cell designed according to the principle of this invention.

Fig 4: Shows how the searching cycles can be time-interlaced in order to increase the number of searching cycles per time unit.

Fig 5: shows an embodiment where, for each CAM-Cell, the word of memory is divided in several sub-words, and one Match Line is defined for each Sub-word.

Fig 6: shows a CAM array comprising a great number of CAM cells, each CAM cell being able to store one Sub-word, with a conditional pre-charge circuit disposed
between two consecutive CAM Cells, the conditional pre-charge circuit receiving as input a Command signal to define the starting point of a new comparison unit.

**Detailed Description of the Invention in Respect of a Preferred Embodiment:**

The present invention relates to a method and circuit that can be used in a CAM in order to significantly reduce power consumption, without reducing the speed of operation, and with a minimum addition to the circuit area.

In order to better clarify the invention, a CAM of the known type will be first described, and the inventive CAM with reduced power consumption will be described in reference to this CAM; however it must be understood that the principle of the invention hereinbelow can be applied to any type of CAM.

In Fig 1 is shown a CAM of the existing type. An array of CAM Cells is able to store a number of words. To each CAM Cell, a comparator and a Match Line are associated. The output of the comparator is a signal set on the Match Line. Commonly, a Searching Cycle will comprise three main steps:

- In a first step, a Precharge circuit, activated by a control circuit, will charge the Match Line to a pre-defined first potential, Charge-potential.
- In a second step, the comparators are activated, and if mismatch occurs at a CAM-Cell, then the associated Match Line is discharged to a pre-defined second potential, Discharge-potential.
- In a third step, the potential of the Match Line is evaluated. If it is at the Charge-potential, then it indicates a Match condition. The Match Signal is then input to an Address Output circuit that will output the address of one of the CAM Cells for which a Match condition was found.

In Fig 2, a more detailed description of such a CAM-Cell is shown. A Compare register is used to store the searched data during the compare operation. The data of the Compare register is conveyed to all the CAM-Cells by means of the bit lines. Each CAM bit Cell is able to store one bit of data, and to compare the stored bit with the data set on the bit lines. If there is a match, the CAM-bit Cell will set a Bit-Match signal to a low potential. If there is a mismatch, the Bit-Match signal will be set to a High potential. This Bit-Match signal is then applied to the gate of a transistor connecting the Match Line to the Discharge Potential. If any bit of the word stored in the CAM has non-matching data, then the bit Match signal will be high. The transistor will then be made conducting and the Match line will be discharged, i.e. connected to the Discharge-potential. Example of such a CAM bit Cell is shown in paper by Hisatada and all, IEEE journal of solid-state circuits, vol. 36 No. 6, June 2001, page 959 Fig 3.

The CAM-Cell is operated in three steps:

- In the first step, the Match Line is precharged, and all the CAM-bit-Cells have been disabled for comparison, i.e. all bit-match signals are kept low.
- In the second step, the precharging is stopped, the data to be searched is set on the bit lines, and the comparison is enabled for each CAM-bit Cell. If any CAM-Bit Cell is storing non-matching data, the Bit Match signal will be high, and the Match Line will be discharged, as explained before.
In the third state, the potential of the Match Line is evaluated by other circuits of the CAM (not shown here), typically to output the address of one of the CAM-Cells having matching data.

In Fig 1 and 2 a Control Circuit is shown that controls the Precharge and comparison operations. It must be understood that the control of the three steps mentioned above could be implemented in many different ways, and the Control Circuit is shown here only for general understanding.

The invention will be now described in respect of a preferred embodiment, with reference to Fig. 3. It will be understood however that many variations and modifications of the invention may be made that still remain within the scope of the description and the claims.

In Fig 3 a new design of the CAM-Cell is shown, designed for the purpose of reducing the power consumption of the CAM.

The CAM-Bit Cells of each CAM-Cell have been divided in two groups, or Sub-words, each Sub-word associated with a Match Line. The first Match Line, associated with the first Sub-word, is connected to a Precharge circuit, in a similar way as described above in Fig 2. The second Match Line is connected to a modified Precharge circuit further called here a Conditional Precharge circuit. This Conditional Precharge circuit receives as input the signal set on the first Match Line, and its function will be to Precharge the second Match Line only if the first Match Line has not been discharged during the compare cycle, i.e. if a match was found in first sub-word. If the first Match Line has been discharged, then the Conditional Precharge circuit will not precharge the second Match line or it will discharge the second Match line in case that it was left charged by an eventual previous comparison cycle. Other functions of the CAM-Cell will be similar to that described in reference to Fig 2.

In accordance with the inventive method, the CAM-Cell of the invention is now operated through the following steps:

Step 1: The first Match Line is Precharged, the Precharge circuit being activated by a Control Circuit, and all CAM-Bit Cells are disabled for comparison.

Step 2: The Precharge circuit is disabled, and a comparison is enabled on the first Sub-word. If there is a match, then the first Match Line remains charged, otherwise it is discharged.

Step 3: The Conditional Precharge circuit is enabled by the control circuit. It will then Precharge the second Match Line only if the first Match Line is charged, i.e. if the first Sub-word has matching data, otherwise it will discharge that second Match Line.

Step 4: The Conditional Precharge circuit is disabled, The CAM-bit cells of the second Sub-Word are enabled for comparison, and the Second Match Line is discharged if a mismatch occurs at any bit of the second Sub-Word.

Step 5: The state of the Second Match Line is evaluated: If the Second Match Line remained charged, then there was a match for the whole word stored in the CAM Cell.

It will be understood by those versed in the art that in many applications, there is only a small number of occurrences of the searched word in the Array of memory. In that case, the number of CAM Cells for which the first Sub-word will make a Match is very small. Consequently, in the great majority of CAM-Cells, the second Match Line
will not be charged, and the power consumption of the CAM array will be greatly reduced.

The inventive method is operated using 5 steps in a search cycle, instead of 3 in common CAM’s. However each step has a reduced duration, since each Match Line is now shorter and has a reduced capacitance, so that the total searching time will be of the same order.

Furthermore, it is one of the advantages of the inventive method that when successive searching operations are to be done, the steps of successive searches may be time-interlaced, so that the total number of search operations per time unit may be increased.

In Fig 4 is shown an example where searching cycles are interlaced. The time axis is shown going downward. In that example, step 1 of a searching cycle N is done simultaneously with step 3 of a previous searching cycle (N-1). Step 2 of cycle N is done simultaneously with step 4 of (N-1) cycle. Step 3 of cycle N is done simultaneously with step 5 of cycle (N-1) and step 1 of next searching cycle (N+1), etc….

The principle of Conditional Precharge circuit has been shown here in the case where there are two match lines. It will be understood however that the same principle can be applied where the CAM Cell has been subdivided in any number of Sub-words and the same number of Match Lines are implemented, associated to the said Sub-Words.

Fig 5 shows a CAM Cell with 5 Match Lines and 5 Sub-words, a precharge circuit associated with the first Match Line and 4 conditional precharge circuits, each associated with one of the 4 subsequent Match lines. The first Match Line of the CAM Cell will be charged for each searching cycle, but the other Match Lines of the said CAM Cell will be charged only if the preceding Match Line of the same CAM Cell was not discharged by a comparison on the previous sub-word.

The number of bits of each Sub-word can be optimized to best fit the applications and minimize the power consumption of the device. It will be understood that when the first Sub-Word is composed of a few bits, then the probability that there will be a Match on that first Sub-Word will have a considerable value. However the power dissipated on each first Match Line will be small, since the number of CAM Bit Cells associated with that Match Line is small. In the other case where the first Sub-Word is composed of a larger number of bits, then the probability that there will be a Match on that first Sub-Word becomes very small. However the power dissipated on each first Match Line is greater, since a larger number of CAM Bit Cells are associated with each match line. When evaluating the overall power consumption of the CAM device, an optimum value for the number of bits for each sub-word can be chosen for minimum power consumption.

In Fig 6 is shown how a conditional pre-charge circuit can be used in a CAM array that is used to search words of different sizes. An example of such a CAM is described in PCT/IL 01/00436. The CAM array of PCT/IL 01/00436 comprises a plurality of Sub-words. In this embodiment the Sub-words are not necessarily grouped in words in a predefined way. Instead, each Conditional pre-charge circuit associated with each Sub-word receives as input the signal set on the Match line of the previous Sub-word. This Conditional pre-charge circuit receives an additional input signal (Command Signal). This Conditional pre-charge circuit now functions in order to
charge the match line of the associated Sub-word on condition that either the previous Sub-word was found matching in a previous compare operation, or the Command Signal is set. By selectively setting the command signals, a group of sub-words that are between two set Command Signals form a Comparison unit, i.e. the Match signal on the match lines will propagate on all Sub-words of the comparison unit until a Mismatch occurs. Whenever a Mismatch occurs, then the propagation of the Match signal along a comparison is stopped. By selecting only Match signals that occur at the end of a comparison unit, it is now possible to select only Matches that occur for an entire comparison unit. In this manner, words of arbitrary size can be searched, and this with a reduced power consumption. The reduced power consumption is obtained by the fact that statistically, if the word searched is not matching the word stored in a comparison unit, then a mismatch will occur with a great probability at the beginning of the comparison unit. As a result, during the following comparison cycles the Match lines of the following sub-words of the comparison unit will not be pre-charged.
Claims:

1. A CAM cell that is capable of storing at least two subwords, with a first match line associated to a first subword, and consecutive match lines associated to each consecutive subword respectively in a predefined order, the said cell further comprising a comparator for each of the said match lines, a precharge circuit associated with the said first match line and a conditional precharge circuit associated with each of the said consecutive match lines, wherein the said comparator is designed to discharge a match line in case that the data stored in the said associated subword is not matching the data of a searched word, the said precharge circuit is always precharged prior to a search operation and the said conditional precharge circuits will charge the said match lines for a compare operation on the said associated subwords only where the condition is fulfilled that the previous match line in the said predefined order was not discharged.

2. A CAM cell in accordance with claim 1 hereinabove wherein the said CAM cell comprises two subwords.

3. A CAM memory for searching a word of data comprising an array of CAM cells designed according to either of claims 1 or 2 hereinabove.

4. A CAM array for searching words of variable size with a plurality of CAM cells arranged in a given order, each CAM cell being capable of storing one subword, and each CAM cell being associated with a Match line and a conditional precharge circuit, the said CAM cell further comprising a compator and the said conditional precharge circuit receiving as input a command signal, wherein the said match line is precharged for a compare operation on the condition that either the match line of the preceding CAM cell has been left charged by a previous compare operation or the command signal is set, such that the search may be limited to a chain of subwords of a desired length.

5. A conditional precharge circuit associated with a CAM cell, the said CAM cell being capable of storing at least two subwords with a first match line associated to a first subword and one match line associated to each consecutive subword in a predefined order, characterized in that the said conditional precharge circuit is associated with one of the said consecutive match lines and the said conditional precharge circuit receives a match line that is preceding to the said consecutive match line in the said predefined order wherein the said conditional precharge circuit outputs a signal that allows the said consecutive match line to be precharged for a compare operation only in case that the said preceding match line has not been discharged.

6. A conditional precharge circuit to be used in an array of CAM cells arranged in a given order, each CAM cell being capable of storing one subword and each CAM cell being associated with a match line wherein
the said conditional precharge circuit receives as input a) a first match line that is associated with a first CAM cell and b) a command line and the said conditional precharge circuit outputs a signal that allows a second match line, that is consecutive to the said first match line in a predefined order to be precharged in case that the said first match line has been left charged by a previous compare operation or the command signal is set.

7. A method for searching data in a CAM memory array with a plurality of memory cells, each memory cell comprising a plurality of bit cells, the said bit cells being divided into subwords, each subword comprising a predefined number of the said bit cells and each subword being associated with a compare cycle and a match line wherein a first match line is associated with a precharge circuit and each of the consecutive match lines respectively is associated with a conditional precharge circuit, the said method comprising the following steps:

a. The said first match line is charged by the said precharge circuit while the said consecutive match lines are kept in a discharged state
b. The said compare cycle of the said first subword enables comparison of the data to be searched with the data stored in the said first subword wherein the said first match line is discharged if there is a mismatch
c. Each of the said conditional precharge circuits respectively allows the said associated consecutive match line to be precharged only in the event that the preceding match line is not discharged

Whereby a consecutive subword is only precharged on the condition that the match line associated to a preceding subword was found matching and the preceding match line remains charged, such that the energy required for the search operation is considerably reduced.

8. A method for searching words of variable size in a CAM array with a plurality of CAM cells arranged in a predefined order, each CAM cell being capable of storing one subword, each CAM cell comprising a comparator circuit and each CAM cell being associated with a Match line and a conditional precharge circuit, the said conditional precharge circuit receiving as input a command line and a Match line wherein the said Match line is associated with a CAM cell that is preceding in the said predefined order, the said method comprising the following steps:

a. One or more command signals are set on the command lines of the CAM array
b. each conditional precharge circuit allows the said associated match line to be precharged only in case that the associated command line is set or the said match line of the said preceding CAM cell has been left charged by a previous compare operation
c. in CAM cells having an associated match line that has been precharged a compare cycle enables comparison of the data to be
searched with the data stored in the said cell wherein the said associated match line is discharged if there is a mismatch whereby the search may be limited to a chain of subwords of a desired length.

9. A method for searching data in a CAM memory array according to any of claims 6 or 7 hereinabove wherein successive searching operations are time interlaced such that one or more searching steps of one search operation are executed simultaneously with one or more steps of preceding or consecutive search operations.

10. A CAM cell substantially as described herein with reference to the drawings.

11. A CAM memory array substantially as described herein with reference to the drawings.

12. A conditional precharge circuit for a CAM memory array substantially as described herein with reference to the drawings.

13. A method for searching data in a CAM memory array substantially as described herein with reference to the drawings.
Step 1: Precharge of Match Line 1
Step 2: Compare Sub-Words 1
Step 3: Conditional Precharge of Match Line 2
Step 4: Compare Sub-Word 2 of word N
Step 5: Evaluate Match of Word N

Searching operation for Word N
Searching operation for Word (N+1)
Searching operation of Word (N+2)

Time axis

Fig 4
INTERNATIONAL SEARCH REPORT
International Application No
PCT/IL 01/01140

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C15/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>column 2, line 36 - line 37 column 4, line 17 - line 67 column 7, line 63 -column 9, line 52 figures 3,7-9</td>
<td>9</td>
</tr>
<tr>
<td>X</td>
<td>ZUKOWSKI C A ET AL: &quot;Use of selective precharge for low-power on the match lines of content-addressable memories&quot; RECORDS OF THE INTERNATIONAL WORKSHOP ON MEMORY TECHNOLOGY, DESIGN AND TESTING, 1997, pages 64-68, XP002106385 the whole document</td>
<td>1-3,5,7</td>
</tr>
<tr>
<td>Y</td>
<td></td>
<td>4,6,8</td>
</tr>
</tbody>
</table>

X Further documents are listed in the continuation of box C. X Patent family members are listed in annex.

* Special categories of cited documents:
  *A* document defining the general state of the art which is not considered to be of particular relevance
  *E* earlier document but published on or after the international filing date
  *L* document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
  *O* document referring to an oral disclosure, use, exhibition or other means
  *P* document published prior to the international filing date but later than the priority date claimed

*"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
*"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
*"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

Date of the actual completion of the international search
16 May 2002

Date of mailing of the international search report
17/06/2002

Name and mailing address of the ISA
European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijwijk
Tel. (+31-70) 340-2040, Tx. 31 651 epos nl, Facs (+31-70) 340-3016

Authorized officer
Colling, P
<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>US 6 166 939 A (NATARAJ BINDIGANAVALE S ET AL) 26 December 2000 (2000-12-26) column 2, line 47 - column 5, line 67 figures 2-4</td>
<td>1-3, 5, 7</td>
</tr>
<tr>
<td>Y</td>
<td>US 6 262 929 B1 (MIYATAKE HISATADA ET AL) 17 July 2001 (2001-07-17) column 1, line 66 - column 4, line 60 figures 3-5</td>
<td>4, 6, 8</td>
</tr>
<tr>
<td>Y</td>
<td>US 6 137 707 A (NATARAJ BINDIGANAVALE S ET AL) 24 October 2000 (2000-10-24) column 4, line 19 - column 6, line 21 figure 4</td>
<td>9</td>
</tr>
<tr>
<td>Y</td>
<td>US 6 144 574 A (KOBAYASHI MASAYOSHI ET AL) 7 November 2000 (2000-11-07) column 9, line 63 - line 67 column 10, line 57 - column 12, line 7</td>
<td>9</td>
</tr>
<tr>
<td>A</td>
<td>EP 0 918 335 A (NIPPON ELECTRIC CO) 26 May 1999 (1999-05-26) column 6, line 1 - column 7, line 47 figure 1</td>
<td>1-8</td>
</tr>
</tbody>
</table>
Continuation of Box I.2

Claims Nos.: 10-13

Rule 6.2 (a) PCT

The applicant’s attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.
<table>
<thead>
<tr>
<th>Patent document cited in search report</th>
<th>Publication date</th>
<th>Patent family member(s)</th>
<th>Publication date</th>
</tr>
</thead>
<tbody>
<tr>
<td>US 6243280 B1</td>
<td>05-06-2001</td>
<td>NONE</td>
<td></td>
</tr>
<tr>
<td>US 6166939 A</td>
<td>26-12-2000</td>
<td>NONE</td>
<td></td>
</tr>
<tr>
<td>US 6137707 A</td>
<td>24-10-2000</td>
<td>NONE</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>JP 11162179 A</td>
<td>18-06-1999</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CN 1220468 A</td>
<td>23-06-1999</td>
</tr>
<tr>
<td></td>
<td></td>
<td>US 6081441 A</td>
<td>27-06-2000</td>
</tr>
<tr>
<td>JP 2001167585 A</td>
<td>22-06-2001</td>
<td>NONE</td>
<td></td>
</tr>
</tbody>
</table>