United States Patent

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[72] Inventors **Benjamin Kazan**
Pasadena;
Arthur W. Vance, Corona Del Mar, both of Calif.

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[73] Assignee **Xerox Corporation**
Rochester, N.Y.

Original application Sept. 29, 1966, Ser. No. 582,911, now Patent No. 3,518,698, dated June 30, 1970. Divided and this application Sept. 29, 1969, Ser. No. 870,878

[54] **METHOD OF REDISTRIBUTING CHARGE ON A DIELECTRIC MEDIUM**
9 Claims, 5 Drawing Figs.

[52] **U.S. Cl.** ..... **346/74 ES,** 340/173 LS, 346/1, 346/74 P
[51] **Int. Cl.** **G01d15/06,** G11b 7/06
[50] **Field of Search** ..... 346/74 ES, 74 CR, 74 P, 1; 340/173 LS, 173 LT; 96/1

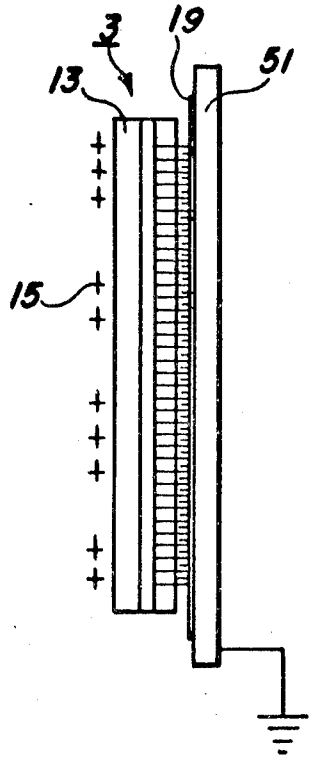
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Primary Examiner—Bernard Konick
Assistant Examiner—Gary M. Hoffman
Attorneys—John E. Beck, James J. Ralabate and Laurence A. Wright

ABSTRACT: This application relates to an imaging system and method utilizing a conductive pin matrix for redistributing charge on a charge-dielectric surface which is placed in contact therewith. Conductivity between adjacent pins and therefore charge redistribution is controlled by means of a field-effect semiconductor layer and an electric field applied thereto, the presence of the electric field modifies the conductivity of the electrical path between adjacent pins through the field-effect semiconductor layer.



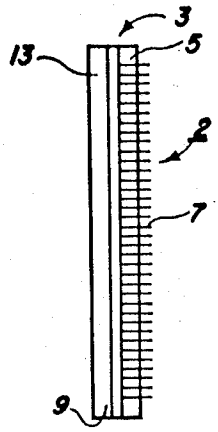


FIG. 1

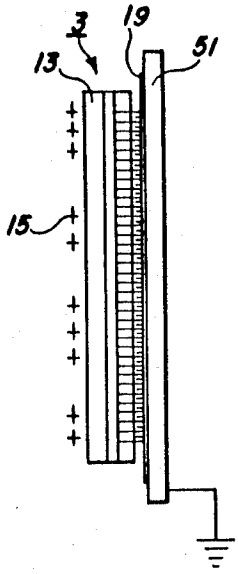


FIG. 2

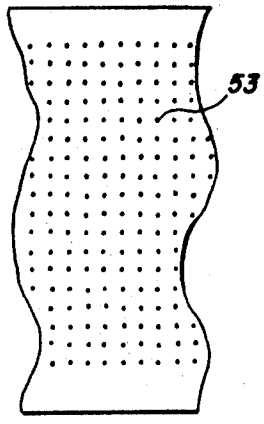


FIG. 3

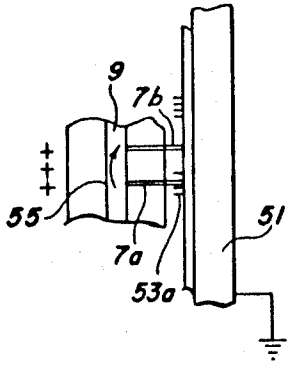


FIG. 4

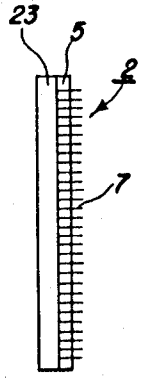


FIG. 5

INVENTORS
BENJAMIN KAZAN
ARTHUR W. VANCE

METHOD OF REDISTRIBUTING CHARGE ON A DIELECTRIC MEDIUM

This is a division of application Ser. No. 582,911, filed Sept. 29, 1966 now U.S. Pat. No. 3,518,698.

This invention relates generally to graphic imaging apparatus and more particularly to apparatus wherein the electrical condition of conductive elements in a matrix is made to vary on an elemental basis in accord with an information input to the apparatus.

At present numerous devices are known in which matrices of electrically conductive pins are by some means or other activated to effect electrical variations among the pins corresponding to an optical or electrical input to the device. A simple and common approach, for example, is shown in U.S. Pat. No. 3,186,839 in which a plurality of such pins are mounted in an insulating slab, each pin being in series with a photoconductive element. When an electrical potential is applied across the sandwiched structure and the apportioned photoconductor in series with an individual pin is impinged by light, that pin is electrically activated and presumably may be utilized to deposit a point charge on an adjacent dielectric web. If desired, the resulting charge pattern may be thereafter developed in accord with standard xerographic techniques to produce a visible replica of the input pattern. Numerous problems are associated with operating this type of apparatus, but even at its best such device is only an image converter and requires a constant input—and in an optical form—in order to produce an output.

Another very common type of device—but one of much greater complexity—is the well-known cathode-ray pin tube, of which several designs are commercially available. In general such devices are used to produce a charge pattern on a moving dielectric web in accordance with an electrical input signal supplied to the tube control grid. In addition to requiring that the input be electrical in form such tubes require high potentials of the order of hundreds of volts, and do not usually have storage capability.

In accordance with the foregoing it is one object of the present invention to provide imaging apparatus adapted to produce an electrical output at a conductive element matrix in accordance with an electrostatic charge pattern established and in effect stored at an input surface of the device.

It is a further object of the present invention to provide imaging apparatus in which the electrical properties of a pin matrix may be varied in accordance with an electrostatic charge pattern established at an input surface of the device, which charge pattern may optionally be established through electrical or optical means.

It is an additional object of the present invention to provide imaging apparatus wherein the electrical character of pin members of a conductive pin matrix are varied in accordance with an electrostatic charge pattern established on a separate control layer, and wherein the pin matrix may be utilized for production of additional images without in any way altering the electrostatic charge pattern present at the control surface.

It is yet a further object of the present invention to provide an imaging method and apparatus for use therewith according to which redistribution—as opposed to dissipation—of a fixed quantity of electrostatic charge on a dielectric surface is achieved in the desired image configuration.

Now in accordance with the present invention these objects, and others as will become apparent upon reading of the ensuing specification, are achieved by means of a structure including an input surface upon which an electrostatic charge pattern may be established either through direct electrical deposition or—where the surface is suitably composed—via optical projection of a light pattern. The resulting electrostatic charge pattern serves by means of field-effect action to selectively establish a conductivity pattern in a semiconductor, which may or may not be directly bounded by the same surface upon which the charge pattern is established. A matrix of conductive pins is positioned with respect to the semiconductor layer such that portions of the semiconductor material now

possessing the varying conductivity pattern are interposed between adjacent pins. Accordingly, an impedance pattern is established between proximate pins in accord with the conductivity pattern in the semiconductor which in turn corresponds to the electrostatic charge pattern present on the input surface of the device.

Such a variable impedance pattern may then be used to produce images or the like corresponding to the electrostatic pattern present at the input surface by bringing the pin matrix into contact with a dielectric surface that has previously been charged at discrete portions thereof. As the conductivity between adjacent pins will vary throughout the matrix in accord with the input charge pattern, the charge on the dielectric surface will be accordingly redistributed. Since the charge pattern present at the input surface referred to is in no way in contact with the pin matrix itself, which is to say that the charge pattern serves merely to control the electrical state of the pins, such pattern is in no way dissipated or otherwise disturbed by the use to which such pins may be put. It follows therefore that a device of the nature described possesses storagability in a very simple manner for information input supplied to the input surface, and it also follows in consequence that numerous and successive output images or the like may be obtained from such a structure without effecting renewal or reintroduction of the pattern present at the input surface.

A fuller understanding of the present invention may now best be gained by reading of the following detailed specification and by a simultaneous examination of the drawings appended hereto in which:

FIG. 1 diagrammatically illustrates a basic embodiment of the present invention.

FIG. 2 illustrates the manner in which the FIG. 1 apparatus may be utilized to produce a developable image output.

FIG. 3 schematically depicts on a much magnified scale a portion of a charged dielectric sheet with which the present invention may be effectively utilized.

FIG. 4 depicts on a much magnified scale the manner in which redistribution of the FIG. 3 charge pattern is achieved.

FIG. 5 illustrates a variation on the FIG. 1 embodiment.

In FIG. 1 a simplified cross section view is shown of a basic embodiment of the instant invention. The structure 3 is seen to include an insulating plate 5 containing a matrix 2 of conducting pins 7 extending therethrough. These pins 7 may protrude slightly from the outside face of the plate as this surface will normally be brought into contact with a printing sheet, dielectric web or the like when the structure is utilized for imaging purposes. The other ends of pins 7 terminate flush with the inner face of plate 5, thereby presenting a matrix of conductive points at this planar face. The insulating layer 5 can be formed from any of numerous materials having high dielectric breakdown properties and may for example be thought of as comprising glass.

A field-effect semiconductor layer 9 is in intimate contact with the innerface of plate 5 and hence is also in contact with the exposed flush ends of pins 7. The semiconductor layer 9 will be chosen with some variation depending upon the impedance range that one ultimately desires to establish at the pin matrix 2. A large list of generally suitable semiconductors may be found at page 9 of *Field-Effect Transistors*, ed. by Wallmark and Johnson, Prentice-Hall Inc. Englewood Cliffs, N.Y. (1966). By way of some specific examples, one may choose a relatively conductive type of material such as zinc oxide, or alternatively one may utilize a relatively low conductivity semiconductor material such as zinc sulfide or arsenic sulfide. The semiconductor layer 9 will ordinarily be quite thin and will be deposited upon the inner face of plate 5 in such a manner that a low resistance contact between the flush ends of pins 7 and the semiconductor layer is assured. In a typical instance and by way of example, layer 9 may comprise a zinc oxide film having a thickness of about 1 micron. This composition may be deposited upon the inner face of plate 5 by evaporation or sputtering, both techniques being well known

in thin-film technology. As another example the layer 9 may alternatively comprise a microcrystalline evaporated layer of cadmium sulfide having a thickness of the order of 1 micron or so.

To complete the structure 3 a highly insulating layer 13 is established overlying the semiconductor layer 9. This insulating layer may by way of example suitably comprise a thin evaporated layer of silicon monoxide or magnesium fluoride, either element of which is so highly insulating as to retain a charge pattern deposited thereon for many hours or even days.

The present inventive structure is utilized by establishing at the outside surface of insulating layer 13 an electrostatic charge pattern representative—in a general sense—of input data. Such a pattern may be established in numerous ways and will be of a polarity chosen in accord with the nature of the particular semiconductor material utilized for layer 9. Where a negative electrostatic pattern is desired for layer 13 the pattern may be readily laid down by direct electron deposition. For such purposes a stream emanating from an electron gun may be made to impinge upon the surface of layer 13 in an evacuated chamber. Modulation of the electron stream as it sweeps across the surface of layer 13 in a rastered manner achieves the desired pattern. The same technique can also be used to deposit a positive charge image if conditions and materials are utilized to achieve adequate secondary electron emission from the surface of layer 13.

The pattern may also be established in a quite simplified fashion by deposition of charged particles emanating from a positive or negative corona source positioned adjacent but spaced from layer 13. The conductive pin elements 7 may be grounded during such a charging operation to allow induced charges to flow from these pins to the junction between insulator 13 and the field-effect semiconductor layer 9. A conductive stencil positioned between the corona source and insulating layer 13 may be utilized here to selectively intercept particles whereby charge is deposited in desired character configurations or so forth.

Another simple technique, and one that like corona charging requires no evacuated atmosphere, utilized dielectric breakdown between the layer and a shaped conducting character or the like separated from layer 13 and its grounded conductive pins 7 to deposit charge on the surface of layer 13 corresponding to the shaped characters utilized. Processes of this latter type have become generally known under the acronym TESI printing, and numerous references may be cited to systems of this general type including, for example, U.S. Pat. Nos. 3,060,432 and 3,060,481.

The manner in which the present structure operates to produce an output image faithfully representative of the electrostatic charge pattern present at layer 13 may now be readily understood. Referring specifically to FIG. 2 a structure 3 is shown having an electrostatic charge pattern 15 present upon the outside face of insulating layer 13. The pattern as would be expected varies across the face of the layer as is suggested by the nonuniform application of positive charge symbols to the face of this layer.

An insulating receptor sheet 19 which may be a dielectric web, a piece of paper, or so forth, is brought over a conductive backing member 51 and into contact with the pins 7 of pin matrix 2. The sheet 19 has been charged in such a manner that a fine pattern of discretely charged areas is formed on the sheet 19 much resembling a halftone screen. This effect is graphically depicted in FIG. 3, the charge pattern on the sheet 19 being designated at 53. All of the charged areas are at the same potential, there being numerous ways in which such a pattern may be laid down, including application of charge through a conductive halftone screen, or application of uniform charge followed by contact of the surface with a studded or similarly patterned conductive roller.

The variation in impedance path between pins occurs in accordance with the charge pattern 15 because by field-effect action the pattern 15 selectively controls the electrical conductivity in semiconductor layer 9 by means of the electric field such charge effects. For the embodiment depicted in FIG. 2 this type of action is basically quite similar to what takes place in an insulated-gate field-effect transistor. This is illustrated for structure 3 in the greatly magnified sectional view of FIG. 4. More specifically we may consider the case where as has been previously suggested as one possibility, layer 9 comprises a thin layer of the semiconductor cadmium sulfide. A pin 7*a* by virtue of its proximity to a discrete charged area 53*a* upon the sheet 19 serves in effect as a "source." Similarly an adjacent pin 7*b*, not in contact with a charged area effectively acts as a "drain" by virtue of its capacitive coupling to ground via member 51. With a positive polarity charge pattern 15 as shown in FIG. 4 the conductivity in volumes of the semiconductor layer 9 immediately below charged areas will be increased by attraction of carriers into the semiconductor so that the impedance path between adjacent pins 7*a* and 7*b* below such volumes is correspondingly decreased. The result here is thus to effectively cause current to flow between such affected pins, as is suggested by the arrow 55, which thus "smears" out the electrostatic charge pattern on areas on receptor sheet 19 immediately below charged areas on insulating layer 13, in effect equalizing the charge on layer 19, between pins 7*a* and 7*b*. Like the transistor structure of which the device is reminiscent, a negative bias may also be utilized on surface 13—which is to say that the electrostatic charge pattern deposited thereon may be of negative polarity. With the connections otherwise as shown the effect of charged areas of this polarity on layer 13 will then be such as to repel electrons out of the semiconductor layer 9 so that decreased conductivity results in such affected areas. In this manner a charge image may be established upon receptor sheet 19 which ignoring the polarity of the charge is in terms of charge variation directly in accord with pattern 15 rather than in inverse accord as would be the case where positive charge is utilized for pattern 15.

While the depiction of FIG. 4 particularly illustrates how the present apparatus cooperates with a dielectric sheet having discretely charged areas of a single given polarity, (in FIG. 4 the areas are thus seen to be negative) it will nevertheless be appreciated by those skilled in the art that the charge pattern 53 of FIG. 3 may very well consist of alternating discrete areas of positive and negative charge. A technique for depositing charge in this manner is fully set forth in a patent application entitled "Charging System" filed by John H. Lennon on or about July 1, 1966, and assigned to the same assignee as the present application. When a charge pattern so characterized is established the manner in which the present apparatus functions to selectively rearrange the charges is identical to the operation described in connection with FIGS. 2 and 4.

Regardless of whether the discrete areas in pattern 53 alternate in polarity or are of the same sign it will be appreciated that image resolution may be made of a high and very consistent quality by the simple expedient of depositing the discrete charged areas with a pattern displaying frequency and spacing of such areas appropriate to that existing among the pin matrix elements themselves. In the case illustrated in FIG. 3 for example the charged areas will ideally be deposited so as to display the spatial frequency spacing of the pin elements 7. That is, there will be a corresponding charged area for each conductive pin in the pin matrix and during operation, the pins and corresponding charged areas will be in substantially exact registration. Under such conditions the pin matrix may in use be placed in register with the charge pattern 53 with the assurance that initially,—that is prior to redistribution of the charge—the potential difference between any two adjacent pins is of the same order of magnitude. Accordingly on subsequent redistribution of charge, the resulting variation across the image will reflect only the impedance variation between adjacent pins and will not include minor perturbations introduced by periodic spatial displacements of pins from charge areas, an effect which would result if the half-frequency spacing of the pin elements differed substantially from the spacing of discrete charge areas.

Again by way of example it will be obvious that where the discrete charging scheme involves alternate positive and negative areas ideally the spatial frequency of such areas should coincide with the frequency of occurrence of pins in the matrix. In any event in the absence of appropriately precise registration between the pins and the charged areas, good imaging is still brought about but for the reasons indicated in the prior paragraph objectionable moire patterns tend to occur.

Registration between the pin matrix **2** and the discretely charged areas of sheet **19** may be assured by any of numerous techniques well known in the registration art. As one simple example a rigid frame may be provided with a recessed planar portion for placement of the sheet **19**. A charging matrix of pin elements having spatial frequency appropriately related to the matrix **2** is then provided for mating with the frame so that the charging elements come to rest slightly spaced from the sheet **19**. A discharge is effected between the charging matrix and the sheet to provide the desired pattern, after which the charging matrix is removed and the imaging device **3** is positioned in the frame in its stead. Mating means are utilized such as complementary pins and recesses in the mating parts to assure exact registration between the sheet **19** positioned within the frame and the charging or pin matrix **2** joined thereto.

After sufficient time has transpired for the output charge pattern to be formed upon sheet **19** the sheet is removed and where desired may be developed according to methods common place in the art of xerography. In the simplest instance the visual pattern may thus be produced by applying to the charge pattern now on receptor sheet **19** a colored particulate material which selectively adheres in those areas of relatively high charge density. Where the latent electrostatic image is formed—as has been previously described—from a charge pattern displaying alternating polarity from discrete area, to discrete area a development method such as that described in Bixby U.S. Pat. No. 3,013,890 may be used. According to this latter teaching positively and negatively charged areas are simultaneously developed by contacting the surface bearing the electrostatic images with a carrier surface having thereon both positively and negatively charged toner particles.

In FIG. **5** a variation upon the FIGS. **1** and **2** embodiment is shown which eliminates the necessity for separate semiconductor and insulating layers. In FIG. **3** the pin matrix **2** and insulating plate **5** are identical with corresponding elements discussed in connection with FIGS. **1** and **2**. A layer **23** of storing semiconductor material, however, is now deposited directly over the plate **5** at the surface of which are the exposed ends of pin **7**. As in previously described embodiments this deposition process is carried forth in such a manner that a low resistance contact is made between the semiconductor material and the electrically conductive elements **7**.

For purposes of the present discussion the term "storing semiconductor material" refers to members of a subclass of field-effect semiconductor materials which are adapted to retain electrostatic charge on their surface, to conduct current through the central portion thereof without substantially dissipating such charge, and to dissipate such charge in response to impinging radiation. Zinc oxide is the best known example of such material; however in addition to zinc oxide there are other materials such as lead oxide and cadmium oxide which exhibit similar characteristics and which may be used in formation of layer **23**.

Where the preferred zinc oxide composition is utilized for layer **23** it may be deposited by any convenient means including spraying of zinc oxide powder in a binder. In a typical instance a coating having a thickness of approximately 1 mil is desirable. This coating composition may have the same formulation as that used for electrophotographic paper coating. A specific example of such coating composition is as follows:

Material	Pounds per 100 Gallons
Zinc Oxide	533.000
Pliolite S-5D	107.000
Chlorinated Paraffin	27.000
Toluene	533.000
Bromophenol Blue	0.021
Methyl Green	0.016
Acridine Orange	0.016
	1200.053

*Pliolite S-5D is a styrene butadine copolymer produced by the Chemical Division of the Goodyear Tire and Rubber Co., Akron, Ohio. A detailed discussion of the aforementioned zinc oxide composition is set forth in the publication titled "Tech-Book Facts," Formulations PLS-37, Chemical Division Goodyear Tire and Rubber Co., Akron, Ohio.

Besides substantially pure zinc oxide a wide variety of zinc oxide compositions can be utilized which consist essentially of zinc oxide dispersed in a nonconductive binder resin. Zinc oxide to nonconducting resin ratios as set forth in the aforementioned composition is approximately 5:1. However in order to vary the conductivity zinc oxide concentration may be increased so that the ratio is increased up to 50:1 or decreased so that the ratio is about 3:1. Similarly various dyes and sensitizers may be added to the composition to extend the spectral response of the composition with the ones in the table noted being typical.

In addition to the spraying technique set forth, various of the methods evolved in thin-film technology may be utilized for producing layer **23**. For example sputtering or evaporation in vacuum may be used to provide a layer of elemental zinc ranging down to the several micron vicinity. Such an elemental layer may be conveniently converted to the oxide by merely heating in an oxygen-rich atmosphere.

The apparatus depicted in FIG. **5** may be used in essentially the same manner as has been described in connection with the prior embodiments. As a rule an initial deposition of charge upon the surface of layer **23** however is effected by use of negative ion corona in an atmosphere including oxygen. Where such technique is utilized the charge deposition is principally effected by negative oxygen ions which are trapped on the surface of the storing photoconductor causing the dark conductivity of layer **23** to be greatly decreased. The negative charge pattern may either be established upon the storing semiconductor layer by the direct methods that have been previously alluded to or alternatively the photoconductive properties of zinc oxide itself may be utilized to directly establish a charge image in accord with an optical input.

In the situation where a negative charge pattern is directly applied to the layer **23** the mechanism of operation of the device is essentially similar to the operation of the FIG. **1** apparatus **3**. That is to say that the presence of negative charge at points on layer **23** acts by field-effect action to repel negative carriers in the vicinity of the underlying grid and pin elements, as a result of which conductivity condition in the volumes of semiconductor so affected is reduced, and the impedance path presented to associated adjacent pins correspondingly increased.

While the present invention has been particularly described in terms of specific embodiments thereof it will be understood that in view of the present disclosure numerous deviations therefrom and modifications thereupon may be readily devised by those skilled in the art. Accordingly the present invention is to be broadly construed and limited only by the scope of the claims now appended hereto.

What is claimed is:

1. A method of forming a latent electrostatic image on a dielectric surface comprising:

a. subjecting a semiconductor layer to an electric field in the configuration of an image said semiconductor layer adapted to display conductivity variations in response to said electric field,

b. establishing discrete areas of electrostatic charge on said dielectric surface, and

c. electrically connecting adjacent charged areas on said dielectric surface through corresponding portions of said semiconductor layer for limited periods of time whereby said electrostatic charge is redistributed in accordance with said electric field.

2. The method of claim 1 wherein said electric field is provided by establishing an electrostatic charge pattern in image configuration contiguous to said semiconductor layer said electrostatic charge pattern serving as the source of said electric field.

3. A method of forming a latent electrostatic image on a dielectric surface comprising:

providing a matrix of mutually insulated conductive elements imbedded in and extending through a first planar side of an insulating support layer;

placing a layer of field-effect semiconductor material over a second planar side of said insulating support layer said field-effect semiconductor layer capable of displaying varying conductivity at volumes thereof in response to an image-configurated electric field imposed thereon,

subjecting said field-effect semiconductor layer to an electric field in the configuration of an image;

establishing discrete areas of electrostatic charge on a dielectric surface; and

contacting the exposed ends of said matrix of conductive elements to the charged areas on said dielectric surface whereby said electrostatic charge is redistributed in accordance with said image-configurated electric field.

4. The method of claim 3 wherein said field-effect semiconductor material is a storing field-effect semiconductor material having an exposed surface substantially parallel to second planar surface of said insulating support layer and said image configurated electric field is provided by establishing an electrostatic charge pattern on said exposed surface, said electrostatic charge pattern serving as the source of said field.

5. The method of claim 3 wherein said conductive element matrix structure further includes a second insulating layer in overlying contact with said field-effect semiconductor layer, said second insulating layer having an exposed surface substantially parallel to said planar surface of said insulating support layer said image-configurated electrical field being provided by establishing an electrostatic charge pattern on said exposed surface of said second insulating layer said electrostatic charge pattern serving as the source of said field.

6. The method of claim 3 including maintaining discrete areas of electrostatic charge on said dielectric surface at the same potential by grounding the back of said dielectric material to a grounded conductive backing member.

7. The method of claim 3 including maintaining said discrete areas of electrostatic charge on said dielectric surface alternating areas of positive and negative charge.

8. The method of claim 3 further including the step of making visible the redistributed, latent electrostatic image on said dielectric surface.

9. The method of claim 3 wherein steps of establishing discrete areas of electrostatic charge on said dielectric surface and contacting the ends of said conductive elements to the charged areas on said dielectric surface are repeated with at least one additional discretely charged dielectric surface whereby a plurality of redistributed, latent electrostatic images can be obtained from a single image-configurated electric field and in accordance therewith.

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