

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
14 August 2008 (14.08.2008)

PCT

(10) International Publication Number
WO 2008/097448 A2

(51) International Patent Classification:
H01L 21/20 (2006.01)

(21) International Application Number:
PCT/US2008/001126

(22) International Filing Date: 28 January 2008 (28.01.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/704,466 7 February 2007 (07.02.2007) US

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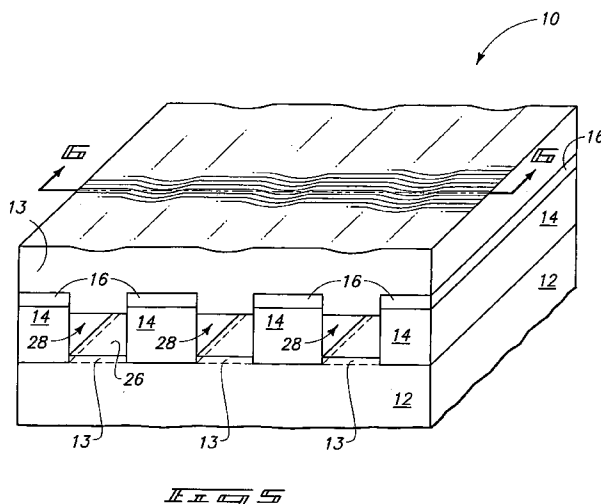
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(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— without international search report and to be republished upon receipt of that report

(54) Title: METHODS OF FORMING ONE OR MORE COVERED VOIDS IN A SEMICONDUCTOR SUBSTRATE, METHODS OF FORMING FIELD EFFECT TRANSISTORS, METHODS OF FORMING SEMICONDUCTOR-ON-INSULATOR SUBSTRATES, METHODS OF FORMING A SPAN COMPRISING SILICON DIOXIDE, METHODS OF COOLING SEMICONDUCTOR DEVICES, METHODS OF FORMING ELECTROMAGNETIC RADIATION EMITTE



(57) Abstract: Some embodiments include methods of forming voids within semiconductor constructions. In some embodiments the voids may be utilized as microstructures for distributing coolant, for guiding electromagnetic radiation, or for separation and/or characterization of materials. Some embodiments include constructions having micro-structures therein which correspond to voids, conduits, insulative structures, semiconductor structures or conductive structures.

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DESCRIPTION

**METHODS OF FORMING ONE OR MORE COVERED VOIDS IN A SEMICONDUCTOR
SUBSTRATE, METHODS OF FORMING FIELD EFFECT TRANSISTORS, METHODS
5 OF FORMING SEMICONDUCTOR-ON-INSULATOR SUBSTRATES, METHODS OF
FORMING A SPAN COMPRISING SILICON DIOXIDE, METHODS OF COOLING
SEMICONDUCTOR DEVICES, METHODS OF FORMING ELECTROMAGNETIC
RADIATION EMITTERS AND CONDUITS, METHODS OF FORMING IMAGER
SYSTEMS, METHODS OF FORMING NANOFLUIDIC CHANNELS, FLUORIMETRY
10 METHODS, AND INTEGRATED CIRCUITRY**

TECHNICAL FIELD

Embodiments disclosed herein pertain to methods of forming one or
more covered voids in semiconductor substrates, to methods of forming field
15 effect transistors, to methods of forming semiconductor-on-insulator
substrates, to methods of forming spans comprising silicon dioxide, to
methods of forming electromagnetic radiation emitters and conduits, to
methods of forming imager systems, to methods of forming nanofluidic
channels, to fluorimetry methods, to methods of cooling semiconductor
20 devices, and to integrated circuitry.

BACKGROUND ART

A continuing goal in semiconductor device fabrication is to make the
devices smaller and positioned closer to one another while maintaining the
25 integrity and desired performance characteristics of the individual devices.
Such has led to the development and improvement of various semiconductor
constructions, including, for example, recessed access devices (RADs),
semiconductor-on-insulator constructions, partial and/or pseudo
semiconductor-on-insulator constructions, fin field effect transistors
30 (FinFET) and others. Such may be used in logic, memory, or other circuitry,
for example for use in dynamic random access memory (DRAM), NOR,
NAND, FLASH memory, and floating body memory, among other
semiconductor devices and circuitry. Semiconductor device fabrication has
also been applied to the development of a diversity of micro-structures. For
35 example, such include the development of optical wave guides fabricated in

semiconductor materials and the development of micro-electro-mechanical systems (MEMS).

During fabrication, circuitry or micro-structures may be formed to have voids formed therein. Such may be wholly or partially filled with one or more materials during subsequent processing, left empty, or evacuated, and any remaining voids may be used for various purposes. Regardless, forming desired voids may be a challenge in achieving desired position and size of the voids.

A continuing goal of analytical sciences is to develop tools and methods for rapid separation and/or characterization of materials. For example, there is a continuing goal to develop tools for rapid separation and/or characterization of biomaterials, such as nucleotide sequences and amino acid sequences. There has been interest in developing micro-structures suitable for utilization in the separation and/or characterization of materials, but there remains a need for improved methods for making and using such micro-structures.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagrammatic perspective view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 2 is a view of the Fig. 1 substrate taken through line 2-2 in Fig. 1.

Fig. 3 is a view of the Fig. 1 substrate at a processing step subsequent to that shown by Fig. 1.

Fig. 4 is a view of the Fig. 3 substrate taken through line 4-4 in Fig. 3.

Fig. 5 is a view of the Fig. 3 substrate at a processing step subsequent to that shown by Fig. 3.

Fig. 6 is a view of the Fig. 5 substrate taken through line 6-6 in Fig. 5.

Fig. 7 is a view of the Fig. 5 substrate at a processing step subsequent to that shown by Fig. 5.

Fig. 8 is a view of the Fig. 7 substrate taken through line 8-8 in Fig. 7.

Fig. 9 is a diagrammatic perspective view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 10 is a view of the Fig. 9 substrate taken through line 10-10 in Fig. 9.

Fig. 11 is a view of the Fig. 9 substrate at a processing step subsequent to that shown by Fig. 9.

Fig. 12 is a view of the Fig. 11 substrate taken through line 12-12 in Fig. 11.

5 Fig. 13 is a diagrammatic perspective view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 14 is a view of the Fig. 13 substrate at a processing step subsequent to that shown by Fig. 13.

10 Fig. 15 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 16 is a view of the Fig. 15 substrate at a processing step subsequent to that shown by Fig. 15.

Fig. 17 is a view of the Fig. 16 substrate at a processing step subsequent to that shown by Fig. 16.

15 Fig. 18 is a view of the Fig. 17 substrate at a processing step subsequent to that shown by Fig. 17.

Fig. 19 is a view of the Fig. 18 substrate at a processing step subsequent to that shown by Fig. 18.

20 Fig. 20 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 21 is a view of the Fig. 20 substrate at a processing step subsequent to that shown by Fig. 20.

Fig. 22 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

25 Fig. 23 is a view of the Fig. 22 substrate at a processing step subsequent to that shown by Fig. 22.

Fig. 24 is a view of the Fig. 23 substrate at a processing step subsequent to that shown by Fig. 23.

30 Fig. 25 is a view of the Fig. 24 substrate at a processing step subsequent to that shown by Fig. 24.

Fig. 26 is a view of the Fig. 25 substrate at a processing step subsequent to that shown by Fig. 25.

Fig. 27 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 28 is a view of the Fig. 27 substrate at a processing step subsequent to that shown by Fig. 27.

Fig. 29 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

5 Fig. 30 is a view of the Fig. 29 substrate at a processing step subsequent to that shown by Fig. 29.

Fig. 31 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

10 Fig. 32 is a view of the Fig. 31 substrate at a processing step subsequent to that shown by Fig. 31.

Fig. 33 is a view of the Fig. 32 substrate at a processing step subsequent to that shown by Fig. 32.

Fig. 34 is a view of the Fig. 33 substrate at a processing step subsequent to that shown by Fig. 33.

15 Fig. 35 is a view of the Fig. 34 substrate at a processing step subsequent to that shown by Fig. 34.

Fig. 36 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

20 Fig. 37 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 38 is a view of the Fig. 37 substrate at a processing step subsequent to that shown by Fig. 37.

Fig. 39 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

25 Fig. 40 is a view of the Fig. 39 substrate at a processing step subsequent to that shown by Fig. 39.

Fig. 41 is a view of the Fig. 40 substrate at a processing step subsequent to that shown by Fig. 40.

30 Fig. 42 is a view of the Fig. 41 substrate at a processing step subsequent to that shown by Fig. 41.

Fig. 43 is a view of the Fig. 42 substrate at a processing step subsequent to that shown by Fig. 42.

Fig. 44 is a view of the Fig. 43 substrate at a processing step subsequent to that shown by Fig. 43.

Fig. 45 is a view of the Fig. 44 substrate at a processing step subsequent to that shown by Fig. 44.

Fig. 46 is a diagrammatic perspective view of a portion of a substrate in process in accordance with an embodiment of the invention.

5 Fig. 47 is a view of the Fig. 46 substrate taken through line 47-47 in Fig. 46.

Fig. 48 is a diagrammatic perspective view of a portion of a substrate in process in accordance with an embodiment of the invention.

10 Fig. 49 is a view of the Fig. 48 substrate taken through line 49-49 in Fig. 48.

Fig. 50 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 51 is a view of the Fig. 50 substrate at a processing step subsequent to that shown by Fig. 50.

15 Fig. 52 is a view of the Fig. 51 substrate at a processing step subsequent to that shown by Fig. 51.

Fig. 53 is a view of the Fig. 52 substrate at a processing step subsequent to that shown by Fig. 52.

20 Fig. 54 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 55 is a view of the Fig. 54 substrate at a processing step subsequent to that shown by Fig. 54.

Fig. 56 is a view of the Fig. 55 substrate at a processing step subsequent to that shown by Fig. 55.

25 Fig. 57 is a view of the Fig. 56 substrate at a processing step subsequent to that shown by Fig. 56.

Fig. 58 is a view of the Fig. 57 substrate at a processing step subsequent to that shown by Fig. 57.

30 Fig. 59 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 60 is a view of the Fig. 59 substrate at a processing step subsequent to that shown by Fig. 59.

Fig. 61 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 62 is a view of the Fig. 61 substrate at a processing step subsequent to that shown by Fig. 61.

Fig. 63 is a view of the Fig. 62 substrate at a processing step subsequent to that shown by Fig. 62.

5 Fig. 64 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 65 is a view of the Fig. 64 substrate at a processing step subsequent to that shown by Fig. 64.

10 Fig. 66 is a view of the Fig. 65 substrate at a processing step subsequent to that shown by Fig. 65.

Fig. 67 is a view of the Fig. 66 substrate at a processing step subsequent to that shown by Fig. 66.

Fig. 68 is a view of the Fig. 67 substrate at a processing step subsequent to that shown by Fig. 67.

15 Fig. 69 is a view of the Fig. 68 substrate at a processing step subsequent to that shown by Fig. 68.

Fig. 70 is a view of the Fig. 69 substrate at a processing step subsequent to that shown by Fig. 69.

20 Fig. 71 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 72 is a view of the Fig. 71 substrate at a processing step subsequent to that shown by Fig. 71.

Fig. 73 is a view of the Fig. 72 substrate at a processing step subsequent to that shown by Fig. 72.

25 Fig. 74 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

Fig. 75 is a view of the Fig. 74 substrate at a processing step subsequent to that of Fig. 74.

30 Fig. 76 is a view of the Fig. 75 substrate at a processing step subsequent to that of Fig. 75.

Fig. 77 is a view of the Fig. 76 substrate at a processing step subsequent to that of Fig. 76.

Fig. 78 is a view of the Fig. 77 substrate at a processing step subsequent to that of Fig. 77.

Fig. 79 is a top sectional view of the Fig. 78 substrate along the line 79-79; with the Fig. 78 view being along the line 78-78 of Fig. 79.

Fig. 80 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

5 Fig. 81 is a view of the Fig. 80 substrate at a processing step subsequent to that of Fig. 80.

Fig. 82 is a view of the Fig. 81 substrate at a processing step subsequent to that of Fig. 81.

10 Fig. 83 is a view of the Fig. 82 substrate at a processing step subsequent to that of Fig. 82.

Fig. 84 is a top sectional view of the Fig. 83 substrate along the line 84-84; with the Fig. 83 view being along the line 83-83 of Fig. 84.

Fig. 85 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

15 Fig. 86 is a view of the Fig. 85 substrate at a processing step subsequent to that of Fig. 85.

Fig. 87 is a view of the Fig. 86 substrate at a processing step subsequent to that of Fig. 86.

20 Fig. 88 is a view of the Fig. 87 substrate at a processing step subsequent to that of Fig. 87.

Fig. 89 is a view of the Fig. 88 substrate at a processing step subsequent to that of Fig. 88.

Fig. 90 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention.

25 Fig. 91 is a view of the Fig. 90 substrate at a processing step subsequent to that of Fig. 90.

Fig. 92 is a view of the Fig. 91 substrate at a processing step subsequent to that of Fig. 91.

Fig. 93 is a diagrammatic perspective view of the Fig. 92 substrate.

30 Figs. 94 and 95 are a diagrammatic sectional view and a diagrammatic top view, respectively, of a portion of a substrate in process in accordance with an embodiment of the invention. The view of Fig. 95 is along the line 95-95 of Fig. 94, and the view of Fig. 94 is along the line 94-94 of Fig. 95.

Figs. 96 and 97 are a diagrammatic sectional view and a diagrammatic top view, respectively, of the substrate of Figs. 94 and 95 at a processing stage subsequent to that of Figs. 94 and 95. The view of Fig. 96 is along the line 96-96 of Fig. 97, and the view of Fig. 97 is along the line 97-97 of Fig. 96.

Fig. 98 is a diagrammatic perspective view of the substrate of Figs. 96 and 97.

Fig. 99 is a diagrammatic view of a computer embodiment.

Fig. 100 is a block diagram showing particular features of the motherboard of the Fig. 99 computer embodiment.

Fig. 101 is a high level block diagram of an electronic system embodiment.

Fig. 102 is a simplified block diagram of a memory device embodiment.

Fig. 103 is a photomicrograph of a substrate in process in accordance with one embodiment of the invention.

Fig. 104 is a photomicrograph of the Fig. 103 substrate at a processing step subsequent to that of Fig. 103.

Fig. 105 is a diagrammatic sectional view of a portion of a substrate in process in accordance with an embodiment of the invention, and is alternate processing to that depicted by Fig. 70 subsequent to that depicted by Fig. 69.

Fig. 106 is a view of the Fig. 105 substrate at a processing step subsequent to that shown by Fig. 106.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Example embodiments of methods of forming one or more covered voids in a semiconductor substrate are initially described. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive

substrates described above. The covered void(s) may be subsequently filled in whole or in part with solid, liquid, and/or gaseous material(s). One or more remaining voids may be evacuated of gas therein. Further, a covered void may exist in the final construction being fabricated, a void may be partially filled, or a void may be completely filled such that no portion of the void exists in the final construction being fabricated. Further and regardless, the one or more covered voids may be wholly or partially formed within semiconductive material of the semiconductor substrate or be received entirely outside of any semiconductor material of the semiconductor substrate.

Referring initially to Figs. 1 and 2, a portion of a semiconductor substrate is indicated generally with reference numeral 10. In one embodiment, substrate portion 10 may be considered as comprising a first material 12, a second material 14, and a third material 16. In one embodiment, first material 12 comprises a semiconductor material. For example and by way of example only, material 12 may comprise, consist essentially of, or consist of one or more of Si, Ge, Ga, Ga/Al, Si/Ge, Ga/As, SiC, and Ga/Al/N, and may be monocrystalline, polycrystalline, or amorphous. For instance, semiconductive material 12 may comprise elemental form silicon, for example monocrystalline silicon such as bulk monocrystalline silicon of a bulk wafer. In one embodiment, substrate 12 comprises a monocrystalline-containing substrate comprising a <100> plane direction as shown (Fig. 1).

Second material 14 is formed over first material 12, and is in whole or in part compositionally different from first material 12. Second material 14 may be one or more of insulative, conductive, or semiconductive. Example semiconductive materials include those described above for first substrate material 12. Example conductive materials include any conductive metal, alloy of conductive metals, or any suitable conductive metal compound. Example insulative materials include at least one of silicon dioxide or silicon nitride. An example thickness range for second material 14 is from about 1,500 Angstroms to about 3,000 Angstroms.

Third material 16 is received over second material 14, and is in whole or in part compositionally different from second material 14. An example thickness range for material 16 is from about 200 Angstroms to about

800 Angstroms. Third material 16 may be compositionally the same as or different from first material 12. Regardless, example third materials include elemental-form silicon, including for example elemental-form amorphous silicon and/or monocrystalline silicon, and any one or more of elemental-form W, elemental-form Ti, a silicide, elemental-form Ge, and a combination of Ga and As. In some embodiments, material 16 may be considered as an "epitaxial seed material" which is different compositionally from second material 14. In the context of this document, an "epitaxial seed material" is a material which will seed epitaxial growth of a material of the same composition as or different composition from the epitaxial seed material, with some example epitaxial growth being described in examples below. The epitaxial seed material may or may not have been epitaxially grown itself. In some embodiments, material 16 may be considered as a "seed material" (not preceded by "epitaxial") which is different compositionally from second material 14. In the context of this document, a "seed material" (not preceded by "epitaxial") is a material which will facilitate growth of a material of the same composition as or different composition from the seed material. In one embodiment, semiconductor substrate 10 may be considered as comprising or defining some mean outermost global surface 15 which may or may not be substantially planar.

Referring to Figs. 3 and 4, a plurality of openings 17, 18, and 19 have been formed through third material 16 and second material 14 to first material 12. In one embodiment, such may be considered as forming or providing substrate projections 20, 21, 22, and 23. In one embodiment, any two immediately adjacent of such projections may be considered as comprising a pair of projections comprising second material 14 which projects upwardly from or relative to first material 12, and which comprises projection sidewalls 24. Openings 17, 18 and 19 may also, of course, be formed to extend into first material 12 (not shown) as opposed to immediately terminating at the outermost surface thereof.

Such provides but one example embodiment of providing exposed different first and second materials on a semiconductor substrate, where the second material comprises a pair of projections projecting upwardly relative to the first material and comprises sidewalls which in the depicted example comprise walls of an opening. An exposed third material is provided atop

the second material projections. In one embodiment, a plurality of such openings may be formed by any suitable etching or other technique(s), and whether existing or yet-to-be developed. In the Figs. 3 and 4 example, openings 17, 18, and 19 are provided to comprise elongated trenches
5 running generally parallel mean outermost global surface 15. In one embodiment, trenches 17, 18 and 19 may comprise monocrystalline-containing material bases 26 which run parallel the <100> plane direction.

Referring to Figs. 5 and 6, additional first material 13 has been selectively grown (relative to the second material, at least) from exposed
10 first material 12 and selectively (relative to the second material, at least) from exposed third material 16 effective to bridge across the respective pairs of second material projections to form covered voids 28 between the respective pairs of projections. In the context of this document, selective growth defines a rate of growth which is at least 2:1 compared to all other
15 different composition exposed material, or at least to some other different composition exposed material to which the selectively grown material is being compared, for at least about 100 Angstroms of growth. By way of example only, the selectively growing may be of conductive material or semiconductive material. In one embodiment, the selectively growing is
20 devoid of growing detectable first material 13 from at least a majority of second material sidewalls 24. In the example Figs. 5 and 6 embodiment, essentially no additional first material 13 grows from sidewalls 24, with the depicted covering of portions of sidewalls 24 by material 13 within openings 17, 18, and 19 only occurring as the result of upward growth of material 13
25 from first material 12 and itself, and downwardly of material 13 from third material 16 and itself. As material 12 and 13 are each of the first material, former bases 26 of material 12 within openings 17, 18, and 19 are shown as dashed lines. Such interface of material 12 and 13 may or may not be perceptible. In one embodiment the selectively growing is at a selectively
30 relative to the second material of at least ten to one, and in one embodiment at least one hundred to one. In one embodiment, the selectively growing of the first material is of at least 100 Angstroms and achieves selectivity relative to the second material of at least one hundred to one.

In one embodiment, the selectively growing comprises epitaxial
35 silicon-comprising growth. For example and by way of example only, a

manner of selectively growing epitaxial silicon from example monocrystalline silicon material 12 and where third material 16 comprises monocrystalline silicon, and/or any one or more of elemental-form W, elemental-form Ti, or a silicide, includes chemical vapor deposition using dichlorosilane, hydrogen chloride, and hydrogen at a temperature of 850°C and at a pressure of 40 Torr. In one embodiment, the selectively growing comprises growing any one or more of elemental-form W or a silicide. For example, where third material 16 comprises elemental-form silicon, elemental-form W may be selectively grown from material 16 by chemical vapor deposition using WF₆ and a silane as precursors at 350 degrees C and 20 mTorr, and otherwise as described in U.S. Patent No. 5,043,299. For example, where third material 16 comprises elemental-form silicon, titanium silicide may be selectively grown from material 16 by plasma enhanced chemical vapor deposition including simultaneously flowing titanium tetrachloride and hydrogen to the substrate at a temperature of from about 550 degrees C to about 680 degrees C at a pressure of about 5 Torr to about 8 Torr (with or without plasma).

In one embodiment, the selectively growing comprises polysilicon-comprising growth.

In one embodiment where the first material comprises monocrystalline elemental-form silicon comprising a <100> plane direction, third material comprises elemental-form monocrystalline silicon comprising a <100> plane direction which is parallel that of the first material. Regardless, in one embodiment where the first material comprises monocrystalline elemental-form silicon comprising a <100> plane direction, openings (which may include trenches) are etched to have sides running parallel such <100> plane direction.

In one embodiment, a method of forming a covered void in a semiconductor substrate comprises forming a pair of projections projecting upwardly from a semiconductor substrate. By way of example only, any two adjacent of projections 20, 21, 22, and 23 may constitute an example pair of such projections. Elemental-form silicon is provided atop the pair of projections. For example, material/layer 16 may comprise any elemental-form silicon. A polysilicon-comprising material is selectively grown relative to at least portions of the projection sidewalls from the elemental-form

silicon effective to bridge across the pair of openings to form a covered void between the pair of projections. In one embodiment, at least some of the selectively grown polysilicon-comprising material is oxidized to form a silicon dioxide-comprising bridge atop the covered void. In one embodiment, all
5 such material is oxidized.

In one embodiment, the elemental-form silicon is formed by depositing amorphous silicon and annealing such to be polycrystalline and from which the selectively growing of polysilicon-comprising material occurs. For example, Fig. 103 depicts a photomicrograph of a substrate 900 comprising
10 monocrystalline silicon 902, silicon dioxide projections 904, and amorphous silicon 906. Such was formed by deposition of amorphous silicon, over silicon dioxide, over monocrystalline silicon substrate 902. The amorphous silicon and silicon dioxide were etched to form projections 904 having amorphous silicon 906 thereover, with trenches 908 being formed between
15 the projections. Referring to Fig. 104, such was annealed at a temperature of about 625°C which rendered the amorphous silicon polycrystalline. Polysilicon 910 was grown therefrom at a temperature of about 850°C and a pressure of about 40 Torr using H₂, HCl, and SiH₂Cl₂ as precursors.

In one embodiment, a method of forming a covered void in a
20 semiconductor substrate comprises forming a pair of projections projecting upwardly from a semiconductor substrate. By way of example only, any two adjacent of projections 20, 21, 22, and 23 may constitute an example pair of such projections. Elemental-form silicon is provided atop the pair of projections. For example, material/layer 16 may comprise any elemental-
25 form silicon. At least one of elemental-form W or a silicide is selectively grown relative to at least portions of the projection sidewalls from the elemental-form silicon effective to bridge across the pair of projections to form a covered void between the pair of projections. By way of example only and with respect to the above-described embodiment, any of covered
30 voids 28 constitute example such covered voids.

In one embodiment, a method of forming a plurality of covered voids in a semiconductor substrate includes depositing insulative material over an elemental-form silicon-containing material. For example and by way of
35 example only, material 12 in the above-described embodiment may comprise an elemental-form silicon-containing material over which an insulative

material 14 is deposited. Amorphous silicon is deposited over the insulative material. For example with respect to the above-described embodiment, material/layer 16 may comprise amorphous silicon which is deposited over an insulative material 14. An elemental-form silicon-comprising material is selectively grown relative to the insulative material from the elemental-form silicon-containing material and from the amorphous silicon effective to bridge across the plurality of openings to cover the plurality of openings. For example with respect to the above-described embodiments, material 13 constitutes an example elemental-form silicon-comprising material which has been so selectively grown.

In one embodiment, a method of forming a plurality of covered voids in a semiconductor substrate comprises depositing insulative material over a first elemental-form silicon-containing material. A second elemental-form silicon-containing material is formed over the insulative material. A plurality of openings is etched through the second elemental-form silicon-containing material and the insulative material to the first elemental-form silicon-containing material. A first elemental-form silicon-comprising material is epitaxially grown from the first elemental-form silicon-containing material. A second elemental-form silicon-comprising material is selectively grown relative to the insulative material from the second elemental-form silicon-containing material effective to bridge across the plurality of openings to cover the plurality of openings. Any other of the above and below attributes with respect to any other of the disclosed embodiments are of course contemplated.

In one embodiment, a method of forming a plurality of covered voids in a semiconductor substrate comprises depositing insulative material over a first elemental-form silicon-containing material. An amorphous elemental-form silicon-containing material is formed over the insulative material. A plurality of openings is etched through the amorphous elemental-form silicon-containing material and the insulative material to the elemental-form silicon-containing material. The amorphous elemental-form silicon-containing material is annealed effective to form a polycrystalline silicon-containing material. A first elemental-form silicon-comprising material is epitaxially grown from the elemental-form silicon-containing material while selectively growing relative to the insulative material a polysilicon-

comprising material from the polycrystalline silicon-containing material effective to bridge across the plurality of openings to cover the plurality of openings. Any other of the above and below attributes with respect to any other of the disclosed embodiments are of course contemplated.

5 Referring to Figs. 7 and 8, at least a majority of each covered trench 28 (not designated in Figs. 7 and 8) has been filled with one or more conductive materials 30, whereby for example, the voids exist no more as having been completely filled with solid material. Such may be used to form elongated conductive lines therefrom. For example, individual of the
10 elongated trenches may be provided to have at least one open end into or through which conductive material may be deposited to within the covered elongated trenches effective to form conductive lines within the trenches. For example, suitable chemical vapor deposition and/or atomic layer deposition techniques may be utilized to isotropically fill covered elongated
15 trenches from one or more ends, or from other access location(s) thereto. Such conductive lines may be utilized as local interconnects, substantially globally running conductive lines, field effect transistor gate lines, and/or other conductive lines.

For example and by way of example only, Figs 9-12 depict an
20 alternate embodiment portion of a substrate 10a. Like numerals from the Figs. 5-8 embodiment substrate have been utilized where appropriate, with differences being indicated with the suffix "a" or with different numerals. Figs. 9 and 10 depict the forming of a gate dielectric 32 within covered elongated trenches 28a. An example such material is silicon dioxide, which
25 may be formed for example by a thermal oxidation of material 13 where such comprises at least some elemental-form silicon. Figs. 11 and 12 depict conductive material 30a as having been deposited to within the covered elongated trenches over gate dielectric 32 from at least one open end effective to form conductive gate lines within the trenches. Field effect
30 transistor source/drain regions 34 and field effect transistor channel regions 36 have been formed within example selectively grown semiconductive material 13. Such may be fabricated by suitable masked or maskless conductivity-modifying doping of material 13 which extends over projections 20, 21, 22, and 23 and bridges over former voids 28.

In one embodiment, a method of forming field effect transistors includes providing a monocrystalline silicon-containing substrate which comprises a $\langle 100 \rangle$ plane direction. Insulative material is deposited over the monocrystalline silicon-containing substrate. A plurality of trenches are etched through the insulative material to silicon-containing material of the substrate parallel the $\langle 100 \rangle$ plane direction to provide monocrystalline silicon-containing material bases of the trenches which run parallel the $\langle 100 \rangle$ plane direction.

An elemental-form silicon-comprising material is epitaxially grown from the monocrystalline silicon-containing material of the trench bases and over the insulative material effective to bridge across the trenches with elemental-form silicon-comprising material and form covered trench voids within the trenches. In one embodiment, the monocrystalline silicon-containing material bases may be wet etched prior to the epitaxially growing. By way of example only, an exposure to a dilute HF solution comprises an example such wet etching. Regardless and in one embodiment, an exposed epitaxial seed material different from the insulative material may be provided over the insulative material prior to the epitaxially growing and from which the elemental-form silicon-comprising material bridging across the trenches is grown during the epitaxially growing. In one embodiment, the epitaxial seed material and the monocrystalline silicon-containing material bases may be wet etched prior to the epitaxially growing, for example utilizing a dilute HF solution as described above, or using some other solution.

At least one of field effect transistor channel regions or field effect transistor source/drain regions are formed within the elemental-form silicon-comprising material which bridges across the trenches. By way of example only, Fig. 12 depicts both such field effect transistor regions and field effect transistor source/drain regions being so formed in material 13 received over material 16. Further in one example embodiment, field effect transistor gates are formed within the trench voids. In one embodiment, an underside of the elemental-form silicon-comprising material bridging across the trenches is oxidized to at least partially form a gate dielectric on such underside within the covered trench voids. After such oxidizing, conductive material is deposited within the covered trench voids to form field effect transistor gates within the covered trench voids.

The above-described embodiments depict example second material-comprising projections which resulted in the formation of elongated trenches. Any alternative forms of projections, including combination of different shaped projections, are also of course contemplated. For example, alternate example projections 38 are depicted in Figs. 13 and 14 with respect to an alternate embodiment substrate portion 10b. Like numerals from the first-described embodiment substrate have been utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Figs. 13 and 14 depict projections 38 as comprising spaced free-standing pillars. Fig. 14 depicts the selectively growing to form material 13b to comprise a ceiling which covers a void 28b, with the ceiling be supported at least in part by the plurality of pillars 38 which are received within void 28b.

The above-depicted embodiments include but example methods of forming a covered void in a semiconductor substrate including the provision of exposed first, second, and third materials and projections. Alternate methods and constructions are of course contemplated independent of provision of exposed first, second, and third materials. For example and by way of example only, another embodiment substrate portion is indicated generally with reference numeral 40 in Fig. 15. Such includes an example elemental-form silicon-containing material 42 having a conductive material 44 deposited thereover. Example elemental-form silicon-containing materials include monocrystalline, polycrystalline, or amorphous silicon alone or in combination with other materials. Example conductive materials 44 include any one or combination of elemental metals, alloys of elemental metals, and/or conductive metal compounds. An example thickness range for conductive material 44 is from about 1,500 Angstroms to about 3,000 Angstroms.

Referring to Fig. 16, a plurality of openings 45, 46, and 47 have been etched through conductive material 44 to elemental-form silicon-containing material 42. In one embodiment, openings 45, 46, and 47 comprise elongated trenches, for example which run generally parallel a mean outermost global surface of the semiconductor substrate, for example as described in some of the other embodiments. Regardless and for purposes of the continuing discussion, openings 45, 46, and 47 may be considered as

comprising respective sidewalls 50 and bases 51. Of course, the etching to may also occur into material 42 (not shown) and not necessarily stop thereon.

Referring to Fig. 17, at least sidewalls 50 of openings 45, 46, and 47
5 have been lined with an insulative material 52. By way of example only, materials include silicon dioxide and/or silicon nitride. An example thickness range for insulative material 52 is from 60 Angstroms to 300 Angstroms. In one embodiment, bases 51 are also lined with insulative material 52 while lining sidewalls 50 with insulative material 52. In one embodiment,
10 material 52 is formed by chemical vapor deposition and/or atomic layer deposition.

Referring to Fig. 18 and in but one embodiment, insulative material 52 has been etched from atop the elevational outermost surfaces of conductive material 44 and from bases 51 within openings 45, 46, and 47. An example
15 technique for doing so includes utilizing a dry anisotropic fluorocarbon etching chemistry.

Referring to Fig. 19, an elemental-form silicon-comprising material 54 has been selectively grown relative to the insulative material over a plurality of openings 45, 46, and 47 effective to bridge across such openings to cover
20 such openings, thereby forming covered openings or covered voids 49. In one embodiment, elemental-form silicon-comprising material 55 has also been epitaxially grown from bases 51 within openings 45, 46, and 47 while selectively growing elemental-form silicon-comprising material 54. By way of examples only, materials 54 and 55 may comprise the same or different
25 compositions, and an elemental-form silicon-containing material may be so selectively grown to bridge across the plurality of openings for example as described above where conductive material 44 comprises any one or combination of elemental-form W or a silicide.

In one embodiment, the selectively growing of an elemental-form
30 silicon-comprising material effective to bridge across the plurality of openings may be devoid of epitaxially growing elemental-form silicon-comprising material from bases of the plurality of openings. Fig. 20 depicts an example alternate embodiment substrate portion 40a compared to that of Fig. 18. Like numerals from the Figs. 15-19 embodiment have been utilized
35 where appropriate, with differences being indicated with the suffix "a" or with

different numerals. Fig. 20 depicts alternate processing of a substrate portion 40a prior or subsequent to that of Fig. 17. In Fig. 20, the insulative material 52 of Fig. 17 has been removed from atop conductive material 44 or never provided thereover, but remains as an insulative material lining 52a within openings 45, 46, and 47 over bases 51. Such may be accomplished by any suitable etch or mechanical and/or chemical mechanical polishing process of material 52 of Fig. 17 at least to conductive material 44. Alternately by way of example only, some form of selective growth of material 52a may be conducted over sidewalls 50 and 51 but not over the tops of material 44. For example and by way of example only, tops of material 54 may be masked with a suitable layer of material, while sidewalls 50 and bases 51 are left unmasked during a selective growth of material 52a.

Referring to Fig. 21, elemental-form silicon-comprising material 54 has been selectively grown over the plurality of openings 45, 46, and 47 to bridge across and cover such openings, forming covered openings or covered voids 49a.

In one embodiment, an exposed seed material or an exposed epitaxial seed material may be provided proximate the tops of the plurality of openings over the conductive material prior to the selective growth, with such selective growth being an epitaxial growth from the exposed epitaxial seed material. One alternate example such embodiment is initially described in connection with a substrate portion 40b in Figs. 22-26. Like numerals from the Figs. 15-19 embodiment have been utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Referring to Fig. 22, an exposed seed material 58 or an exposed epitaxial seed material 58 has been provided over conductive material 44. Example materials include amorphous silicon, monocrystalline silicon, elemental-form W, elemental-form Ti, a silicide, and combinations thereof. An example thickness range for material 58 is from about 200 Angstroms to about 800 Angstroms.

Referring to Fig. 23, openings 45b, 46b, and 47b have been etched through material 58 and conductive material 44 to elemental-form silicon-containing material 42. Accordingly in the depicted embodiment, opening sidewalls 50b encompass materials 44 and 58. Also for purposes of the

continuing discussion, epitaxial seed material as received proximate the tops of plurality of openings 45b, 46b, and 47b may be considered as comprising elevationally outermost surfaces 60.

Referring to Fig. 24, an insulative material 52b has been formed to line openings 45b, 46b, and 47b. Referring to Fig. 25, insulative material 52b has been etched effective to remain lining at least sidewalls 50b of openings 45b, 46b, and 47b. Referring to Fig. 26, elemental-form silicon-comprising material 54b has been epitaxially grown over the plurality of openings 45b, 46b, and 47b effective to bridge across such openings to cover such openings, thereby forming covered openings or covered voids 49b. Elemental-form silicon-comprising material 55 has also been epitaxially grown from bases 51 of such openings in the depicted embodiment. Further, by way of example only in such embodiment, elevationally outermost surfaces 60 of material 58 were exposed during the selective growth and from which elemental-form silicon-comprising material 54 was grown during such epitaxial growth.

An alternate embodiment substrate 40c is depicted in Figs. 27 and 28. Like numerals with respect to the 40/40a/40b embodiments are utilized where appropriate, with differences being indicated with the suffix "c" or with different numerals. Referring to Fig. 27, insulative material 52c has been formed over sidewalls of material 44 within openings 45c, 46c, and 47c as well as over bases 51, but not over the sidewalls of material 58. For example, material 52c may be formed utilizing a selective thermal oxidation process whereby a conductive material 44 and elemental-form silicon-containing material 42 are selectively oxidized relative to material 58. Such a selective oxidation may be sufficiently high or essentially infinite for the thickness growth of material 52c such that none forms on material 58. Alternately, some insulative material 52c may so form. In such instance, a timed etch of material 52c may be conducted to clear oxide from material 58 but not from conductive material 44 or elemental-form silicon-containing material 42. For example, many silicides (e.g., tungsten silicide, platinum silicide, and cobalt silicide) will oxidize at a considerably slower rate than either of elemental-form silicon-containing material 42 or an example conductive material 44 of TiN, Ru, or Pt, and a short dilute HF wet etch may be used to clear any resulting oxide from material 58.

Referring to Fig. 28, elemental-form silicon-comprising material 54c has been selectively and/or epitaxially grown over the plurality of openings 45c, 46c, and 47c effective to bridge across and cover such openings,, thereby forming covered openings or covered voids 49c.

5 Figs. 29 and 30 depict an alternate embodiment substrate 40d. Like numerals have been utilized where appropriate with respect to the 40/40a/40b/40c embodiments, with differences being depicted with the suffix "d" or with different numerals. Referring to Fig. 29, insulative material 52d has been formed over the sidewalls of conductive material 44 within
10 openings 45d, 46d, and 47d selectively relative to materials 58 and 42. Referring to Fig. 30, elemental-form silicon-comprising material 54c has been selectively grown over the plurality of openings 45d, 46d, and 47d effective to bridge across such openings and cover such openings. Epitaxially grown elemental-form silicon-comprising material 55 has also
15 been grown from opening bases 51.

The above-described 40/40a/40b/40c/40d embodiments provide elevationally outermost surfaces 60 of material 58 to be outwardly exposed and from which the elemental-form silicon-comprising material 54 was grown. An alternate example embodiment substrate 40e is initially
20 described with reference to Figs. 31-35. Like numerals from the above 40/40a/40b/40c/40d embodiments are utilized where appropriate, with differences being indicated with the suffix "e" or with different numerals. Referring to Fig. 31, and desirably prior to the formation openings 45e, 46e, and 47e, a masking or covering layer 64 has been formed over material 58.
25 Some, none or all of such material may remain in the finished construction, and regardless some material composition other than the composition of material 58 is what is principally contemplated for material 64 in this particular embodiment. Such material may be insulative, conductive, and/or semiconductive. By way of example only, where material 42 comprises
30 silicon, material 44 comprises amorphous silicon, and material 58 comprises tungsten silicide, an example material 64 comprises silicon nitride.

Referring to Fig. 32, at least the sidewalls of the plurality of openings 45e, 46e, and 47e through conductive material 44 are lined with an insulative material 52e, for example and by way of example only analogous

to that depicted and described with respect to insulative material 52c in Fig. 27.

Referring to Fig. 33, elemental-form silicon-comprising material 54e has been selectively and/or epitaxially grown over the plurality of openings 45e, 46e, and 47e effective to bridge across and cover such openings, forming covered openings or covered voids 49e. Accordingly in the example Fig. 33 embodiment, elevationally outermost surfaces 60 of material 58 are covered during such epitaxial growth.

Referring to Fig. 34 and by way of example only, some subsequent processing of substrate 40e has been depicted. Specifically, masking material 64 is shown as having been removed substantially selectively relative to elemental-form silicon-comprising material 54e and material 58. Further possible subsequent processing is depicted in Fig. 35, whereby material 58 has been selectively removed relative to elemental-form silicon-comprising material 54e and conductive material 44.

Fig. 36 illustrates alternate example subsequent processing with respect to the processing depicted by Fig. 33. Like numerals from the 40e embodiment have been utilized where appropriate, with differences being indicated with the suffix "f" or with different numerals. In Fig. 33, elemental-form silicon-comprising material 54e was not grown to the point of bridging over masking material 64. Fig. 36 depicts wafer portion 40f having been processed to grow elemental-form silicon-comprising material 54f to bridge over masking material 64.

By way of example only, Figs. 37 and 38 depict an alternate embodiment substrate portion 40g analogous to that of Fig. 32, but wherein insulative material 52g is not formed, or has been removed from, over bases 51. Like numerals from the embodiment of Figs. 32 and 33 have been utilized where appropriate, with differences being indicated with the suffix "g".

Embodiments of methods of forming one or more covered voids in a semiconductor substrate are now additionally described in connections with Figs. 39-45. Referring to Fig. 39, a semiconductor substrate portion is indicated generally with reference numeral 70. Such comprises some base substrate 72, for example and by way of example only, bulk monocrystalline silicon. A first material 74 is deposited over substrate 72. A second material

76 is deposited over first material 74. A third material 78 is deposited over second material 76. Second material 76 is thereby received intermediate first material 74 and third material 78, and second material 76 is compositionally different from first material 74 and from third material 78.

5 The first and third materials may be compositionally the same or different. The first and third materials may be insulative, conductive, and/or semiconductive, with insulative being preferred. Example materials include one or a combination of silicon dioxide or silicon nitride. By way of example only, example second materials include elemental-form silicon (including
10 amorphous and/or crystalline forms of elemental-form silicon), elemental-form W, elemental-form Ti, and a silicide, including mixtures/combinations thereof. For purposes of the continuing discussion, third material 78 may be considered as having an elevationally outermost surface 79, and which may or may not be planar.

15 An example thickness range for each of layers 74, 76, and 78 is from 200 Angstroms to 3,000 Angstroms. Further by way of example only, first material 74 may be thicker or thinner than third material 78. Further, third material 78 may be thicker or thinner than second material 76. Further, any two or all three of materials 74, 76, and 78 may be of about the same
20 thickness.

Referring to Fig. 40, openings 80 have been formed through third material 78, second material 76, and first material 74 to substrate material 72. Such openings may also, of course, extend into material 72. In one embodiment, openings 80 may be formed by etching, and in one
25 embodiment comprise a plurality of elongated trenches.

In one embodiment, openings 80 may be considered as providing or defining respective pairs of upwardly-projecting sidewalls 82 relative to a semiconductor substrate 70. Sidewalls 82 have a space 83 therebetween which comprises opposing first, second, and third materials 74, 76, and 78,
30 respectively.

Referring to Fig. 41, a fourth material 86 has been grown from opposing second material 76 of sidewalls 82 selectively relative at least to first material 74 and third material 78 effective to form a bridge of fourth material 86 across space 83 to form respective covered voids 87 between
35 sidewalls 82. In one embodiment, essentially no fourth material 86 grows

from sidewalls of first material 74 and third material 78, with the depicted covering of portions of sidewalls of materials 74 and 78 within openings 80 by material 86 only occurring as the result of upward and downward growth of material 86 from itself within openings 80. The second and fourth materials may be compositionally the same or different. In one embodiment, such selectively growing forms the fourth material to comprise elemental-form silicon. In one embodiment, the fourth material is formed to comprise any one or more of elemental-form W or a silicide. Example processing and materials may be as described in any of the above-described embodiments.

Fig. 41 depicts an embodiment whereby a material 88 deposits atop and/or also selectively from substrate material 72 during the growth of material 86 from second material 76. In such event, material 88 may be compositionally the same as or different from material 86.

Fig. 41 also depicts an embodiment wherein the selectively growing does not grow fourth material 86 to extend over an elevationally outermost surface 79 of third material 78. Fig. 42 depicts continued processing and/or an alternate embodiment whereby the selectively growing of material 86 is continued sufficiently to grow fourth material 86 to extend over elevationally outermost surfaces 79 of third material 78.

Referring to Fig. 43, substrate 70 has been polished inwardly to at least third material 78 to leave fourth material 86 bridging over covered voids 87. Fig. 44 illustrates example subsequent or continued processing whereby polishing of substrate 70 has been conducted inwardly to at least second material 76 to leave fourth material 86 bridging over covered voids 87. Fig. 45 illustrates still subsequent or continued processing whereby substrate 70 has been polished inwardly to first material 74 to still leave some fourth material 86 bridging over covered voids 87.

In one embodiment, a method of forming a covered void within a semiconductor substrate includes providing a bulk monocrystalline silicon-containing substrate. By way of example only with respect to Fig. 39, material 72 may constitute a bulk monocrystalline silicon-containing substrate. A first insulative material is deposited over the bulk monocrystalline silicon-containing substrate. With respect to the Fig. 39 embodiment, material 74 may comprise an example such first insulative material. An elemental-form silicon-containing material is deposited over the

first insulative material. In the context of the Fig. 39 embodiment, material 76 may comprise an example such elemental-form silicon-containing material. A second insulative material is deposited over the elemental-form silicon-containing material. In the context of the Fig. 39 embodiment, material 78 may comprise such a second insulative material. The first insulative material may be compositionally be the same as or different from the second insulative material. In one embodiment, the first insulative material comprises silicon dioxide and the second insulative material comprises silicon nitride. In one embodiment, the elemental-form silicon-containing material deposited over the first insulative material comprises amorphous silicon and/or monocrystalline silicon.

A plurality of trenches is etched through the second insulative material, the elemental-form silicon-containing material, and the first insulative material to the bulk silicon-containing material of the substrate. By way of example only, Fig. 40 depicts such example processing. Again of course, etching may occur into material 72.

A silicon-comprising material is selectively grown from the elemental-form silicon-containing material and from the bulk silicon-containing material of the substrate within the trenches effective to bridge across the trenches with elemental-form silicon-comprising material to form covered trench voids within the trenches. By way of example only, Figs. 41 and 42 depict examples of such processing. In one embodiment, at least one of field effect transistor channel regions or field effect transistor source/drain regions are formed within the elemental-form silicon-comprising material bridging across the trenches.

Also of course with respect to any of the above described embodiments, the covered openings/voids which are formed may subsequently be wholly or partially filled with any one or combinations of insulative, conductive, or semiconductive materials. Also and regardless, any of the above embodiments may not form trenches and/or provide other configuration projections forming one or more covered openings/voids. For example and by way of example only, the embodiment of Figs. 13 and 14 may be utilized in the context of free-standing pillar formation. Regardless, any other of the above and below attributes with respect to any other of the disclosed embodiments are of course contemplated.

Embodiments herein encompass methods of forming a span comprising silicon dioxide. For example, an opening comprising sidewalls is formed within a semiconductor substrate. Further, the one or more covered voids may be wholly or partially formed within semiconductive material of the semiconductor substrate or be received entirely outside of any semiconductor material of the semiconductor substrate. An elemental-form silicon-containing material is selectively grown relative to at least some portion of the sidewalls to bridge across the opening to form a covered cavity within the opening. By way of examples only, any of the above-depicted and described embodiments of selectively growing an elemental-form silicon-containing material to bridge across an opening to form a covered cavity or void within the opening are of course contemplated.

In one embodiment, at least an outermost upper half of the selectively grown elemental-form silicon-containing material is oxidized across the opening to form a silicon dioxide-comprising bridge across the opening over the cavity. By way of example only, Figs. 46 and 47 depict a wafer portion 10c processed in accordance with an example of the just-described embodiment. Figs. 46 and 47 depict substrate portion 10 of Figs. 5 and 6 at a processing step alternate to that depicted by Figs. 7 and 8, and is accordingly designated 10c. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "c" or with different numerals. Figs. 46 and 47 depict an outermost upper half of selectively grown elemental-form silicon-containing material 13 which bridges across the depicted openings as having been oxidized, thereby forming a silicon dioxide-comprising bridge 90 across the openings over the cavities and leaving bridging silicon-containing material 13c. Figs. 46 and 47 depict the oxidizing as being of less than all of the epitaxially grown elemental-form silicon-containing material, with only about half of such material being oxidized to form the silicon dioxide-comprising bridge 90. Regardless and in one embodiment, elemental-form silicon-comprising material may be epitaxially grown from a base of the opening or openings while selectively growing the elemental-form silicon-containing material which bridges across the opening, for example as depicted in Figs. 46 and 47. Elemental-form silicon-containing material 13 may be selectively grown from elemental-form silicon-containing material and/or

from at least one of elemental-form W, elemental-form Ti, or a silicide. Processing may otherwise be conducted, by way of example only, as described above in connection with the substrate 10/10a/10b and other embodiments.

5 Figs. 48 and 49 illustrate an alternate embodiment substrate portion 10d. Like numerals from the first-described substrate 10/10c embodiments have been utilized where appropriate, with differences being indicated with the suffix "d" or with different numerals. Figs. 48 and 49 depict substrate portion 10d wherein all of the selectively grown elemental-
10 form silicon-containing material of Fig. 5 and 6 has been oxidized to form a silicon dioxide-comprising bridge 90d across the respective openings over the respective cavities. Processing may otherwise occur as described above with respect to the substrate 10/10a/10b/10c and other embodiments.

Additional embodiments of methods of forming covered voids in a
15 semiconductor substrate are next described with reference to Figs. 50-53. Referring to Fig. 50, a substrate portion 100 comprises some base substrate 102, for example monocrystalline silicon and/or at least one other semiconductor material. Projections 104, 105, and 106 project upwardly from substrate 102, and comprise sidewalls 108. Projections 104, 105,
20 and 106 comprise different composition first and second materials 110 and 112, respectively, with second material 112 comprising at least some outwardly-exposed portion which is received over first material 110. First and second materials 110, 112 may be insulative, conductive, semiconductive, and including any combination thereof. Example materials
25 of construction and dimensions for materials 110 and 112 are as described above in connection with the first-described embodiment for layers 14 and 16, respectively. For purposes of the continuing discussion, second material 112 may be considered as comprising elevationally outermost surfaces 114 and second material sidewalls 116.

30 Referring to Fig. 51, a third material 120 has been selectively grown from second material 112 elevationally inward along projection sidewalls 108 and effective to bridge across projections 104, 105, and 106 with third material 120 to form respective covered voids 122 between adjacent pairs of the projections. Example attributes, materials, and methods are otherwise
35 as described in connection with any of the above embodiments. The third

material may be of the same composition as the second material, or of different composition. In one embodiment, the third material comprises elemental-form silicon, and the selectively growing comprises selective and/or epitaxial silicon-comprising growth. In one embodiment, the second material comprises elemental-form silicon. In one embodiment, the second material comprises any one or more of elemental-form W, elemental-form Ti, or a silicide. In one embodiment, the second material comprises elemental-form silicon, and the selectively growing comprises any one or more of elemental-form W or a silicide. In one embodiment, the second material comprises any one or more of elemental-form W, elemental-form Ti, or a silicide, and the selectively growing comprises epitaxial silicon-comprising growth. In the Fig. 51 embodiment, selective growth of third material 120 occurs from exposed elevationally-outermost surfaces 114 of second material 112 and from exposed sidewalls surfaces 116 of second material 112. Alternately, portions or all of at least one of such may be covered during the selective growth.

Referring to Fig. 52, third material 120 has been removed inwardly at least to second material 112 and effective to leave a third material-comprising bridge 120 across the respective adjacent pair of projections over the respective covered voids 122. Such removing may comprise any one or combination of etching, mechanical polishing, and/or chemical mechanical polishing. Further, such removing of third material 120 may be conducted inwardly to first material 110, for example as shown in Fig. 53. Again for example in such instance, such removing of the third material is effective to leave a third material-comprising bridge 120 over the respective pairs of projections over the covered voids.

Other attributes and methods may otherwise be as described in any of the above and below embodiments. For example and by way of example only, the covered voids may be provided to comprise elongated trenches running generally parallel a mean outermost global surface of the semiconductor substrate. Further in one embodiment, at least a majority of such trenches may be filled with conductive material to form elongated conductive lines therefrom. Alternately and by way example only, the pair of projections may be formed to comprise other structures, for example spaced free-standing pillars, prior to the stated selective growth. In one

embodiment, the selective growth may form one or more voids to be covered by a ceiling supported at least in part by the plurality of pillars received within the void.

Embodiments herein also include methods of cooling semiconductor devices. For example, any of the structures shown and described herein which provide covered trenches or openings may be utilized in such method embodiments and in structure embodiments. Example materials of construction and dimensions are otherwise as disclosed herein. A method of cooling semiconductor devices in accordance with an embodiment comprises etching trenches into an insulative material. An elemental-form silicon-containing material is selectively grown across the trenches to convert the trenches to elongated covered conduits. At least one integrated circuit device is formed and is received at least partially within the elemental-form silicon-containing material received at least across one of the elongated covered conduits. Coolant is provided within the conduits, and preferably comprises the flowing of coolant therethrough for example in the form of one or both of liquid or gas.

In one embodiment, the trenches are provided to have exposed trench bases which comprise elemental-form silicon-containing material over which the insulative material is deposited. In one embodiment, an elemental-form silicon-containing material was epitaxially grown from the trench bases during the selectively growing of the elemental-form silicon-containing material across the trenches to convert the trenches to elongated covered conduits.

In one embodiment, etching of the trenches first comprises depositing insulative material over an elemental-form silicon-containing material. The trenches are then etched into such insulative material. An exposed seed material, which is different from the insulative material, is provided over the insulative material prior to the selective growth and from which the elemental-form silicon-comprising material received across the trenches is selectively grown during such selective growth. Of course, any of the above-described seed materials may be utilized, and regardless such seed material may be provided over the insulative material prior to or after the etching to form the trenches. If provided before, the act of etching the plurality of trenches will also occur first through the seed material and then

through the insulative material. In one embodiment, the selective growth comprises epitaxial growth of the elemental-form silicon-containing material.

Embodiments herein also include methods of forming semiconductor-on-insulator substrates. For example referring to Fig. 54, a portion of a semiconductor-on-insulator substrate is indicated generally with reference numeral 130. Such comprises some base substrate 132, an insulator layer 134 received thereover, and a silicon-containing semiconductor layer 136 received over insulator layer 134. Base substrate 132 may comprises a bulk monocrystalline silicon-containing substrate. Example materials for insulator 134 include one or both of silicon dioxide or silicon nitride. An example thickness range for layer 134 is from about 1,000 Angstroms to about 3,000 Angstroms. An example thickness range for silicon-containing semiconductor layer 136 is from about 600 Angstroms to about 2,000 Angstroms, with example materials including monocrystalline silicon and SiGex, where "x" ranges from 0.01 to 2.0.

Referring to Fig. 55, a plurality of openings 138, 140, and 142 have been etched through semiconductor layer 136. Such etching may also be conducted to extend openings 138, 140, and 142 partially into or completely through insulator layer 134 (not shown in Fig. 55). Openings 138, 140, and 142 may be of any shape, for example shapes as disclosed herein, with one embodiment being of elongated trenches running generally parallel a mean outermost global surface of the semiconductor-on-insulator substrate. Substrate portion 130 in Fig. 55 is depicted as having a planar outermost global surface defined by the outermost surface of silicon-containing semiconductor layer 136, although planarity is of course not required.

Referring to Fig. 56, an elemental-form silicon-comprising material 144 has been epitaxially grown over silicon-containing semiconductor layer 136 received over insulator layer 134 effective to bridge across openings 138, 140, and 142 with elemental-form silicon-comprising material, and to form covered voids 146 within openings 138, 140, and 142. At least one of field effect transistor channel regions or field effect transistor source/drain regions are formed within the elemental-form silicon-comprising material bridging across openings 138, 140, and 142.

For example and by way of example only, Fig. 57 depicts both field effect transistor channel regions 154 and field effect transistor source/drain

regions 156 formed within material 144. Gate constructions 148 have been formed directly over openings 138, 140, and 142. Such are depicted as comprising conductive regions 150 formed over a gate dielectric region 152.

Covered voids 146, in whole or in part, may remain as part of the finished circuitry construction, for example provided with coolant fluid flowing or statically received therein. In one embodiment, covered voids 146 are wholly or partially filled with one, two, or three of any of conductive, semiconductive, and/or insulative materials. In one embodiment, a field effect transistor gate construction is provided within previous voids 146, and perhaps with gate constructions 148 in such embodiment being eliminated. Alternately by way of example only, field effect transistor gate constructions may be provided both within previously covered voids 146 and thereover, for example as depicted in Fig. 58. Substrate portion 130 in Fig. 58 is depicted as comprising a gate dielectric 160 and conductive material 162 within previous covered voids 146. Thereby, example channel regions 154 are gated from above and below. By way of example only, the gate dielectric may be formed by a thermal oxidation utilizing gases which access covered voids 146 (Fig. 57) from one or more ends thereof, followed by an isotropic deposition of any suitable conductive material 162, for example as described elsewhere in this document.

In one embodiment, Figs. 54-58 depict epitaxial growth of an elemental-form silicon-comprising material 144 from exposed portions of an example silicon-containing semiconductor layer 136. By way of example only in but one alternative, an exposed epitaxial seed material may be provided over the silicon-containing semiconductor layer prior to the epitaxial growth and from which the elemental-form silicon-comprising material is grown during such epitaxial growth. Such an example embodiment is depicted with respect to a substrate portion 130a in Figs. 59 and 60. Like numerals from the first-described embodiment have been utilized where appropriate, with differences being indicated with the suffix "a" or with different numerals. Fig. 59 depicts substrate portion 130a as comprising an exposed epitaxial seed material 166 received over silicon-containing semiconductor layer 136, and through which openings 138a, 140a, and 142a are formed. Example epitaxial seed materials are as described elsewhere in this document. Fig. 60 depicts subsequent epitaxial

growth of an elemental-form silicon-comprising material 144a over layer 136 effective to bridge across the openings with elemental-form silicon-comprising material 144a to form covered voids 146 within openings 138a, 140a, and 142a.

5 Another embodiment is described in connection with Figs. 61-63 with respect to a substrate portion 130b. Like numerals from the substrate portion 130 embodiment are utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Referring to Fig. 61, openings 138b, 140b, and 142b have not only been etched through
10 semiconductor 136, but also through insulator layer 134 to a bulk monocrystalline silicon-containing material 132 of a bulk monocrystalline silicon-containing substrate. Openings 138b, 140b, and 142b comprise monocrystalline silicon-containing bases 168. Of course, etching may also occur into material 132 (not shown).

15 Referring to Fig. 62, an elemental-form silicon-comprising material 145 is epitaxially grown from monocrystalline silicon-containing bases 168, and an elemental-form silicon-comprising material 144b is epitaxially grown from over silicon-containing semiconductor layer 136 received over insulator layer 134 effective to bridge across openings 138b,
20 140b, and 142b, and form covered voids 146b within such openings. At least one of field effect transistor channel regions or field effect transistor source/drain regions are formed within elemental-form silicon-comprising material 144b bridging across openings 138b, 140b and 142b.

Any of the processing and constructions as depicted and described in
25 the Figs. 54-60 embodiments may be fabricated with respect to the Fig. 62 embodiment. For example and by way of example only, Fig. 63 depicts the fabrication of gate constructions 172 within what were previously-covered voids 146b (Fig. 62). Dielectric material 174 has been formed, for example by thermal oxidation of materials 144b and 145 within the covered voids
30 146b of Fig. 62. A conductive gate material 176 has been subsequently deposited thereover, with at least the uppermost dielectric material 174 received against material 144b comprising a gate dielectric. Channel regions 154b and source/drain regions 156b have been formed within epitaxially grown elemental-form silicon-comprising material 144b.

Embodiments herein encompass integrated circuitry. In one embodiment, integrated circuitry comprises a semiconductor-on-insulator substrate having some mean outermost global surface. The substrate comprises monocrystalline silicon-containing material, an insulator received
5 over the monocrystalline silicon-containing material, and an elemental-form silicon-comprising material received over the insulator. A plurality of elongated cooling conduits runs generally parallel to the mean outermost global surface within the insulator (i.e., within at least some portion of the insulator). Cooling fluid is received within the cooling conduits. In certain
10 embodiments, one or both of field effect transistor channel regions and/or field effect transistor source/drain regions are received within the elemental-form silicon-comprising material that is over the cooling conduits. Example constructions, materials, dimensions, and methods of fabrication are otherwise as described anywhere else in this document.

Embodiments of methods of forming a semiconductor-on-insulator substrate are next described with reference to Figs. 64-70 with respect to a substrate portion 200. Referring to Fig. 64, such comprises a base substrate 202 having an insulative layer 204 formed thereover. In one embodiment, an epitaxial seed material 206 or a seed material 206 is formed
15 over insulative material 204. In one embodiment, base substrate 202 comprises a bulk monocrystalline silicon wafer and/or a carrier substrate. Regardless and for purposes of the continuing discussion, base substrate 202 may be considered as comprising a base region 208, a silicon-containing semiconductor region 212 over base region 208, and a
20 release region 210 provided intermediate silicon-containing semiconductor region 212 and base region 208. In one embodiment, base substrate 202 comprises bulk monocrystalline silicon, and in one embodiment release region 210 is formed by implanting hydrogen into base substrate 202. For example, a hydrogen-implanted release region 210 may be formed by
25 implanting hydrogen ions (H⁺) at about 40-210 KeV at a dose of about 5E16/cm². Alternately and by way of example only, another example release region 210 may be formed to comprise an insulator layer received over base region 208. For example, such may be formed by the suitable implant of oxygen atoms and a subsequent anneal to form a silicon dioxide
30 region 210. As an alternate example, a suitable silicon dioxide or other
35

layer may be deposited atop a base substrate 208, and a silicon-containing semiconductor region 212 formed thereover subsequently. Regardless, an example thickness range for release region 210 is from about 200 Angstroms to 2 about microns, and some interface 215 is inherently
5 provided or formed relative to release region 210 and silicon-containing semiconductor region 212.

Referring to Fig. 65, cooling trenches 218 have been etched into insulative layer 204 to silicon-containing semiconductor region 212. Where material 206 is provided, cooling trenches 218 are also etched therethrough
10 as shown in the depicted embodiment.

Referring to Fig. 66, a bridging material 220 has been selectively grown (relative to the insulative layer, at least) over insulative layer 204 effective to bridge across cooling trenches 218 with bridging material, and form covered elongated cooling trenches 224. Example materials and
15 dimensions for, and methods of forming, bridging material 220 are as described above in other embodiments for the covering of voids/trenches. Of course as in embodiments described elsewhere in this document, epitaxial seed materials and seed materials such as disclosed may be utilized, and regardless growth of epitaxial material may occur from bases of
20 openings 218, for example as shown. Regardless, covered elongated cooling trenches 224 may, at this point or later, be partially filled with one or more of insulative, semiconductive, and/or conductive materials.

Referring to Fig. 67, and in but one example embodiment, an insulator layer 223 has been formed on an outer surface of bridging material 220
25 bridging across cooling trenches 218. In one embodiment, such is formed to have a substantially planar outer surface 225.

Referring to Fig. 68, at interface 215 of release region 210 (not shown) and silicon-containing semiconductor region 212, separation has occurred of a) base region 208 (not shown) and release region 210 (not
30 shown) from b) silicon-containing semiconductor region 212, insulative layer 204 with covered elongated cooling trenches 224, and bridging material 220. By way of example only, techniques for doing so include so-called "smart-cut techniques", and for example as described in U.S. Patent No. 6,184,111.

Referring to Fig. 69 and in but one embodiment, substrate 200 has
35 been bonded with a carrier substrate 230. In one embodiment, carrier

substrate 230 comprises some base substrate 232 having an oxide layer 234 formed thereover. Insulator layer 223 of substrate 200 has been bonded to carrier substrate 230, and in the depicted embodiment to oxide layer 234 thereof. Regardless, at least one of field effect transistor channel regions or field effect transistor source/drain regions are formed within silicon-containing semiconductor region 212, and cooling fluid is provided within cooling trenches 224.

For example, Fig. 70 depicts subsequent processing wherein a gate dielectric 240 has been formed over silicon-containing semiconductor region 212, and gates constructions 242 have been formed thereover. Fig. 70 also depicts channel regions 250 and source/drain regions 252 being formed in silicon-containing semiconductor region 212. Cooling fluid may ultimately be provided within the covered elongated cooling trenches. Such cooling fluid may comprise flowing gas, for example air, and/or a suitable flowing liquid.

The above example Figs. 64-70 embodiment encompasses a method wherein the release region was formed prior to the etching to form trenches 218. Figs. 71-73 depict an alternate embodiment substrate portion 200a wherein the release region is formed after the etching to form the cooling trenches. Like numerals from the first-described embodiment are utilized where appropriate, with differences being indicated with the suffix "a". Referring to Fig. 71, base substrate 202a comprises a base region 208a and silicon-containing semiconductor region 212a which is void of a defined release region, at least at this point in the process.

Referring to Fig. 72, cooling trenches 218 have been etched into insulative layer 204 to silicon-containing semiconductor region 212.

Referring to Fig. 73, release region 210a has been formed intermediate silicon-containing semiconductor region 212a and base region 208a. Such may be formed, by way of example only, by implanting one or more of hydrogen atoms and/or oxygen atoms. A wholly or partially sacrificial planarized layer may be provided over substrate 200a prior to such implanting effective to fill openings 218 to provide uniform thickness material for ion implanting therethrough to form release region 210a. Processing may proceed subsequently as described above, or otherwise, with respect to the Figs. 64-70 embodiment.

Embodiments of methods of forming a semiconductor-on-insulator substrate are next described with reference to Figs. 105 and 106 with respect to a substrate portion 200b. Like numerals from the Figs. 64-70 substrate portion 200 embodiment are utilized where appropriate, with
5 differences being indicated with the suffix "b" or with different numerals.

Referring to Fig. 105, alternate processing to that depicted by Fig. 70 is shown. Specifically, suitable gate dielectric material 227 and conductive first field effect transistor gates 229 have been formed within trenches 224. Accordingly in this embodiment at least with respect to the depicted
10 trenches 224, such do not function as cooling trenches within which cooling fluid is ultimately received.

Referring to Fig. 106, gate dielectric 231 has been formed over silicon-containing semiconductor region 212. Second field effect transistor gates 233 have been formed opposite first field effect transistor gates 229
15 over silicon-containing semiconductor region 212. Field effect transistor channel regions 235 have been formed within material of silicon-containing semiconductor region 212 received between first field effect transistor gates 229 and second field effect transistor gates 233. Source/drain regions 237 have been formed within silicon-containing semiconductor region 212.
20 Processing sequence to produce the Fig. 106 structure may of course be in any order with respect to components/regions 227, 229, 231, 233, 235, and 237. Processing may otherwise occur as described above with respect to either of the Figs. 64-70 embodiment or the Figs. 71-73 embodiment, and by way of examples only.

25 Some embodiments herein include electromagnetic radiation guides (such as conduits) and methods of forming electromagnetic radiation guides. An example embodiment is described with reference to Figs. 74-79.

Referring to Fig. 74, a semiconductor construction 300 comprises a base 302 and a material 304 over the base. The base 302 may comprise
30 one or more semiconductor materials, such as silicon or germanium. In some embodiments, the base may be configured to generate electromagnetic radiation upon appropriate electrical stimulus. In such embodiments, the base may comprise, consist essentially of, or consist of III/IV material (for example, may contain one or more of InAlP, GaS, and

GaN), or a II/VI material (for example, may contain one or both of zinc selenide and cadmium telluride).

Material 304 is ultimately patterned into projections over base 302, and may comprise any material suitable to form such projections. Material 304 may be electrically insulative, conductive or semiconductive. In some
5 304 may be electrically insulative, conductive or semiconductive. In some embodiments, material 304 is electrically insulative and comprises, consists essentially of, or consists of silicon dioxide and/or silicon nitride.

Referring to Fig. 75, material 304 is patterned into a plurality of projections 306, with such projections being spaced from one another by
10 gaps 308 extending to base 302. Although the gaps are shown extending only to an upper surface of base 302, in other embodiments the gaps may extend into base 302.

Material 304 may be patterned utilizing any suitable processing. For instance, photolithographically patterned photoresist may be provided over
15 material 304 to define the pattern which is ultimately be formed in material 304; an etch may be conducted to transfer the pattern from the photoresist to the material 304; and subsequently the photoresist may be removed to leave the construction of Fig. 75.

Referring to Fig. 76, a metal-containing layer 310 is formed along
20 sidewalls of projections 306 within openings 308. The metal-containing layer may comprise, consist essentially of, or consist of one or more of elemental metal (such as titanium or tungsten), metal alloys, and metal-containing compositions (such as metal nitride). The metal-containing layer 310 may be formed to line only the sidewalls of projections 304 by any
25 suitable processing. For instance, the metal-containing material may be initially formed as a layer extending across an entire upper topography of construction 300, and then such layer may be subjected to an anisotropic etch to leave the construction of Fig. 76.

Referring to Fig. 77, seed material 312 is formed over upper surfaces
30 of projections 304. The seed material may be formed by a selective deposition onto the upper surfaces of projections 304, or may be formed by a non-selective deposition followed by an etch. Although the seed material is formed after the patterning of projections 306 in the shown embodiment, in other embodiments the seed material may be provided over material 304

prior to the patterning of the projections. In such other embodiments, the seed material may be patterned during the patterning of the projections.

The seed material may comprise any of the seed materials discussed previously in this disclosure. Accordingly, the seed material may comprise
5 crystalline semiconductor material, tungsten, titanium, silicide, etc.

Referring to Figs. 78 and 79, a covering material 314 is grown from the seed material to bridge across the projections 306. The material 314 may comprise the same composition as the seed material 312. Accordingly, material 314 may merge with the seed material to form a single
10 homogeneous composition extending across the projections 306 and bridging over the openings 308.

Fig. 79 shows that the openings 308 form a plurality of conduits extending over base 302. In operation, base 302 may be stimulated to generate electromagnetic radiation which enters the conduits and is then
15 guided by the conduits to desired locations. The electromagnetic radiation may comprise any suitable wavelength, and in some embodiments may correspond to visible light. The metal-containing lining (or cladding) 310 may polarize electromagnetic radiation generated by base 302. In some embodiments, the metal-containing lining may be omitted.

20 Openings 308 may be open spaces at the processing stage of Fig. 78 (as shown), or may be at least partially filled with material. For instance, a material may be provided within the openings that has refractive properties different from those of base 302, cover 314 and metal-containing layer 310 to enhance retention of electromagnetic radiation within the conduits. If the
25 openings are to be at least partially filled with material, such material may be provided prior to the formation of cover 314 across the openings in some embodiment.

In some embodiments, base 302 may comprise a composition which is not an electromagnetic radiation emitter, and instead electromagnetic
30 radiation may be introduced into the conduits from a source other than the base.

Another example embodiment method of forming an electromagnetic radiation guide is described with reference to Figs. 80-84.

Referring to Fig. 80, a construction 320 comprises a base 322 having a
35 plurality of projections 324 supported thereover. The projections comprise a

material 326 and another material 328. In some embodiments, base 322 may comprise monocrystalline silicon, material 326 may comprise silicon dioxide, and material 328 may comprise monocrystalline silicon. Accordingly, construction 320 may correspond to a patterned silicon-on-insulator (SOI) structure similar to that of Fig. 61. In some embodiments, base 322 may be considered to comprise a first material, material 326 may be considered a second material, and material 328 may be considered a third material. In some embodiments, material 328 may comprise one or more of elemental-form tungsten, elemental-form titanium, or silicide.

Referring to Fig. 81, covering material 330 is epitaxially grown from material 328, and accordingly material 328 functions as a seed layer. Material 330 may comprise monocrystalline silicon, and accordingly may comprise the same composition as the material of base 322.

The growth of material 330 forms conduits 332 contained between projections 324, base 322, and a cover defined by material 330.

Referring to Fig. 82, materials 328 and 330 may be oxidized to form an oxide 334. In embodiments in which material 326 comprises silicon dioxide, and materials 328 and 330 comprise silicon, such oxidation may form oxide 334 to be a silicon dioxide which merges with the silicon oxide of projections 326, as shown.

Referring to Figs. 83 and 84, conduits 332 are lined with material 340, and the lined conduits are then filled with material 342. The materials 340 and 342 may be chosen to have light-refracting characteristics which substantially retain particular wavelengths of electromagnetic radiation within the conduits so that such wavelengths may be guided by the conduits from one location to another. For instance, one or both of materials 340 and 342 may have different light refracting properties than the material of base 332, or one or both of materials 326 and 334. In some embodiments, materials 328 and 330 will not be oxidized to form material 334, and in such embodiments one or both of materials 340 and 342 may have different light refracting properties than one or both of materials 328 and 330. In some embodiments, one or both of the materials 340 and 342 may be omitted. In some embodiments, one or both of materials 340 and 342 may comprise metal. The metal may be in elemental form, alloy form, or in the form of a metal-containing composition (for example a nitride or a silicide).

Fig. 84 shows that conduits 332 having the materials 340 and 342 therein form electromagnetic radiation-guiding paths. Specifically, electromagnetic radiation is diagrammatically illustrated by arrows 344 as entering the conduits at one end, being directed along the conduits, and exiting the conduits at another end.

Some embodiments herein include imager systems and methods of forming imager systems. An example embodiment is described with reference to Figs. 85-89.

Referring to Fig. 85, a construction 350 comprises a semiconductor base 352 and a material 354 formed over the base. The material 354 may comprise an electrically conductive composition, and may accordingly comprise metal, metal-containing compounds, and/or conductively-doped semiconductor material. The material 354 comprises a different composition than semiconductor base 352. In some embodiments, base 352 may comprise monocrystalline silicon.

A seed region 356 is provided over material 354. An approximate boundary where the seed material joins material 354 is diagrammatically illustrated with a dashed line 355. In some embodiments, the seed material may be identical in composition to the remainder of material 354, and is defined only by its location at an uppermost region of material 354 from which growth of additional materials ultimately occurs. The seed regions may comprise monocrystalline silicon. In some embodiments, both material 354 and material 356 comprise, consist essentially of, or consist of monocrystalline silicon. In other embodiments, material 354 comprises a composition other than monocrystalline silicon, while material 356 comprises, consists essentially of, or consists of monocrystalline silicon. In such other embodiments, material 354 may comprise one or more electrically conductive compositions, such as elemental metal and/or one or more metal-containing compounds.

Referring to Fig. 86, material 354 and seed material 356 are patterned to form a plurality of openings 358 extending to base 352, and to form a plurality of projections 360 comprising material 354 and seed material 356. Materials 354 and 356 may be patterned by any suitable method. For instance, a photolithographically patterned photoresist mask may be formed over the materials, a pattern may be transferred from the mask to the

materials with the one or more suitable etches, and then the mask may be removed to leave the construction of Fig. 86.

Referring to Fig. 87, openings 358 are at least partially filled with dielectric material 362. In the shown embodiment, the openings are entirely
5 filled with dielectric material 362 and a planarized surface 363 extends across material 356 and dielectric material 362. The construction of Fig. 87 may be formed by providing dielectric material 362 to entirely fill the openings 358 and to extend across projections 360, followed by planarization (for example chemical-mechanical polishing) to remove
10 material 362 from over the projections and form the shown planarized surface 363. Dielectric material 362 may comprise, consist essentially of, or consist of silicon dioxide. In some embodiments, the openings may be left open rather than being at least partially filled with dielectric material (in other words, the processing of Fig. 87 may be omitted).

Referring to Fig. 88, monocrystalline silicon 364 is grown from seed
15 material 356, and over openings 358. In the shown embodiment, the openings 358 are filled with dielectric material 362, and accordingly monocrystalline silicon 364 is grown over such dielectric material.

Referring to Fig. 89, a pixel 370 (specifically, a CMOS imager device)
20 is formed to be supported by monocrystalline silicon 364. The pixel includes first and second gate constructions 371 and 373, and source/drain regions 372, 382 and 384; with source/drain region 372 corresponding to a photodiode. The photodiode extends across several pockets of dielectric material 362. The buried dielectric material 362 may provide some electrical
25 isolation to charge flowed into the underlying base 352, without excluding the ability to use conventional isolation structures, (such as the shallow trench isolation structures 374), to isolate pixels from one another in layer 364.

The pockets of dielectric material 362 may have sub-wavelength width
30 and depth dimensions relative to wavelengths of visible light. Such sub-wavelength width and depth dimensions of the pockets may reduce loss of incident light and improve sensitivity of the pixel. Since silicon has a different index of refraction than dielectric material 362, some incident light passing through layer 364 will be reflected at the interfaces between
35 dielectric material 362 and material 364. Light reflected at the silicon-

dielectric interface is redirected to the photodiode of the pixel, as shown diagrammatically with arrows 375 representing light in Fig. 89.

Pixel 370 may be one of numerous identical pixels of a pixel array. Pixel cross-talk between the various pixels of the array may be reduced due to buried dielectric 362 reducing pixel-to-pixel carrier mobility within base 352.

Some embodiments herein include fluorimetry systems and fluorimetry methods. An example embodiment is described with reference to Figs. 90-93.

Referring to Fig. 90, a construction 400 comprises a base 402 having a plurality of projections 404 supported thereover. The projections comprise a material 406 and another material 408. In some embodiments, base 402 may comprise monocrystalline silicon, material 406 may comprise silicon dioxide, and material 408 may comprise monocrystalline silicon. Accordingly, construction 400 may correspond to a patterned SOI structure similar to that of Fig. 61. The material 408 may be referred to as a seed material.

The projections 404 are spaced from one another by gaps 405 that extend to base 402.

Referring to Fig. 91, monocrystalline semiconductor material 410 is grown from seed material 408 to form a cover extending across gaps 405.

Referring to Fig. 92, materials 408 and 410 (Fig. 91) are oxidized to form an oxide material 412. In the shown embodiment, oxide 412 comprises the same material as 406 so that the oxide 412 merges with material 406. Fig. 92 also shows base 402 oxidized to form an oxide 414. The oxide 414 is shown being of the same composition as material 406 so that the oxide 414 and material 406 merge as a single material. In some embodiments, material 406 and oxides 412 and 414 all consist essentially of, or consist of silicon dioxide.

The oxides 406, 412 and 414 surround gaps 405. In some embodiments, the oxides 406, 412 and 414 may be considered windows surrounding conduits corresponding to gaps 405. Such windows are transparent to various wavelengths of electromagnetic radiation, and accordingly the construction 400 of Fig. 92 may be utilized as a sample-retaining structure of a fluorimeter. Fig. 93 shows a perspective view of the

construction of Fig. 92 and shows a fluid sample 420 within one of the conduits corresponding to a gap 405. The view of Fig. 93 also diagrammatically illustrates the conduits beneath material 414 in dashed-line view.

5 Fig. 93 shows an electromagnetic radiation emitting source 422, and an electromagnetic radiation detector 424. The detector and emitter are arranged at right angles relative to one another as is typical of fluorimeters. In operation, radiation 423 is directed toward sample 420 from source 422, causing a component of the sample to fluoresce. The fluorescence 425 is
10 then detected by detector 424.

 Although the emission is shown going through one of the projections and detection shown through the cover 414, in other embodiments the relative locations of the detector and emitter could be reversed. Also, in some embodiments one of the detector and emitter could be positioned
15 beneath base 414.

 Some embodiments herein include nanofluidic channels and methods of forming nanofluidic channels. An example embodiment is described with reference to Figs. 94-98.

 Referring to Figs. 94 and 95, a construction 500 comprises a base
20 502 having a plurality of projections 504 supported thereover. The projections comprise a material 506 and another material 508. In some embodiments, base 502 may comprise monocrystalline silicon, material 506 may comprise silicon dioxide, and material 508 may comprise monocrystalline silicon. Accordingly, construction 500 may correspond to a
25 patterned SOI structure similar to that of Fig. 61. The material 508 may be referred to as a seed material.

 The projections 504 are spaced from one another by gaps (or trenches) 505 that extend to base 502.

 Portions of base 502 are conductively-doped to form conductive
30 regions 510 at the bottoms of gaps 505, while leaving insulative regions 512 adjacent the conductive regions. The top view of Fig. 95 shows that in some embodiments only portions of the base at the bottoms of the gaps 505 are doped to form the regions 510. Accordingly, there are also insulative regions 512 along some portions of the base at the bottoms of the gaps 505.

Referring to Figs. 96 and 97, monocrystalline semiconductor material 514 is grown from seed material 508 to form a cover extending across gaps 505. Such converts the gaps into conduits extending between cover 514 and base 502. Portions of cover 514 are conductively-doped to form conductive regions 520 over gaps 505, while leaving insulative regions 522 adjacent the conductive regions. The top view of Fig. 97 shows that in some embodiments only portions of the cover over the gaps 505 are doped to form the regions 520, so that there are also insulative regions 522 of the cover directly over some portions of the gaps 505. The gaps 505 are diagrammatically illustrated in dashed-line view in Fig. 97 to assist the reader in understanding the location of the gaps relative to the shown conductive and insulative regions of the cover 514.

Fig. 98 shows a perspective view of the construction of Figs. 96 and 97, and shows fluidic samples 530 within the conduits corresponding to gaps 505. The view of Fig. 98 also diagrammatically illustrates the conduits 505 beneath material cover 514 in dashed-line view.

The conductive regions 510 and 520 form paired conductive plates offset from one another by spaces corresponding to conduits 505. The paired conductive plates are electrically connected to monitoring apparatuses 550, 552 and 554. The monitoring apparatuses may monitor electrical properties between the paired plates to detect changes occurring as a sample fluid 530 passes between the plates. Such changes may be catalogued relative to various macromolecules (such as, for example, nucleotides or proteins) so that construction 500 of Fig. 98 may ultimately be utilized for characterization and/or sequencing of macromolecules. Although three separate monitoring apparatuses 550, 552 and 554 are shown, in other embodiments the monitoring apparatuses may be encompassed by a single processor.

The conductive plates may be considered to be a detection system which monitors at least one electrical property of fluid material passing between the plates.

There has been significant research directed toward utilization of nanofluidic channels (in other words, channels having at least some dimensions on the order of nanometers) for sequencing and/or other characterization of macromolecules. It has proven difficult to fabricate

nanofluidic channels using conventional processes. However, some processing as disclosed herein may be utilized to fabricate nanofluidic channels as shown in Figs. 94-98. Further, semiconductor processing may be used to fabricate conductive plates on opposing sides of the channels, and such conductive plates may then be utilized for monitoring materials flowed through the channels. The conductive plates may be conductively-doped regions of semiconductor material (as shown), and/or may comprise patterned metal-containing materials.

Various of the structures described in this disclosure may be incorporated into electronic systems.

Fig. 99 illustrates an embodiment of an electronic system corresponding to a computer system 600. Computer system 600 includes a monitor 601 or other communication output device, a keyboard 602 or other communication input device, and a motherboard 604. Motherboard 604 may carry a microprocessor 606 or other data processing unit, and at least one memory device 608. Memory device 608 may comprise an array of memory cells, and such array may be coupled with addressing circuitry for accessing individual memory cells in the array. Further, the memory cell array may be coupled to a read circuit for reading data from the memory cells. The addressing and read circuitry may be utilized for conveying information between memory device 608 and processor 606. Such is illustrated in the block diagram of the motherboard 604 shown in Fig. 100. In such block diagram, the addressing circuitry is illustrated as 610 and the read circuitry is illustrated as 612.

Processor device 606 may correspond to a processor module, and may comprise various of the structures described in this disclosure.

Memory device 608 may correspond to a memory module, and may comprise various of the structures described in this disclosure.

Fig. 101 illustrates a simplified block diagram of a high-level organization of an electronic system 700. System 700 may correspond to, for example, a computer system, a process control system, or any other system that employs a processor and associated memory. Electronic system 700 has functional elements, including a processor 702, a control unit 704, a memory device unit 706 and an input/output (I/O) device 708 (it is to be understood that the system may have a plurality of processors,

control units, memory device units and/or I/O devices in various embodiments). Generally, electronic system 700 will have a native set of instructions that specify operations to be performed on data by the processor 702 and other interactions between the processor 702, the memory device unit 706 and the I/O device 708. The control unit 704 coordinates all operations of the processor 702, the memory device 706 and the I/O device 708 by continuously cycling through a set of operations that cause instructions to be fetched from the memory device 706 and executed. The memory device 706 may comprise various of the structures described in this disclosure.

Fig. 102 is a simplified block diagram of an electronic system 800. The system 800 includes a memory device 802 that has an array of memory cells 804, address decoder 806, row access circuitry 808, column access circuitry 810, read/write control circuitry 812 for controlling operations, and input/output circuitry 814. The memory device 802 further includes power circuitry 816, and sensors 820, such as current sensors for determining whether a memory cell is in a low-threshold conducting state or in a high-threshold non-conducting state. The illustrated power circuitry 816 includes power supply circuitry 880, circuitry 882 for providing a reference voltage, circuitry 884 for providing a first wordline with pulses, circuitry 886 for providing a second wordline with pulses, and circuitry 888 for providing a bitline with pulses. The system 800 also includes a processor 822, or memory controller for memory accessing.

The memory device 802 receives control signals from the processor 822 over wiring or metallization lines. The memory device 802 is used to store data which is accessed via I/O lines. At least one of the processor 822 or memory device 802 may comprise various of the structures described in this disclosure.

The various electronic systems may be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device(s).

The electronic systems may be used in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules.

The electronic systems may be any of a broad range of systems, such as clocks, televisions, cell phones, personal computers, automobiles, industrial control systems, aircraft, etc..

In compliance with the statute, the subject matter disclosed herein
5 has been described in language more or less specific as to structural and
methodical features. It is to be understood, however, that the claims are not
limited to the specific features shown and described, since the means herein
disclosed comprise example embodiments. The claims are thus to be
afforded full scope as literally worded, and to be appropriately interpreted in
10 accordance with the doctrine of equivalents.

CLAIMS

What is claimed is:

1. A method of forming a covered void in a semiconductor substrate,
5 comprising:

providing exposed different first and second materials on a semiconductor substrate, the second material comprising a pair of projections projecting upwardly relative to the first material and comprising sidewalls;

10 providing an exposed third material atop the second material projections, the third material being different from the second material; and

relative to the second material, selectively growing additional first material from the exposed first material and selectively from the exposed third material effective to bridge across the pair of second material projections to form a covered void between the pair of projections.

15

2. The method of claim 1 comprising providing the third material to be the same as the first material.

3. The method of claim 1 comprising providing the third material to be different from the first material.

20

4. The method of claim 1 comprising providing the first material to comprise monocrystalline elemental-form silicon, and the selectively growing comprises epitaxial silicon-comprising growth from the first material.

5. The method of claim 4 comprising providing the third material to comprise elemental-form silicon.

25

6. The method of claim 5 comprising providing the third material to comprise elemental-form amorphous silicon.

7. The method of claim 5 comprising providing the third material to comprise elemental-form monocrystalline silicon, and wherein the selectively growing comprises monocrystalline epitaxial silicon-comprising growth from the elemental-form monocrystalline silicon.

5 8. The method of claim 7 comprising providing the monocrystalline elemental-form silicon first material to comprise a <100> plane direction, the exposed elemental-form monocrystalline silicon third material comprising a <100> plane direction which is parallel that of the first material.

9. The method of claim 5 wherein the selectively growing
10 comprises polysilicon-comprising growth from the third material.

10. The method of claim 4 comprising providing the third material to comprise any one or more of elemental-form W, elemental-form Ti, or a silicide.

11. The method of claim 1 comprising providing the third material to
15 comprise elemental-form silicon, and the selectively growing comprises growing any one or more of elemental-form W or a silicide.

12. The method of claim 1 comprising providing the third material to comprise elemental-form silicon and elemental-form Ge.

13. The method of claim 1 comprising providing the third material to
20 comprise Ga and As.

14. The method of claim 1 comprising providing the second material to be insulative. 14

15. The method of claim 0 comprising providing the second material to comprise at least one of silicon dioxide or silicon nitride.

16. The method of claim 1 comprising providing the second material
25 to be conductive.

17. The method of claim 1 comprising providing the pair of projections to comprise walls of an opening.

18. The method of claim 17 comprising providing the opening to comprise an elongated trench running generally parallel a mean outermost
5 global surface of the semiconductor substrate.

19. The method of claim 18 comprising filling at least a majority of the covered trench with conductive material and forming an elongated conductive line therefrom.

20. The method of claim 1 comprising providing the pair of
10 projections to comprise spaced free-standing pillars prior to said selectively growing.

21. The method of claim 1 comprising providing the pair of projections to comprise two of a plurality of spaced free-standing pillars prior to said selectively growing, the selectively growing forming the void to be
15 covered by a ceiling supported at least in part by the plurality of pillars received within the void.

22. The method of claim 1 wherein the selectively growing is devoid of growing detectible first material from at least a majority of the second material sidewalls.

20 23. The method of claim 1 wherein the selectively growing comprises growing a semiconductive material, and further comprising providing field effect transistor source/drain regions within the selectively grown semiconductive material.

24. The method of claim 1 wherein the selectively growing
25 comprises growing a semiconductive material, and further comprising providing a field effect transistor channel region within the selectively grown semiconductive material.

25. The method of claim 1 wherein the selectively growing is at a selectivity relative to the second material of at least ten to one.

26. The method of claim 1 wherein the selectively growing is at a selectivity relative to the second material of at least one hundred to one.

5 27. The method of claim 1 wherein the selectively growing of the first material is of least 100 Angstroms and at a selectivity relative to the second material of at least one hundred to one.

28. A method of forming a covered void in a semiconductor substrate, comprising:

10 forming a pair of projections projecting upwardly from a semiconductor substrate, the projections comprising sidewalls;

providing elemental-form silicon atop the pair of projections; and

15 selectively growing relative to at least portions of the projection sidewalls at least one of elemental-form W or a silicide from the elemental-form silicon effective to bridge across the pair of projections to form a covered void between the pair of projections.

29. The method of claim 28 wherein the selectively growing comprises selectively growing elemental-form W.

20 30. The method of claim 28 wherein the selectively growing comprises selectively growing a silicide.

31. The method of claim 28 comprising providing the elemental-form silicon to comprise amorphous silicon.

32. The method of claim 28 comprising providing the elemental-form silicon to comprise monocrystalline silicon.

33. A method of forming a covered void in a semiconductor substrate, comprising:

forming a pair of projections projecting upwardly from a semiconductor substrate, the projections comprising sidewalls;

5 providing elemental-form silicon atop the pair of projections; and

selectively growing relative to at least portions of the projection sidewalls a polysilicon-comprising material from the elemental-form silicon effective to bridge across the pair of projections to form a covered void between the pair of projections.

10 34. The method of claim 33 wherein providing the elemental-form silicon comprises depositing amorphous silicon, and annealing the amorphous silicon to be polycrystalline; and wherein the selectively growing occurs from the polycrystalline silicon.

15 35. The method of claim 33 comprising oxidizing the selectively grown polysilicon-comprising material to form a silicon dioxide-comprising bridge atop the covered void.

36. The method of claim 35 wherein the oxidizing oxidizes all the selectively grown polysilicon-comprising material to form silicon dioxide-comprising material.

20 37. A method of forming a plurality of covered voids in a semiconductor substrate, comprising:

depositing insulative material over an elemental-form silicon-containing material;

depositing amorphous silicon over the insulative material;

25 etching a plurality of openings through the amorphous silicon and the insulative material to the elemental-form silicon-containing material; and

selectively growing relative to the insulative material an elemental-form silicon-comprising material from the elemental-form silicon-containing material and from the amorphous silicon effective to bridge across the plurality of openings to cover the plurality of openings.

30

38. The method of claim 37 wherein the etching forms the plurality of openings to comprise elongated trenches running generally parallel a mean outermost global surface of the semiconductor substrate.

39. The method of claim 37 wherein the etching forms the plurality
5 of openings to comprise elongated trenches running generally parallel a mean outermost global surface of the semiconductor substrate;

providing individual of the covered elongated trenches to have at least one open end; and

depositing conductive material to within the covered elongated
10 trenches from the at least one open end effective to form conductive lines within the trenches.

40. The method of claim 37 wherein depositing the insulative material comprises depositing silicon dioxide-comprising material.

41. The method of claim 37 wherein depositing the insulative
15 material comprises depositing silicon nitride-comprising material.

42. The method of claim 37 wherein the etching forms the plurality of openings to comprise elongated trenches running generally parallel a mean outermost global surface of the semiconductor substrate;

providing individual of the covered elongated trenches to have at least
20 one open end;

forming a gate dielectric within the covered elongated trenches; and
depositing conductive material to within the covered elongated
trenches over the gate dielectric from the at least one open end effective to
form conductive gate lines within the trenches.

25 43. The method of claim 37 wherein the selectively growing is at a selectivity relative to the insulative material of at least ten to one.

44. The method of claim 36 wherein the selectively growing is at a selectivity relative to the insulative material of at least one hundred to one.

45. The method of forming a plurality of covered voids in a semiconductor substrate, comprising:

depositing insulative material over a first elemental-form silicon-containing material;

5 forming a second elemental-form silicon-containing material over the insulative material;

etching a plurality of openings through the second elemental-form silicon-containing material and the insulative material to the first elemental-form silicon-containing material;

10 epitaxially growing a first elemental-form silicon-comprising material from the first elemental-form silicon-containing material; and

selectively growing relative to the insulative material a second elemental-form silicon-comprising material from the second elemental-form silicon-containing material effective to bridge across the plurality of
15 openings to cover the plurality of openings.

46. The method of claim 45 wherein the forming of the second elemental-form silicon-containing material comprises depositing amorphous silicon.

47. The method of claim 46 comprising annealing the amorphous
20 silicon to be polycrystalline, and wherein the selectively growing forms the second elemental-form silicon-containing material to be polycrystalline.

48. The method of claim 45 wherein the forming of the second elemental-form silicon-containing material comprises forming monocrystalline silicon.

25 49. The method of claim 48 wherein the selectively growing comprises epitaxially growing the second elemental-form silicon-comprising material.

50. The method of claim 45 wherein the etching forms the plurality of openings to comprise elongated trenches running generally parallel a
30 mean outermost global surface of the semiconductor substrate.

51. The method of claim 45 wherein the etching forms the plurality of openings to comprise elongated trenches running generally parallel a mean outermost global surface of the semiconductor substrate;

providing individual of the covered elongated trenches to have at least
5 one open end; and

depositing conductive material to within the covered elongated trenches from the at least one open end effective to form conductive lines within the trenches.

52. The method of claim 45 wherein the etching forms the plurality
10 of openings to comprise elongated trenches running generally parallel a mean outermost global surface of the semiconductor substrate;

providing individual of the covered elongated trenches to have at least one open end;

forming a gate dielectric within the covered elongated trenches; and
15 depositing conductive material to within the covered elongated trenches over the gate dielectric from the at least one open end effective to form conductive gate lines within the trenches.

53. The method of forming a plurality of covered voids in a semiconductor substrate, comprising:

20 depositing insulative material over an elemental-form silicon-containing material;

forming an amorphous elemental-form silicon-containing material over the insulative material;

etching a plurality of openings through the amorphous elemental-form
25 silicon-containing material and the insulative material to the elemental-form silicon-containing material;

annealing the amorphous elemental-form silicon-containing material effective to form a polycrystalline silicon-containing material; and

epitaxially growing a first elemental-form silicon-comprising material
30 from the elemental-form silicon-containing material while selectively growing relative to the insulative material a polysilicon-comprising material from the polycrystalline silicon-containing material effective to bridge across the plurality of openings to cover the plurality of openings.

54. A method of forming a plurality of covered voids in a semiconductor substrate, comprising:

depositing conductive material over an elemental-form silicon-containing material;

5 etching a plurality of openings through the conductive material to the elemental-form silicon-containing material;

after etching the openings, lining at least sidewalls of the plurality of openings with an insulative material; and

10 selectively growing relative to the insulative material an elemental-form silicon-comprising material over the plurality of openings effective to bridge across the plurality of openings to cover the plurality of openings.

55. The method of claim 54 comprising epitaxially growing elemental-form silicon-comprising material from bases of the plurality of openings while said selectively growing elemental-form silicon-comprising material over the plurality of openings effective to bridge across the plurality of openings to cover the plurality of openings.

56. The method of claim 54 comprising lining bases of the plurality of openings with the insulative material while said lining the sidewalls.

20 57. The method of claim 56 comprising etching the lined bases prior to said selectively growing, and epitaxially growing elemental-form silicon-comprising material from the bases while said selectively growing elemental-form silicon-comprising material over the plurality of openings effective to bridge across the plurality of openings to cover the plurality of openings.

25 58. The method of claim 54 being devoid of growing elemental-form silicon-comprising material from bases of the plurality of openings during said selectively growing elemental-form silicon-comprising material over the plurality of openings.

59. The method of claim 54 comprising providing an exposed epitaxial seed material proximate tops of the plurality of openings over the conductive material prior to the selectively growing, the selectively growing comprising epitaxial growth from the epitaxial seed material.

5 60. The method of claim 59 comprising providing exposed portions of the exposed epitaxial seed material to comprise portions of sidewalls of the plurality of openings and from which the elemental-form silicon-comprising material is grown during said epitaxial growth.

10 61. The method of claim 60 comprising providing an elevationally outermost surface of the epitaxial seed material to be covered during said epitaxial growth.

15 62. The method of claim 59 comprising providing exposed portions of the exposed epitaxial seed material to comprise an elevationally outermost surface of the epitaxial seed material, the selectively growing comprising epitaxial growth from the epitaxial seed material.

63. The method of claim 54 comprising etching the plurality of openings to comprise elongated trenches running generally parallel a mean outermost global surface of the semiconductor substrate.

64. A method of forming field effect transistors, comprising:
providing a monocrystalline silicon-containing substrate comprising a
<100> plane direction;

5 depositing insulative material over the monocrystalline silicon-
containing substrate;

etching a plurality of trenches through the insulative material to
silicon-containing material of the substrate parallel the <100> plane direction
and providing monocrystalline silicon-containing material bases of the
trenches which run parallel the <100> plane direction;

10 epitaxially growing an elemental-form silicon-comprising material from
the monocrystalline silicon-containing material of the trench bases and over
the insulative material effective to bridge across the trenches with
elemental-form silicon-comprising material and form covered trench voids
within the trenches; and

15 forming at least one of field effect transistor channel regions or field
effect transistor source/drain regions within the elemental-form silicon-
comprising material bridging across the trenches.

65. The method of claim 64 wherein the forming comprises forming
field effect transistor channel regions within the elemental-form silicon-
20 comprising material bridging across the trenches.

66. The method of claim 64 wherein the forming comprises forming
field effect transistor source/drain regions within the elemental-form silicon-
comprising material bridging across the trenches.

67. The method of claim 64 wherein the forming comprises forming
25 both field effect transistor channel regions and field effect transistor
source/drain regions within the elemental-form silicon-comprising material
bridging across the trenches.

68. The method of claim 64 comprising forming field effect
transistor gates within the trench voids.

69. The method of claim 68 comprising:

oxidizing an underside of the elemental-form silicon-comprising material bridging across the trenches to at least partially form a gate dielectric on said underside within the covered trench voids; and

5 after the oxidizing, depositing conductive material within the covered trench voids to form field effect transistor gates within the covered trench voids.

70. The method of claim 64 comprising wet etching the monocrystalline silicon-containing material bases prior to the epitaxially
10 growing.

71. A method of forming a semiconductor-on-insulator substrate, comprising:

providing a semiconductor-on-insulator substrate comprising a bulk monocrystalline silicon-containing substrate, an insulator layer received over
15 the bulk monocrystalline silicon-containing substrate; and a silicon-containing semiconductor layer received over the insulator layer;

etching a plurality of openings through the semiconductor layer;

epitaxially growing an elemental-form silicon-comprising material over the silicon-containing semiconductor layer received over the insulator layer
20 effective to bridge across the openings with elemental-form silicon-comprising material and form covered voids within the openings; and

forming at least one of field effect transistor channel regions or field effect transistor source/drain regions within the elemental-form silicon-comprising material bridging across the openings.

25 72. The method of claim 71 wherein the epitaxially growing is from exposed portions of the silicon-containing semiconductor layer.

73. The method of claim 71 further comprising providing an exposed epitaxial seed material over the silicon-containing semiconductor layer prior to the epitaxially growing and from which the elemental-form
30 silicon-comprising material is grown during said epitaxially growing.

74. A method of forming a semiconductor-on-insulator substrate, comprising:

providing a semiconductor-on-insulator substrate comprising a bulk monocrystalline silicon-containing substrate, an insulator layer received over the bulk monocrystalline silicon-containing substrate, and a silicon-containing semiconductor layer received over the insulator layer;

etching a plurality of openings through the semiconductor layer and the insulator layer to bulk monocrystalline silicon-containing material of the bulk monocrystalline silicon-containing substrate, the openings comprising monocrystalline silicon-containing bases;

epitaxially growing an elemental-form silicon-comprising material from the monocrystalline silicon-containing bases within the openings and over the silicon-containing semiconductor layer received over the insulator layer effective to bridge across the openings with elemental-form silicon-comprising material and form covered voids within the openings; and

forming at least one of field effect transistor channel regions or field effect transistor source/drain regions within the elemental-form silicon-comprising material bridging across the openings.

75. The method of claim 74 comprising etching the plurality of openings to comprise elongated trenches running generally parallel a mean outermost global surface of the semiconductor-on-insulator substrate.

76. The method of claim 74 wherein the forming comprises forming field effect transistor channel regions within the elemental-form silicon-comprising material bridging across the openings.

77. The method of claim 74 wherein the forming comprises forming field effect transistor source/drain regions within the elemental-form silicon-comprising material bridging across the openings.

78. The method of claim 74 wherein the forming comprises forming both field effect transistor channel regions and field effect transistor source/drain regions within the elemental-form silicon-comprising material bridging across the openings.

79. The method of claim 74 comprising forming field effect transistor gates within the covered voids.

80. The method of claim 74 wherein the epitaxially growing is from exposed portions of the silicon-containing semiconductor layer.

5 81. The method of claim 74 further comprising providing an exposed epitaxial seed material over the silicon-containing semiconductor layer prior to the epitaxially growing and from which the elemental-form silicon-comprising material is grown during said epitaxially growing.

10 82. The method of claim 74 comprising providing the monocrystalline silicon-containing substrate to comprise a <100> plane direction, the etching forming sides of the openings to run parallel said <100> plane direction.

15 83. Integrated circuitry comprising:
a semiconductor-on-insulator substrate having a mean outermost global surface; the substrate comprising monocrystalline silicon-containing material, an insulator received over the monocrystalline silicon-containing material, and an elemental-form silicon-comprising material received over the insulator;
20 a plurality of elongated cooling conduits running generally parallel the mean outermost global surface within the insulator; and
cooling fluid received within the cooling conduits.

84. The integrated circuitry of claim 83 wherein the cooling fluid is flowing within the cooling conduits.

25 85. The integrated circuitry of claim 83 comprising field effect transistor channel regions received within the elemental-form silicon-comprising material that is over the cooling conduits.

86. The integrated circuitry of claim 83 comprising field effect transistor source/drain regions received within the elemental-form silicon-comprising material that is over the cooling conduits.

87. The integrated circuitry of claim 83 comprising field effect transistor channel regions and field effect transistor source/drain regions received within the elemental-form silicon-comprising material that is over the cooling conduits.

5 88. A method of forming a semiconductor-on-insulator substrate, comprising:

providing a base region of a base substrate, a silicon-containing semiconductor region over the base region, and an insulative layer over the silicon-containing semiconductor region;

10 etching cooling trenches into the insulative layer to the silicon-containing semiconductor region;

selectively growing relative to the insulative layer a bridging material over the insulative layer effective to bridge across the cooling trenches with bridging material and form covered elongated cooling trenches;

15 providing a release region intermediate the silicon-containing semiconductor region and the base region of the base substrate;

at an interface of the release region and the silicon-containing semiconductor region, separating a) the base region and release region from b) the silicon-containing semiconductor region, the insulative layer
20 with the elongated covered cooling trenches, and the bridging material;

forming at least one of field effect transistor channel regions or field effect transistor source/drain regions within the silicon-containing semiconductor region; and

providing cooling fluid within the covered elongated cooling trenches.

25 89. The method of claim 88 comprising forming the release region before the etching.

90. The method of claim 89 wherein the forming the release region comprises implanting hydrogen into the base substrate.

91. The method of claim 89 wherein the forming the release region
30 comprises implanting oxygen into the base substrate.

92. The method of claim 89 wherein the forming the release region comprises depositing an insulator layer over the base region, and prior to providing the silicon-containing semiconductor region.

93. The method of claim 88 comprising forming the release region
5 after the etching.

94. The method of claim 93 wherein the forming the release region comprises implanting hydrogen into the base substrate.

95. The method of claim 93 wherein the forming the release region comprises implanting oxygen into the base substrate.

10 96. The method of claim 88 forming an insulator layer on an outer surface of the bridging material bridging across the cooling trenches.

97. The method of claim 96 comprising bonding the insulator layer to a carrier substrate after said separating.

15 98. The method of claim 88 comprising epitaxially growing an elemental-form silicon-comprising material from bases of the cooling trenches while selectively growing the bridging material over the insulator layer effective to bridge across the cooling trenches.

99. The method of claim 88 wherein the selectively growing comprises growing elemental-form silicon-comprising material.

20 100. The method of claim 99 wherein the selectively growing forms the bridging material to comprise polysilicon.

101. The method of claim 99 further comprising oxidizing the silicon-comprising material to form the bridging material to comprise silicon dioxide.

102. The method of claim 88 comprising providing an exposed epitaxial seed material proximate tops of the cooling trenches over the insulative material prior to the selectively growing, the selectively growing comprising epitaxial growing an elemental-form silicon-comprising material
5 to bridge across the cooling trenches.

103. The method of claim 102 comprising providing the exposed epitaxial seed material to comprise elemental-form silicon.

104. The method of claim 103 comprising providing the exposed epitaxial seed material to comprise elemental-form monocrystalline silicon.

10 105. The method of claim 102 comprising providing the exposed epitaxial seed material to comprise any one or more of elemental-form W or a silicide.

106. A method of forming a semiconductor-on-insulator substrate, comprising:

providing a base region of a base substrate, a silicon-containing semiconductor region over the base region, and an insulative layer over the silicon-containing semiconductor region;

etching trenches into the insulative layer to the silicon-containing semiconductor region;

selectively growing relative to the insulative layer a bridging material over the insulative layer effective to bridge across the trenches with bridging material and form covered elongated trenches;

providing a release region intermediate the silicon-containing semiconductor region and the base region of the base substrate;

at an interface of the release region and the silicon-containing semiconductor region, separating a) the base region and release region from b) the silicon-containing semiconductor region, the insulative layer with the elongated covered trenches, and the bridging material;

forming first field effect transistor gates within the covered trench voids; and

forming second field effect transistor gates opposite the first field effect transistor gates over the silicon-containing semiconductor region, and forming field effect transistor channel regions within material of the silicon-containing semiconductor region received between the first and second field effect transistor gates.

107. The method of claim 106 comprising forming field effect transistor source/drain regions within the silicon-containing semiconductor region.

108. The method of claim 106 forming an insulator layer on an outer surface of the bridging material bridging across the trenches.

109. The method of claim 108 comprising bonding the insulator layer to a carrier substrate after said separating.

110. The method of claim 106 comprising epitaxially growing an elemental-form silicon-comprising material from bases of the trenches while selectively growing the bridging material over the insulator layer effective to bridge across the trenches.

5 111. The method of claim 106 wherein the selectively growing comprises growing elemental-form silicon-comprising material.

112. The method of claim 111 wherein the selectively growing forms the bridging material to comprise polysilicon.

10 113. The method of claim 112 further comprising oxidizing the silicon-comprising material to form the bridging material to comprise silicon dioxide.

15 114. The method of claim 106 comprising providing an exposed epitaxial seed material proximate tops of the trenches over the insulative material prior to the selectively growing, the selectively growing comprising epitaxial growing an elemental-form silicon-comprising material to bridge across the trenches.

115. The method of claim 114 comprising providing the exposed epitaxial seed material to comprise elemental-form silicon.

20 116. The method of claim 115 comprising providing the exposed epitaxial seed material to comprise elemental-form monocrystalline silicon.

117. The method of claim 114 comprising providing the exposed epitaxial seed material to comprise any one or more of elemental-form W or a silicide.

25 118. The method of claim 106 comprising forming the release region before the etching.

119. The method of claim 118 wherein the forming the release region comprises implanting hydrogen into the base substrate.

120. The method of claim 118 wherein the forming the release region comprises implanting oxygen into the base substrate.

121. The method of claim 118 wherein the forming the release region comprises depositing an insulator layer over the base region, and prior to
5 providing the silicon-containing semiconductor region.

122. The method of claim 106 comprising forming the release region after the etching.

123. The method of claim 122 wherein the forming the release region comprises implanting hydrogen into the base substrate.

10 124. The method of claim 122 wherein the forming the release region comprises implanting oxygen into the base substrate.

125. A method of forming a covered void within a semiconductor substrate, comprising:

15 providing a pair of upwardly projecting sidewalls relative to a semiconductor substrate; the sidewalls having a space therebetween and comprising opposing first, second, and third materials; the second material being received intermediate the first and third materials and being different from the first and third materials; and

20 growing a fourth material from the opposing second material of the sidewalls selectively relative to the first material and the third material effective to form a bridge of fourth material across the space to form a covered void between the sidewalls.

126. The method of claim 125 comprising providing the first material to be different from the third material.

25 127. The method of claim 125 comprising providing the first material to be the same as the third material.

128. The method of claim 125 comprising providing the second material to be the same as the fourth material.

129. The method of claim 125 comprising providing the first material to be thicker than the third material.

130. The method of claim 125 comprising providing the first material to be thinner than the third material.

5 131. The method of claim 125 comprising providing the third material to be thicker than the second material.

132. The method of claim 125 comprising providing the second material and third material to be about the same thickness.

10 133. The method of claim 125 wherein the selectively growing comprises epitaxially growing the fourth material to comprise a silicon-comprising material.

134. The method of claim 125 comprising providing the second material to be different from the fourth material.

15 135. The method of claim 134 wherein the selectively growing comprises epitaxially growing the fourth material to comprise a silicon-comprising material.

136. The method of claim 134 comprising providing the second material to comprise elemental-form silicon.

20 137. The method of claim 136 comprising providing the fourth material to comprise any one or more of elemental-form W or a silicide.

138. The method of claim 134 comprising providing the second material to comprise any one or more of elemental-form W, elemental-form Ti, or a silicide.

25 139. The method of claim 138 comprising providing the fourth material to comprise elemental-form silicon.

140. The method of claim 125 wherein the selectively growing grows the fourth material to extend over an elevationally outermost surface of the third material.

141. The method of claim 125 wherein the selectively growing does
5 not grow the fourth material to extend over an elevationally outermost surface of the third material.

142. The method of claim 125 comprising after the selectively growing, polishing the substrate inwardly to at least the third material to leave fourth material bridging over the covered void.

10 143. The method of claim 142 comprising after the selectively growing, polishing the substrate inwardly to at least the second material to leave fourth material bridging over the covered void.

144. The method of claim 143, comprising after the selectively growing, polishing the substrate inwardly to the first material to leave fourth
15 material bridging over the covered void.

145. A method of forming a covered void within a semiconductor substrate, comprising:

providing a bulk monocrystalline silicon-containing substrate;

5 depositing a first insulative material over the bulk monocrystalline silicon-containing substrate;

depositing an elemental-form silicon-containing material over the first insulative material;

depositing a second insulative material over the elemental-form silicon-containing material;

10 etching a plurality of trenches through the second insulative material, the elemental-form silicon-containing material, and the first insulative material to bulk silicon-containing material of the substrate; and

relative to the first and second insulative materials, selectively growing a silicon-comprising material from the elemental-form silicon-containing material and from the bulk silicon-containing material of the
15 substrate within the trenches effective to bridge across the trenches with elemental-form silicon-comprising material to form covered trench voids within the trenches.

146. The method of claim 145 comprising providing the first
20 insulative material to be the same as the second insulative material.

147. The method of claim 145 comprising providing the first insulative material to be different from the second insulative material.

148. The method of claim 147 comprising providing the first insulative material to comprise silicon dioxide and the second insulative
25 material to comprise silicon nitride.

149. The method of claim 145 comprising providing the elemental-form silicon-containing material deposited over the first insulative material to comprise amorphous silicon.

150. The method of claim 145 comprising providing the elemental-form silicon-containing material deposited over the first insulative material to comprise polycrystalline silicon.

151. The method of claim 150 providing the elemental-form silicon-containing material deposited over the first insulative material to initially
5 comprise amorphous silicon which is subsequently converted to polycrystalline silicon.

152. The method of claim 145 further comprising forming at least one of field effect transistor channel regions or field effect transistor
10 source/drain regions within the elemental-form silicon-comprising material bridging across the trenches.

153. A method of forming a span comprising silicon dioxide, comprising:

forming an opening comprising sidewalls within a semiconductor
15 substrate;

relative to at least some portion of the sidewalls, selectively growing an elemental-form silicon-containing material to bridge across the opening to form a covered cavity within the opening; and

oxidizing all of the selectively grown elemental-form silicon-containing
20 material which covers the opening to form a silicon dioxide-comprising bridge across the opening over the cavity.

154. The method of claim 153 comprising epitaxially growing an elemental-form silicon-comprising material from a base of the opening while selectively growing the elemental-form silicon-containing material to bridge
25 across the opening.

155. The method of claim 153 wherein the selectively growing comprises epitaxially growing material which consists essentially of elemental-form monocrystalline silicon.

156. The method of claim 153 wherein the selectively growing comprises growing said elemental-form silicon-containing material from elemental-form silicon containing material.

157. The method of claim 156 comprising providing the elemental-
5 form silicon-containing material from which the selectively growing occurs at uppermost opposing edges of the opening.

158. The method of claim 156 comprising providing the elemental-
form silicon-containing material from which the selectively growing occurs
spaced from uppermost opposing edges of the opening, with material other
10 than elemental-form silicon-containing material covering the elemental-form
silicon-containing material from which the selectively growing occurs.

159. The method of claim 153 wherein the selectively growing comprises growing said elemental-form silicon-containing material from at least one of elemental-form W or a silicide.

15 160. The method of claim 159 comprising providing the at least one of elemental-form W or a silicide from which the selectively growing occurs at uppermost opposing edges of the opening.

161. The method of claim 159 comprising providing the at least one of elemental-form W or a silicide from which the selectively growing occurs
20 spaced from uppermost opposing edges of the opening, with material other than said at least one of elemental-form W and a silicide covering the at least one of elemental-form W and a silicide from which the selectively growing occurs.

162. The method of claim 159 wherein the at least one comprises
25 elemental-form W.

163. The method of claim 159 wherein the at least one comprises a silicide

164. The method of claim 153 comprising providing the opening to comprise an elongated trench running generally parallel a mean outermost global surface of the semiconductor substrate.

165. The method of claim 164 comprising filling at least a majority of
5 the trench with conductive material and forming an elongated conductive line therefrom.

166. A method of forming a span comprising silicon dioxide, comprising:

forming an opening comprising sidewalls within a semiconductor
10 substrate;

relative to at least some portion of the sidewalls, selectively growing an elemental-form silicon-containing material to bridge across the opening to form a covered cavity within the opening; and

oxidizing at least an outermost upper half of the selectively grown
15 elemental-form silicon-containing material across the opening to form a silicon dioxide-comprising bridge across the opening over the cavity.

167. The method of claim 166 wherein the oxidizing comprises oxidizing less than all of the selectively grown elemental-form silicon-containing material.

20 168. The method of claim 166 wherein the oxidizing comprises oxidizing only about half of the selectively grown elemental-form silicon-containing material.

169. The method of claim 166 wherein the oxidizing comprises oxidizing more than half of the selectively grown elemental-form silicon-
25 containing material.

170. The method of claim 166 comprising epitaxially growing an elemental-form silicon-comprising material from a base of the opening while selectively growing the elemental-form silicon-containing material to bridge across the opening.

171. The method of claim 166 wherein the selectively growing comprises growing said elemental-form silicon-containing material from elemental-form silicon containing material.

172. The method of claim 166 wherein the selectively growing
5 comprises growing said elemental-form silicon-containing material from at least one of elemental-form W or a silicide.

173. The method of claim 166 comprising providing the opening to comprise an elongated trench running generally parallel a mean outermost global surface of the semiconductor substrate.

10 174. The method of claim 173 comprising filling at least a majority of the trench with conductive material and forming an elongated conductive line therefrom.

175. A method of cooling semiconductor devices, comprising:
etching trenches into an insulative material;
15 selectively growing an elemental-form silicon-containing material across the trenches to convert the trenches to elongated covered conduits;
forming at least one integrated circuit device which is received at least partially within the elemental-form silicon-containing material received across at least one of the elongated covered conduits; and
20 providing coolant within the conduits.

176. The method of claim 175 wherein etching the trenches comprises:

depositing insulative material over an elemental-form silicon-containing material;
25 etching a plurality of trenches into the insulative material; and
providing an exposed seed material different from the insulative material over the insulative material prior to the selectively growing and from which the elemental-form silicon-comprising material received across the trenches is grown during said selectively growing.

177. The method of claim 176 comprising providing the exposed seed material to comprise at least one of amorphous silicon or monocrystalline silicon.

178. The method of claim 176 comprising providing the exposed
5 seed material to comprise any one or more of elemental-form W, elemental-form Ti, or a silicide.

179. The method of claim 176 comprising providing the exposed seed material over the insulative material prior to the etching, the etching the plurality of trenches occurring first through the seed material and then
10 through the insulative material.

180. The method of claim 176 comprising providing the exposed seed material over the insulative material after the etching.

181. The method of claim 175 wherein providing coolant comprises flowing coolant through the conduits.

15 182. The method of claim 175 comprising providing the trenches to have exposed trench bases comprising the elemental-form silicon-containing material over which the insulative material is deposited, and epitaxially growing an elemental-form silicon-containing material from said trench bases during said selectively growing an elemental-form silicon-containing
20 material across the trenches to convert the trenches to elongated covered conduits.

183. The method of claim 175 wherein etching the trenches comprises:

providing a semiconductor-on-insulator substrate comprising a bulk monocrystalline silicon-containing substrate, the insulative material received
5 over the bulk monocrystalline silicon-containing substrate, and a silicon-containing semiconductor layer received over the insulator layer;

etching a plurality of trenches through the silicon-containing semiconductor layer and into the insulative material; and

wherein the selectively growing occurs from the silicon-containing
10 semiconductor layer.

184. The method of claim 183 wherein the etching is conducted through the insulative layer to bulk monocrystalline silicon-containing material of the substrate, and epitaxially growing an elemental-form silicon-containing material from said bulk monocrystalline silicon-containing
15 material of the substrate within the trenches during said selectively growing an elemental-form silicon-containing material across the trenches to convert the trenches to elongated covered conduits.

185. The method of claim 175 wherein the selectively growing comprises epitaxially growing the second elemental-form silicon-comprising
20 material.

186. A method of forming a covered void in a semiconductor substrate, comprising:

forming a pair of first material projections projecting upwardly from a semiconductor substrate, the projections comprising sidewalls;

5 providing an exposed second material over the first material, the second material being different from the first material;

selectively growing relative to the first material of the projections a third material from the second material elevationally inward along the projection sidewalls and effective to bridge across the pair of projections with the third material to form a covered void between the pair of
10 projections; and

after the selectively growing, removing the third material inwardly at least to the second material and effective to leave a bridge across the pair of projections over the covered void.

15 187. The method of claim 186 comprising providing the third material to be the same as the second material.

188. The method of claim 186 comprising providing the third material to be different from the second material.

20 189. The method of claim 186 comprising providing the third material to comprise elemental-form silicon, and the selectively growing comprises epitaxial silicon-comprising growth.

190. The method of claim 189 comprising providing the second material to comprise elemental-form silicon.

25 191. The method of claim 189 comprising providing the second material to comprise any one or more of elemental-form W, elemental-form Ti, or a silicide.

30 192. The method of claim 186 comprising providing the second material to comprise elemental-form silicon, and the selectively growing comprises growing any one or more of elemental-form W, elemental-form Ti, or a silicide.

193. The method of claim 186 comprising providing the first material to be insulative.

194. The method of claim 186 comprising providing exposed portions of the exposed second material to comprise an elevationally outermost surface of the second material and from which the third material is selectively grown.

195. The method of claim 186 comprising providing exposed portions of the exposed second material to comprise sidewalls of second material and from which the third material is selectively grown.

196. The method of claim 195 comprising providing an elevationally outermost surface of the second material to be covered during said selectively growing.

197. The method of claim 186 wherein the removing comprises etching.

198. The method of claim 186 wherein the removing comprises mechanical polishing.

199. The method of claim 186 wherein the removing comprises chemical mechanical polishing.

200. The method of claim 186 wherein the removing of the third material is inward to the first material.

201. The method of claim 186 comprising providing the covered void to comprise an elongated trench running generally parallel a mean outermost global surface of the semiconductor substrate.

202. The method of claim 201 comprising filling at least a majority of the trench with conductive material and forming an elongated conductive line therefrom.

203. The method of claim 186 comprising providing the pair of projections to comprise spaced free-standing pillars prior to said selectively growing.

204. The method of claim 186 comprising providing the pair of
5 projections to comprise two of a plurality of spaced free-standing pillars prior to said selectively growing, the selectively growing forming the void to be covered by a ceiling supported at least in part by the plurality of pillars received within the void.

205. A method of forming an electromagnetic radiation emitter and
10 conduit, comprising:

forming a pair of projections over an electromagnetic radiation generating base material;

forming seed material associated with upper regions of the projections; and growing covering material from the seed material to bridge
15 across the pair of projections and form a conduit contained between the base, cover and projections.

206. The method of claim 205 wherein the forming the seed material comprises depositing seed material over the projections.

207. The method of claim 205 wherein the forming the projections
20 comprises patterning the projections from a first material.

208. The method of claim 207 wherein the first material is an electrically insulative material.

209. The method of claim 205 wherein the forming the projections comprises patterning the projections from a first material; and
25 wherein the forming the seed material comprises depositing seed material over the first material and patterning the seed material during the patterning of the first material.

210. The method of claim 209 wherein the first material is an electrically insulative material.

211. The method of claim 205 wherein the electromagnetic radiation generating base material comprises a III/IV material or a II/VI material.

212. The method of claim 205 wherein the projections have interior sidewalls along a gap between the projections, and further comprising lining
5 the interior sidewalls with metal-containing material prior to growing the covering material.

213. A method of forming an imager system, comprising:
forming a first material over a semiconductor material base;
etching a plurality of openings through the first material to the base;
10 providing seed regions along upper surfaces of the first material;
growing monocrystalline semiconductor material from the seed regions and over the openings; and
forming a pixel array supported by the monocrystalline semiconductor material.

15 214. The method of claim 213 wherein the first material is electrically conductive.

215. The method of claim 214 wherein the first material comprises metal.

20 216. The method of claim 213 wherein the first material is electrically conductive, and wherein the providing the seed regions along the upper surfaces comprises utilizing the upper surfaces of the first material as the seed regions.

25 217. The method of claim 213 wherein the providing the seed regions along the upper surfaces comprises depositing seed material over the upper surfaces.

218. The method of claim 213 wherein the providing the seed regions along the upper surfaces comprises depositing silicon-containing seed material over the upper surfaces.

219. The method of claim 213 further comprising at least partially filling the openings with dielectric material.

220. The method of claim 219 wherein the openings are at least partially filled with the dielectric material prior to the growth of the
5 monocrystalline semiconductor material.

221. The method of claim 219 wherein the dielectric material consists of silicon dioxide.

222. A method of forming an electromagnetic radiation conduit, comprising:

10 providing exposed first and second materials on a semiconductor substrate, the second material comprising a pair of projections projecting upwardly relative to the first material and comprising sidewalls; the second material being compositionally different from the first material;

15 providing an exposed third material atop the second material projections, the third material being compositionally different from the second material;

growing additional first material from the exposed third material to form a bridge across the pair of second material projections; a conduit being created over the first material, between the pair of projections and under the
20 bridge; and

at least partially filling the conduit with fourth material having different light refracting properties than one or more of the first, second and third materials.

223. The method of claim 222 wherein the fourth material comprises
25 a metal.

224. The method of claim 222 comprising providing the third material to be compositionally the same as the first material.

225. The method of claim 224 comprising providing the first material to comprise elemental-form silicon, and wherein the growing the additional
30 first material comprises epitaxial growth.

226. The method of claim 222 comprising providing the third material to be compositionally different from the first material.

227. The method of claim 225 comprising providing the third material to comprise elemental-form silicon.

5 228. The method of claim 227 comprising providing the third material to comprise elemental-form amorphous silicon.

229. The method of claim 225 comprising providing the third material to comprise one or more of elemental-form W, elemental-form Ti, or a silicide.

10 230. A fluorimetry method, comprising:
providing a semiconductor construction comprising a silicon-containing substrate supporting a sample-retaining conduit, the conduit being comprised by a pair of silicon dioxide-containing projections extending upwardly from the substrate and a silicon dioxide-containing cover extending
15 across the projections; the silicon dioxide-containing projections and cover together forming a window partially surrounding the sample-retaining conduit;
providing a sample within the conduit;
passing first electromagnetic radiation through the window to
20 stimulate fluorometric emission of second electromagnetic radiation from the sample; and
detecting the emitted second electromagnetic radiation with a detector exterior of the sample-retaining conduit.

231. The method of claim 230 wherein the substrate comprises
25 monocrystalline silicon.

232. The method of claim 230 wherein the substrate comprises silicon dioxide.

233. The method of claim 230 wherein the substrate consists of silicon dioxide.

234. The method of claim 230 wherein the providing the semiconductor construction comprises:

providing a monocrystalline silicon base;

5 forming the pair of silicon dioxide-containing projections extending upwardly from the base, the projections being spaced from one another by a gap;

forming a seed layer atop the silicon dioxide-containing projections;

epitaxially growing silicon-containing material from the seed material to bridge across the gap; and

10 oxidizing the epitaxially-grown silicon-containing material to form the silicon dioxide-containing cover.

235. The method of claim 234 wherein the projections consist of silicon dioxide, and wherein the cover consists of silicon dioxide.

15 236. The method of claim 234 further comprising oxidizing the monocrystalline silicon base.

237. The method of claim 230 wherein one of the stimulation and detection utilizes electromagnetic radiation passing through one of the projections and does not utilize radiation passing through the cover; and wherein the other of the stimulation and detection utilizes radiation passing
20 through the cover and does not utilized radiation passing through either of the projections.

238. A method of forming a nanofluidic channel, comprising:

providing a semiconductor material base;

25 forming a pair of projections extending upwardly from the base; the projections and base together forming a trench;

forming a seed material at an upper portion of the projections; and

growing a cover from the seed material and across the trench to convert the trench into a nanofluidic channel.

239. The method of claim 238 further comprising:
forming a first conductive region along a bottom of the trench prior to forming the cover;

forming the cover to comprise a second conductive region offset from
5 the first conductive region by an intervening space; and
electrically coupling the first and second conductive regions to a detection system configured to monitor at least one electrical interaction between the first and second conductive regions.

240. The method of claim 239 wherein:
10 the cover comprises monocrystalline silicon;
the forming the first conductive region comprises conductively-doping a region of the base; and
the forming the second conductive region comprises conductively-doping a region of the cover.

15 241. The method of claim 238 further comprising:
forming first and second conductive regions along opposing sides of the trench from one another; and
electrically coupling the first and second conductive regions to a detection system configured to monitor at least one electrical interaction
20 between the first and second conductive regions.

242. An electromagnetic radiation interaction component, comprising:
a monocrystalline semiconductor base;
a pair of electrically insulative projections extending upwardly from
25 the base;
a cover across the electrically insulative projections; the base, projections and cover together comprising a conduit having a periphery which includes regions of the base, projections and cover; and
a material at least partially filling the conduit.

30 243. The component of claim 242 wherein the material comprises a metal.

244. The component of claim 242 wherein the electromagnetic interaction component is configured as a path for a wavelength of light, and wherein the material comprises a composition which refracts the wavelength of light differently than compositions of the base, projections and cover.

5 245. The component of claim 242 wherein the base consists of monocrystalline silicon, the pair of projections consist of one or both of silicon dioxide and silicon nitride, and the cover consists of one or more of elemental-form W, silicide, and silicon.

10 246. The component of claim 242 wherein the base consists of monocrystalline silicon, the pair of projections consist of silicon dioxide, the cover consists of monocrystalline silicon, and the material comprises cadmium.

247. The component of claim 246 wherein the material comprises cadmium oxide.

15 248. A fluorimetry system, comprising:
a sample holder comprising:
a silicon-containing substrate;
a pair of silicon dioxide-containing projections extending upwardly from the substrate;
20 a silicon dioxide-containing cover extending across the projections;
the substrate, projections and cover together encompassing a sample-retaining conduit;
a source of electromagnetic radiation configured to emit radiation through either the base, a projection or the cover; and
25 a detector configured to detect electromagnetic radiation passing out of the sample-retaining conduit, the detector being configured to detect radiation at about 90 degrees relative to a direction along which the source emits radiation.

30 249. The fluorimetry system of claim 248 wherein the source is configured to emit the radiation through the base.

250. The fluorimetry system of claim 248 wherein the source is configured to emit the radiation through a projection.

251. The fluorimetry system of claim 248 wherein the source is configured to emit the radiation through the cover.

5 252. The fluorimetry system of claim 248 wherein the substrate comprises monocrystalline silicon.

253. The fluorimetry system of claim 248 wherein the substrate comprises silicon dioxide.

10 254. The fluorimetry system of claim 248 wherein the substrate consists of silicon dioxide.

255. A semiconductor construction, comprising:
a semiconductor material base;
a pair of projections extending upwardly from the base;
a cover extending across the projections;
15 a nanofluidic channel contained between the projections, base and cover;
first conductive region along a first segment of a periphery of the nanofluidic channel;
a second conductive region along a second segment of the periphery
20 of the nanofluidic channel and spaced from the first conductive region by an intervening segment of the nanofluidic channel; and
a detector electrically coupled to both of the first and second conductive regions.

256. The construction of claim 255 wherein the base comprises
25 monocrystalline silicon, the projections comprise silicon dioxide, and the cover comprises monocrystalline silicon.

257. The construction of claim 255 wherein the first conductive region is along the base and the second conductive region is along the cover.

258. The construction of claim 255 wherein the base comprises monocrystalline silicon, the projections comprise silicon dioxide, and the cover comprises monocrystalline silicon; and wherein the first and second conductive regions are conductively-doped regions of the base and cover,
5 respectively.

259. The construction of claim 255 wherein the first conductive region is along one of the projections and the second conductive region is along the other of the projections.

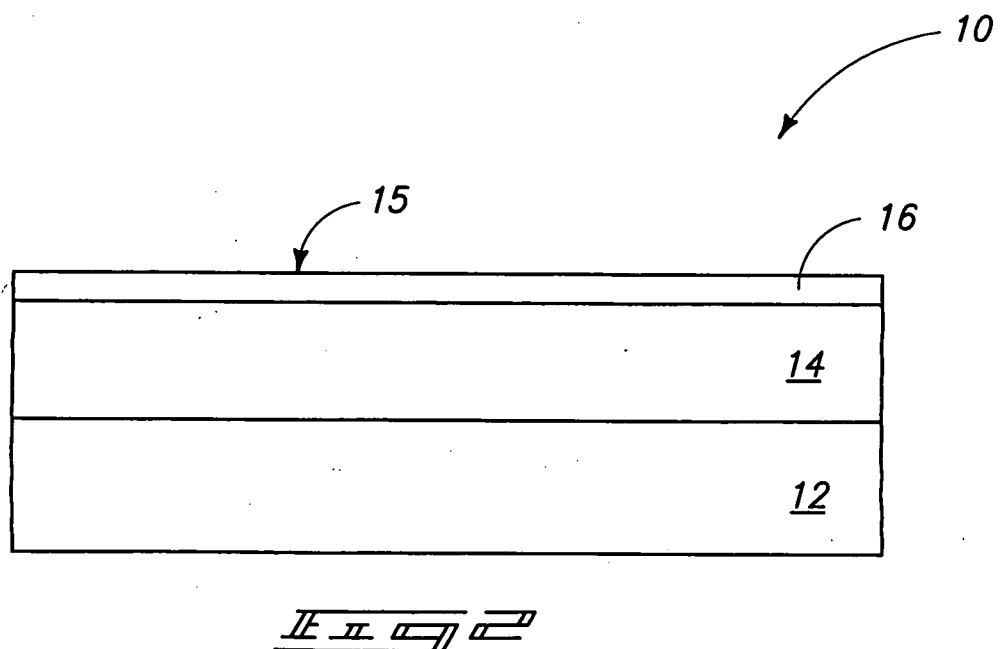
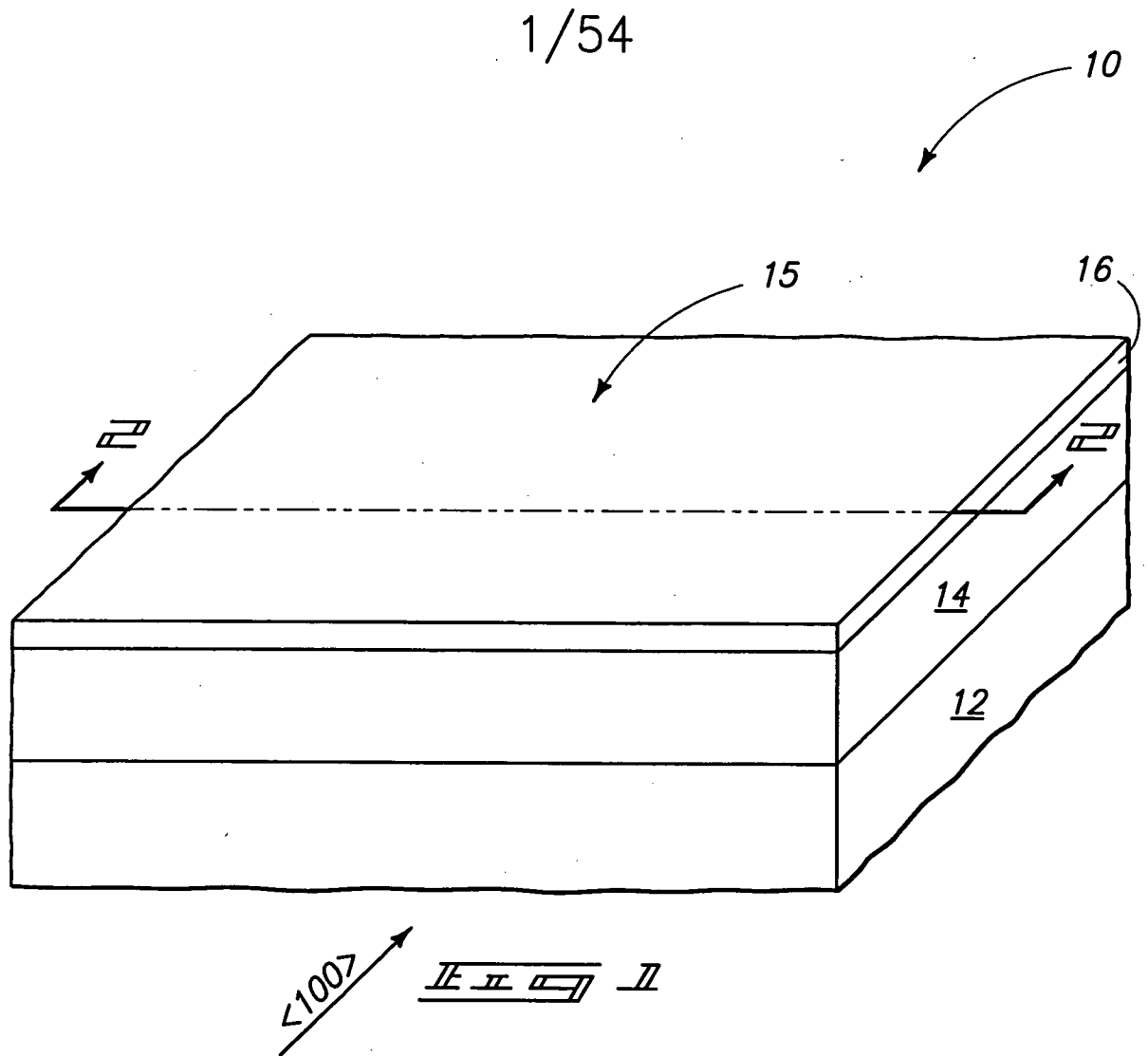
260. An electromagnetic radiation emitter and conduit construction,
10 comprising:

a pair of projections over an electromagnetic radiation generating base material; the projections projecting upwardly relative to the base material and being spaced from one another by a gap; and

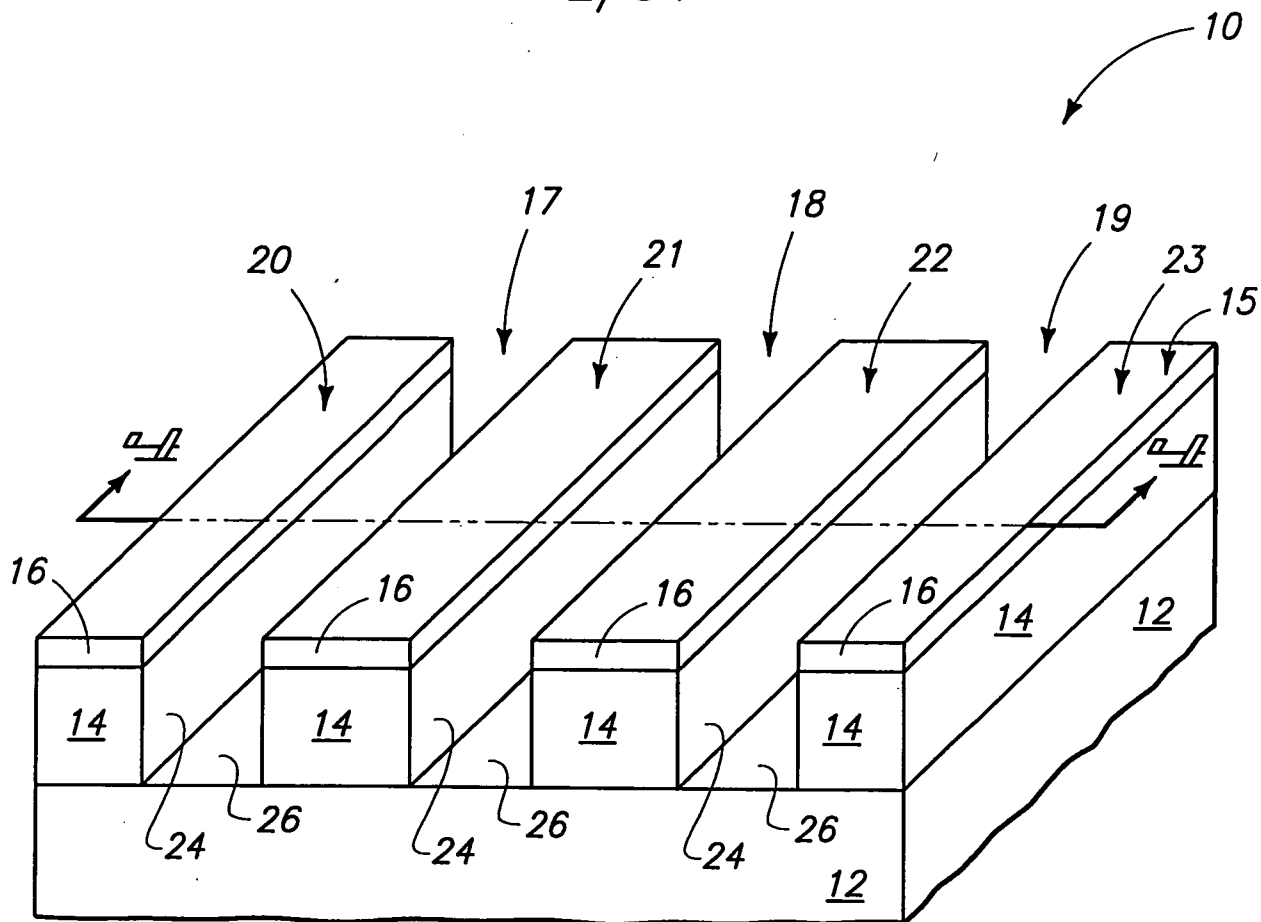
a bridging material extending across the pair of projections and over
15 the gap; a conduit being contained between the base, bridging material and projections.

261. The construction of claim 260 wherein the electromagnetic radiation generating base material comprises a III/IV material or a II/VI material.

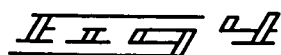
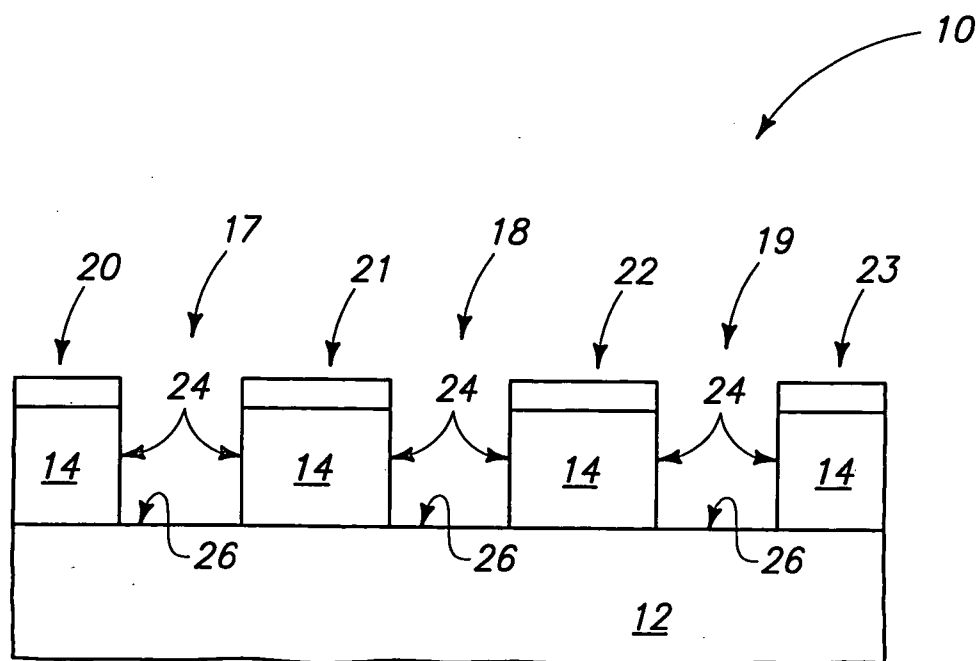
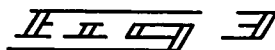
20 262. The construction of claim 260 wherein the projections consist of silicon dioxide, and have interior sidewalls along the gap, and further comprising metal-containing liners along said interior sidewalls.



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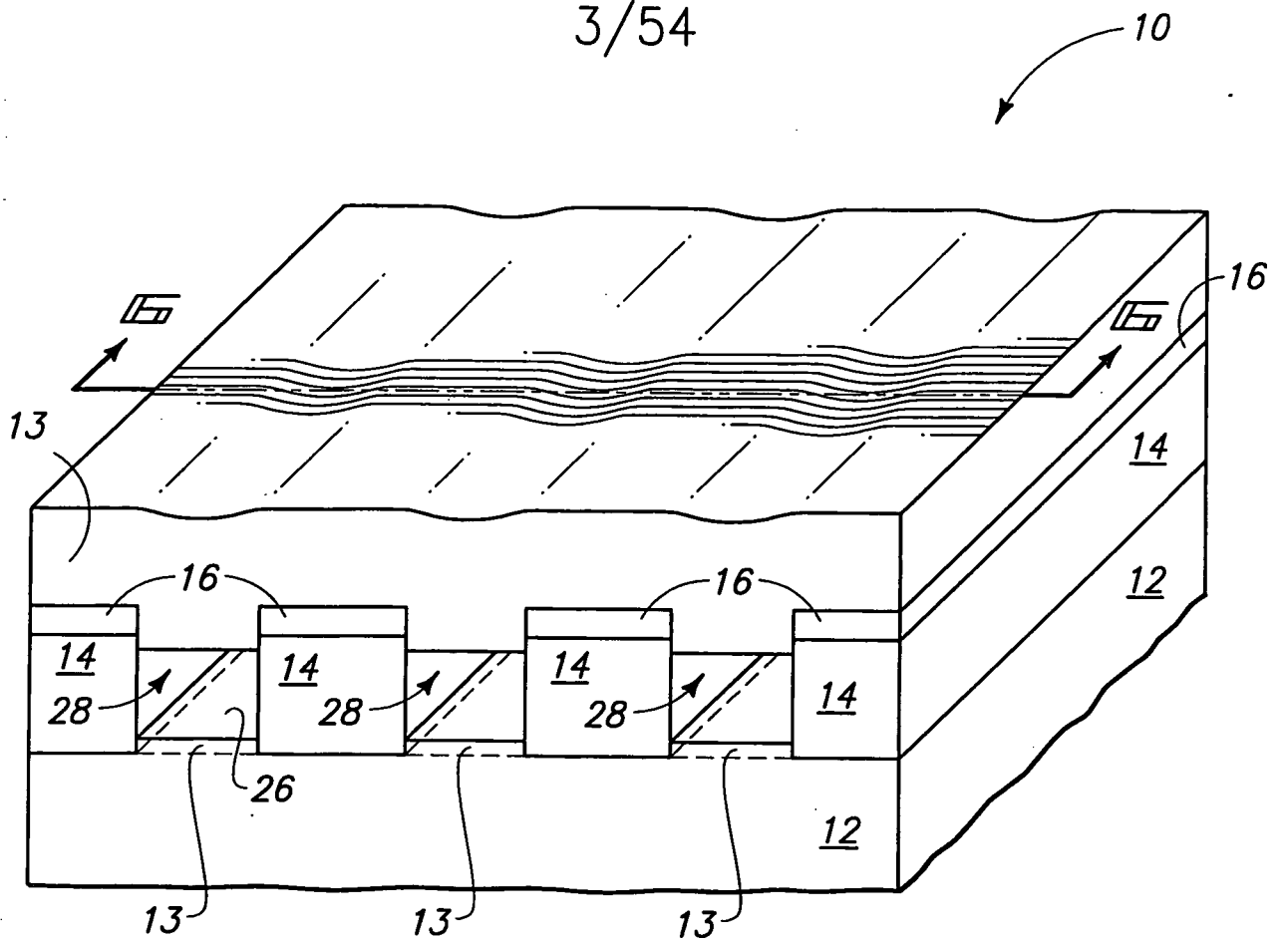


FIG. 3

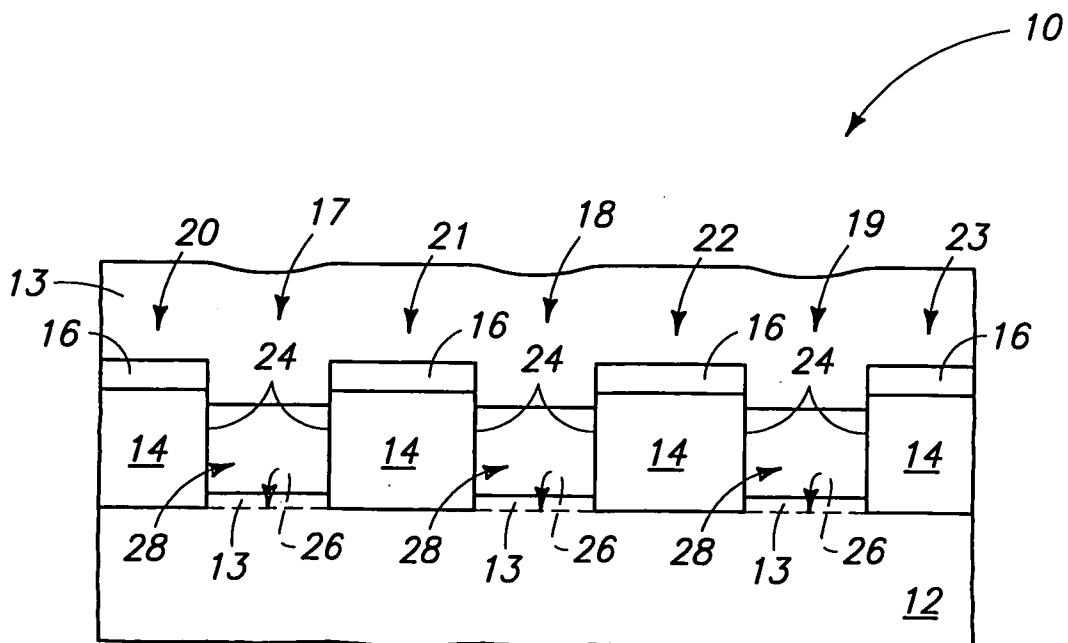
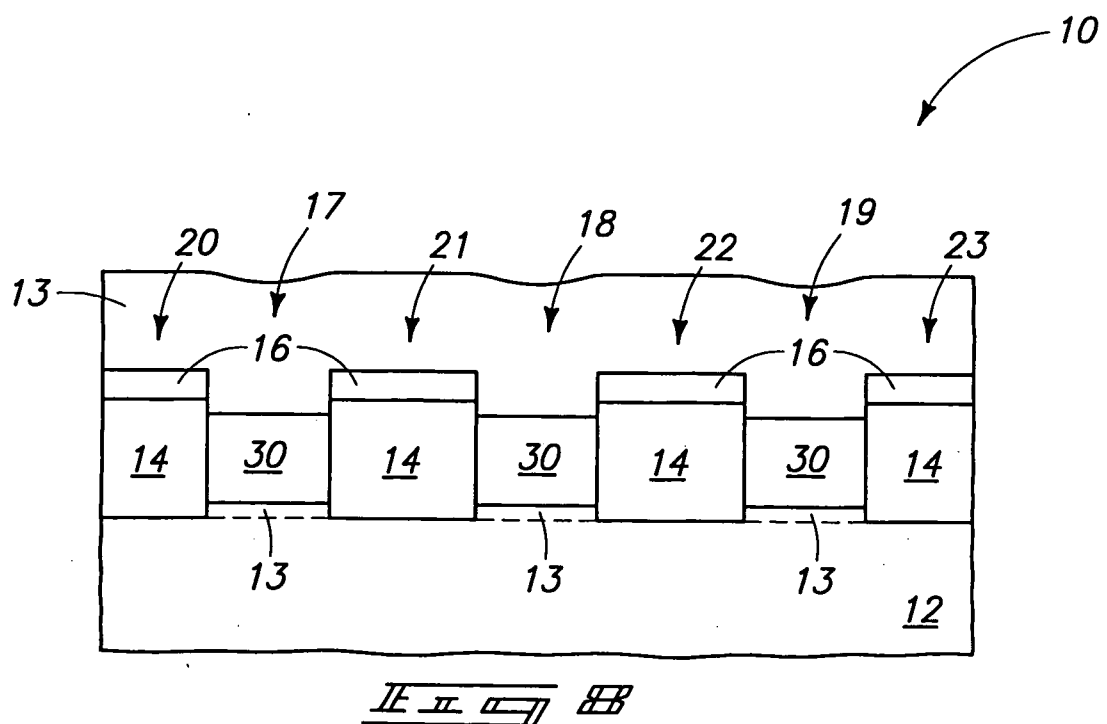
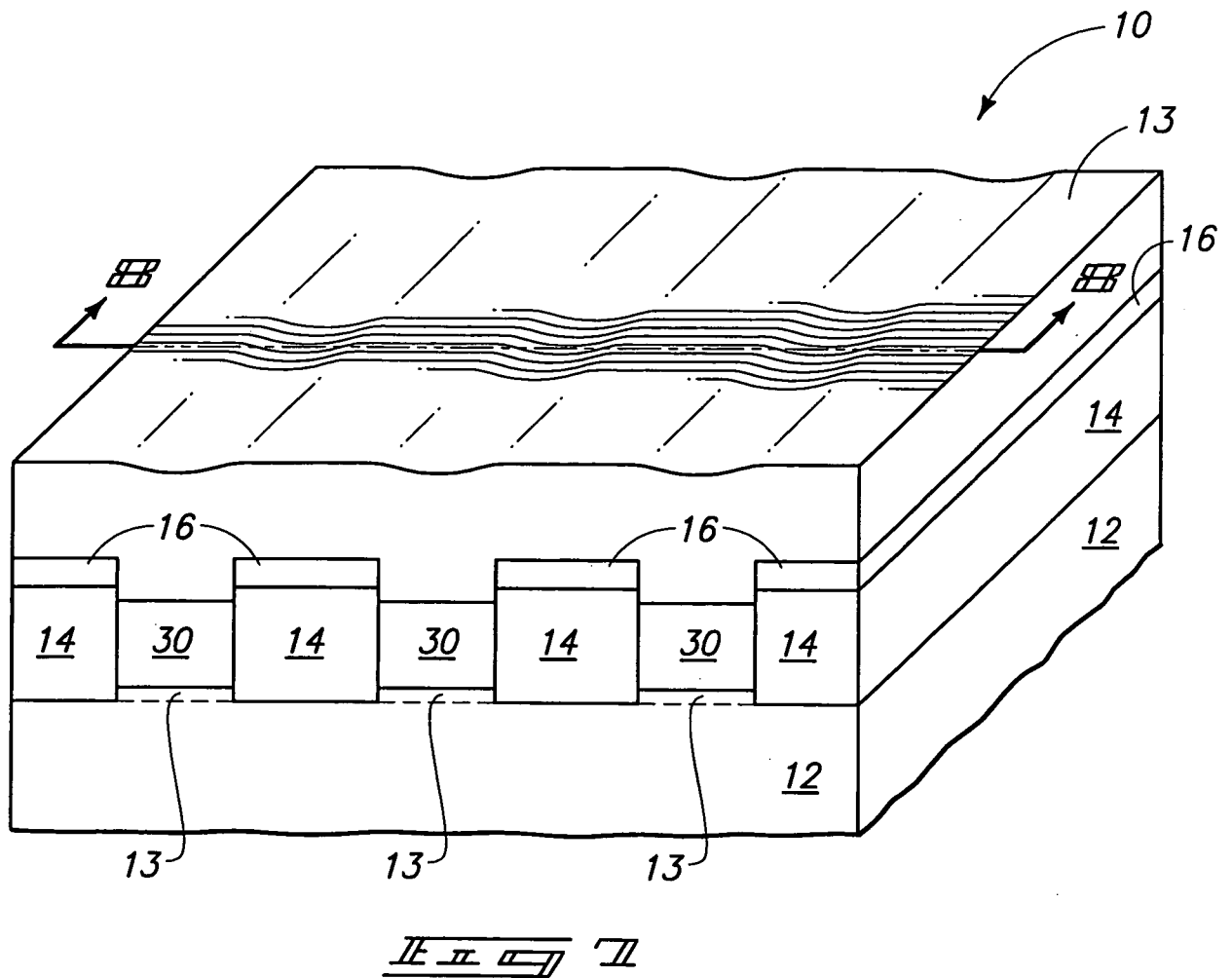
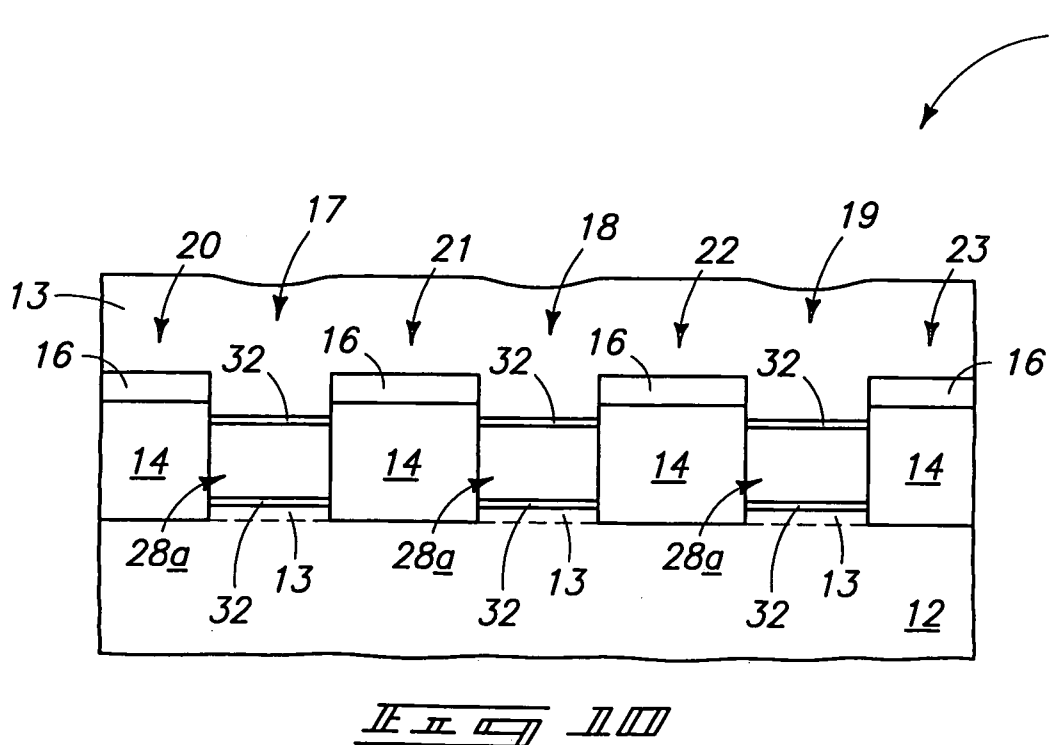
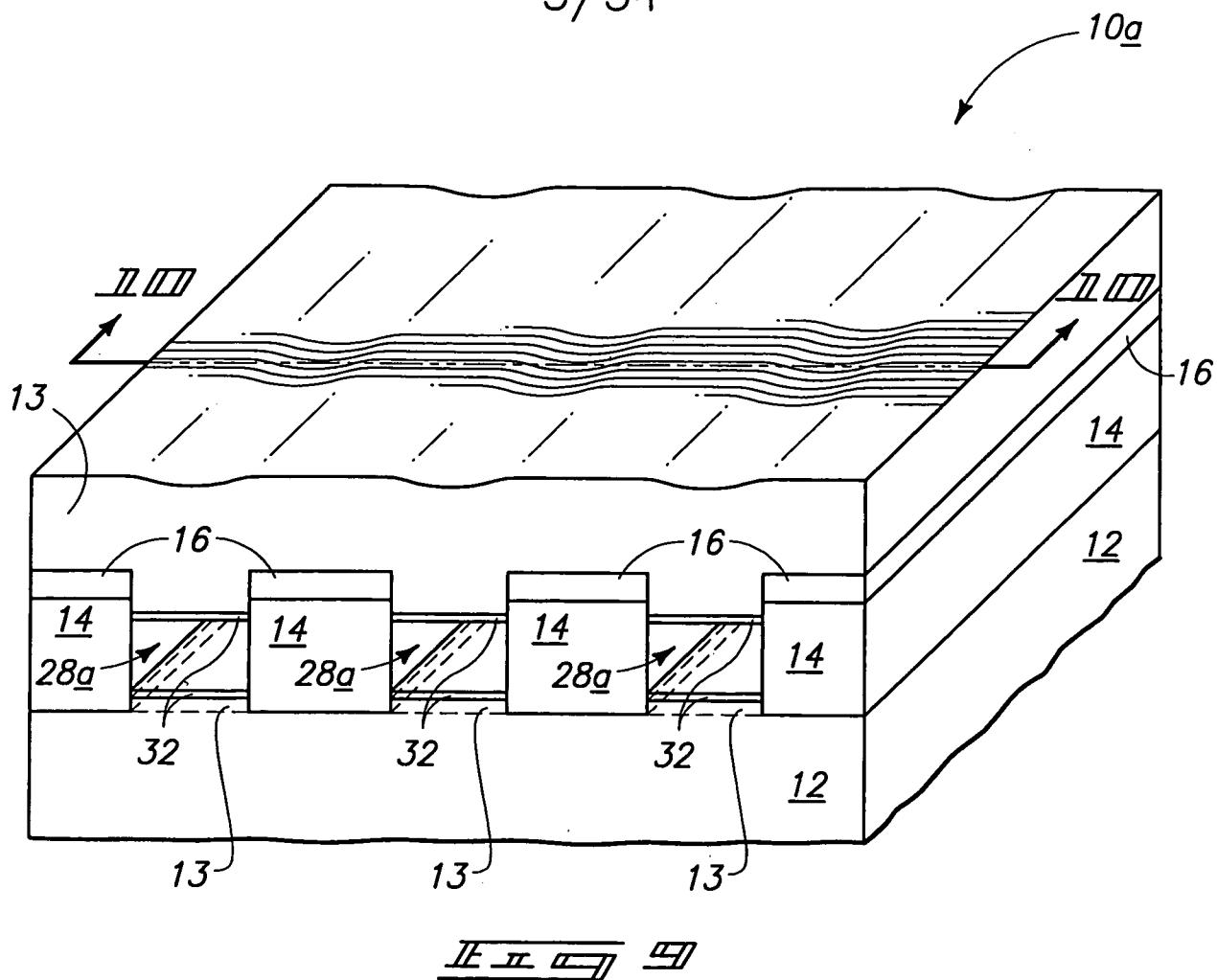


FIG. 4

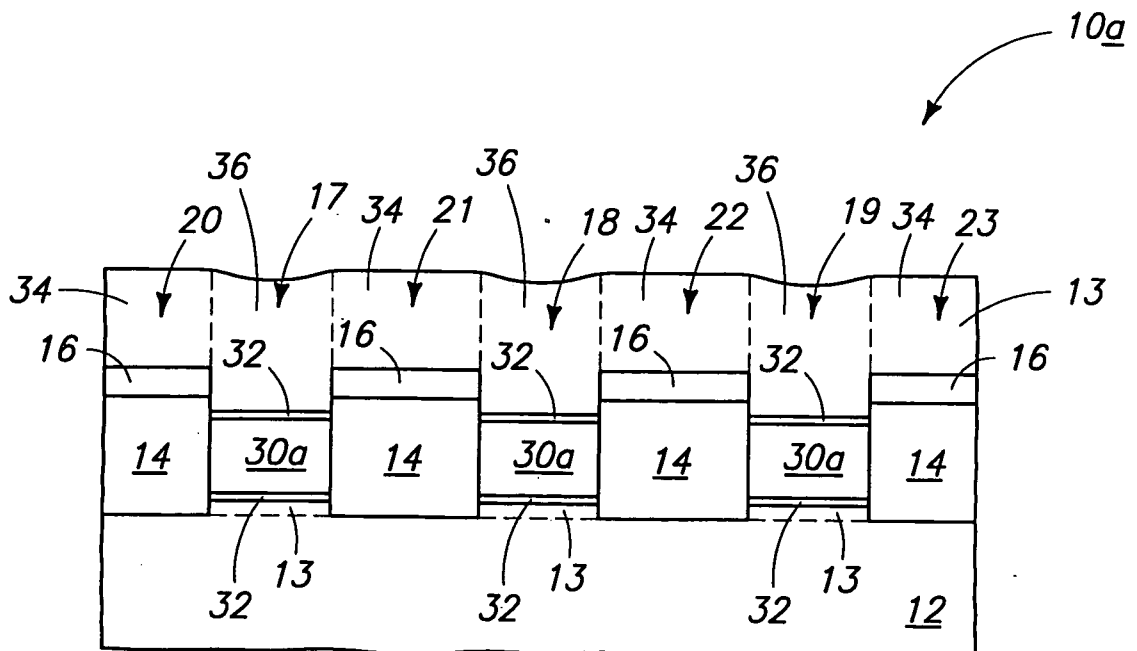
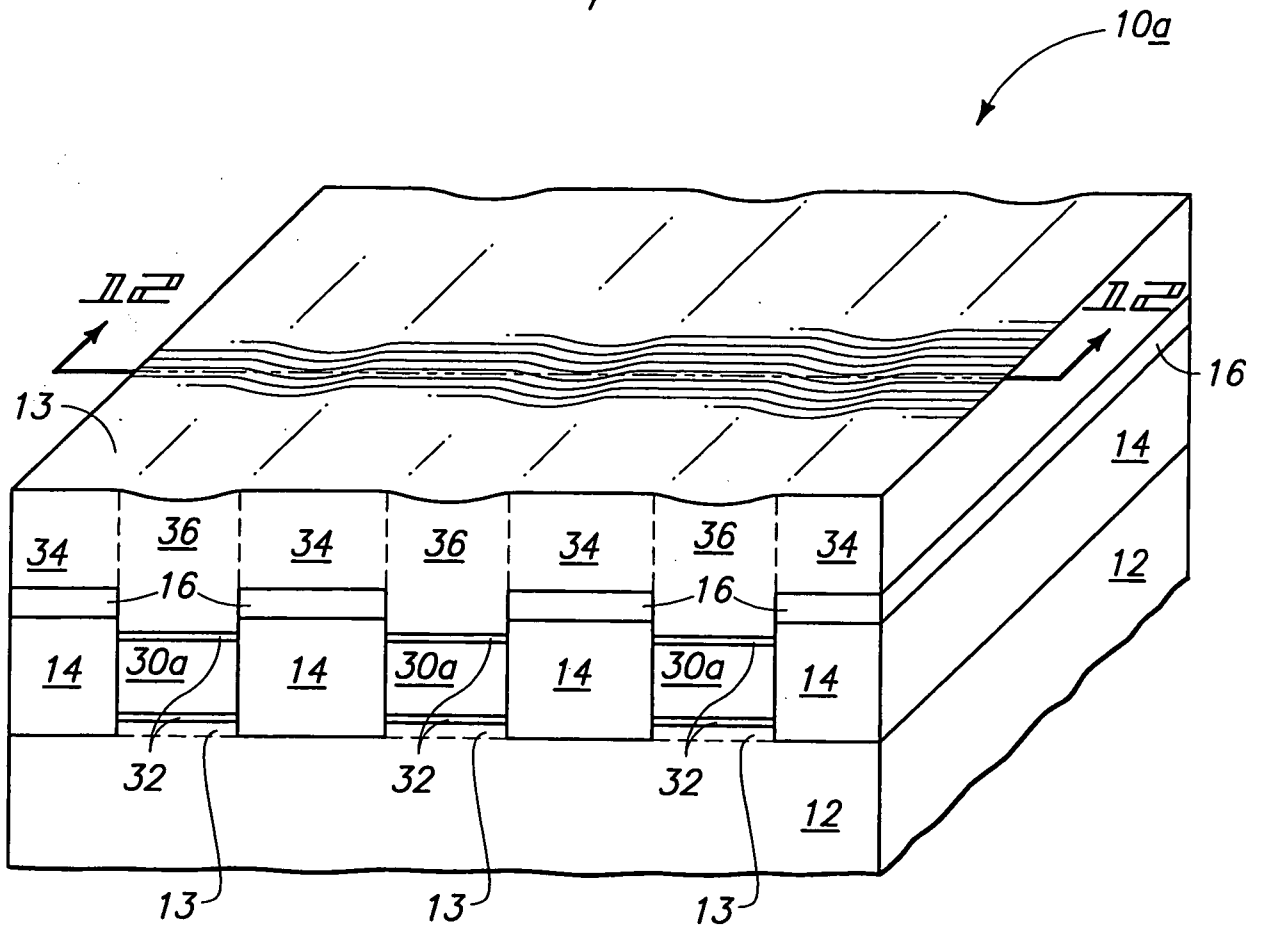
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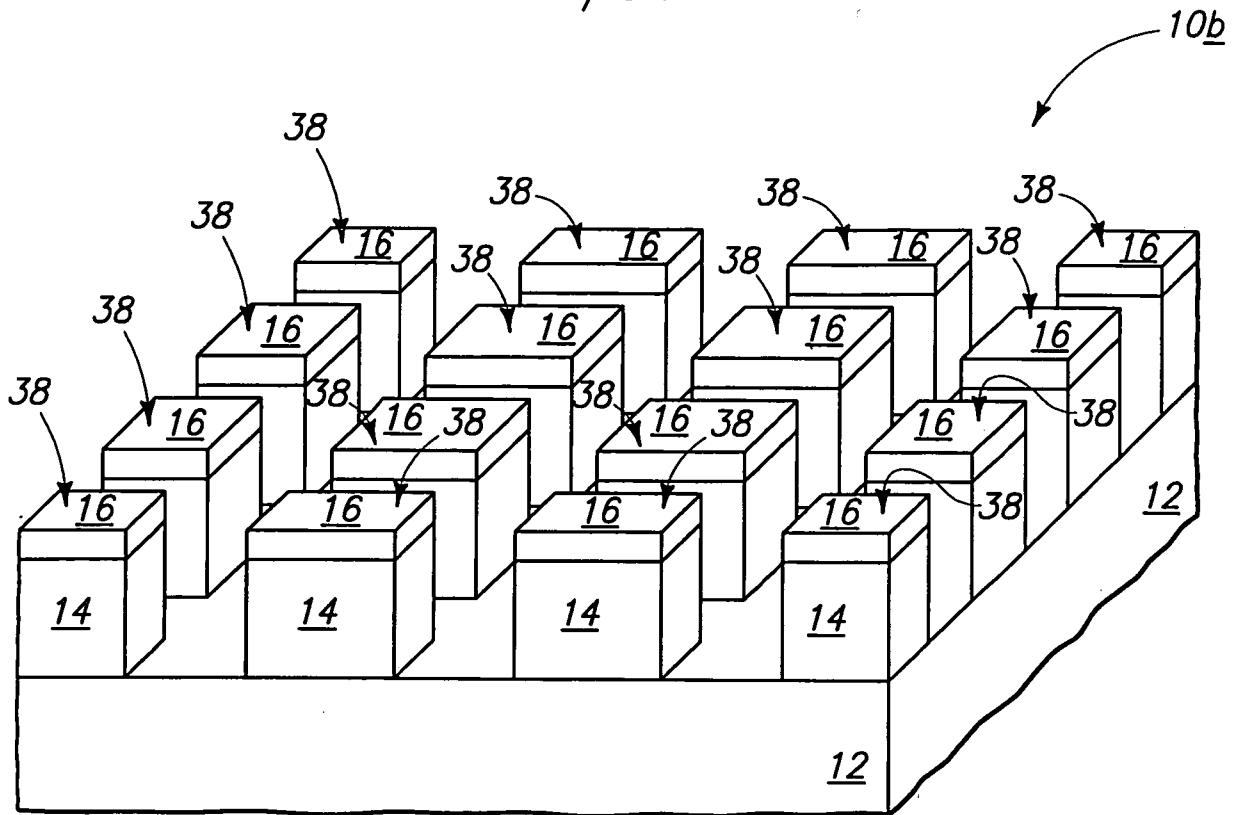


Fig. 54

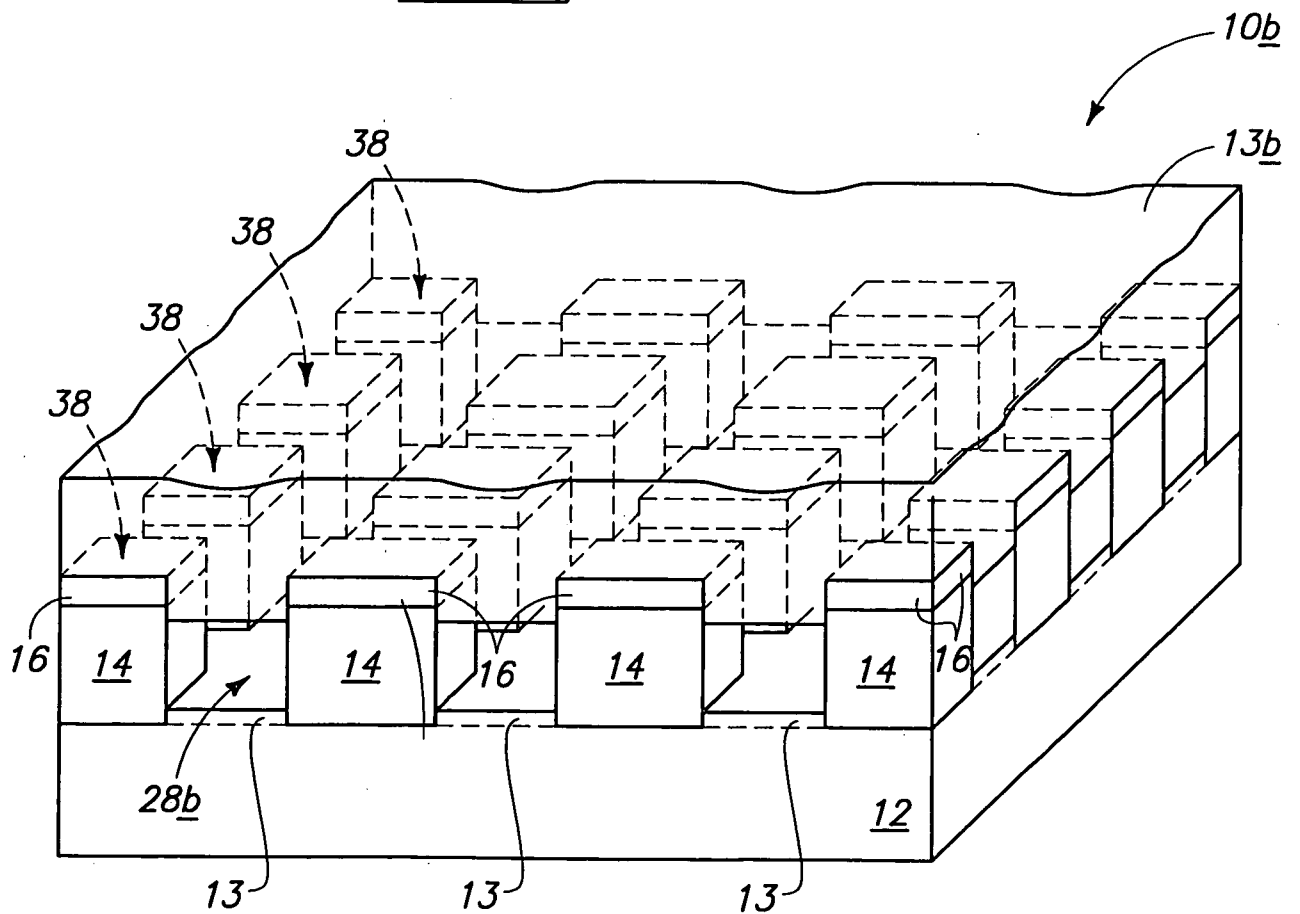
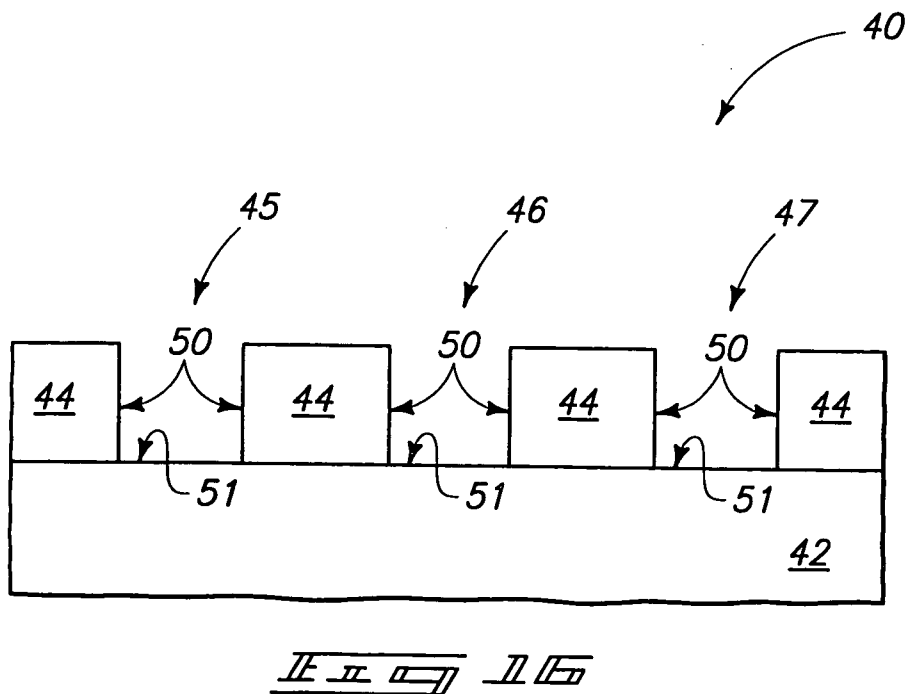
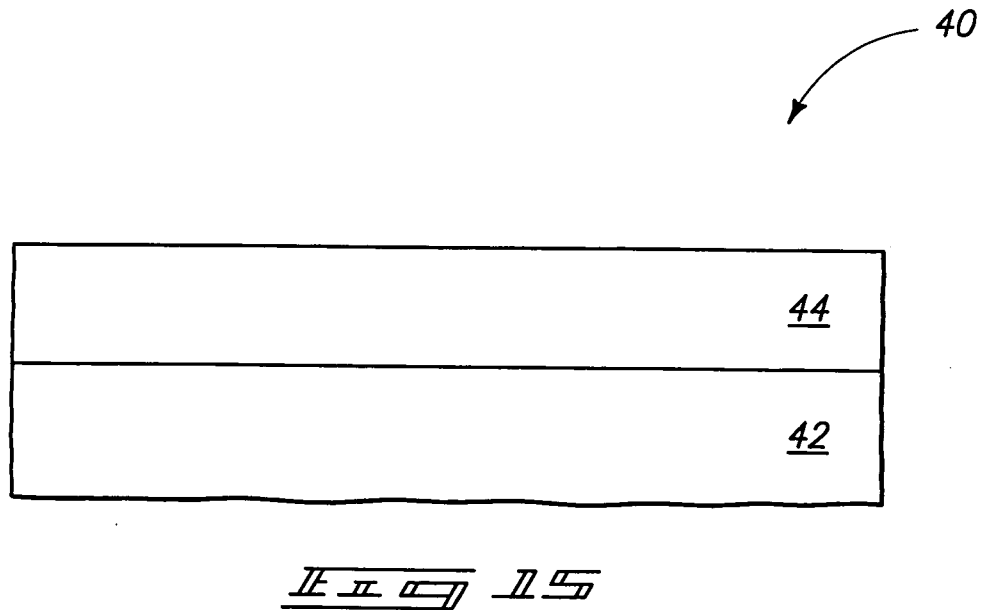
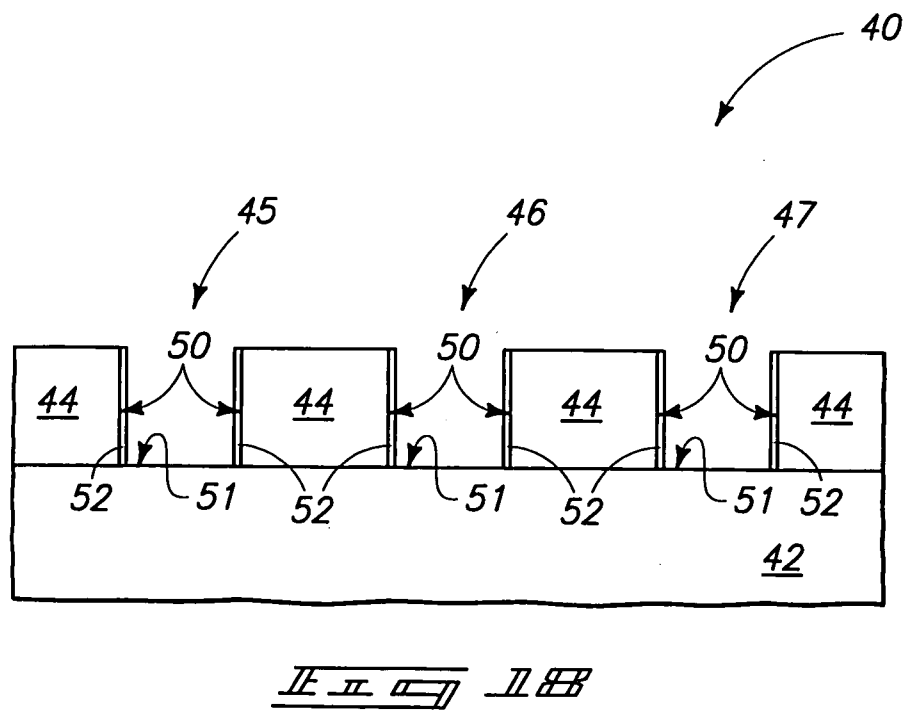
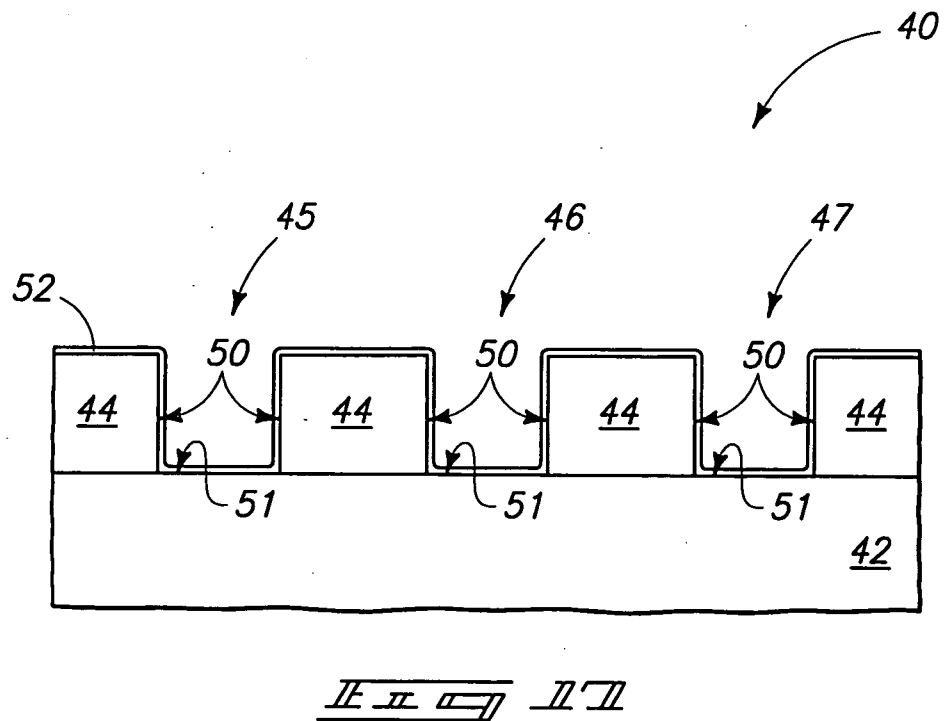


Fig. 55

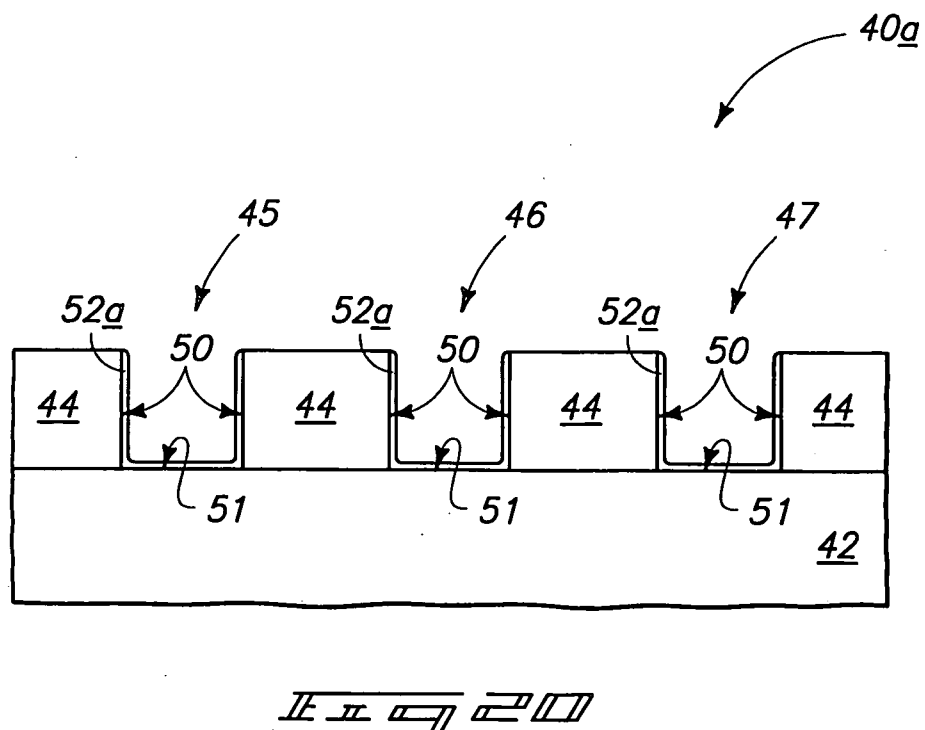
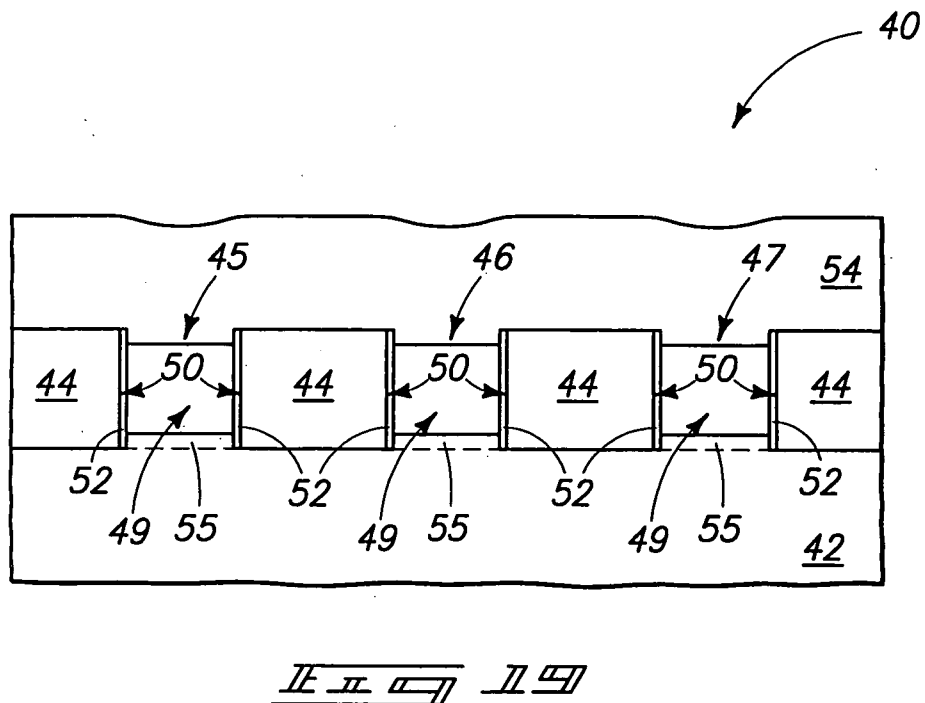
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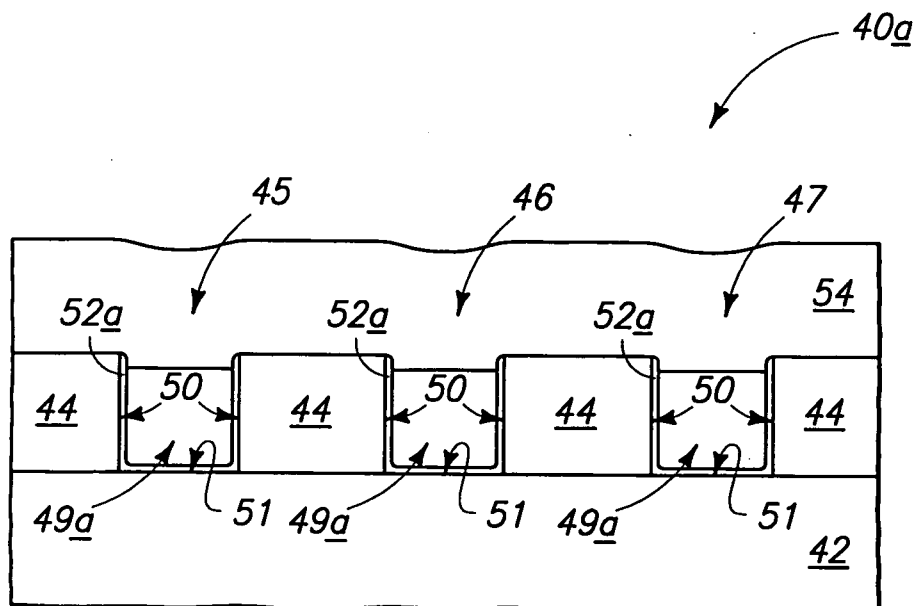
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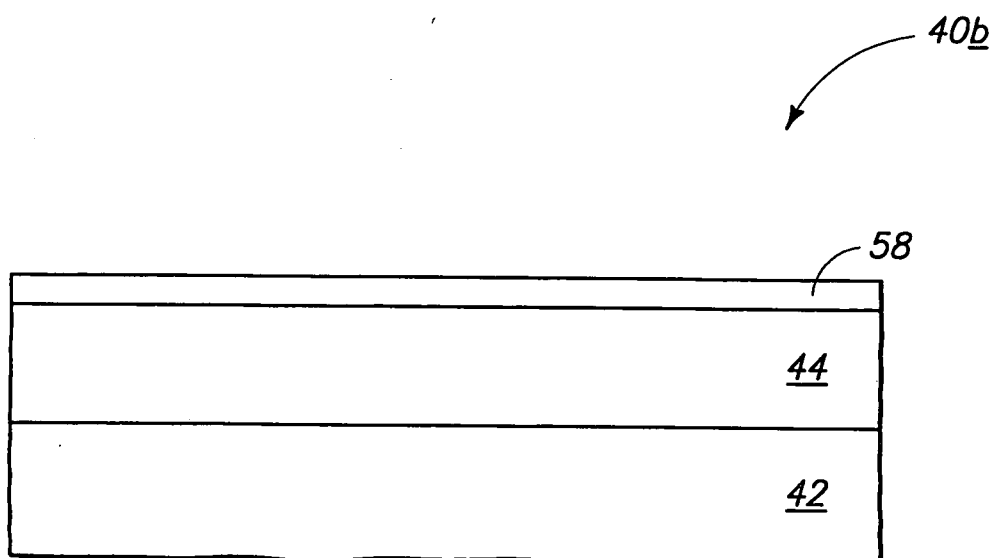
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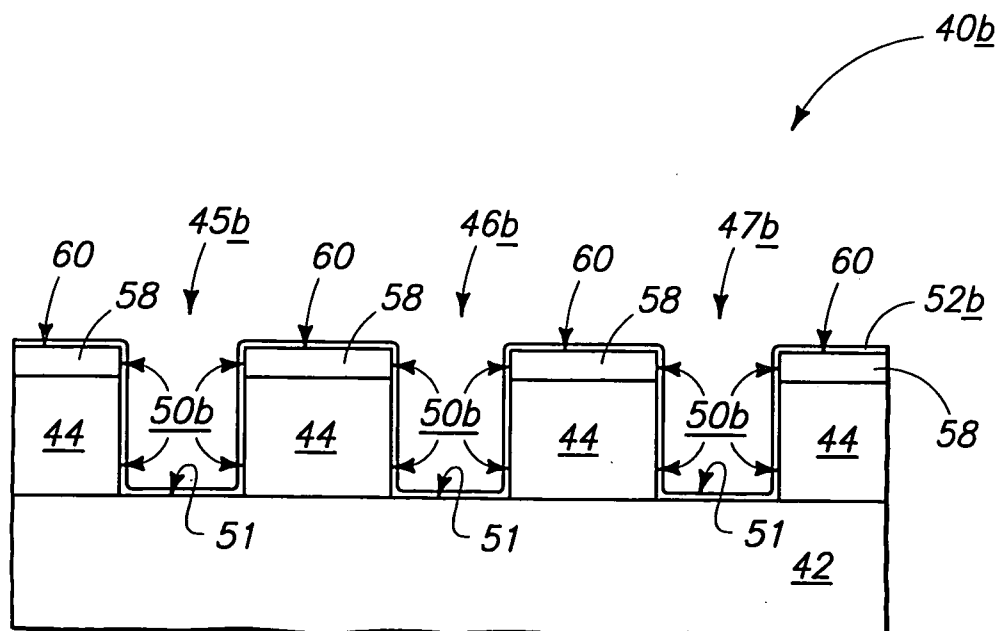
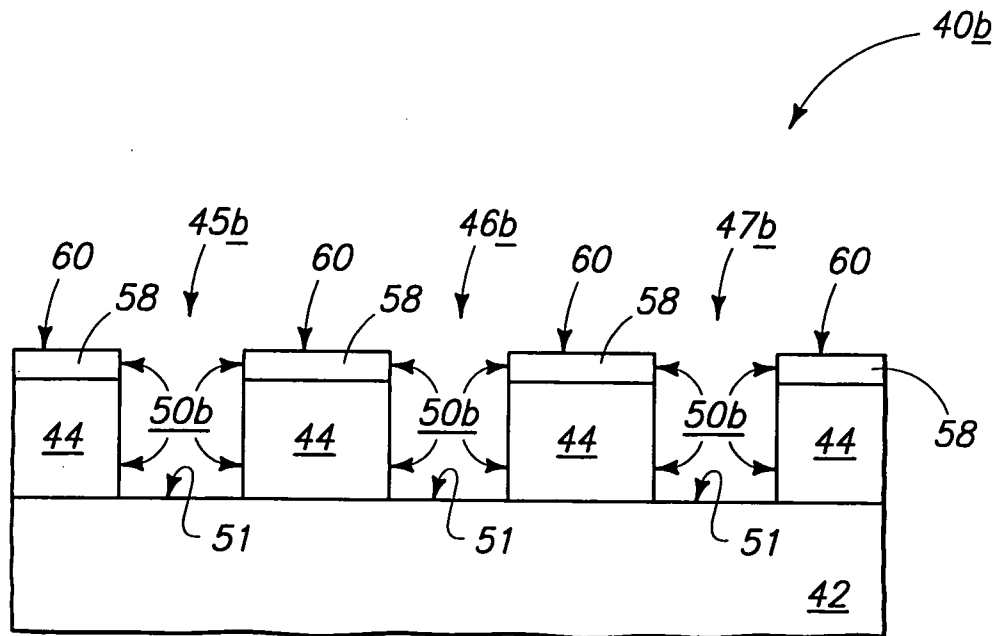


II II

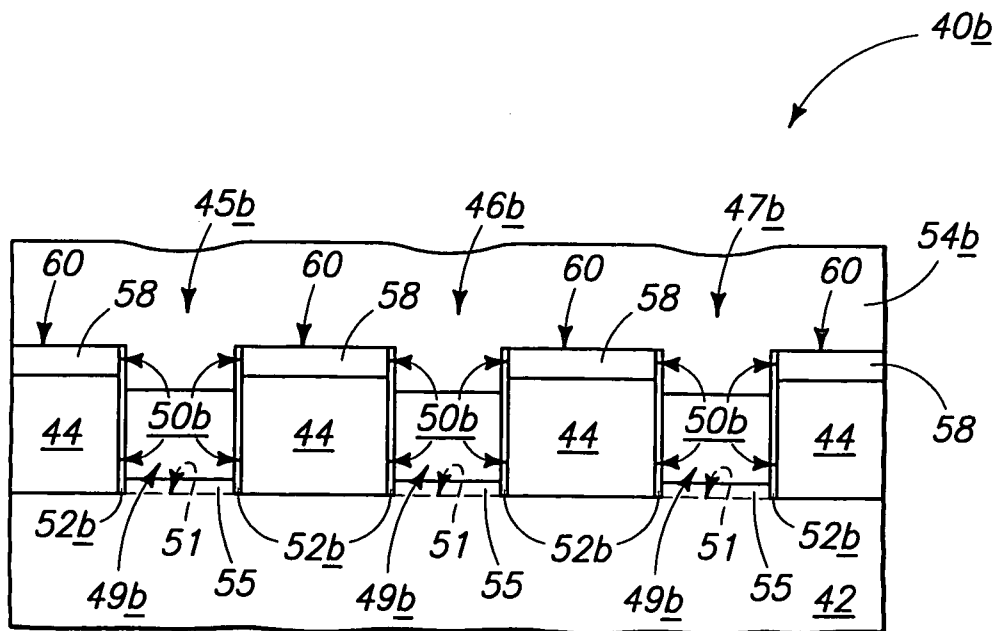
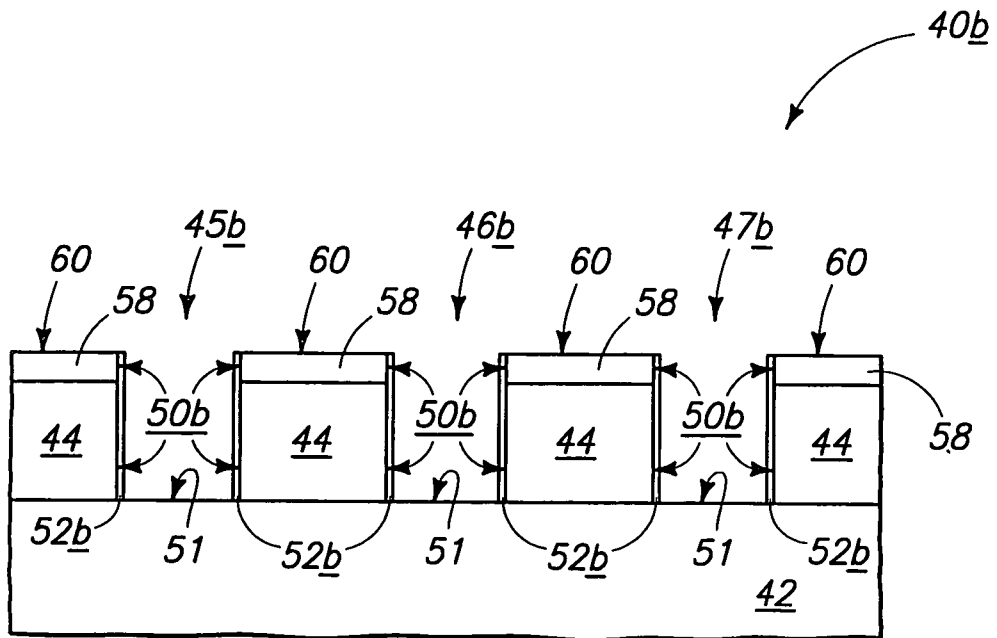


II II

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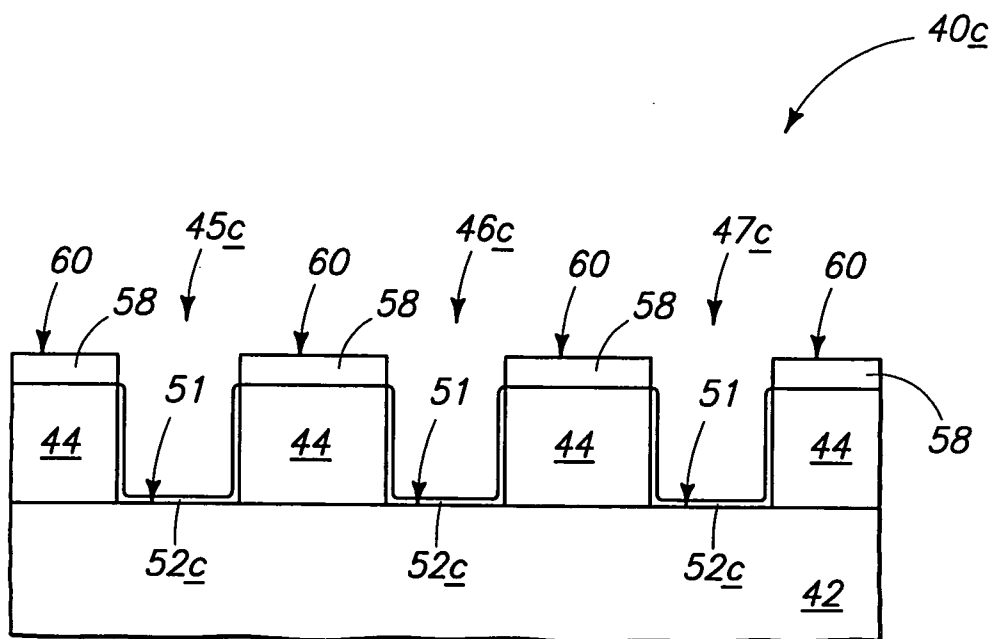


FIG. 14

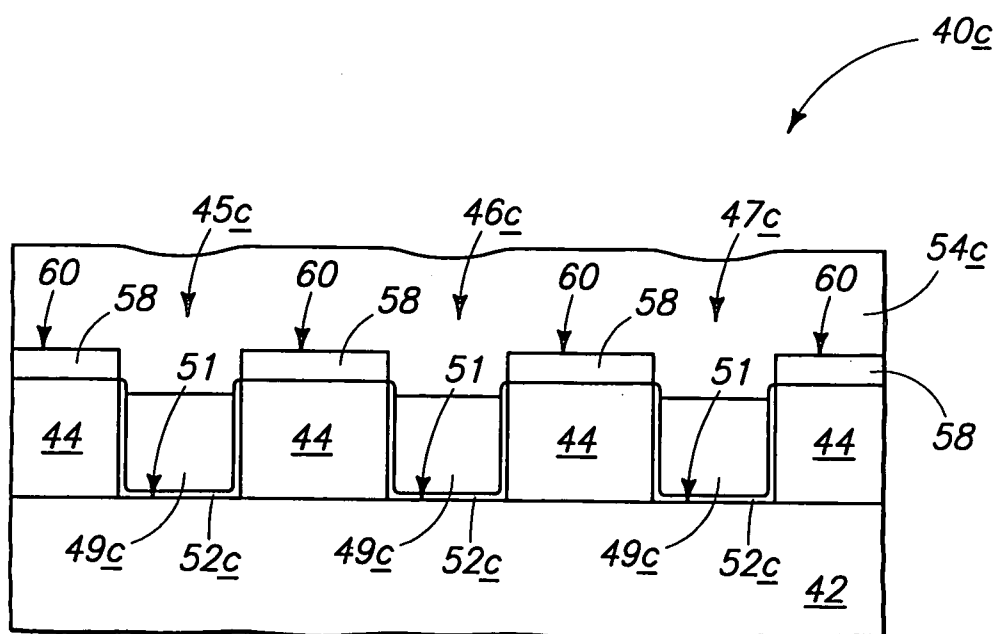
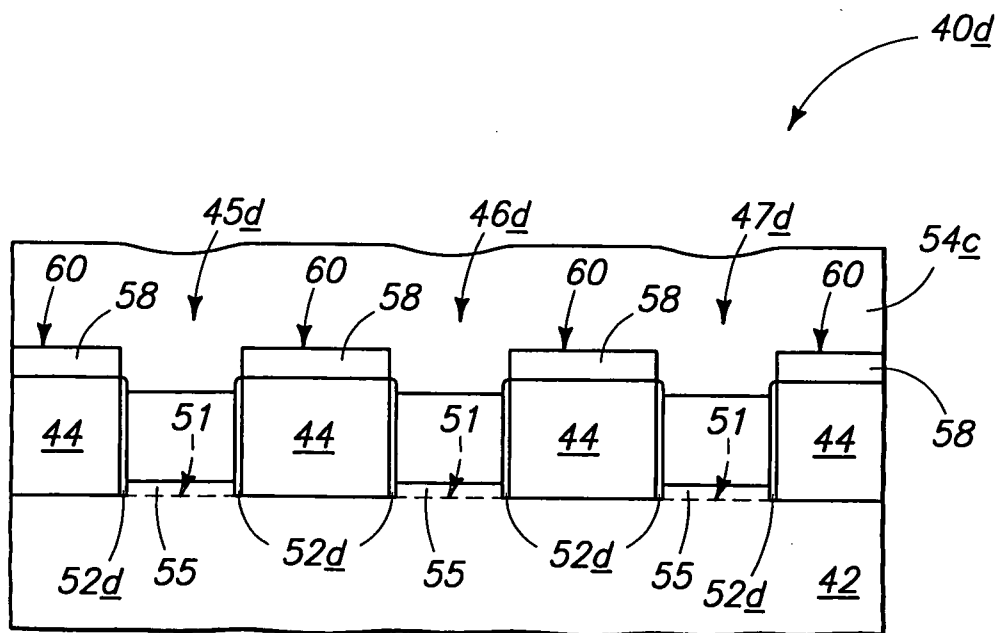
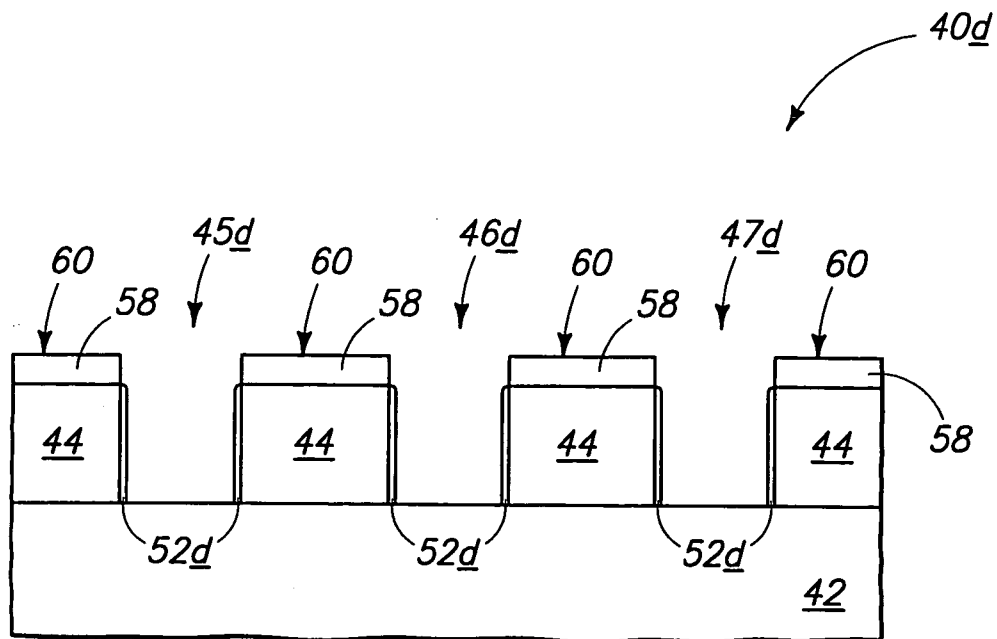
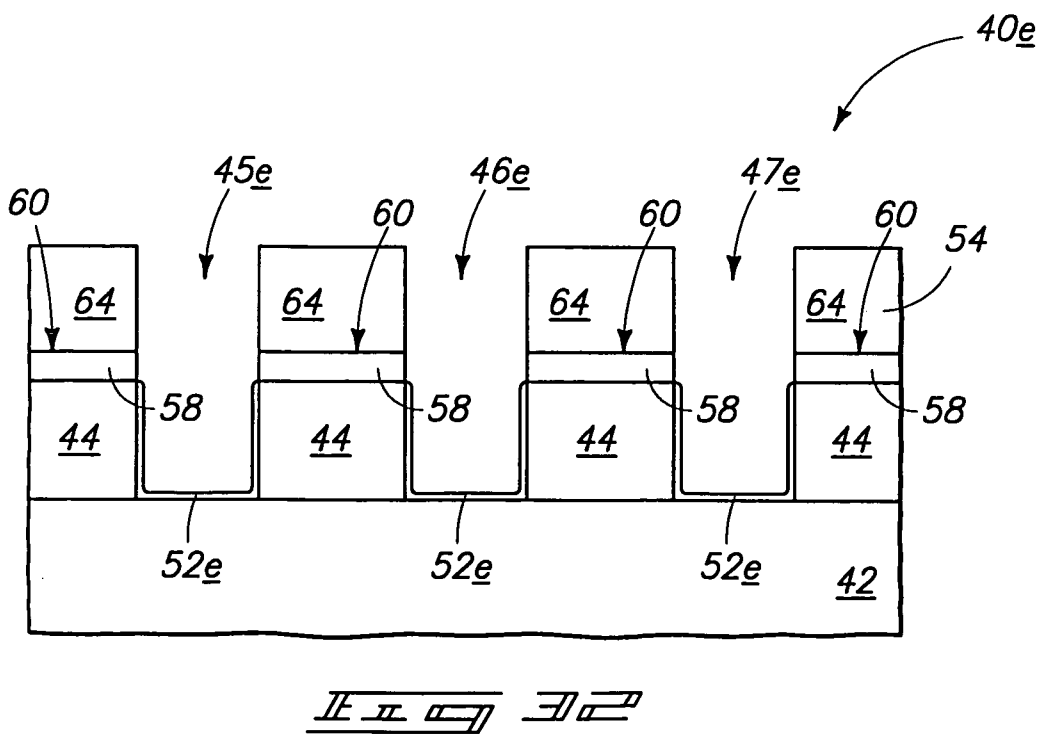
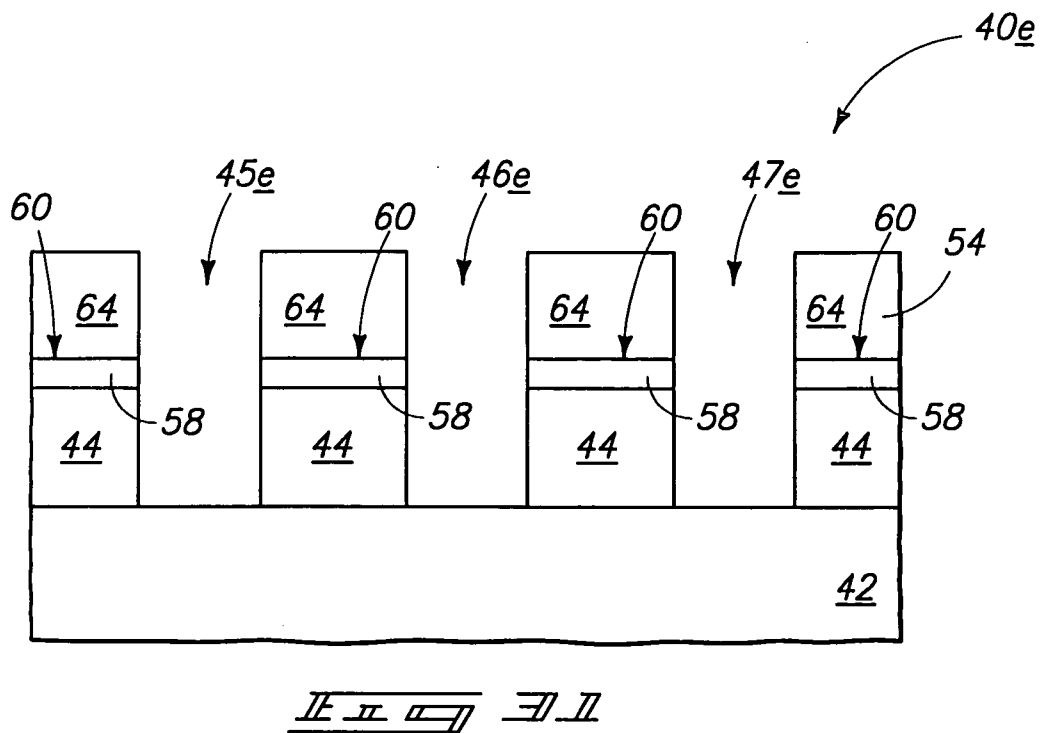


FIG. 15

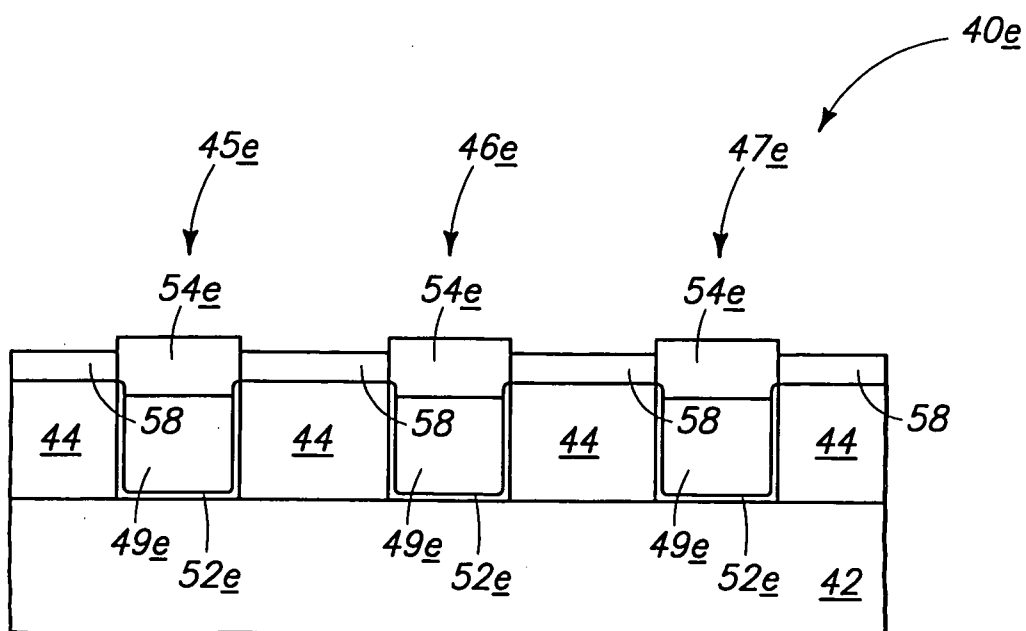
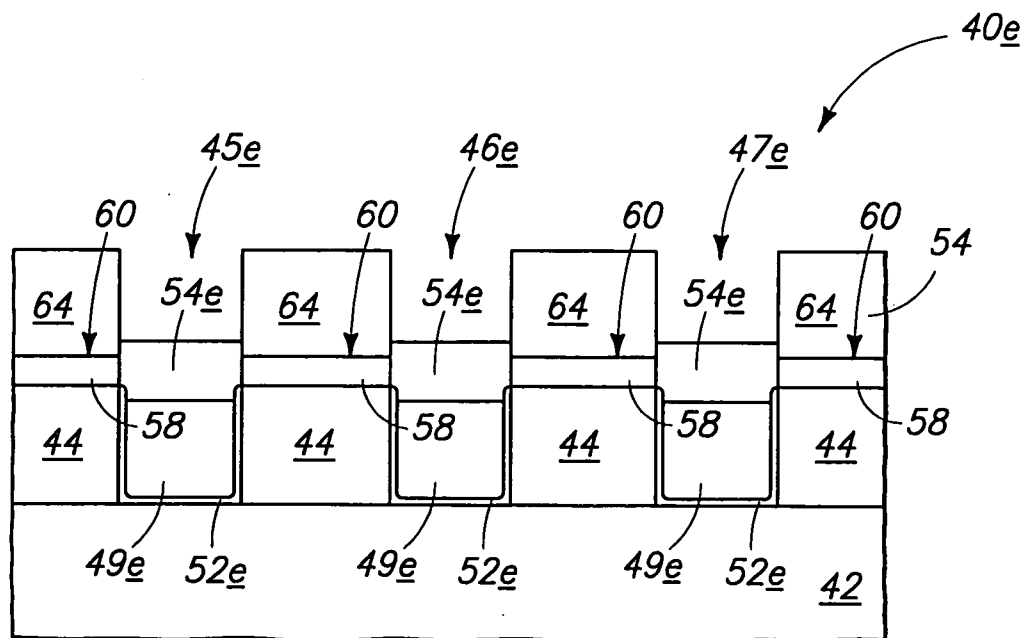
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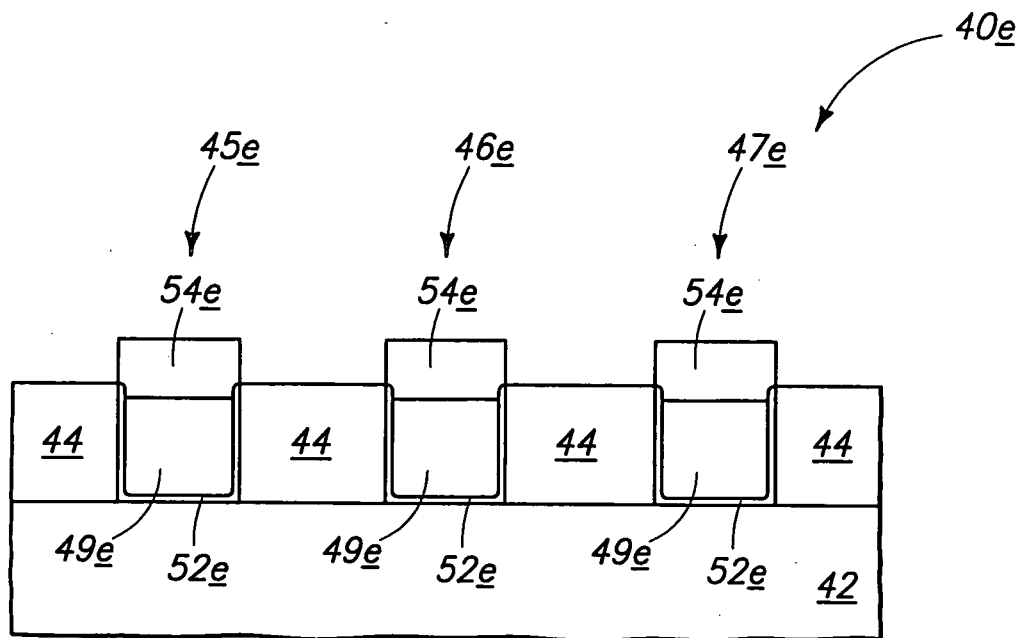
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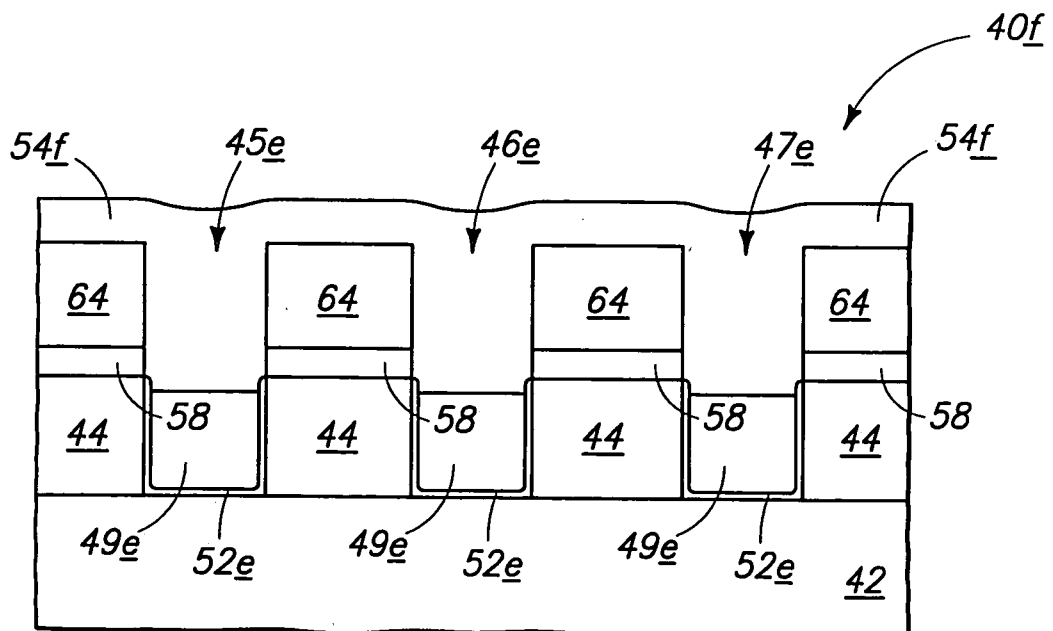
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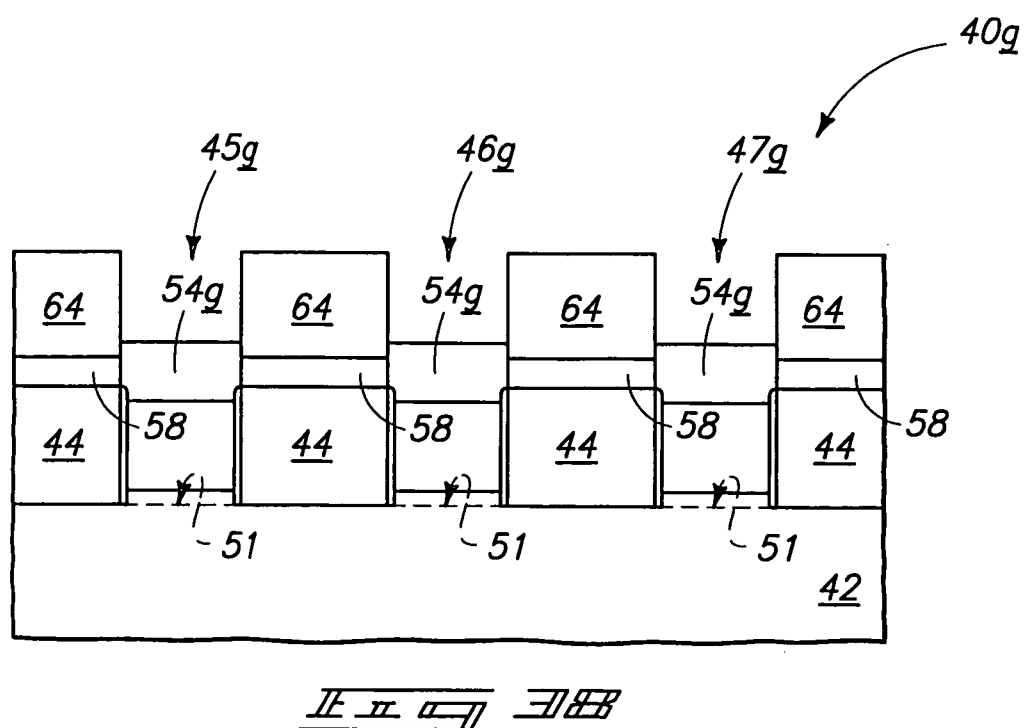
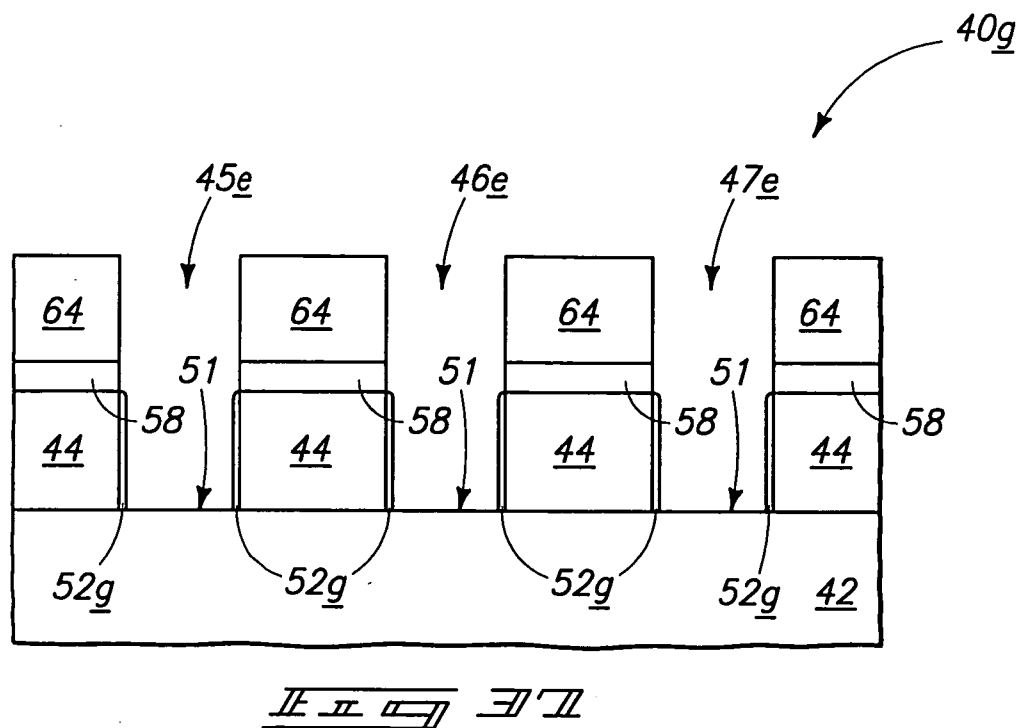


Итого 35



Итого 316

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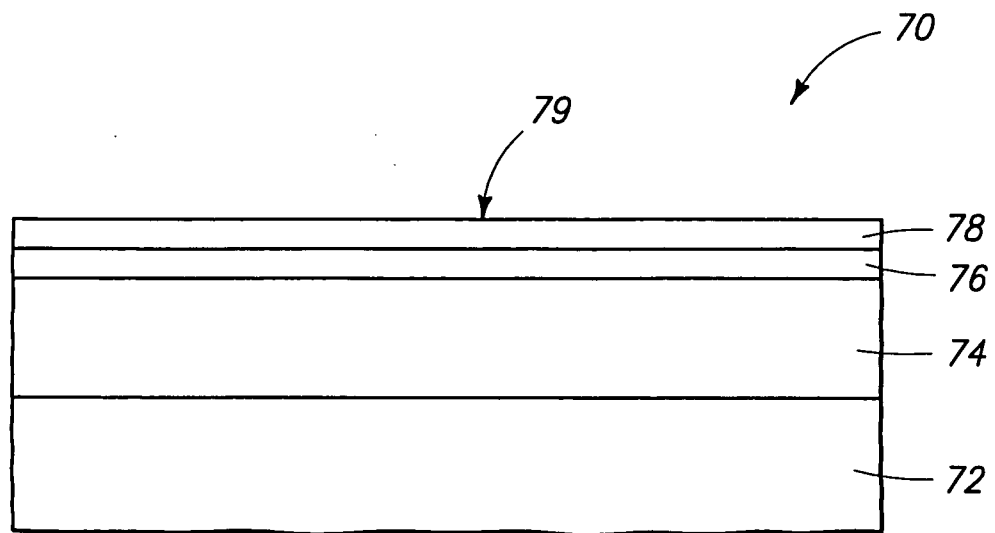


FIG. 3

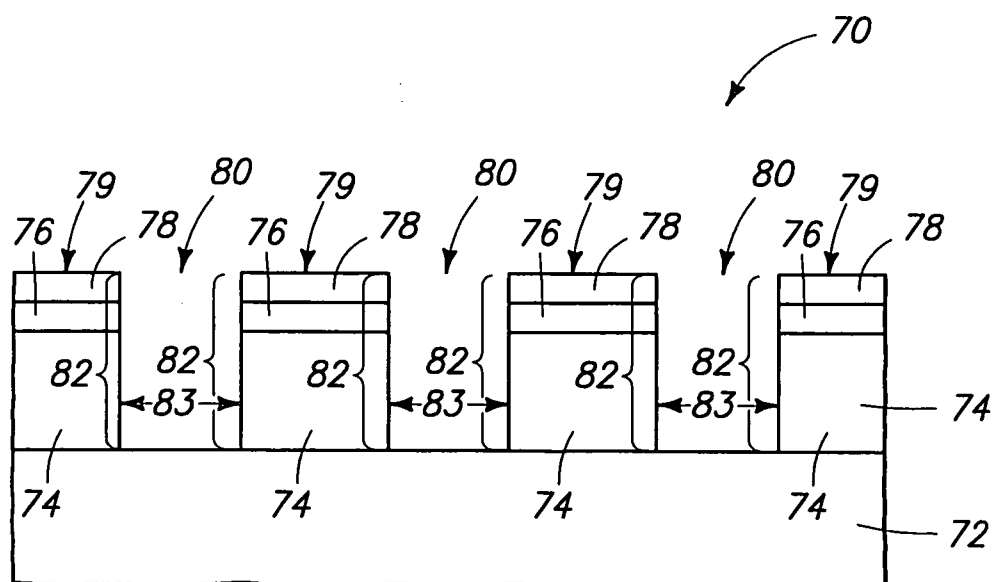


FIG. 4

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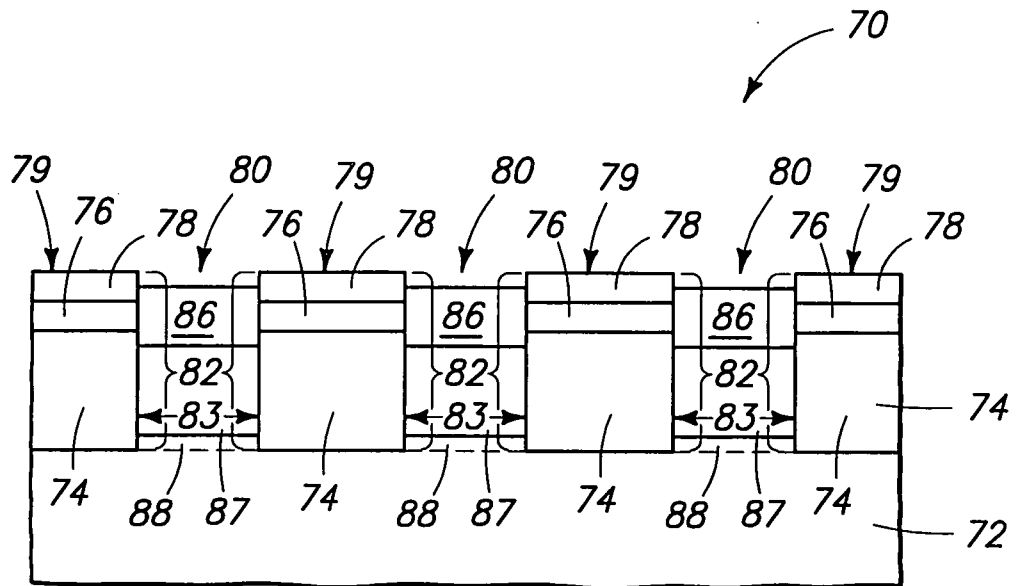


FIG. 1

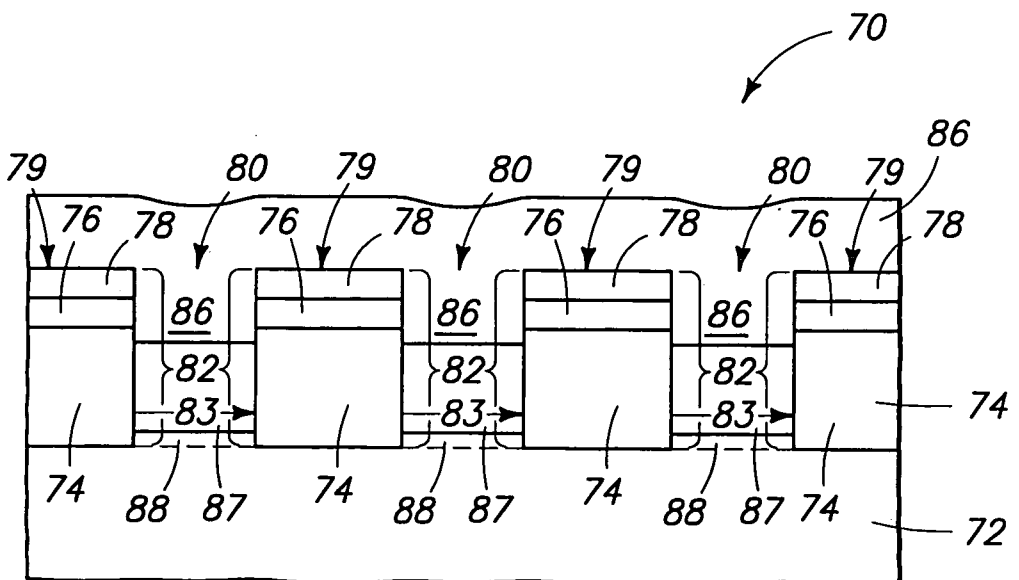


FIG. 2

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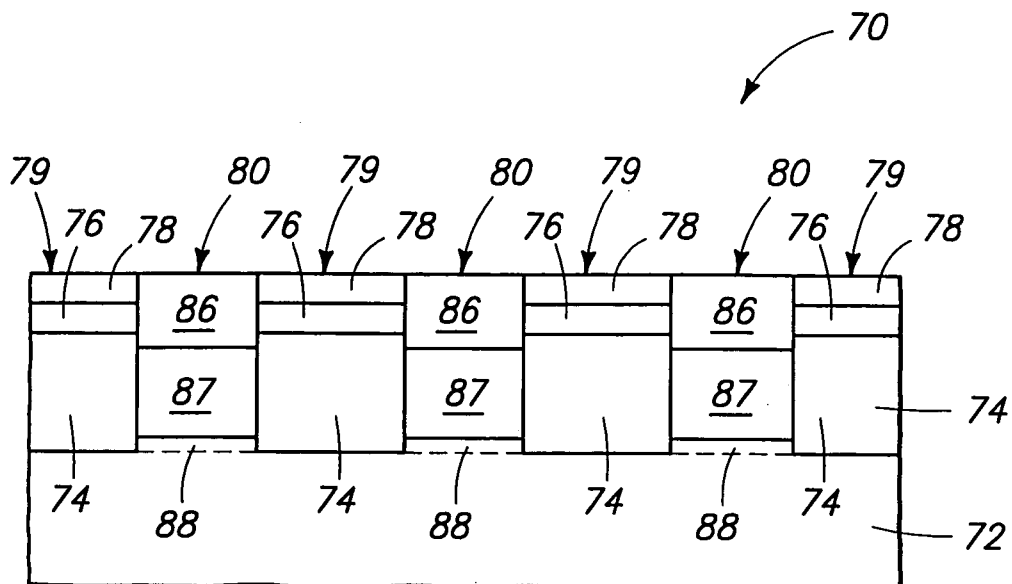


FIG. 22

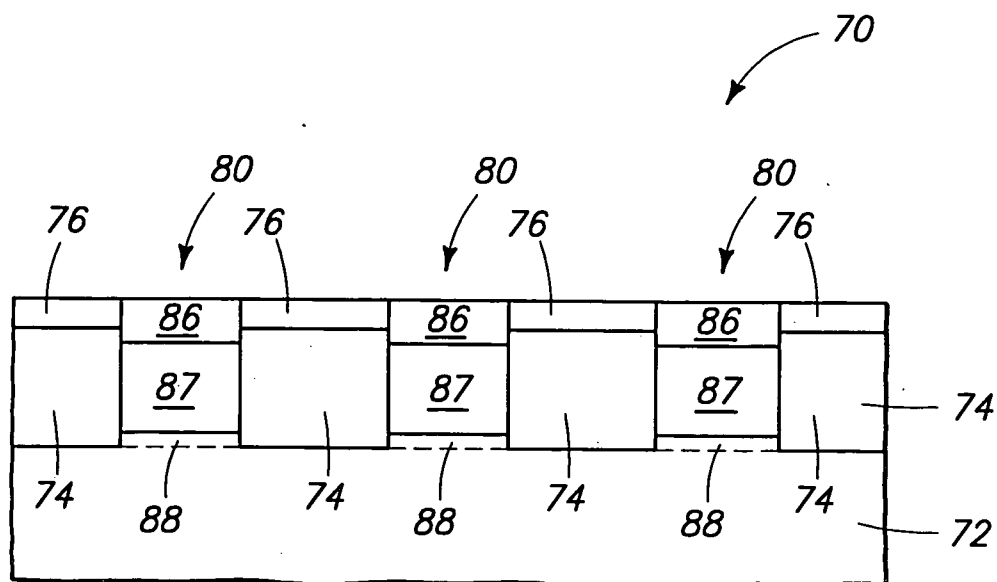
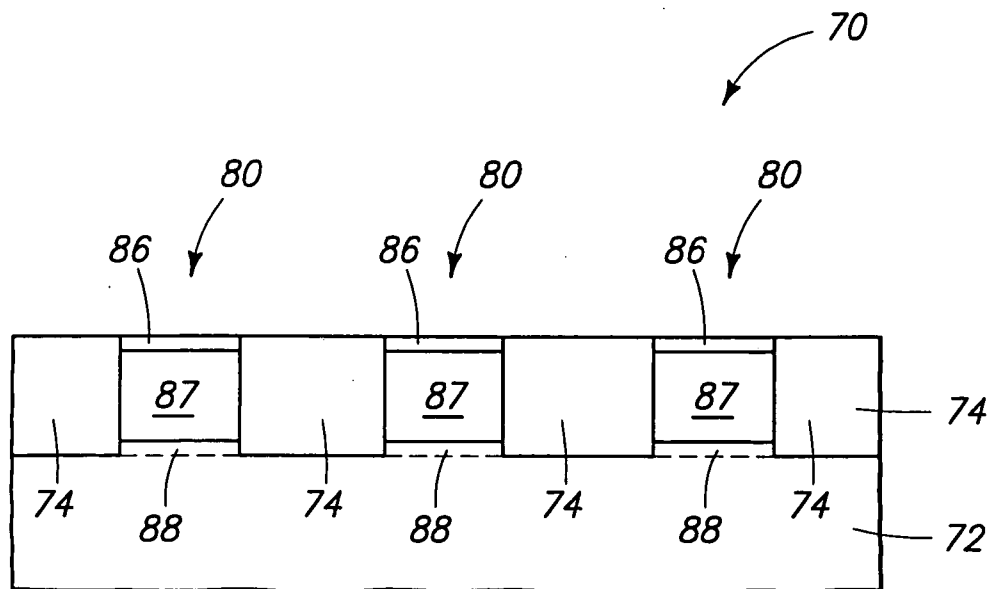
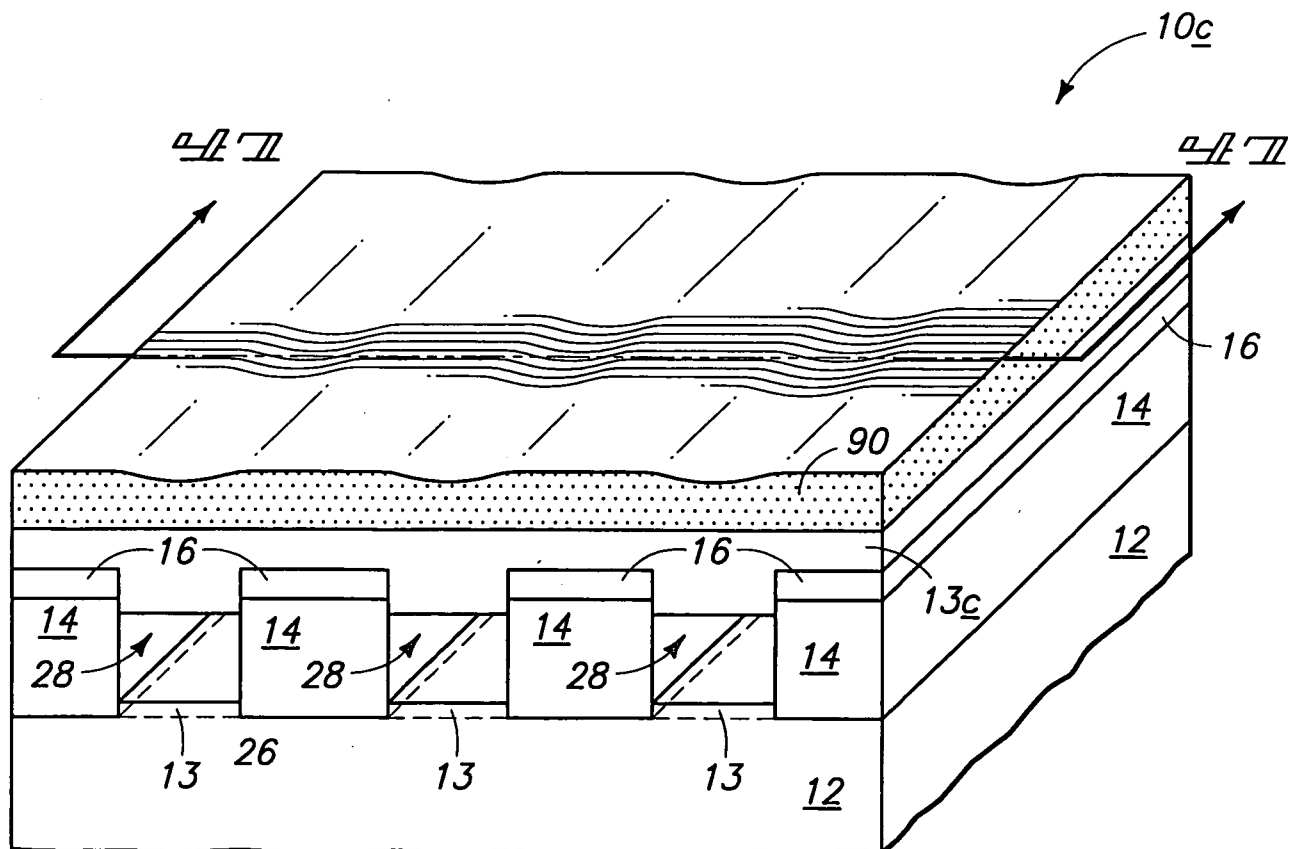


FIG. 23

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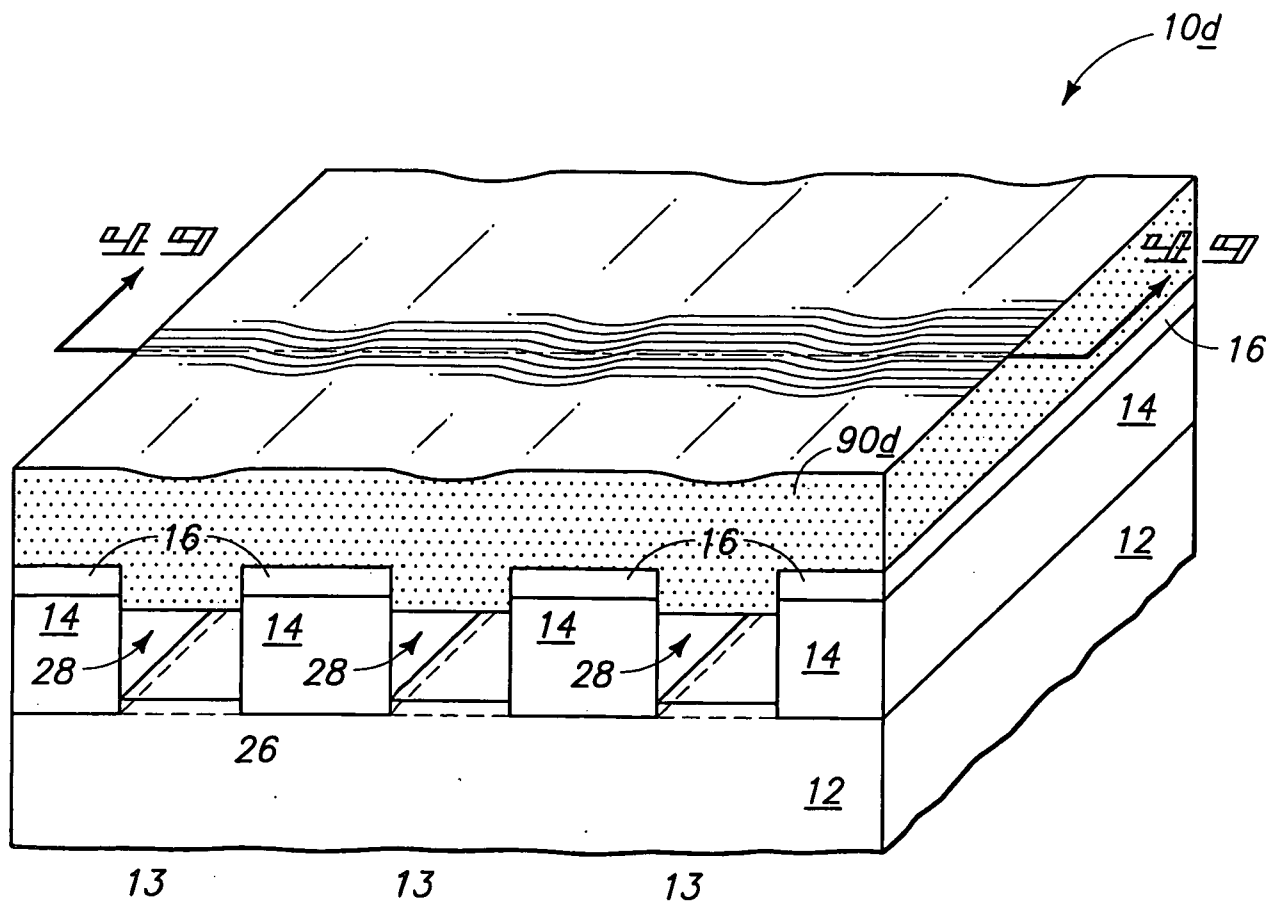
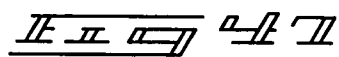
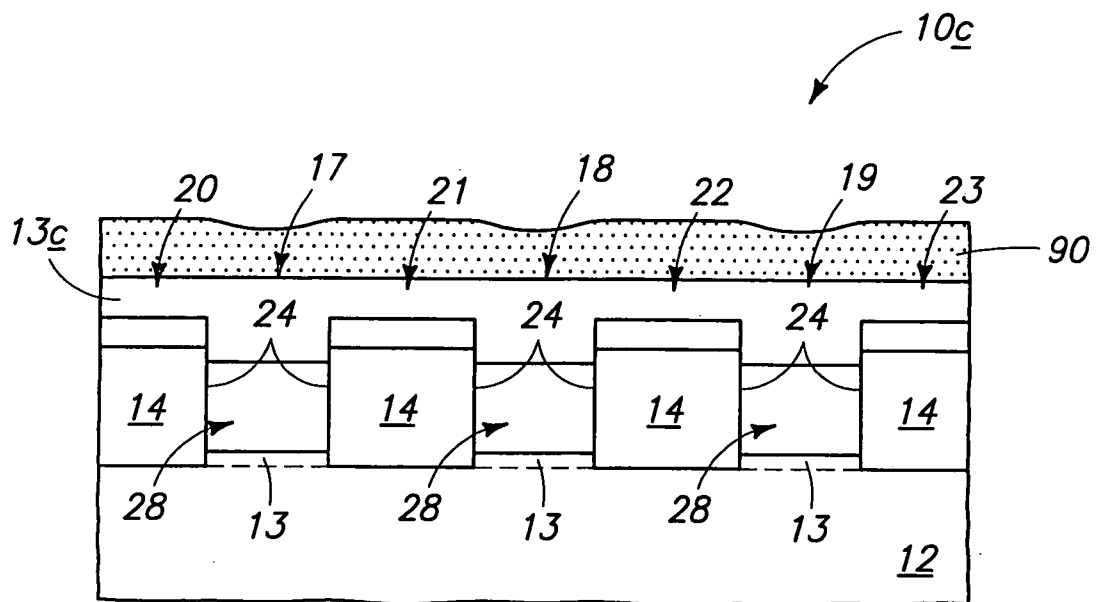


Illegals 45



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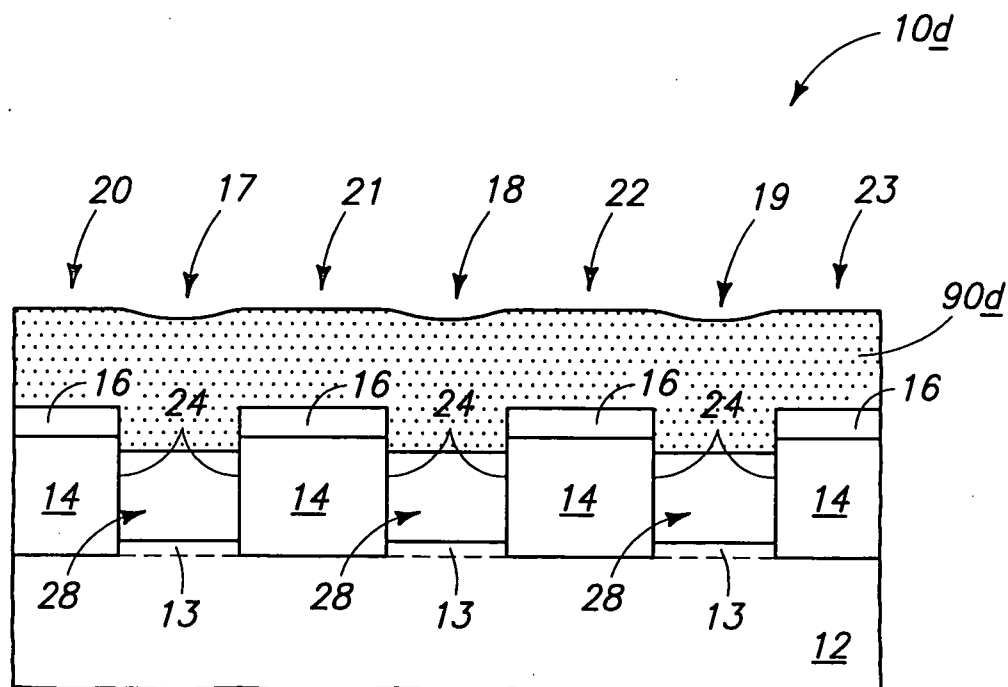


Fig. 5

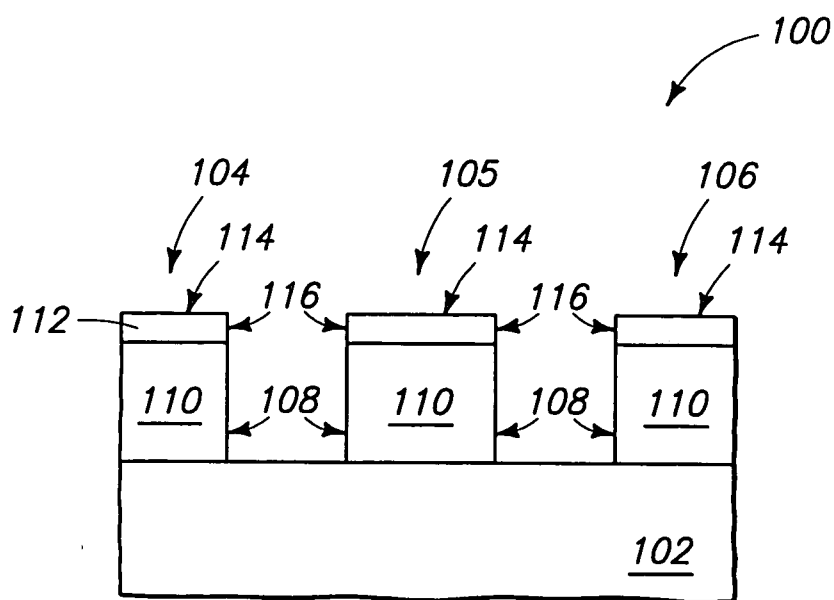


Fig. 6

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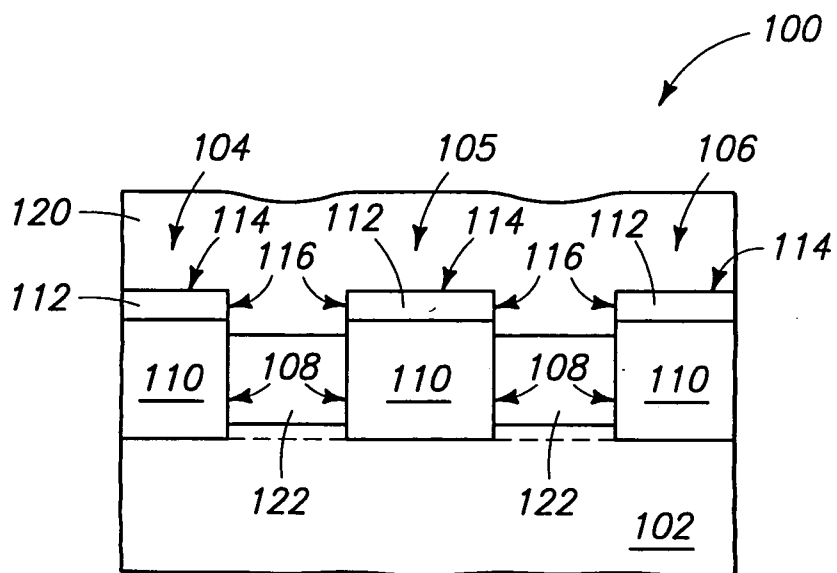


FIG. 5A

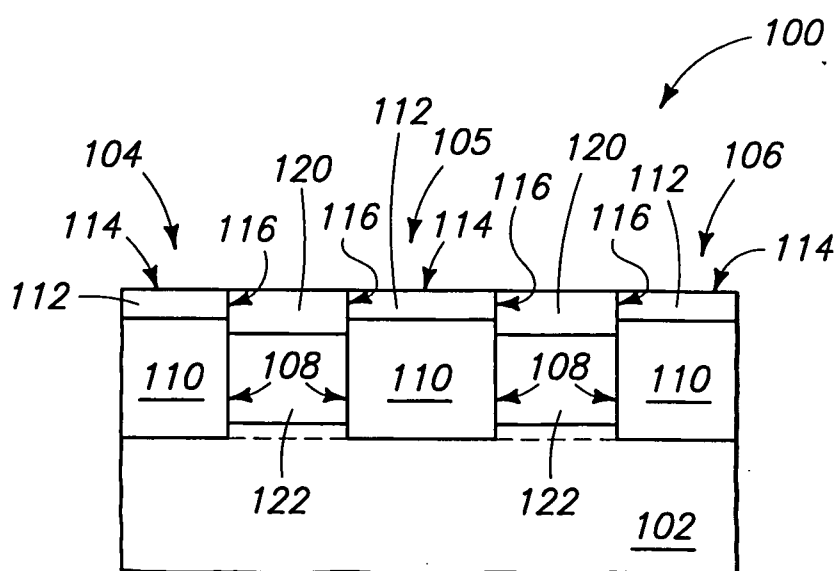


FIG. 5B

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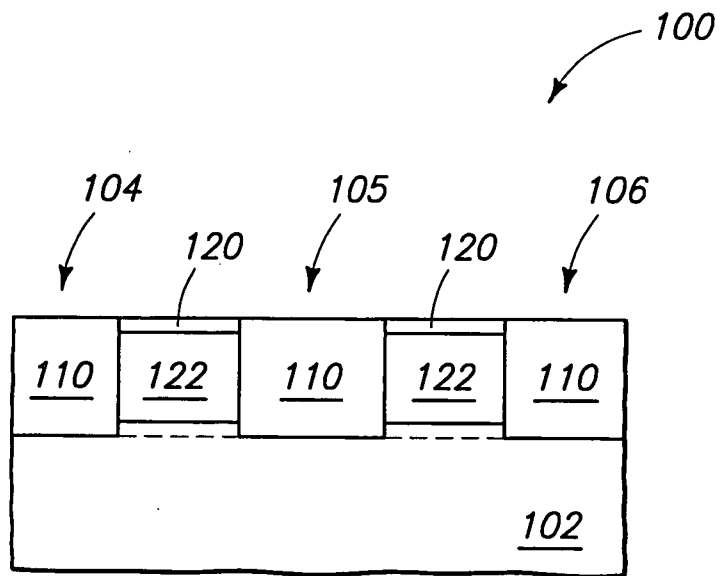


FIG. 5

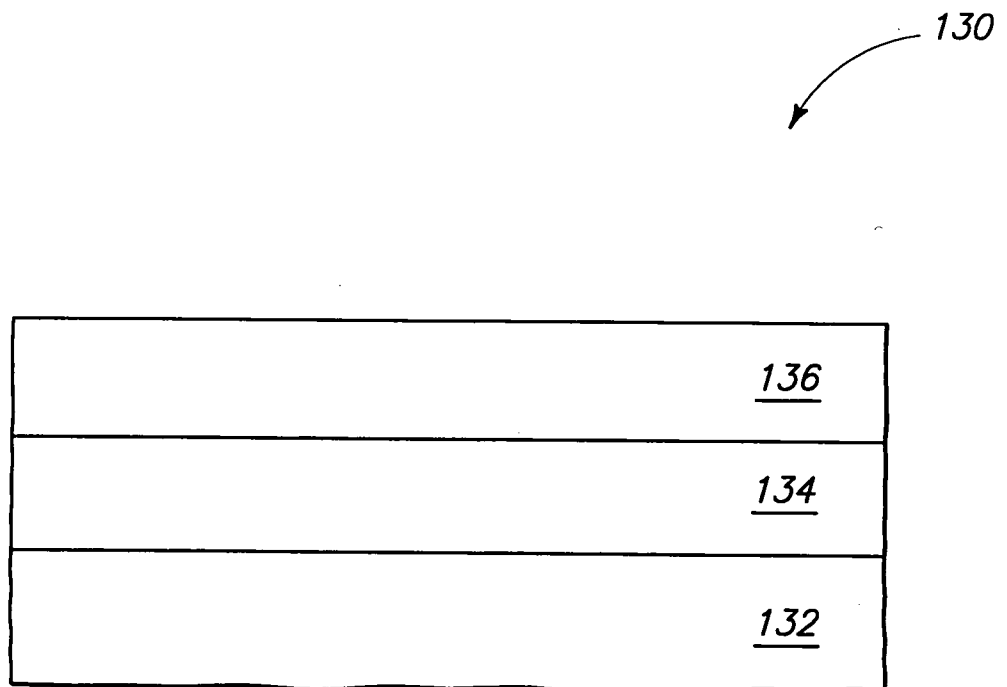
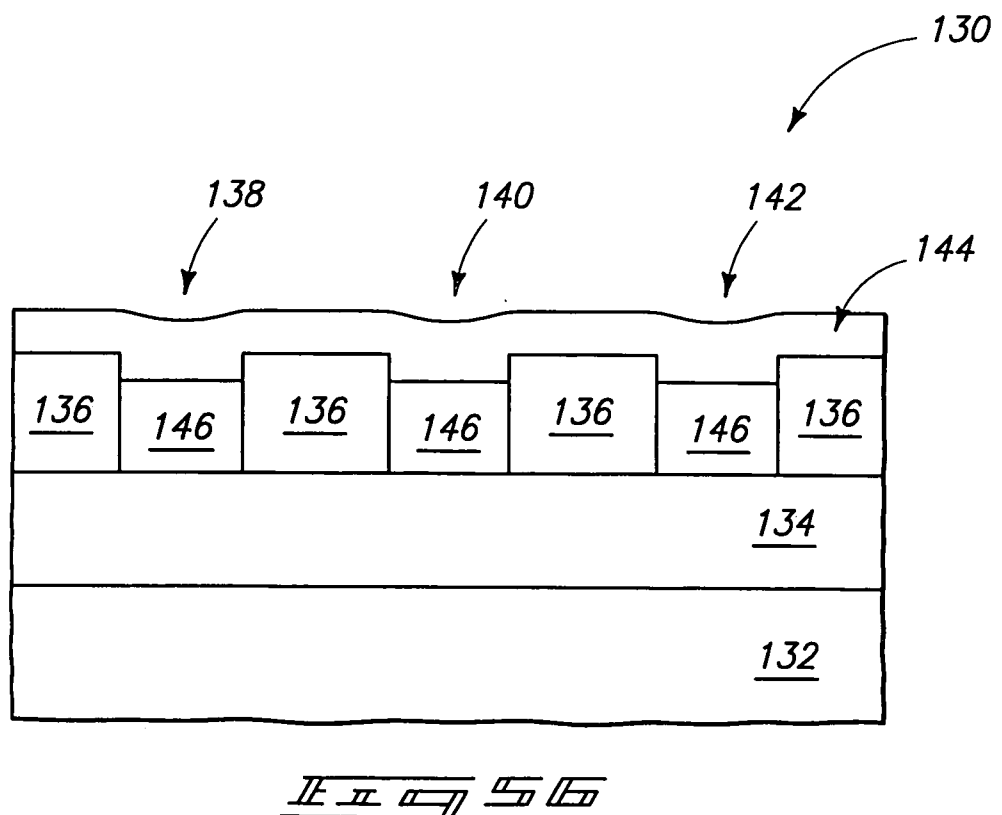
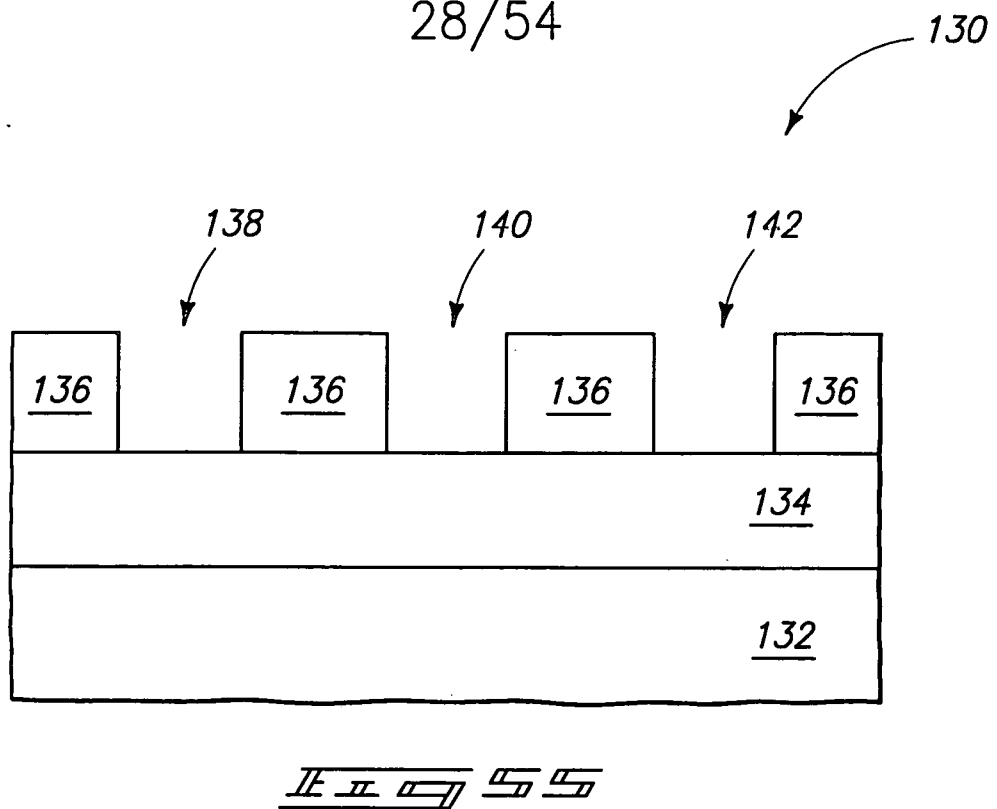
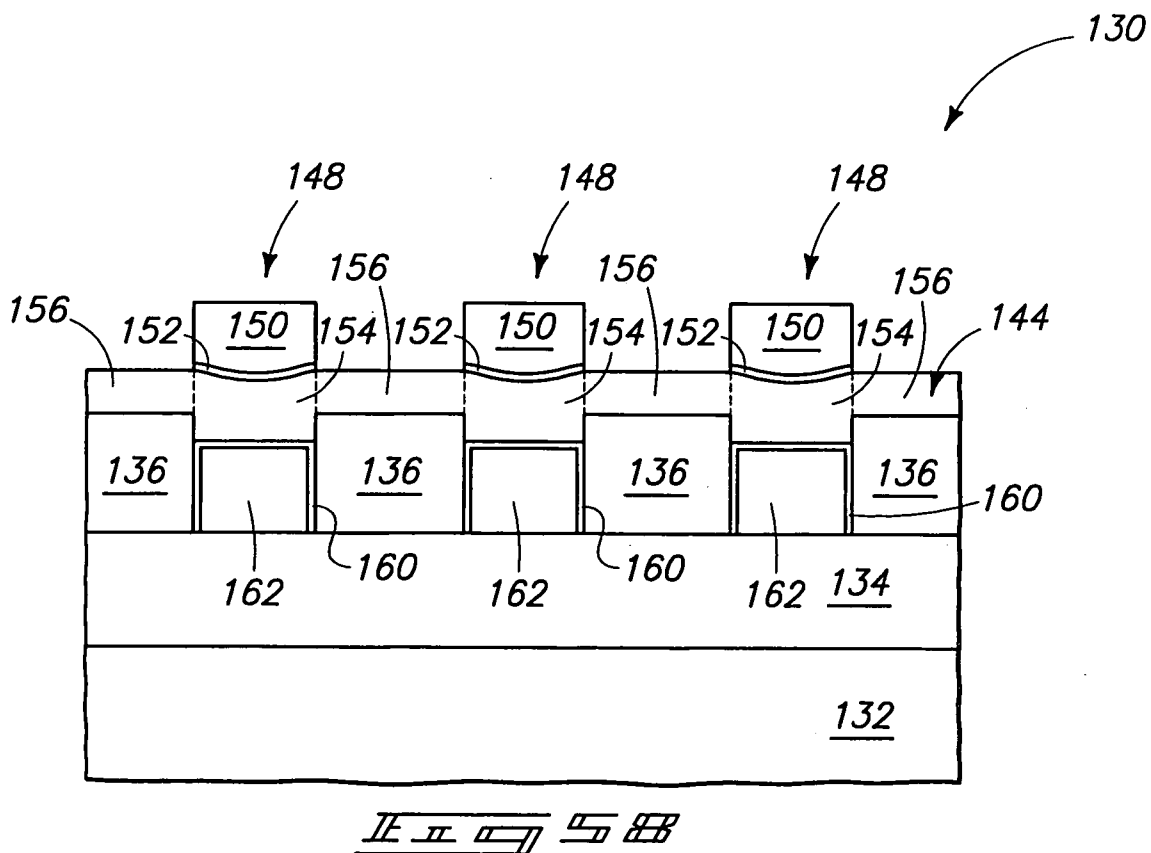
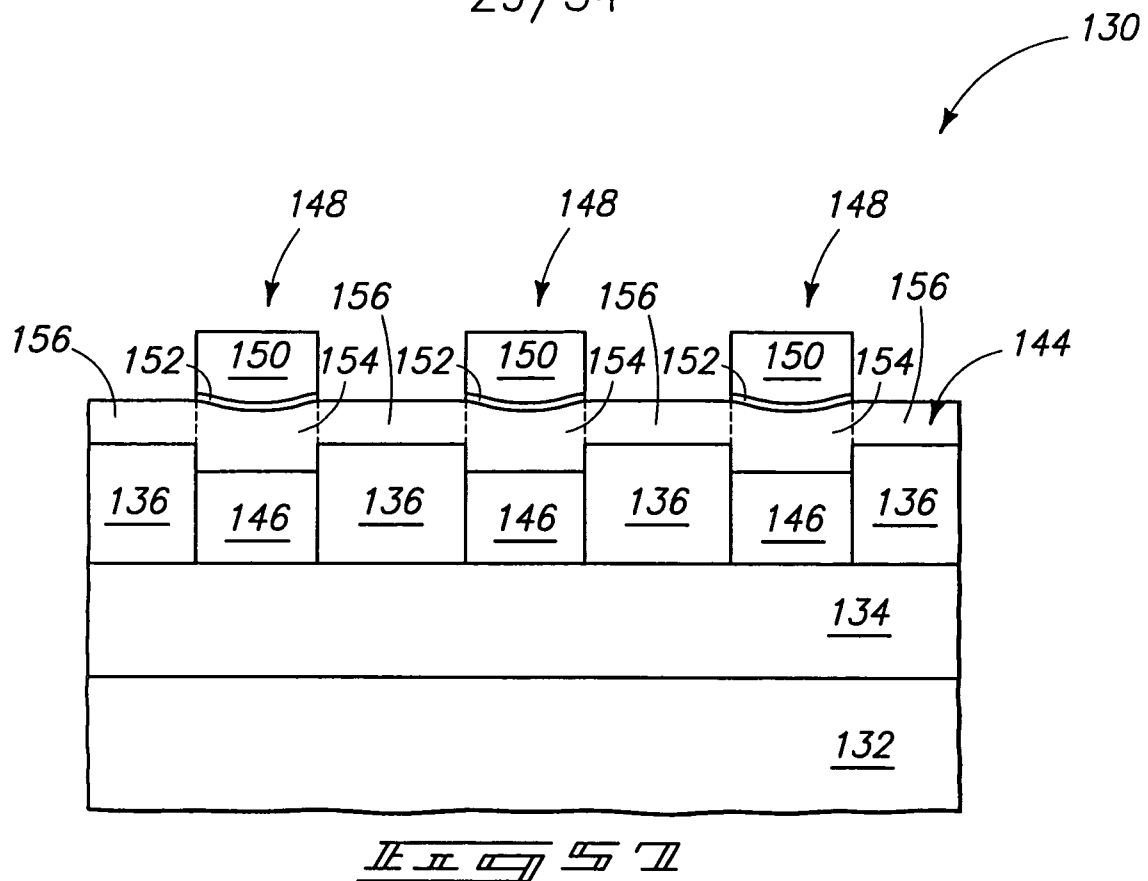


FIG. 6

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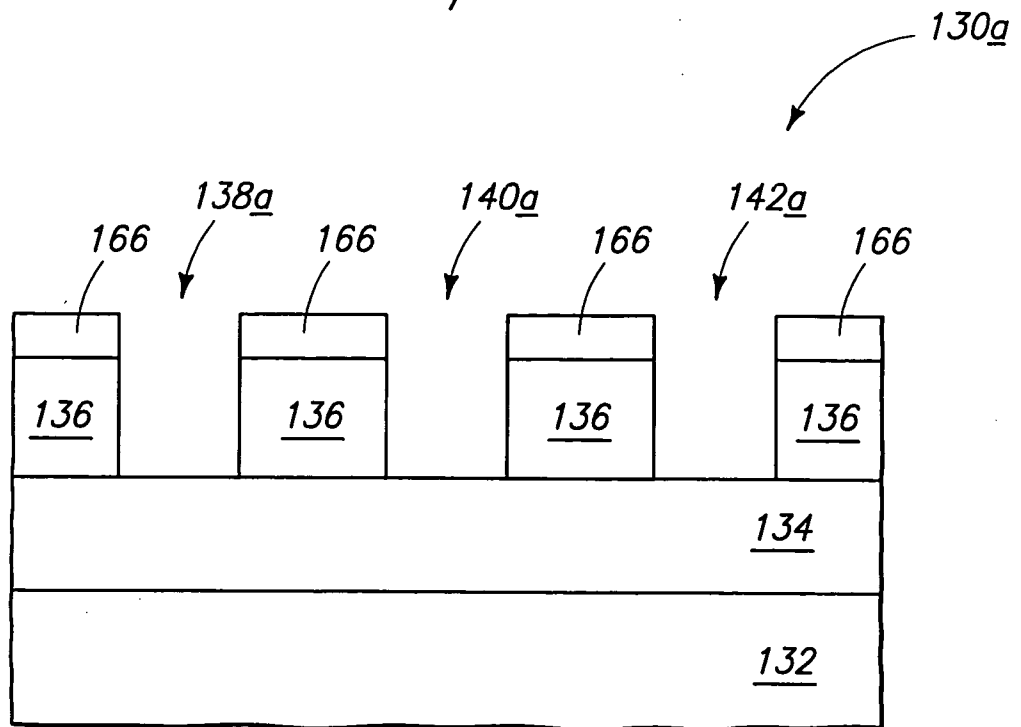


FIG. 54

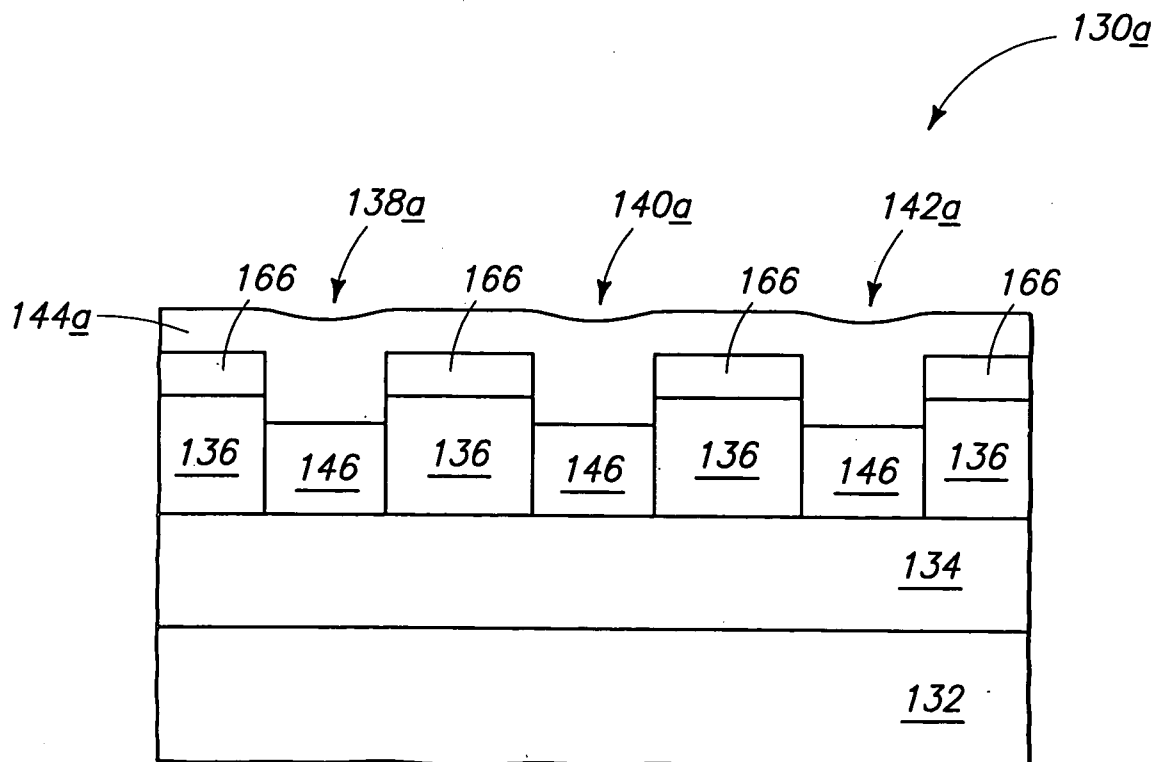
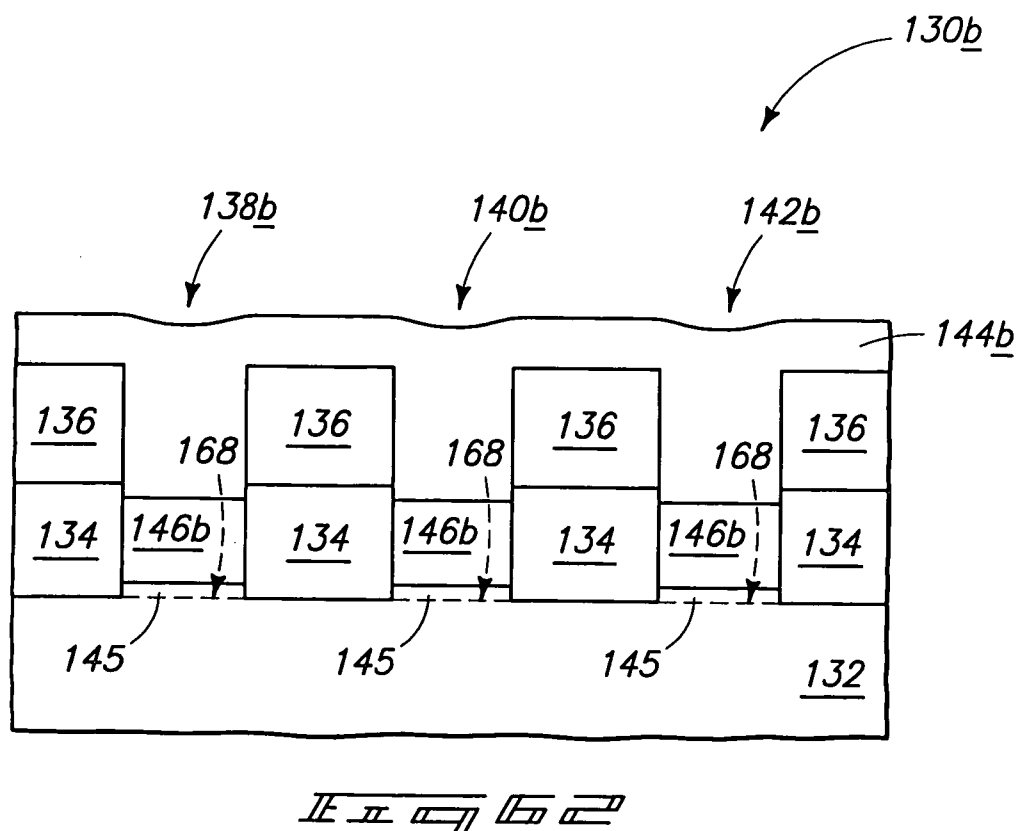
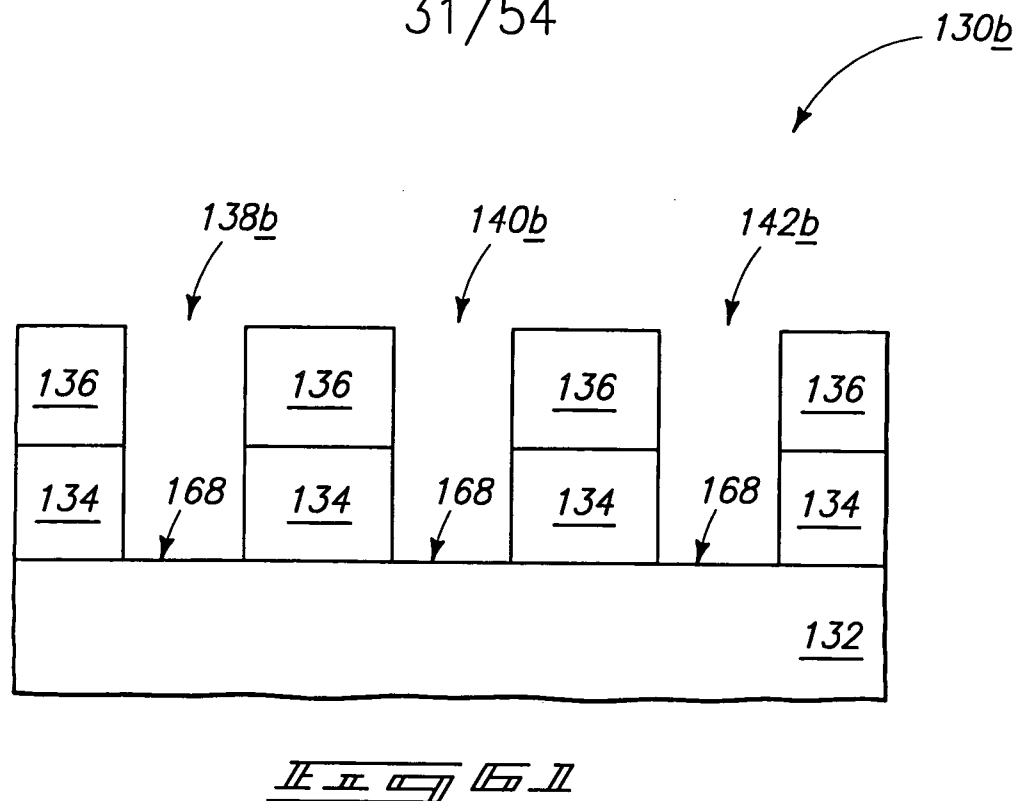


FIG. 55

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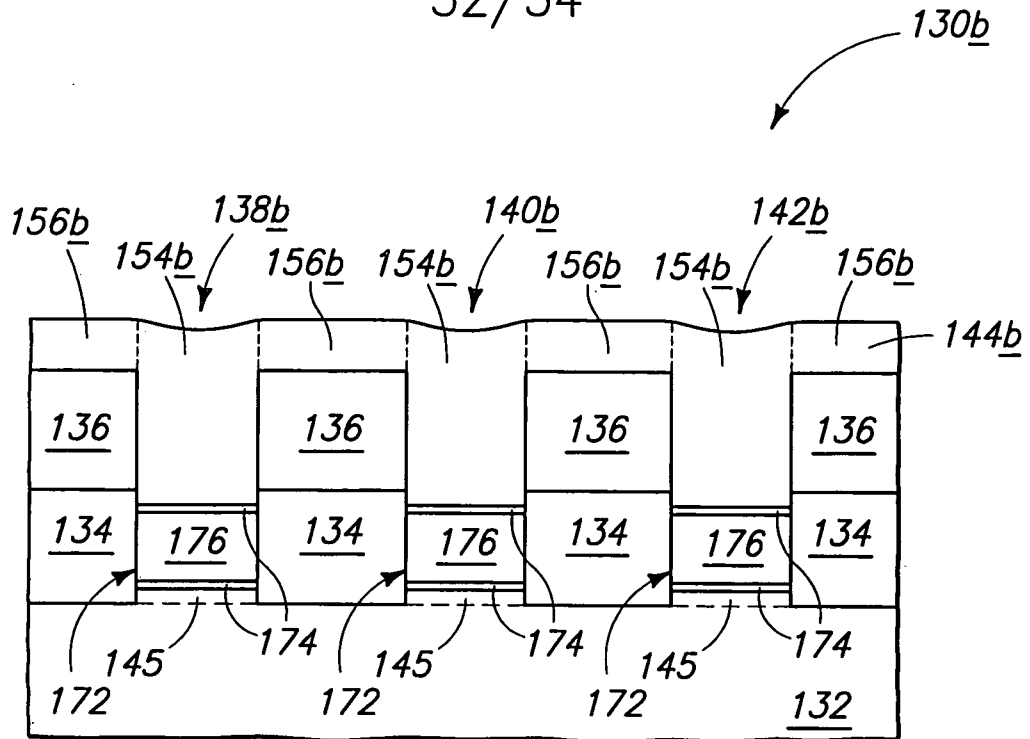


FIG. 3

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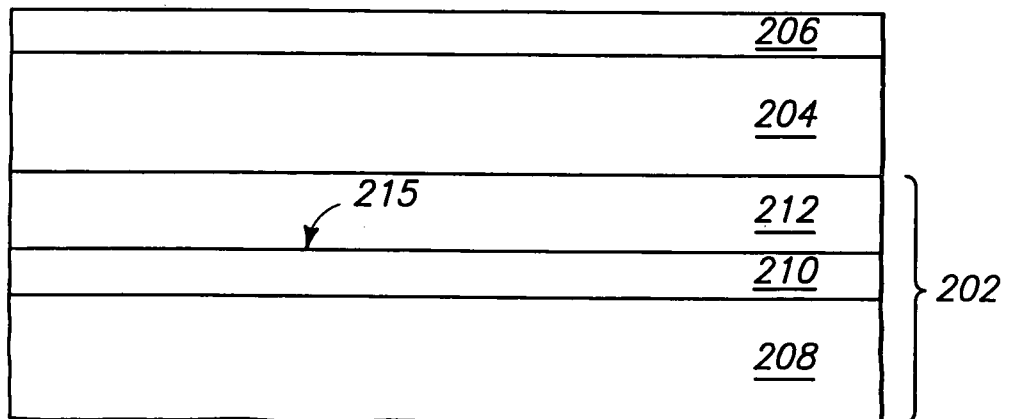


FIG. 4

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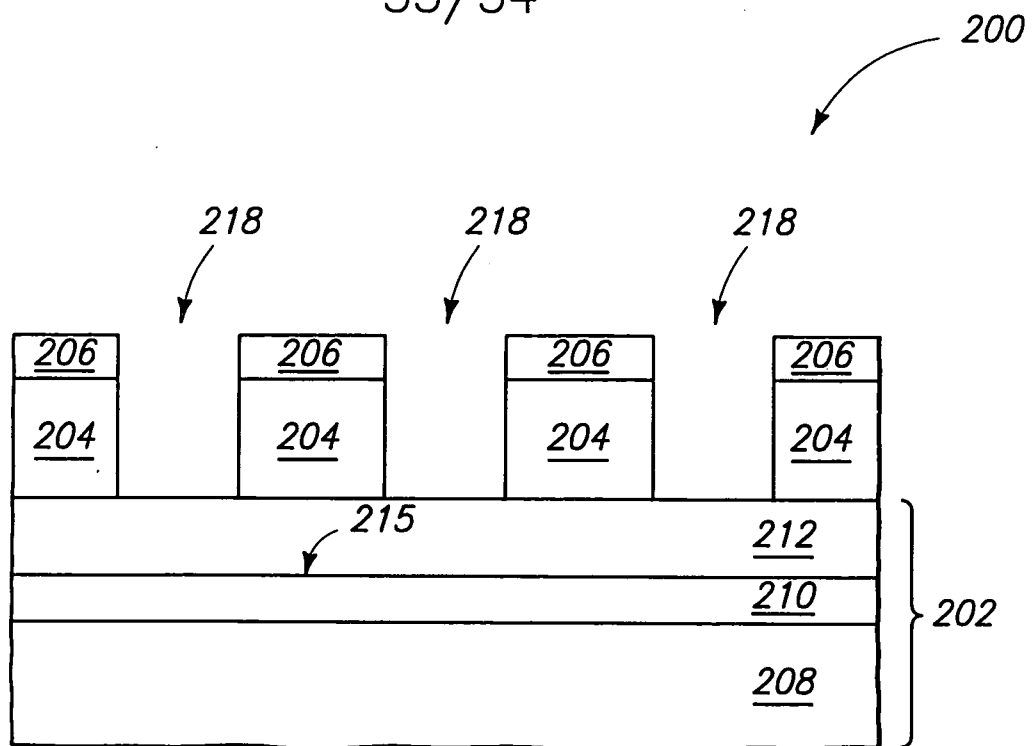


FIG. 5

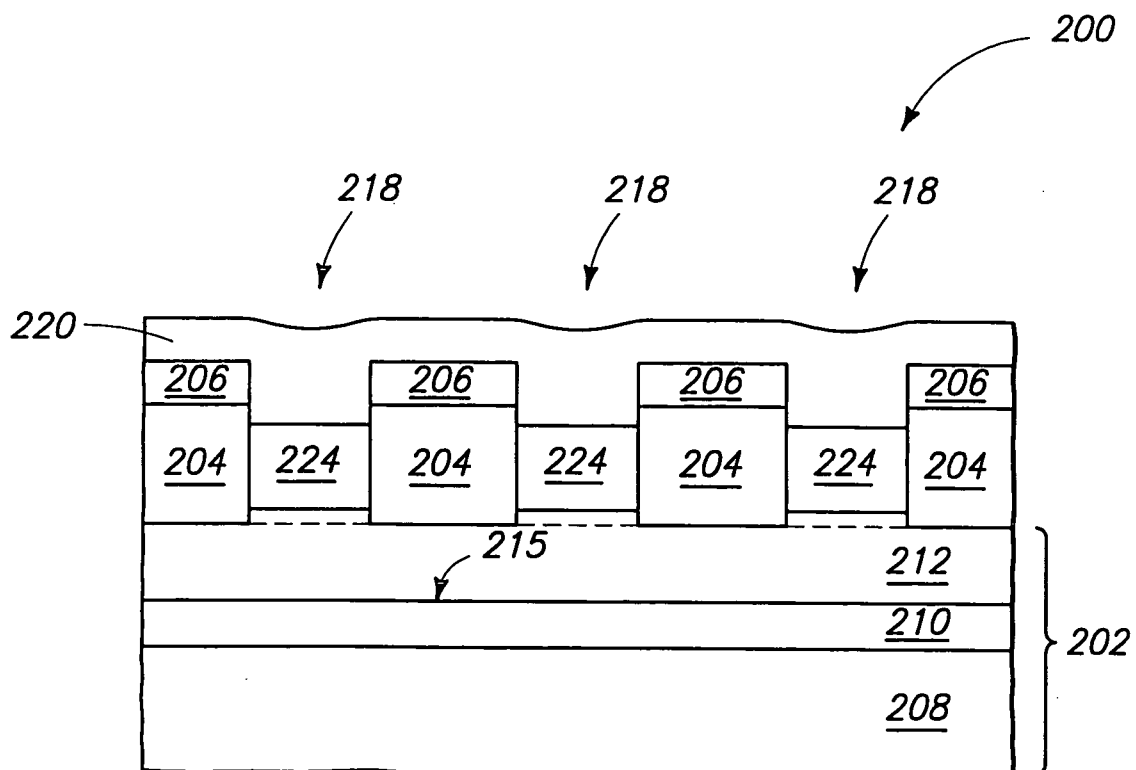
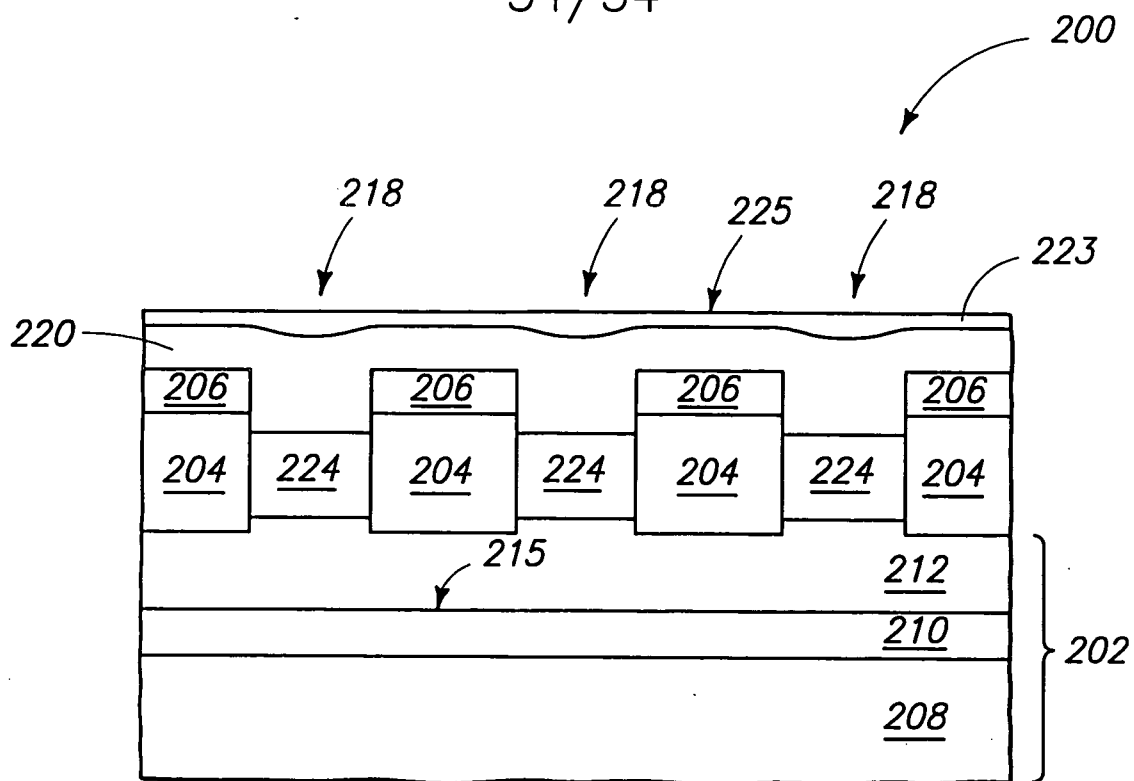
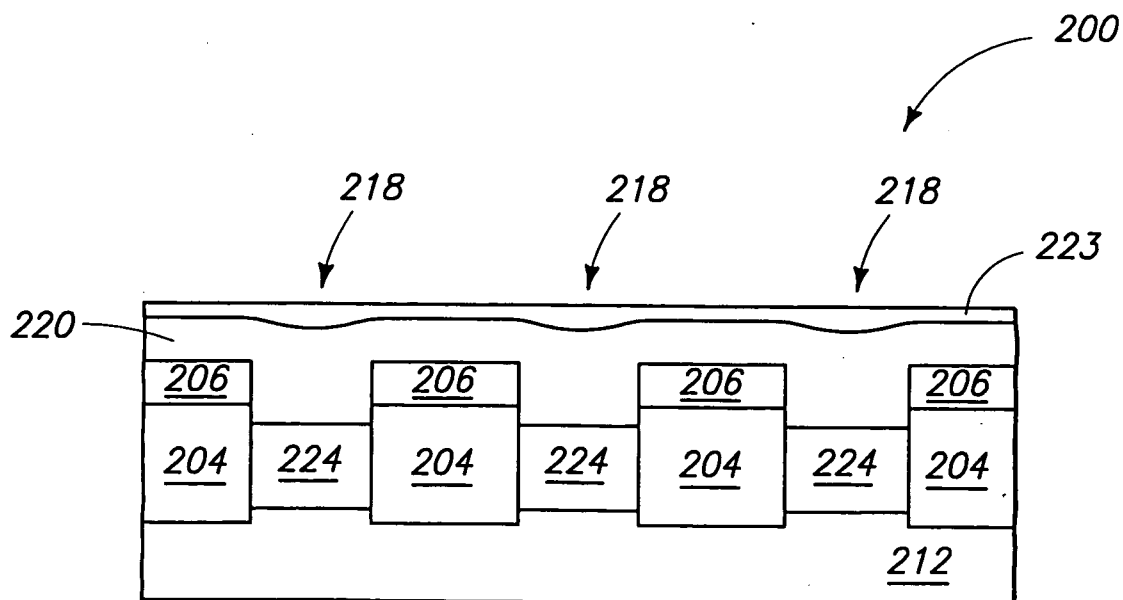


FIG. 6

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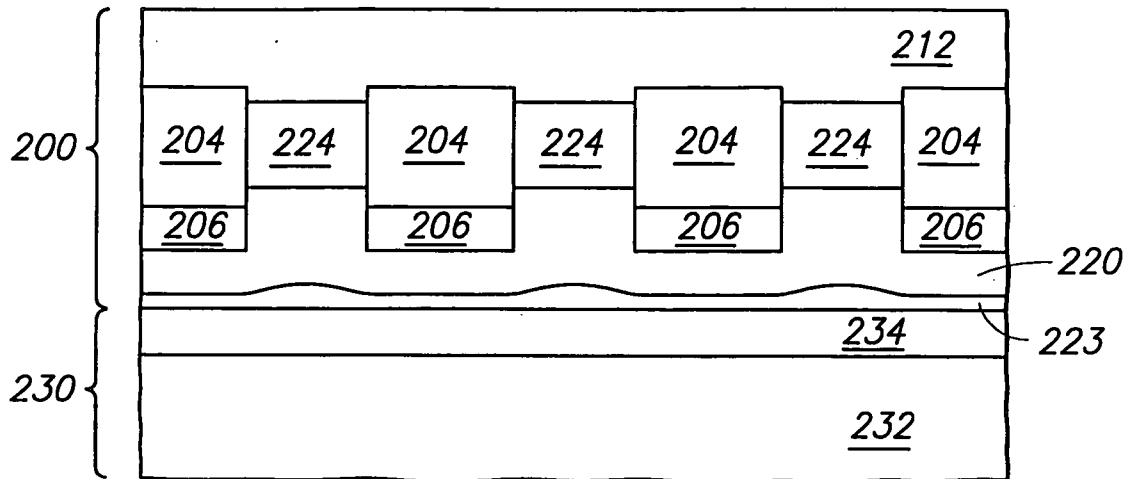


II II II II II

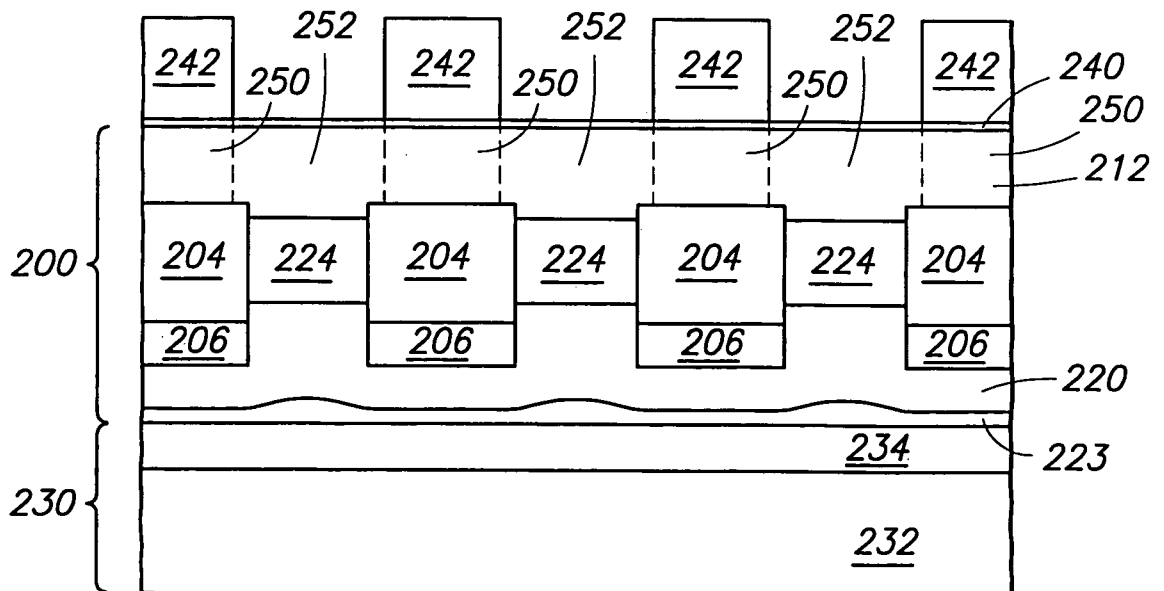


II II II II II

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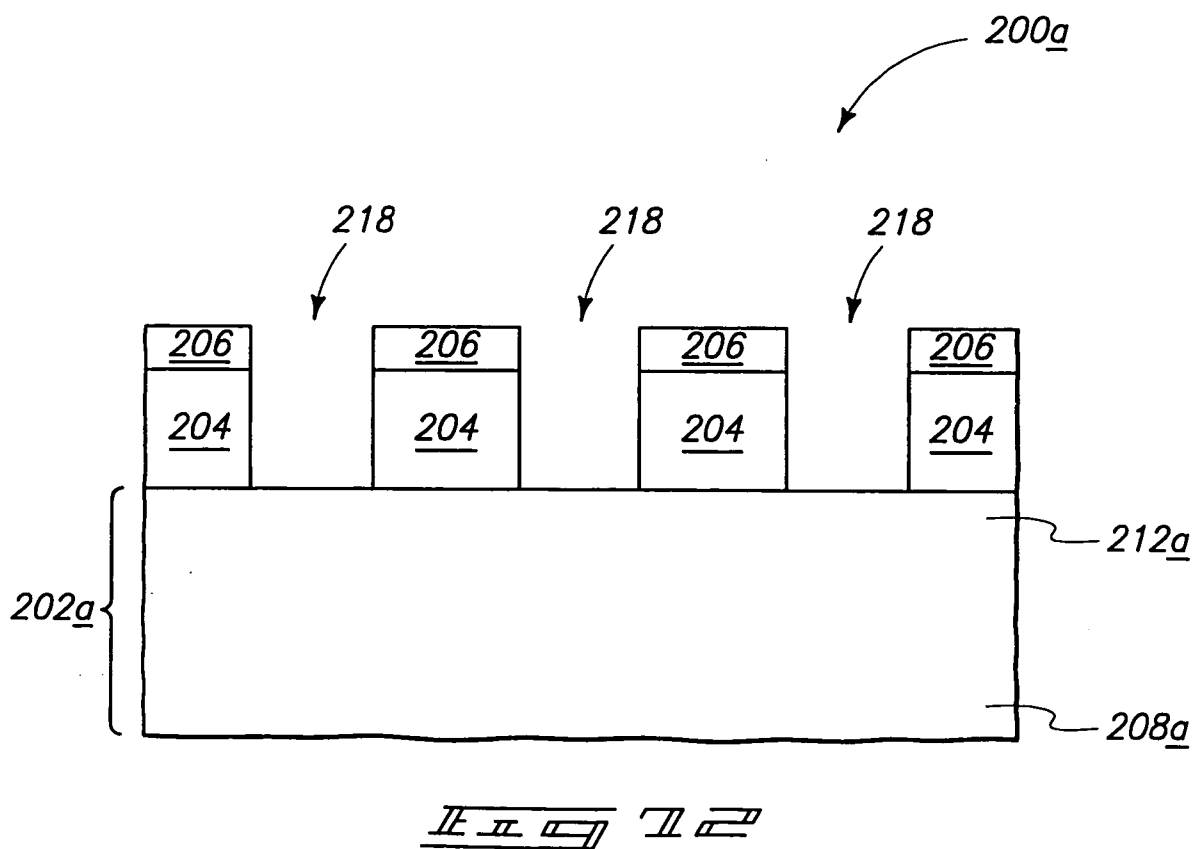
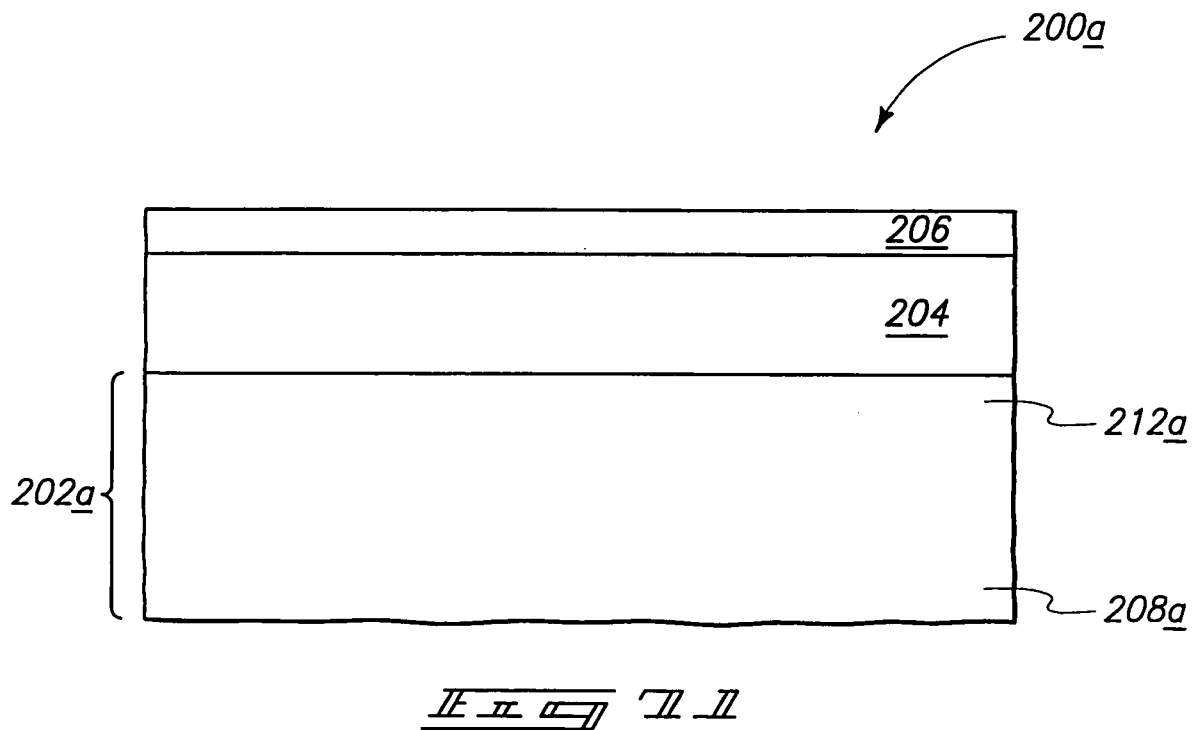


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II II III III

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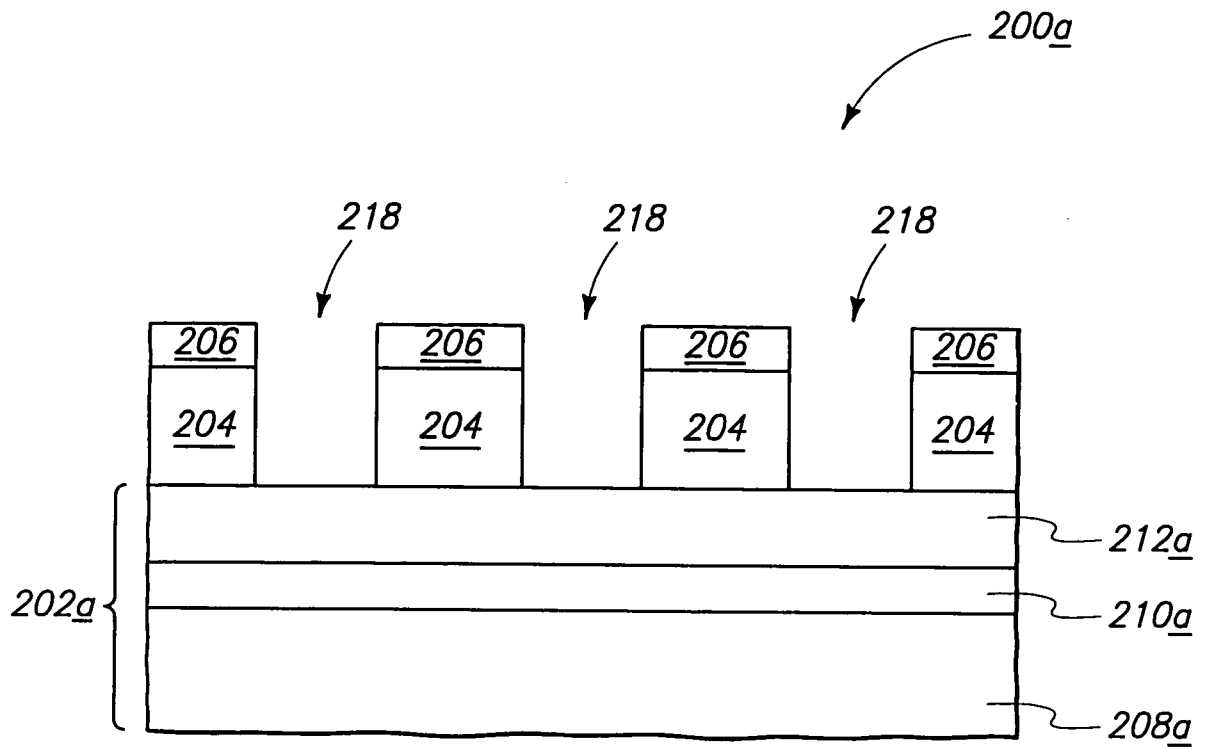
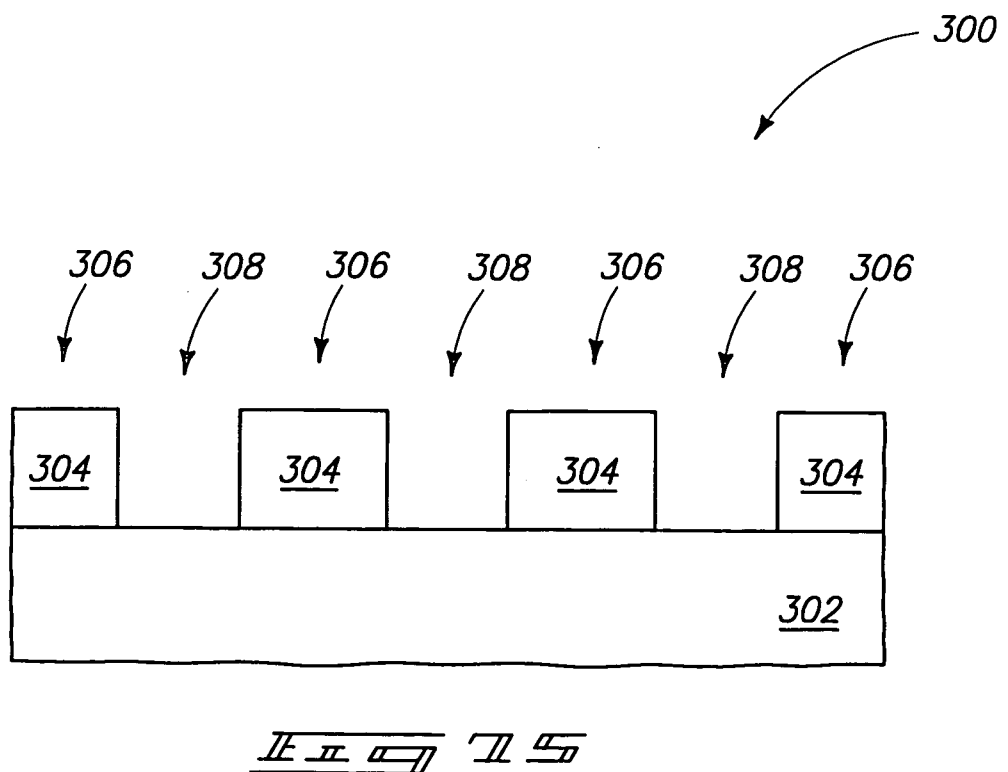
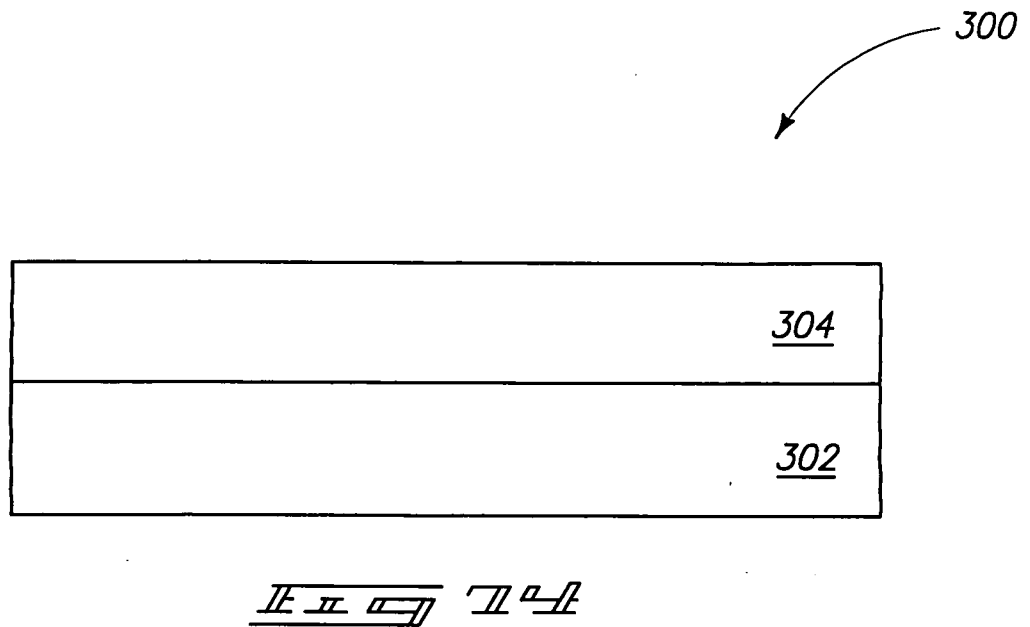


FIG. 37

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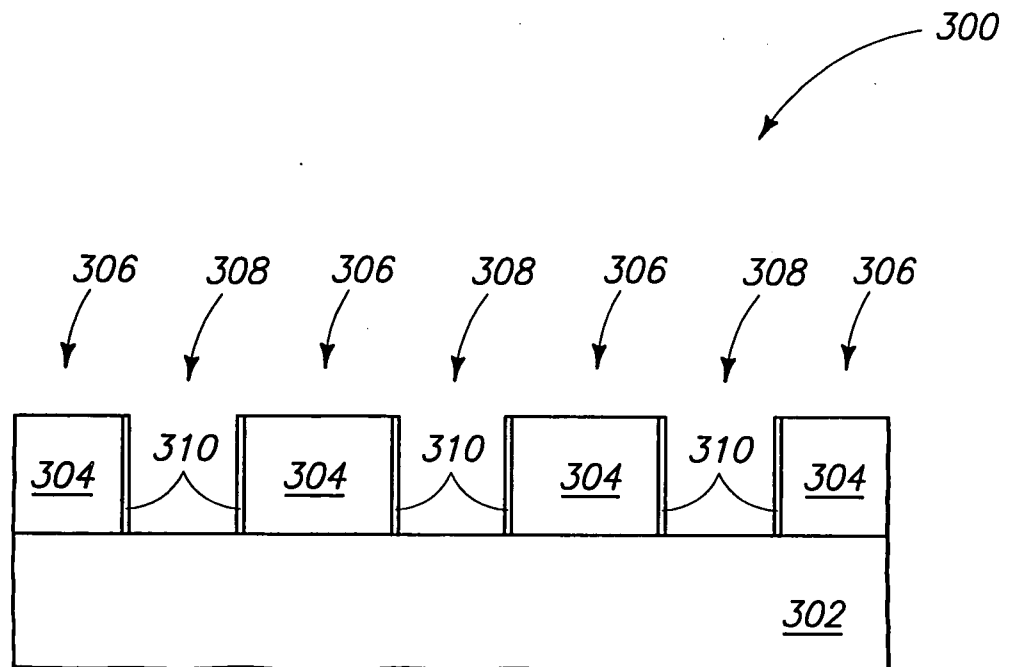


FIG. 1

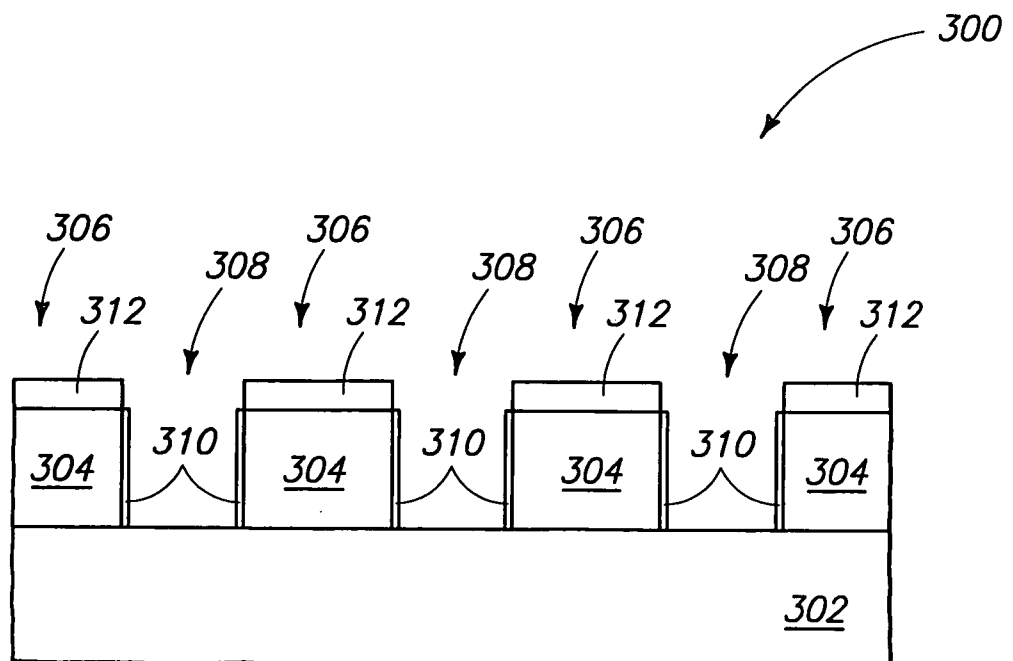
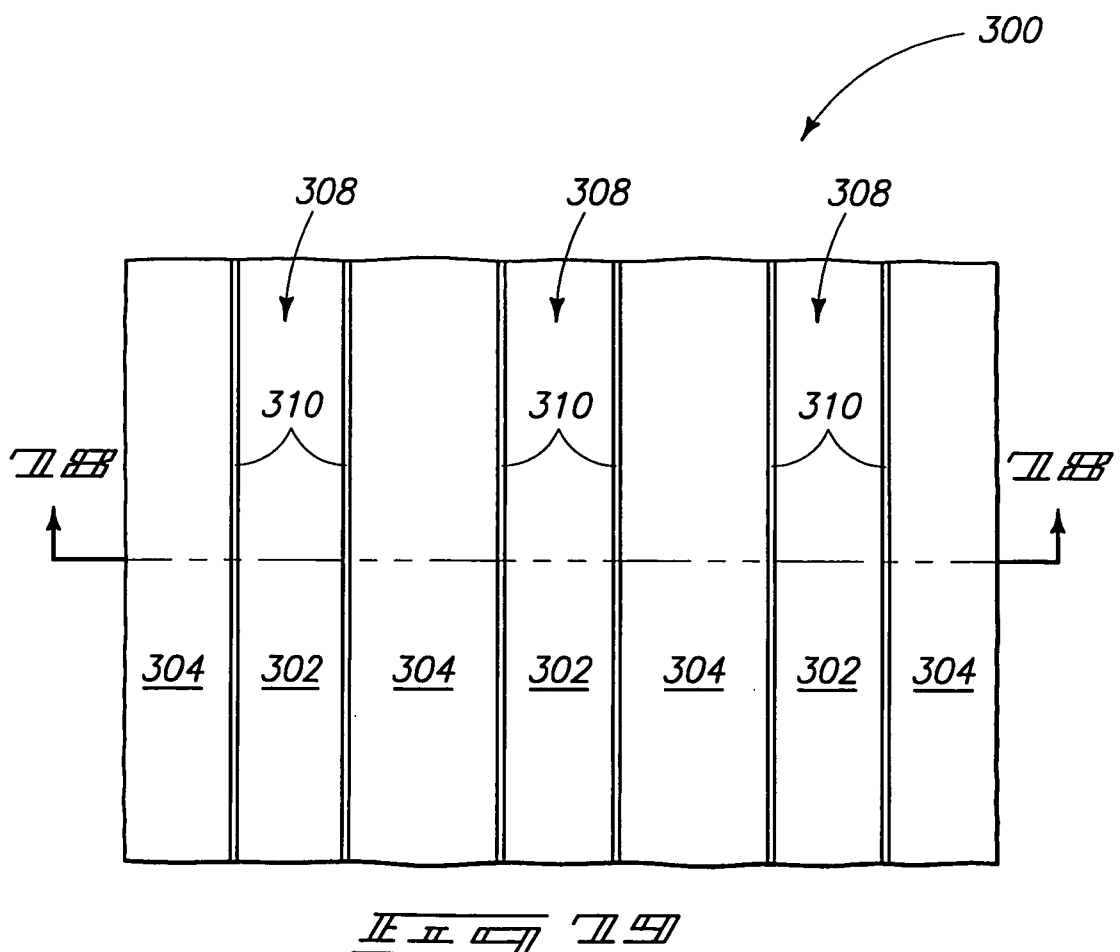
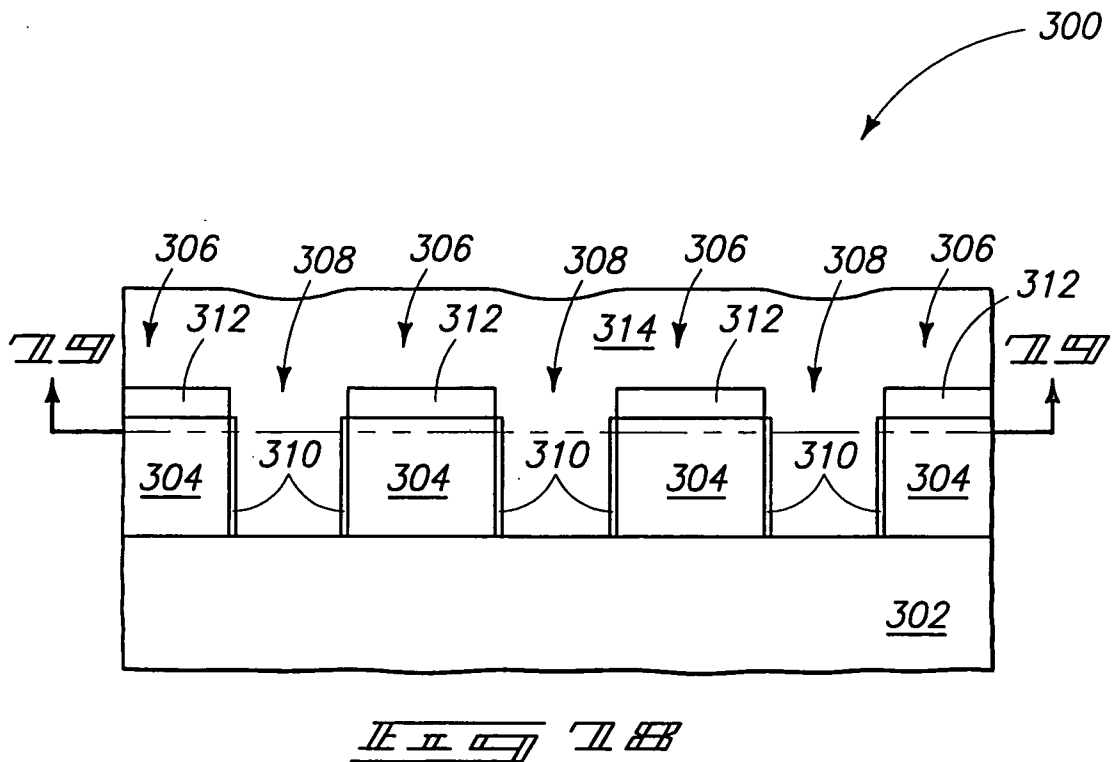


FIG. 2

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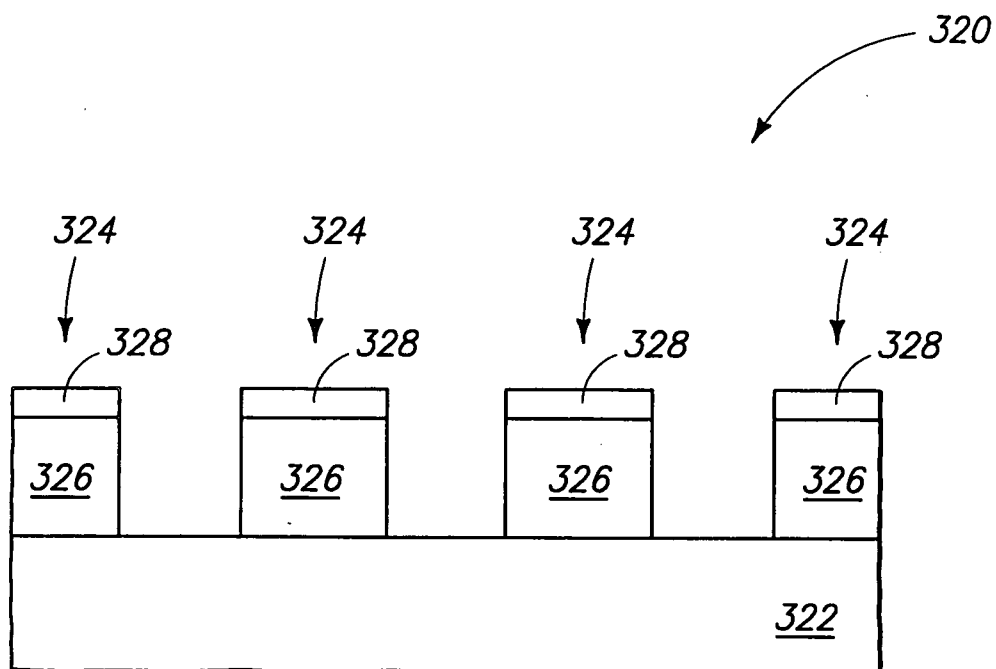


FIG. 41 FIG. 42

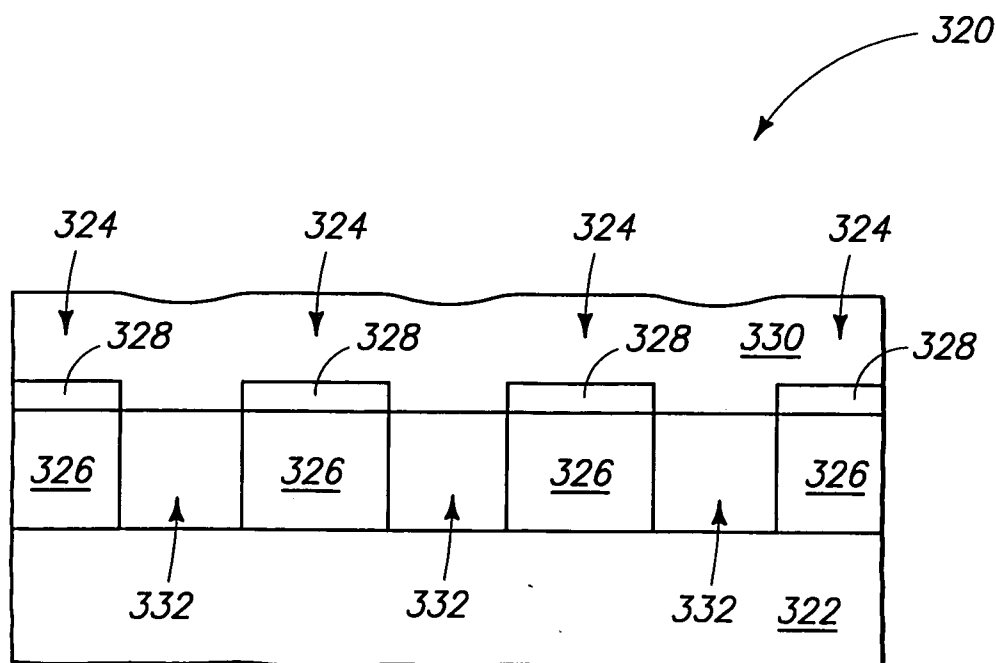
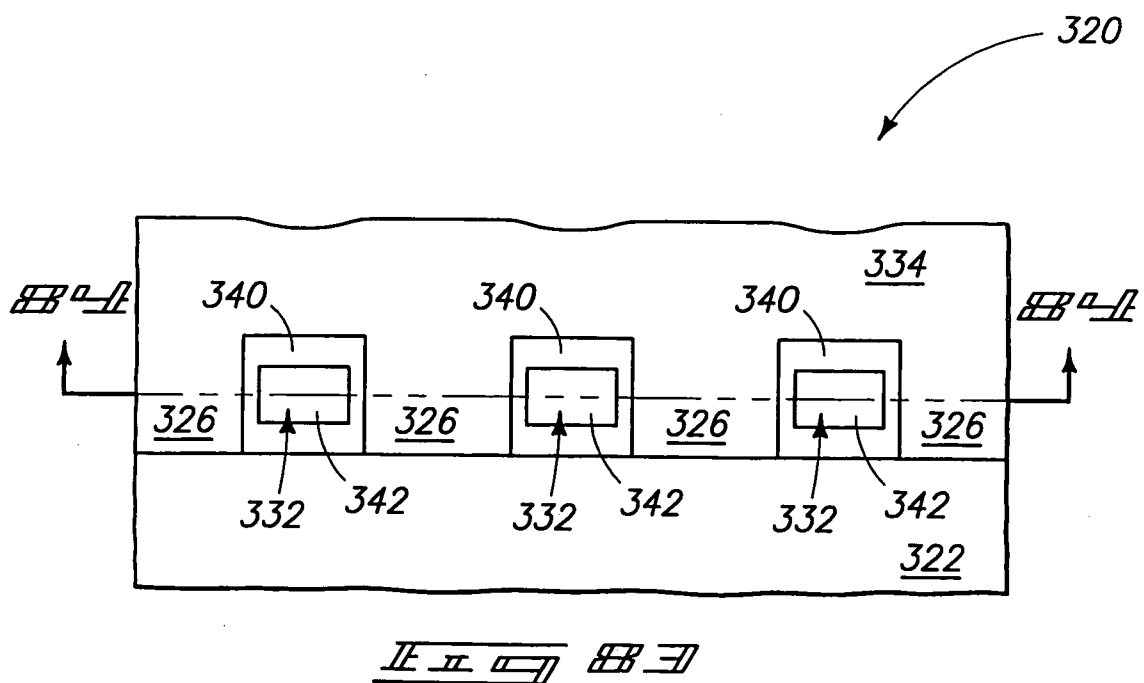
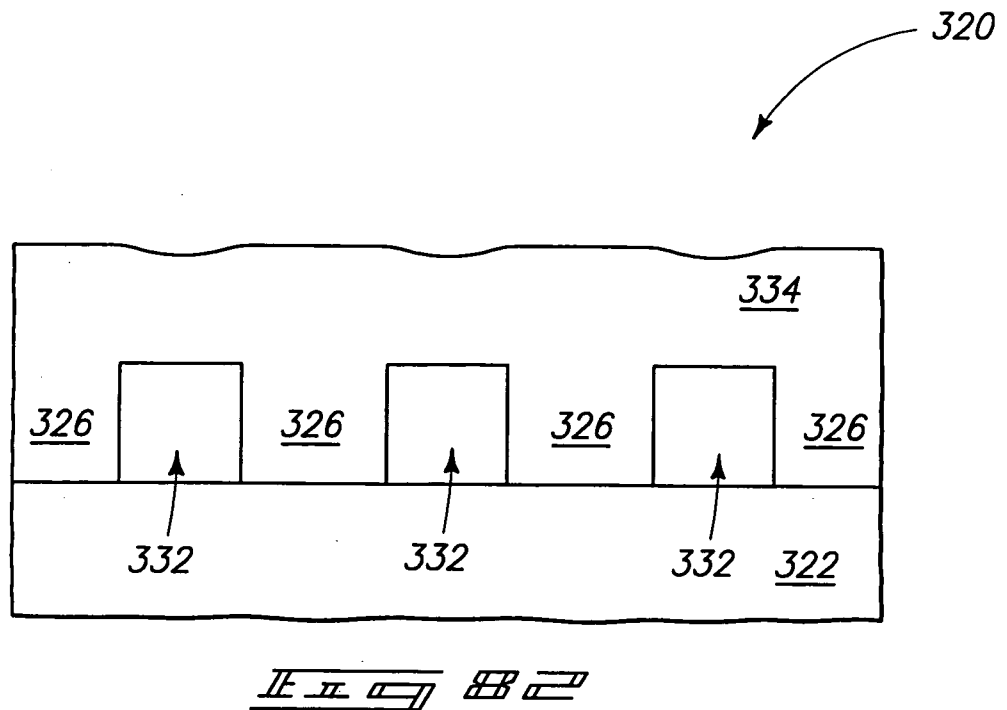
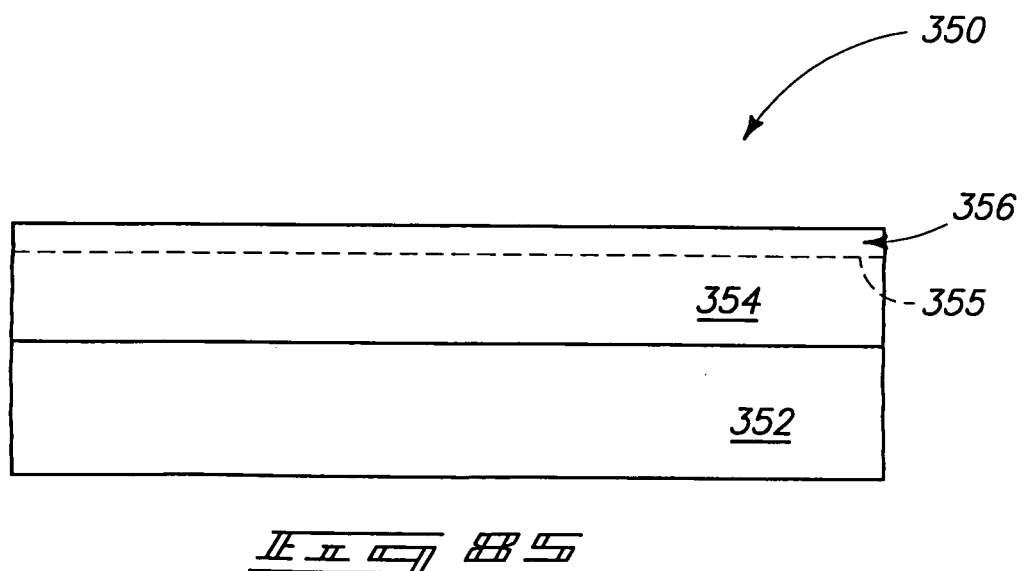
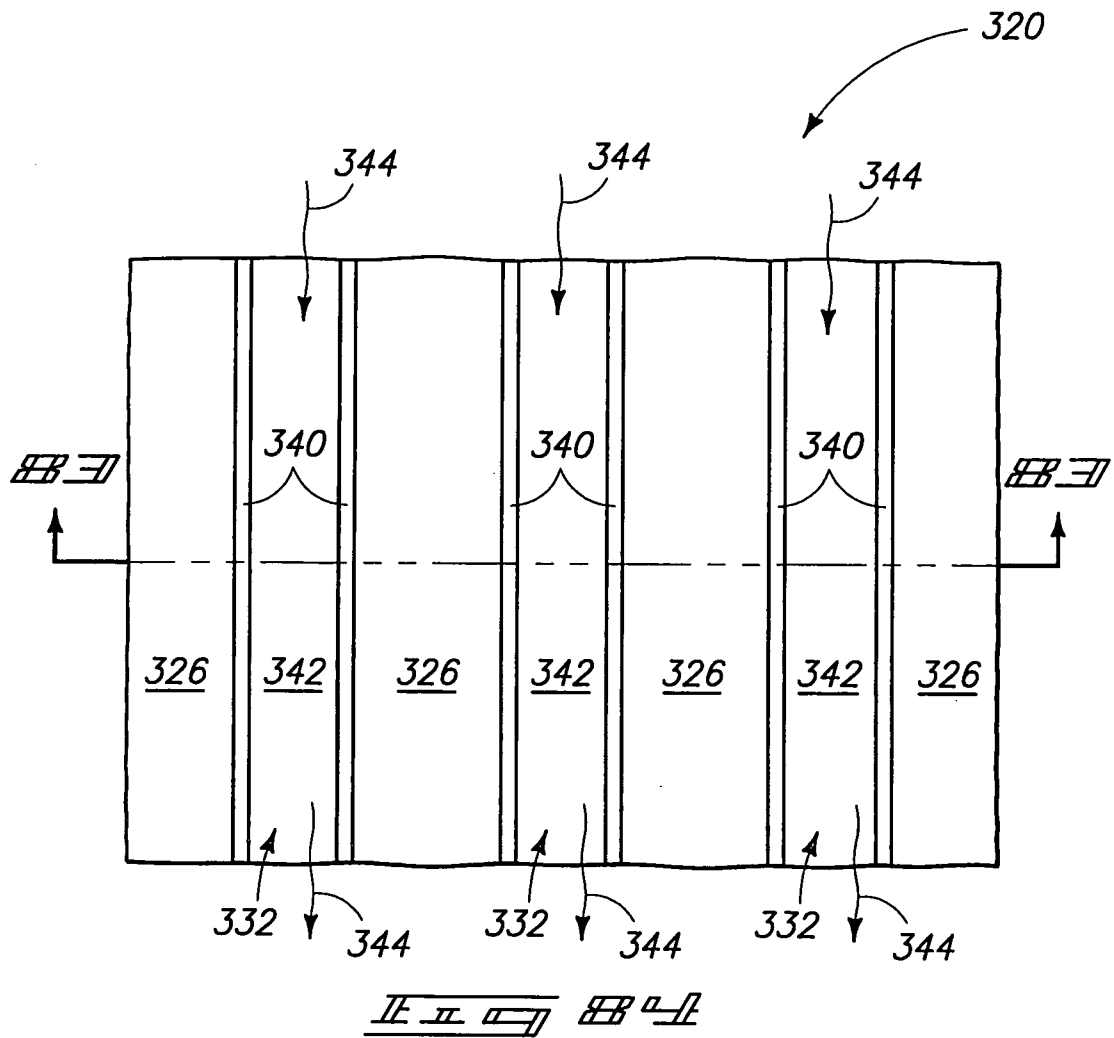


FIG. 43 FIG. 44

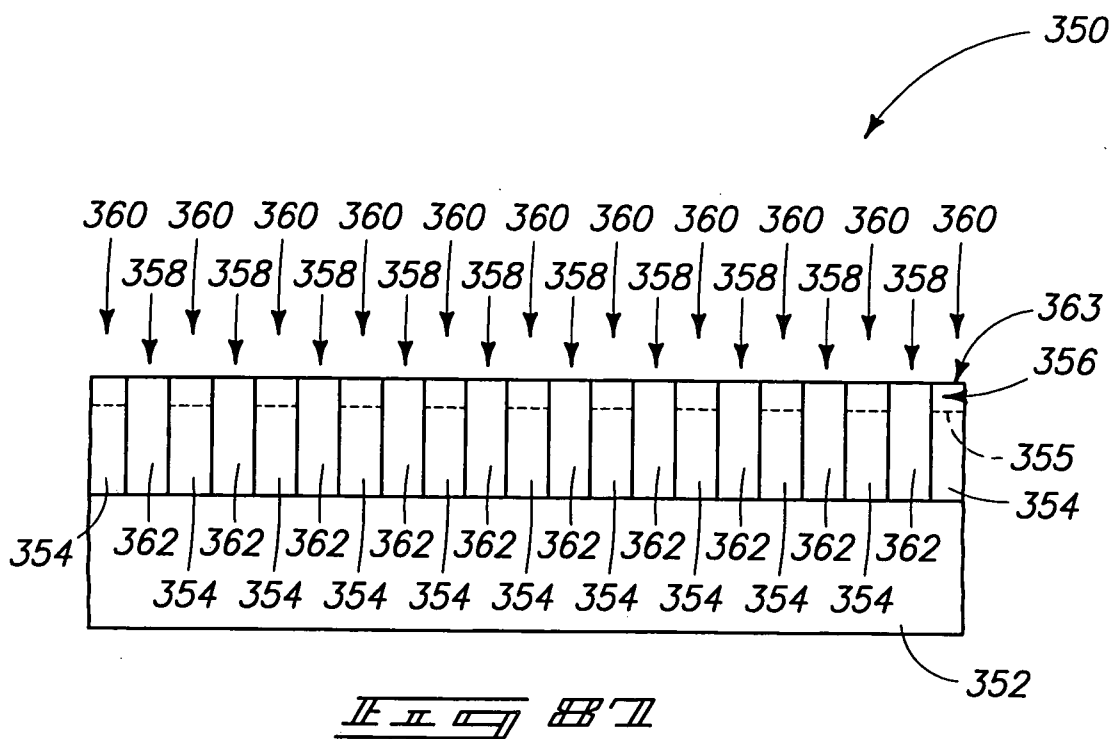
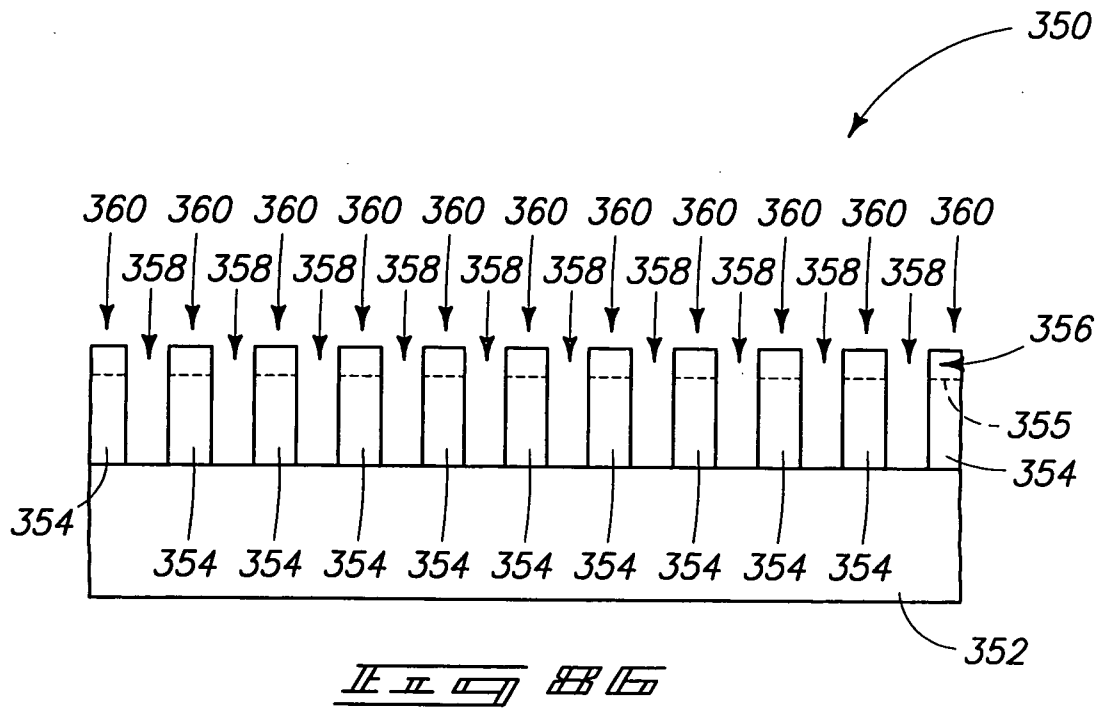
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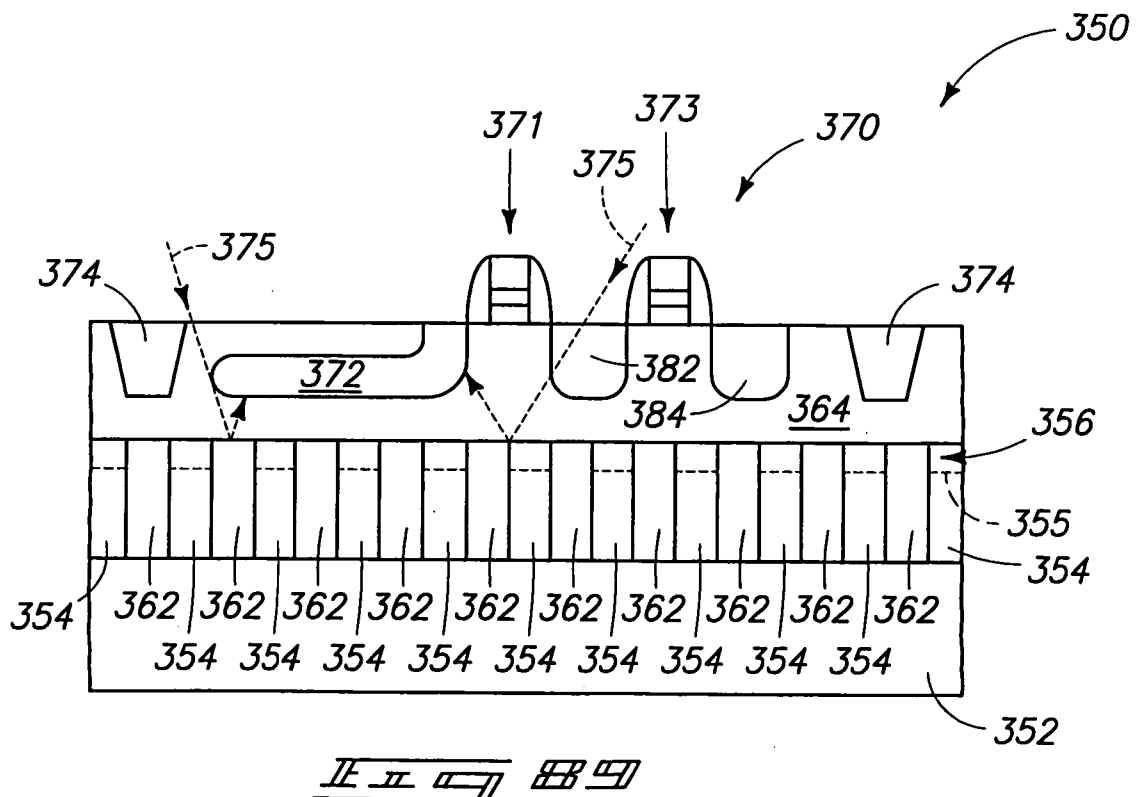
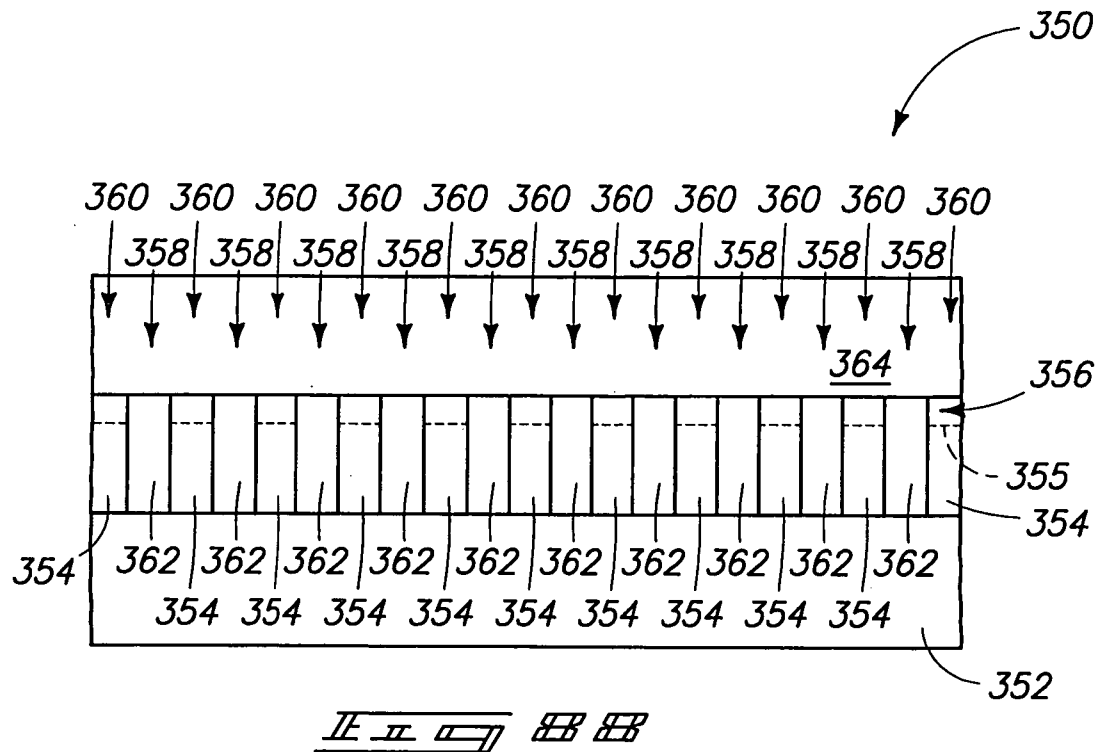
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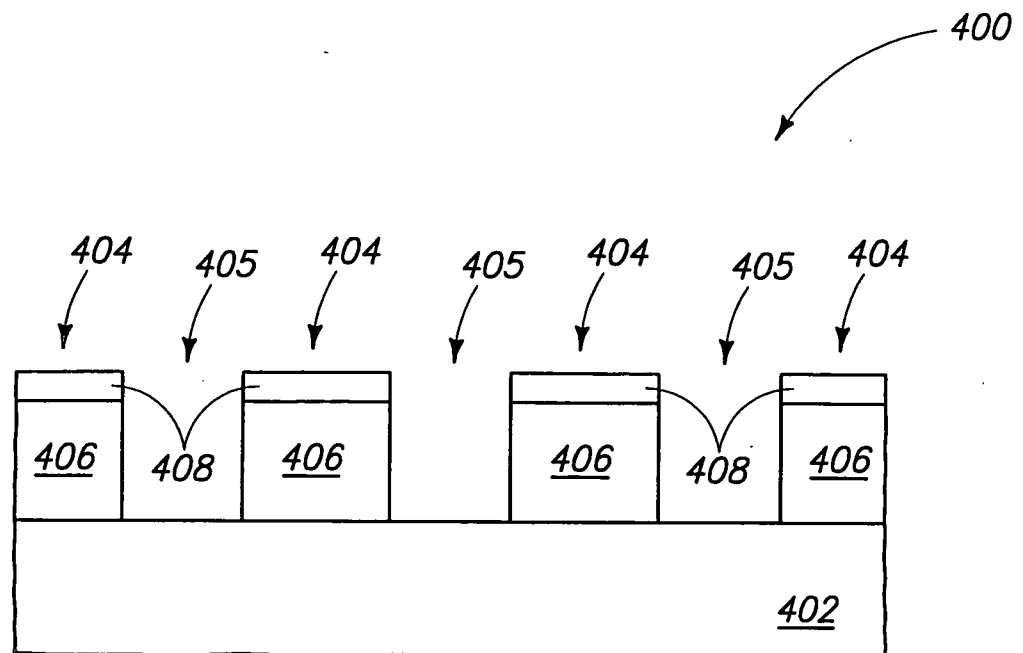


FIG. 4

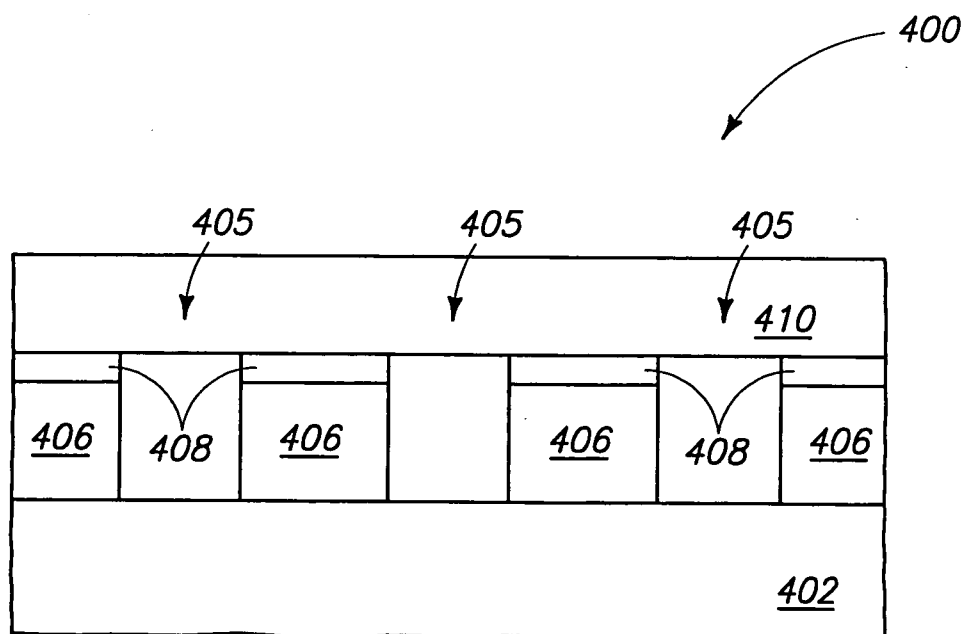
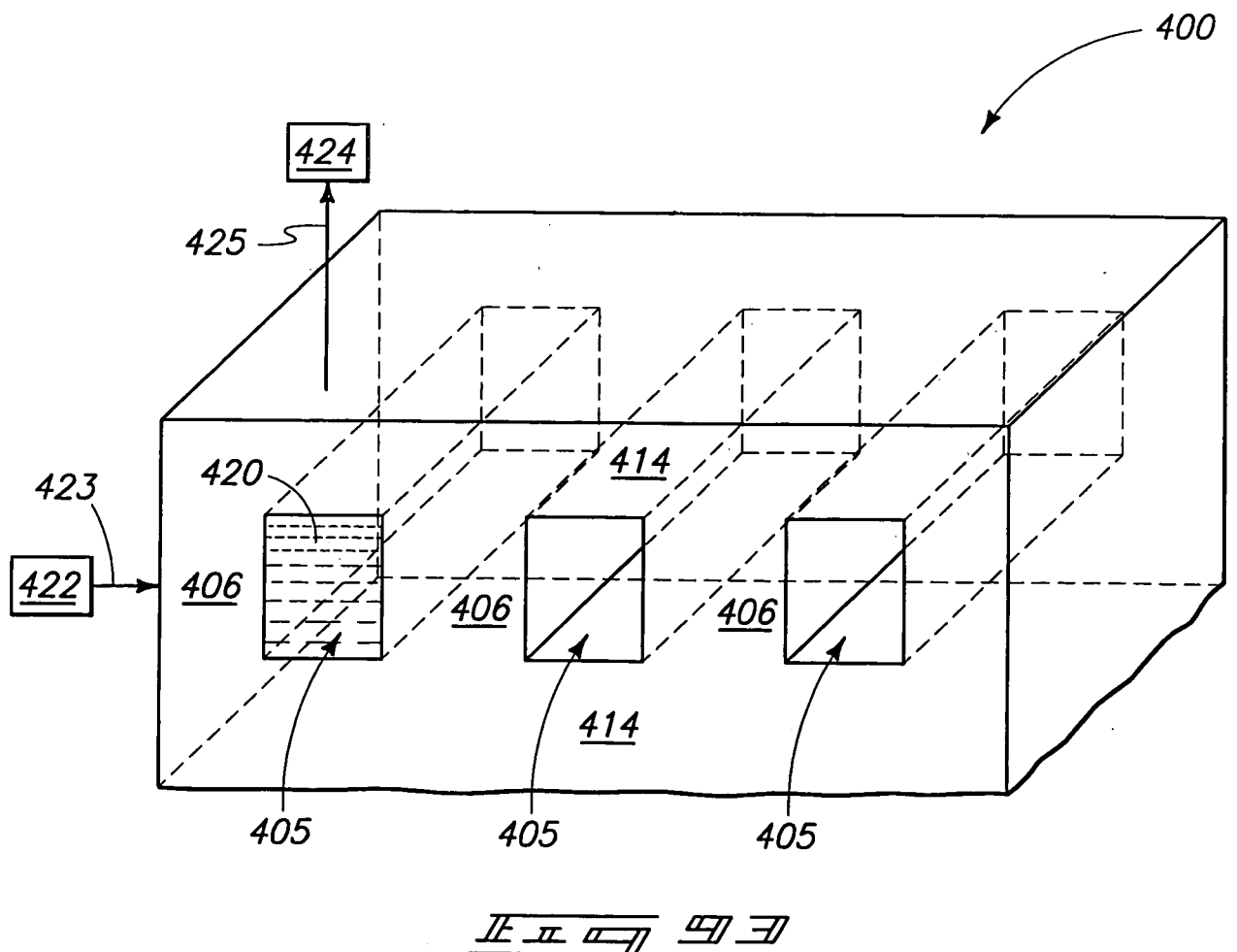
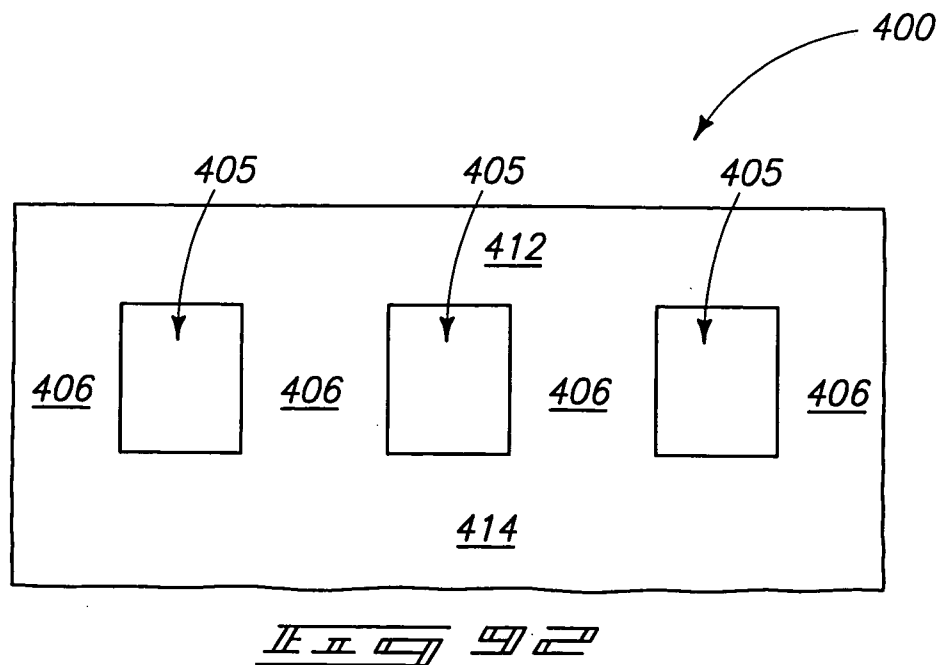
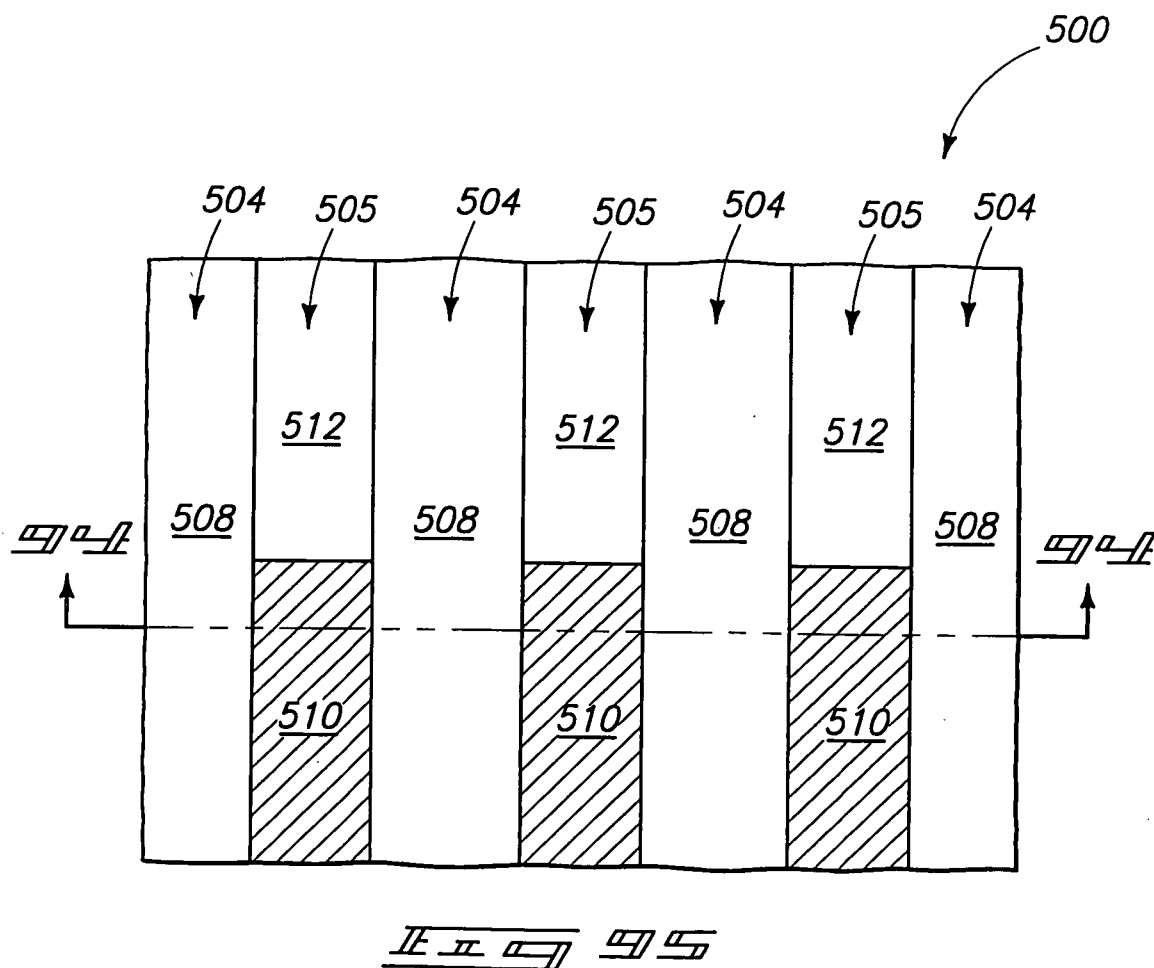
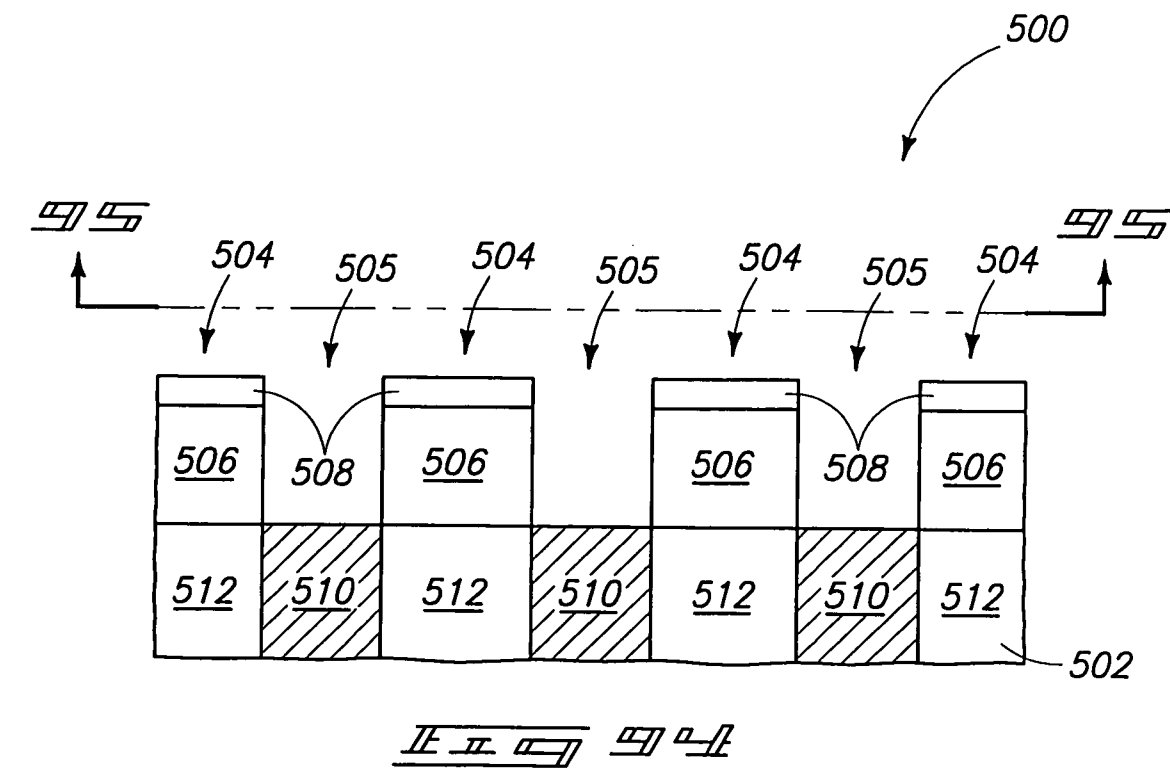


FIG. 5

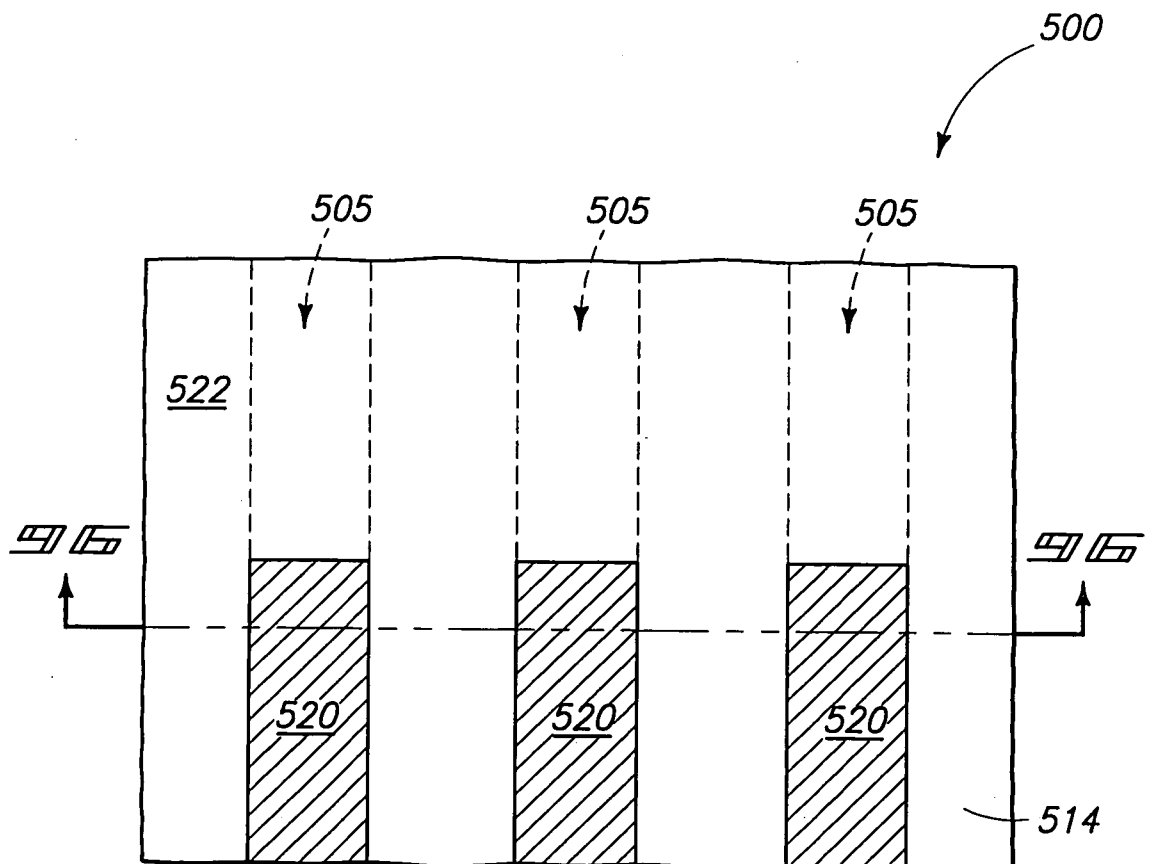
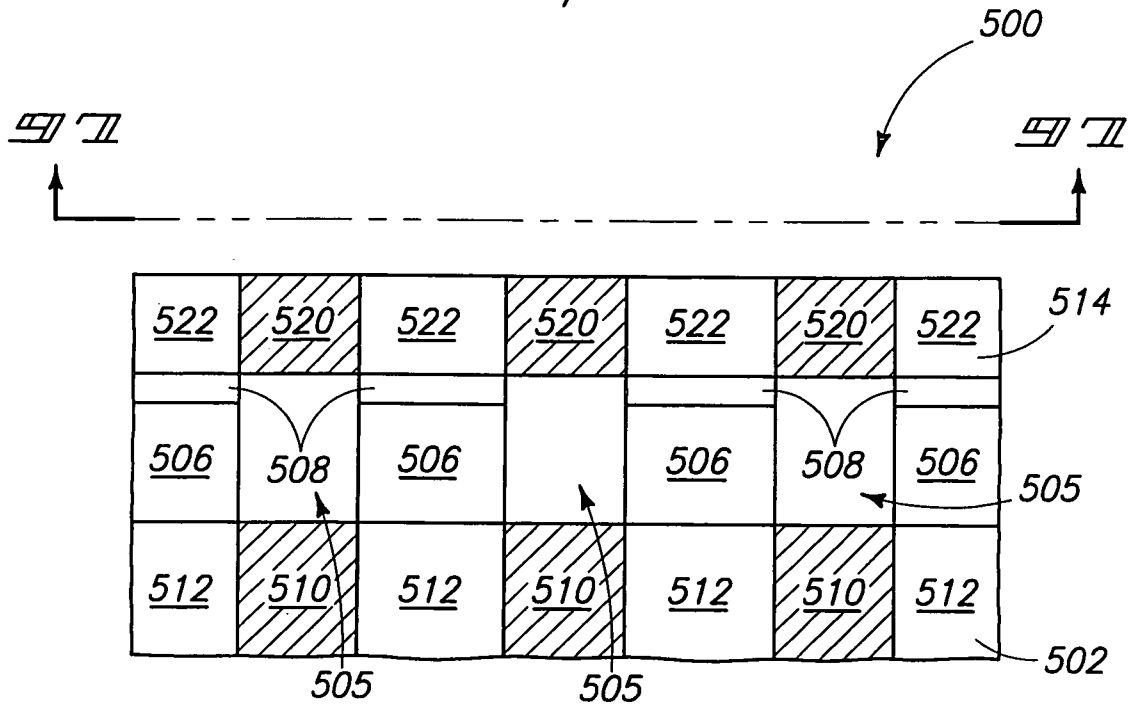
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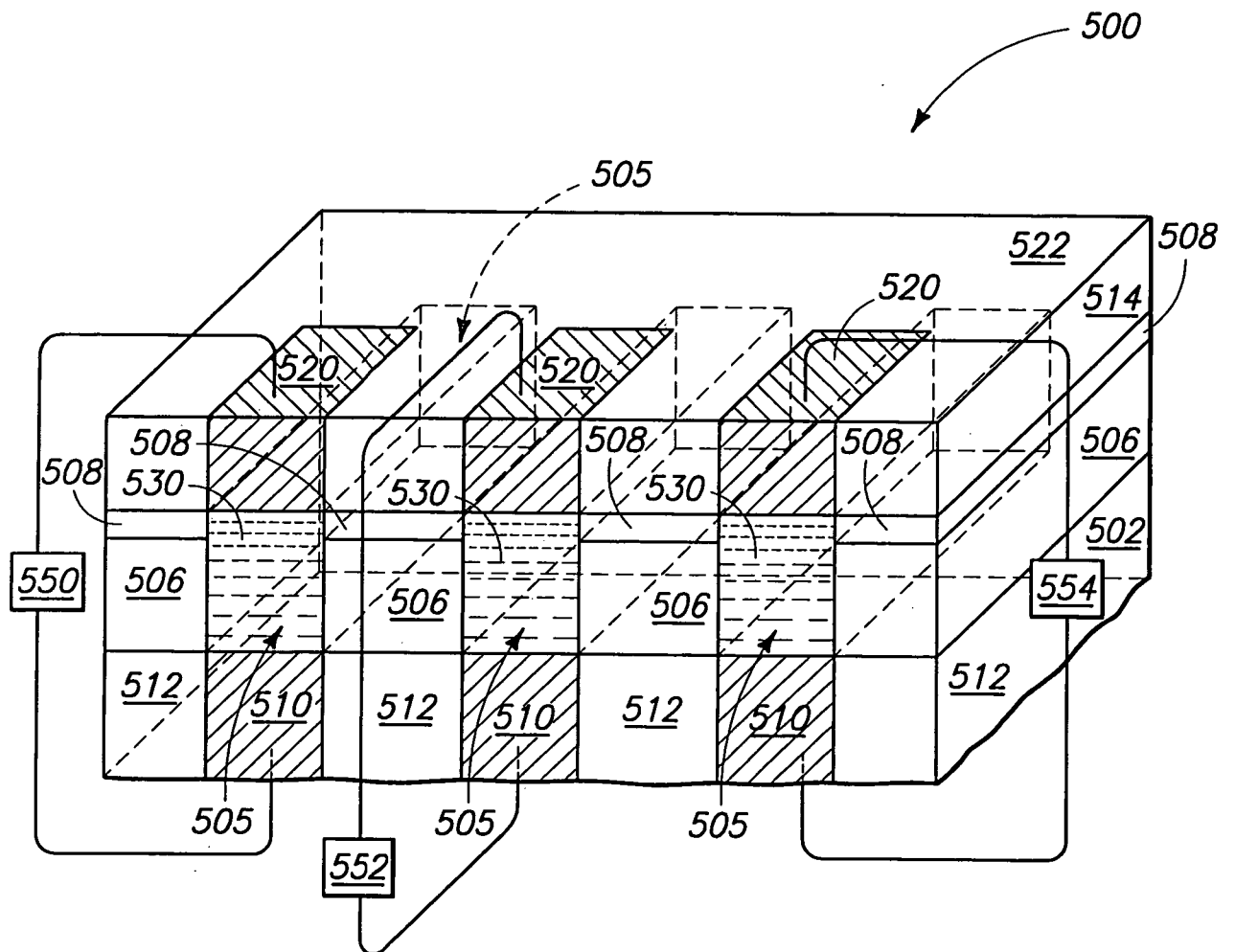
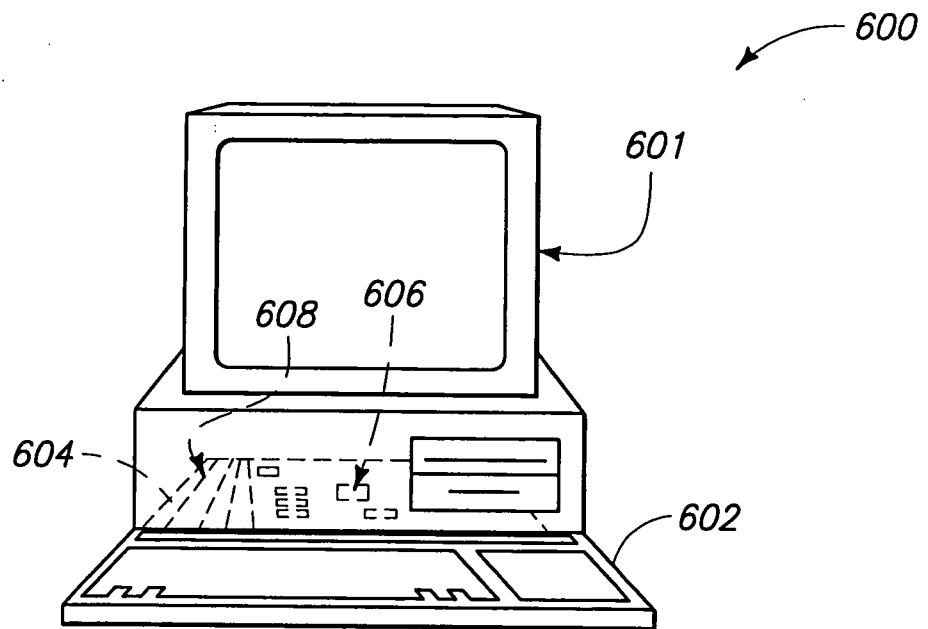
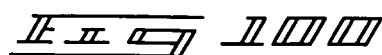
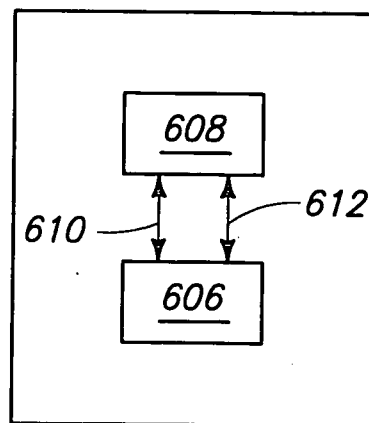


FIG. 50

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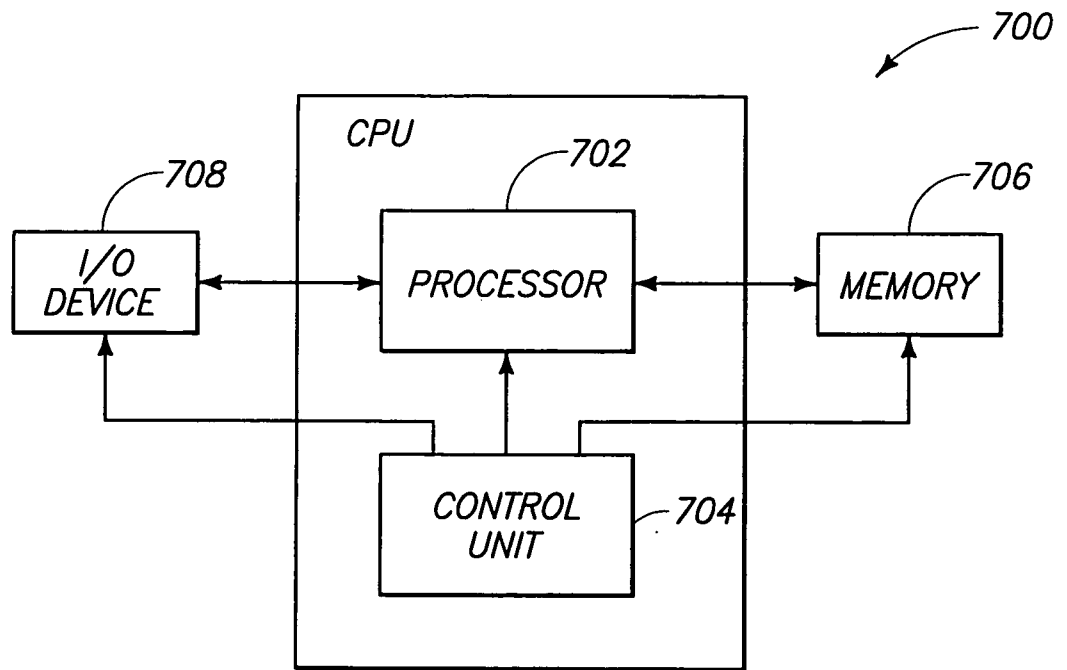


FIG. 52 FIG. 54

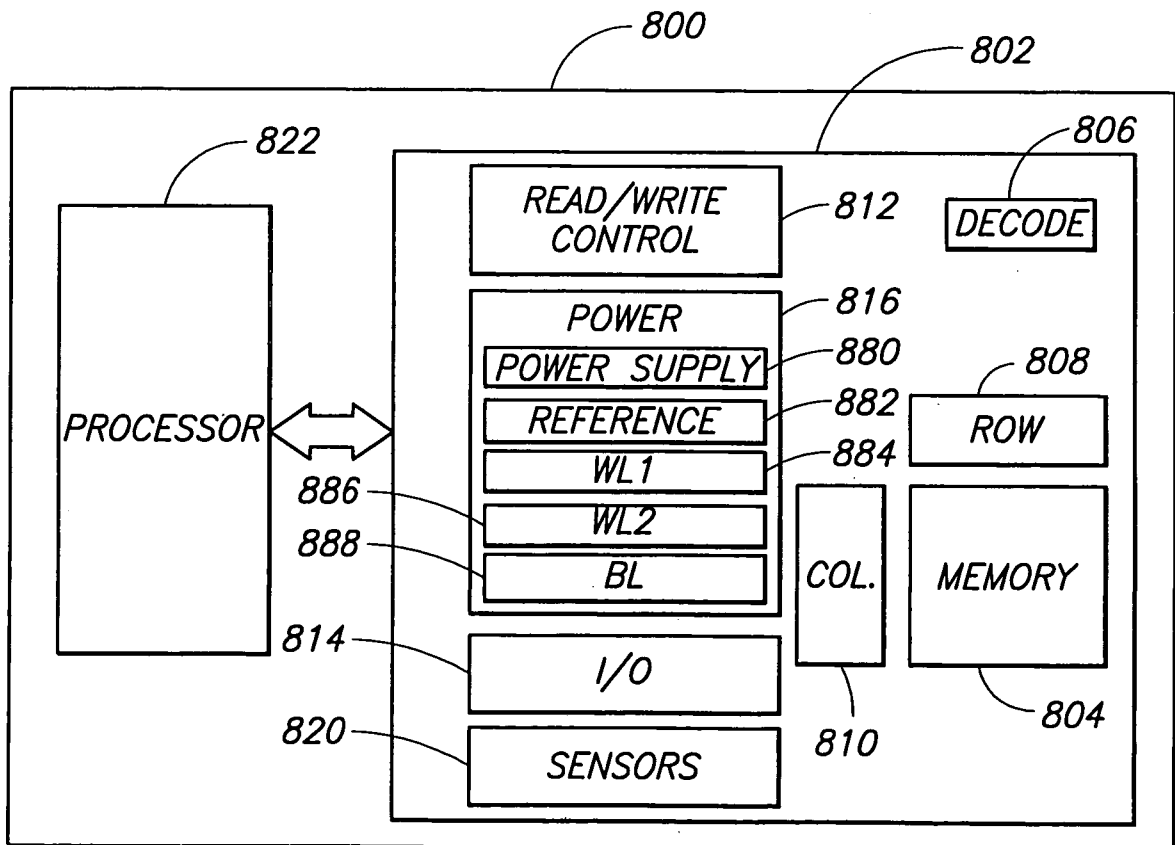
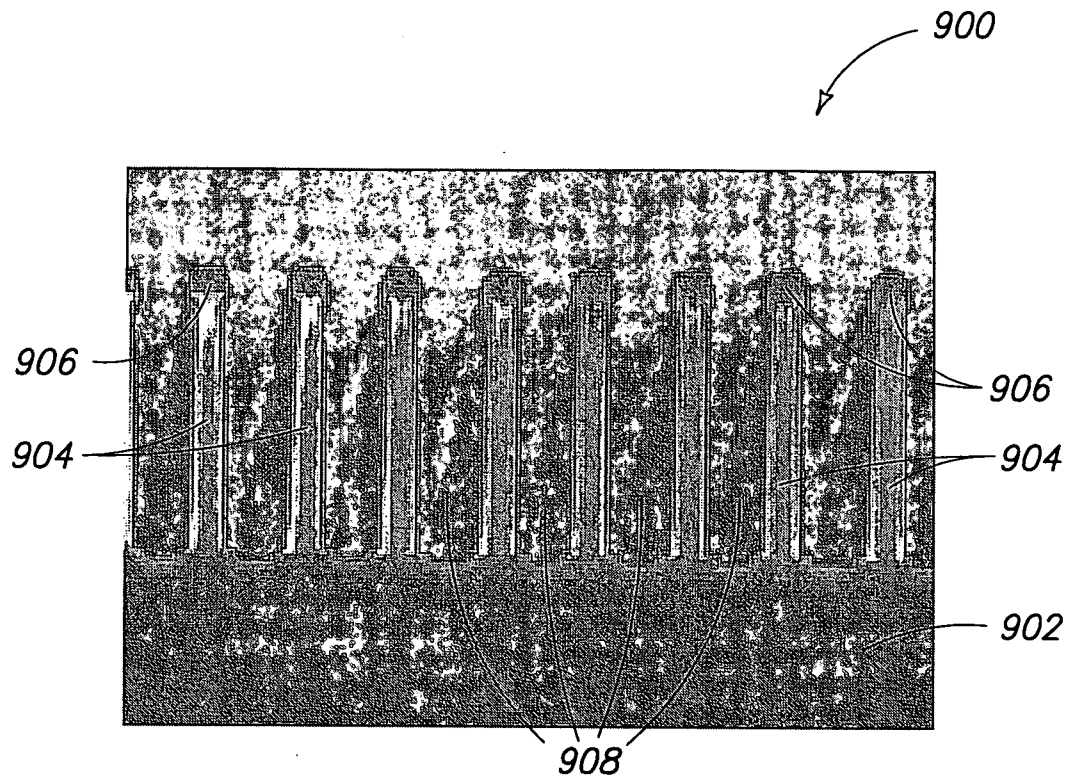
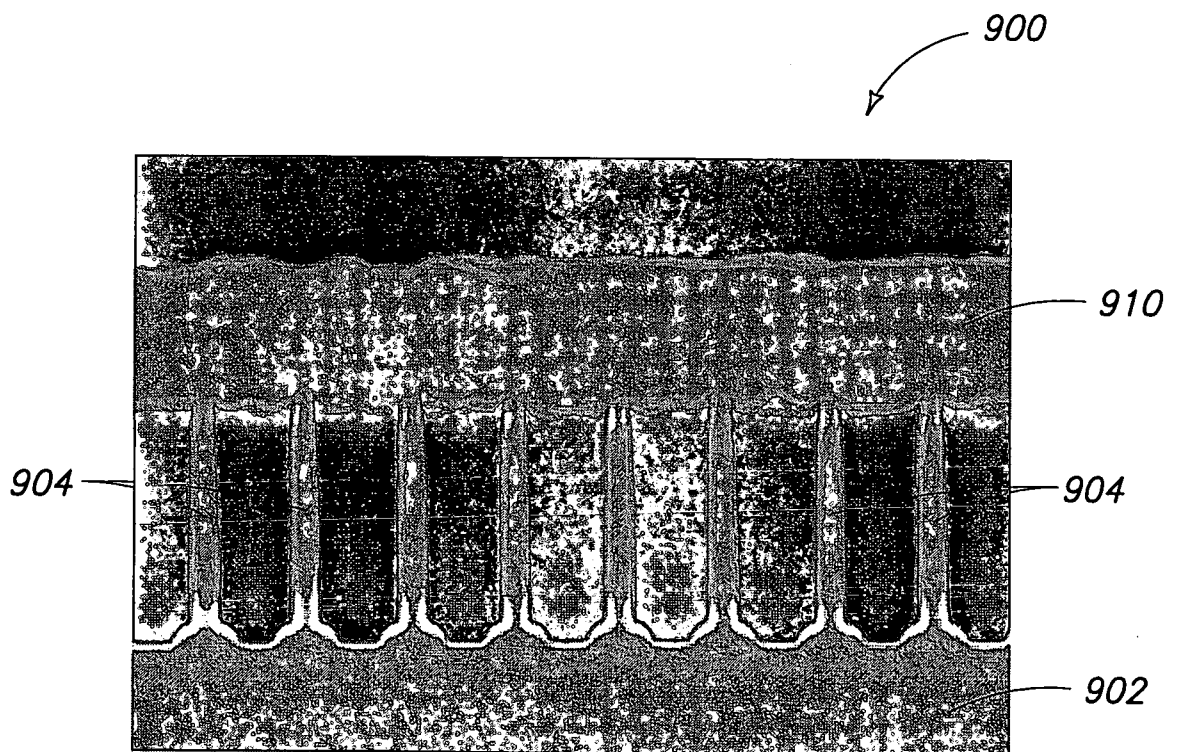


FIG. 800 FIG. 802

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II III



II III

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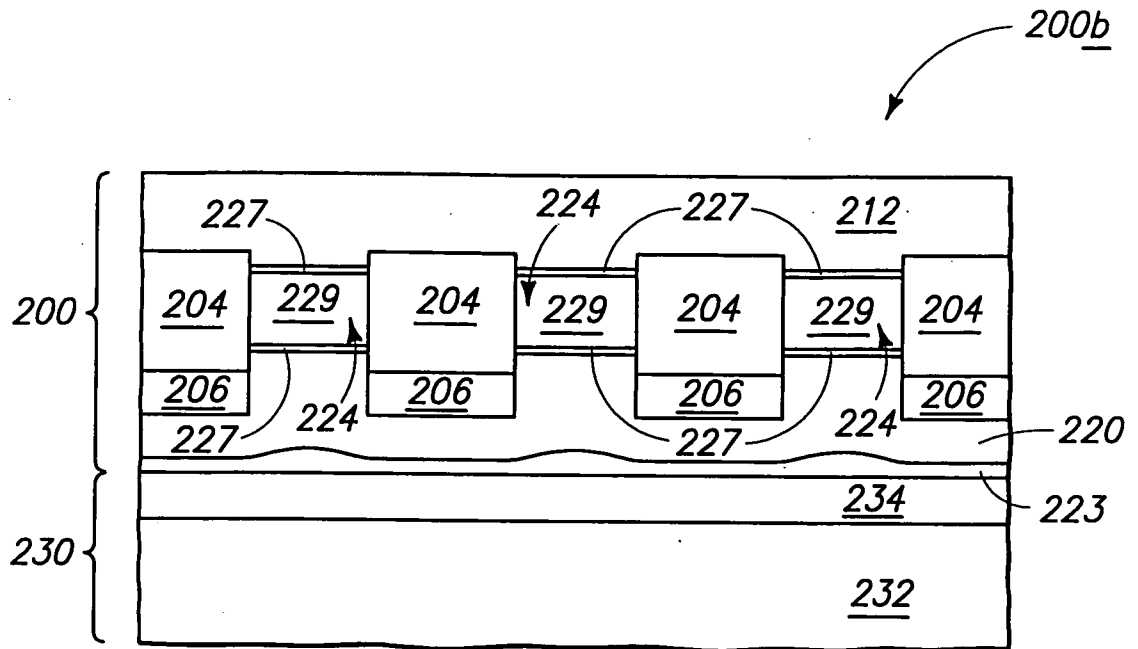


FIG. 54

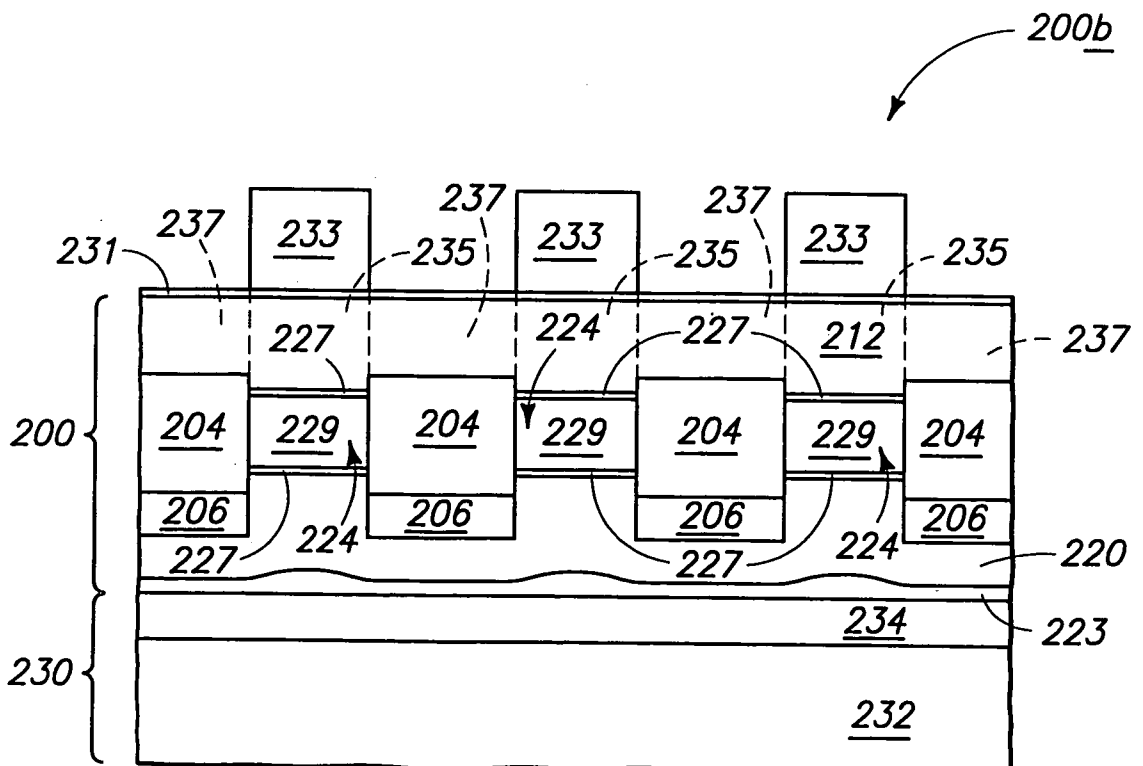


FIG. 55