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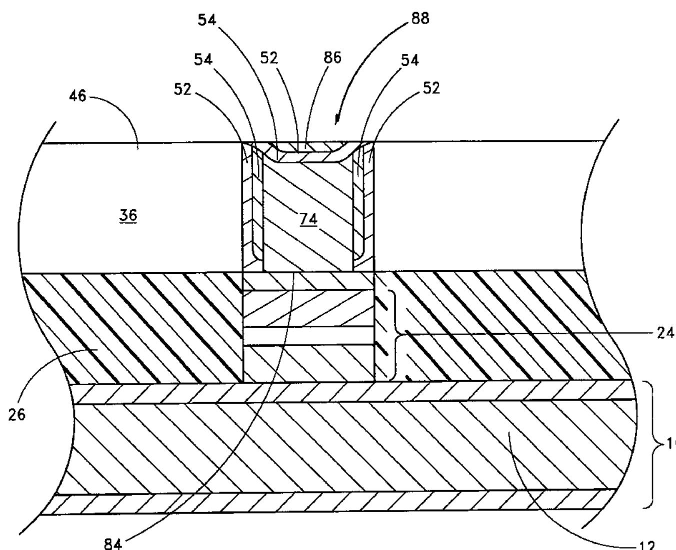

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(57) Abstract: A magnetic memory device, such as a magnetic random access memory (MRAM), and a method for forming same are described herein. The magnetic memory device includes a bit (24), such as a tunneling magneto-resistance (TMR) structure or a giant magneto-resistance (GMR) structure, which is sensitive to magnetic fields and stores data. The bit (24) is preferably disposed between a top electrode (74) with a magnetic keeper (52, 54) and a lower conducting line (12). The top electrode (74) is formed by a damascene process and is preferably formed from copper. The magnetic keeper (52, 54) of the top electrode (74) includes a magnetic material layer (54) (e.g., Co-Fe) and can also include a barrier layer (52) (e.g., Ta). In addition, the magnetic keeper stack (52, 54) can be in contact with one, two, or three surfaces of the top electrode (74) that face away from the bit (24).

KEEPERS FOR MRAM ELECTRODES

Background of the Invention

Field of the Invention

5 This invention is directed generally to magnetic memory devices for storing digital information and, more particularly, to methods and structures for confining magnetic fields produced by these devices.

Description of the Related Art

The digital memory most commonly used in computers and computer system components 10 is the dynamic random access memory (DRAM), wherein voltage stored in capacitors represents digital bits of information. Electric power must be supplied to these memories to maintain the information because, without frequent refresh cycles, the stored charge in the capacitors dissipates, and the information is lost. Memories that require constant power are known as volatile memories.

Non-volatile memories do not need refresh cycles to preserve their stored information, so 15 they consume less power than volatile memories. There are many applications where non-volatile memories are preferred or required, such as in cell phones or in control systems of automobiles.

Magnetic random access memories (MRAMs) are non-volatile memories. Digital bits of information are stored as alternative directions of magnetization in a magnetic storage element or cell. The storage elements may be simple, thin ferromagnetic films or more complex layered 20 magnetic thin-film structures, such as tunneling magneto-resistance (TMR) or giant magneto-resistance (GMR) elements.

Memory array structures are formed generally of a first set of parallel conductive lines covered by an insulating layer, over which lies a second set of parallel conductive lines, perpendicular to the first lines. Either of these sets of conductive lines can be the bit lines and the 25 other the word lines. In the simplest configuration the magnetic storage cells are sandwiched between the bit lines and the word lines at their intersections. More complicated structures with transistor or diode configurations can also be used. When current flows through a bit line or a word line, it generates a magnetic field around the line. The arrays are designed so that each conductive line supplies only part of the field needed to reverse the magnetization of the storage 30 cells. Switching occurs only at those intersections where both word and bit lines are carrying current. Neither line by itself can switch a bit; only those cells addressed by both bit and word lines can be switched.

Magnetic memory arrays can be fabricated as part of integrated circuits (ICs) using thin film technology. As for any IC device, it is important to use as little space as possible. But as 35 packing density is increased, there are tradeoffs to be considered. When the size of a memory cell

is reduced, the magnetic field that is required to write to the cell is increased, making it more difficult for the bit to be written. When the width and thickness of bit lines and word lines are reduced, there is higher current density, which can cause electromigration problems in the conductors. Additionally, as conducting lines are placed closer together, the possibility of cross talk between a conducting line and a cell adjacent to the addressed cell is increased. If this happens repeatedly, the stored magnetic field of the adjacent cell is eroded through magnetic domain creep, and the information in the cell can be rendered unreadable.

In order to avoid affecting cells adjacent to the ones addressed, the fields associated with the bit and word lines must be strongly localized. Some schemes to localize magnetic fields arising from conducting lines have been taught in the prior art.

In U.S. Patent No. 5,039,655, Pisharody taught a method of magnetically shielding conductive lines in a thin-film magnetic array memory on three sides with a superconducting film. At or near liquid nitrogen temperatures (i.e., below the superconducting transition temperature), superconducting materials exhibit the Meissner effect, in which perfect conductors cannot be permeated by an applied magnetic field. While this is effective in preventing the magnetic flux of the conductive line from reaching adjacent cells, its usefulness is limited to those applications where very low temperatures can be maintained.

In U.S. Patent No. 5,956,267, herein referred to as the '267 patent, Hurst et al. taught a method of localizing the magnetic flux of a bottom electrode for a magnetoresistive memory by use of a magnetic keeper. A layered stack comprising barrier layer/soft magnetic material layer/barrier layer was deposited as a partial or full lining along a damascene trench in an insulating layer. Conductive material was deposited over the lining to fill the trench. Excess conductive material and lining layers that were on or extended above the insulating layer were removed by polishing. Thus, the keeper material lined bottom and side surfaces of the bottom conductor, leaving the top surface of the conductor, facing the bit, free of the keeper material.

The process of the '267 patent aids in confining the magnetic field of the cell and avoiding cross-talk among bits. A need exists, however, for further improvements in lowering the writing current for a given magnetic field. By lowering the current required to write to a given cell, reliability of the cell is improved.

Summary of the Invention

In accordance with one aspect of the invention, a magnetic memory array is provided. The array includes a series of top electrodes in damascene trenches wherein each top electrode is in contact with a top magnetic keeper on at least one outer surface of each top electrode, a series of bottom electrodes arranged perpendicular to the top electrodes and bit regions sensitive to magnetic fields and located between the top electrodes and the bottom electrodes at the

intersections of the top electrodes and the bottom electrodes. The bit regions may include multi-layer tunneling magneto-resistance (TMR) or giant magneto-resistance (GMR) structures.

In accordance with another aspect of the invention, a magnetic memory device is provided in an integrated circuit. The device includes a bottom electrode over a semiconductor substrate, a bit region sensitive to magnetic fields over the bottom electrode and an upper electrode in a damascene trench in an insulating layer. The upper electrode has a bottom surface facing toward the bit region, a top surface facing away from the bit region and two side surfaces facing away from the bit region. The device also includes a magnetic keeper in contact with at least one surface of the upper electrode.

In accordance with another aspect of the invention, a magnetic keeper for a top conductor of a magnetic random access memory (MRAM) device is provided. The magnetic keeper comprises a magnetic layer extending along the sidewalls of the top conductor. There is a barrier layer between the magnetic layer and the surrounding insulating layer. The barrier layer also intervenes between a bottom edge of the magnetic layer and the underlying magnetic storage element. In some embodiments, the top conductor is a conductive word line in a damascene trench and is made of copper. The barrier layer can be formed from tantalum, and the magnetic layer can be formed from cobalt-iron.

In accordance with yet another aspect of the invention, a top conductor is provided in a trench in an insulating layer over a magnetic memory device. As part of the top conductor, a magnetic material lining layer is provided along each sidewall of the trench between the conductive material and the insulating layer. The top surface of the lining layer slopes downward from where it meets the insulating layer to where it meets the conductive material.

In one embodiment, the top conductor also includes a first barrier layer between the magnetic material lining layer and each sidewall of the trench. The top surface of the first barrier layer slopes downward from where it meets the insulating layer to where it meets the magnetic lining layer. In another aspect, the top conductor also includes a second barrier layer between the magnetic material lining layer and the conductive material. The top surface of the second barrier layer slopes downward from where it meets the magnetic lining layer to where it meets the conductive material.

In yet another aspect of the invention, the top conductor also includes a magnetic material top layer across the top surface of the conductive material and in contact with the magnetic material lining layers along the sidewalls of the trench. Additionally, there may be a top barrier layer over at least a central portion of the magnetic material top layer.

One embodiment according to the invention is a method of forming a magnetic keeper for a top electrode in a magnetic random access memory (MRAM) device. The method includes

depositing an insulating layer over a magnetic storage element, etching a damascene trench into the insulating layer over the magnetic storage element, filling the trench with a conductive material, such as copper, planarizing to remove the conductive material from over the insulating layer and to leave the conductive material within the trench, and depositing a magnetic material over the conductive material after planarizing. One embodiment of the process further includes forming a recess in a top surface of the conductive layer after planarizing the conductive material, but before depositing the stacked layers. The recess can be formed by a selective etching process. The method can further include forming an initial barrier layer as a trench lining after etching the damascene trench and before filling the trench with conductive material. The method can further include forming a magnetic material layer and then forming a top barrier layer over the initial barrier layer as a complete trench lining.

Another embodiment according to the invention is a method of forming a magnetic keeper for a top electrode in a magnetic random access memory (MRAM). The method includes depositing an insulating layer over a magnetic storage element, etching a damascene trench into the insulating layer over the magnetic storage element, lining the trench with a magnetic material, selectively removing the magnetic material from a bottom of the trench, and filling the trench with a conductive material. The lining of the trench can further include forming a first barrier liner layer before lining the trench with the magnetic material, and forming a second barrier liner layer after lining the trench with the magnetic material. One embodiment of the invention further includes depositing stacked layers of a first barrier layer, a magnetic layer and a second barrier layer onto a top surface of the conductive material.

One embodiment according to the invention further includes lining the bottom and sidewalls of the trench with a first barrier layer prior to lining the bottom and sidewalls of the trench with the magnetic material, lining the bottom and sidewalls of the trench with a second barrier layer after lining the bottom and sidewalls of the trench with the magnetic material, and prior to the filling of the trench with a conductive material, selectively removing the first barrier layer, the magnetic material, and the second barrier layer from the bottom of the trench and from a top surface of the insulating layer such that there is substantially no magnetic material at the bottom of the trench and such that the top surface of the insulating layer is substantially flat.

One embodiment according to the invention further includes lining the bottom and sidewalls of the trench with a first barrier layer prior to lining the bottom and sidewalls of the trench with the magnetic material, prior to the filling of the trench with a conductive material, selectively removing the first barrier layer and the magnetic material from the bottom of the trench and from a top surface of the insulating layer such that there is substantially no magnetic material at the bottom of the trench and such that the top surface of the insulating layer is substantially flat,

selectively etching a recess in a top surface of the conductive material that fills the trench such that the recess is below a flat level of the top surface of the insulating layer, depositing a second barrier layer on the top surface of the insulating layer and on the recess in the top surface of the conductive material, depositing the magnetic material on the second barrier layer, planarizing
5 above the insulating layer to remove the second barrier layer and the magnetic material from the top surface of the insulating layer.

Brief Description of the Drawings

The figures are meant to help illustrate, but not limit, the invention and are not drawn to scale. The illustrated embodiment has bit lines at the bottoms of the figures and has word lines at
10 the tops of the figures. The skilled artisan will understand that there are many other possible configurations for MRAM structures, which can take advantage of the teachings set forth in this invention.

Figure 1A is a cross section of a partially fabricated MRAM structure showing the bottom electrode, the bit region and the overlying insulating layer before the top electrode is fabricated.

15 Figure 1B illustrates the partially fabricated MRAM structure of Figure 1A after a damascene trench has been etched into the insulating layer.

Figure 2 is a cross section showing the damascene trench of Figure 1B lined with a barrier material and filled with copper.

Figure 3A is a cross section showing a blanket layer, comprising a stack of
20 barrier/magnetic/barrier materials, deposited over the structure of Figure 2, in accordance with a first embodiment of the present invention.

Figure 3B shows the structure of Figure 3A after patterning and etching to leave the barrier and magnetic material stack over and slightly wider than the line in which the top electrode is formed.

Figure 4A illustrates the structure of Figure 2 after the conductive material of the top
25 electrode has been etched to make a recess into the top electrode, in accordance with a second embodiment of the present invention.

Figure 4B shows the structure of Figure 4A after a blanket layer, comprising a stack of barrier/magnetic/barrier materials, has been deposited over the recessed top electrode.

Figure 4C illustrates the structure of Figure 4B after planarizing.

30 Figure 5A illustrates the structure of Figure 1B after a stack of barrier/magnetic/barrier materials has been deposited to line the damascene trench, in accordance with a third embodiment of the present invention.

Figure 5B shows the structure of Figure 5A after a spacer etch has removed the horizontal portions of the deposited stack of layers.

Figure 5C is a cross section of the structure of Figure 5B after a blanket conductive layer has been deposited to fill the trench.

Figure 5D shows the structure of Figure 5C after planarization of the conductive layer.

Figure 6A illustrates the structure of Figure 1B after barrier and magnetic layers have been deposited to line the damascene trench, in accordance with a fourth embodiment of the present invention.

Figure 6B is a cross section of a partially fabricated MRAM structure, wherein the conductive material has been selectively recessed, in accordance with a fourth embodiment of the present invention.

Figure 6C is a cross section showing the structure of Figure 6B after a blanket layer, comprising a magnetic material layer and a barrier layer, has been deposited over the recessed conductive material and the insulating layer.

Figure 6D is a cross section showing the structure of Figure 6C after planarizing to remove the barrier and magnetic materials stack from over the insulating layer.

Detailed Description of the Preferred Embodiment

Although aluminum is used commonly as a conductor in semiconductor devices, aluminum has difficulty meeting the high electric current requirements of magnetic memory devices without suffering from damage due to electromigration. Copper is more suitable for high current applications as it is more resistant to electromigration. Whereas aluminum lines can be fabricated by patterning with photoresist and dry etching, copper is difficult to dry etch. Copper lines are thus preferably fabricated by a damascene process. Trenches are formed in an insulating layer, a copper layer is deposited to overfill the trench and the excess copper is removed by polishing down to the surface of the insulating layer.

As discussed above, the '267 patent provides magnetic keepers for bottom electrodes, fabricated by a damascene process. The preferred embodiments described herein provide magnetic keepers, in various configurations, for top electrodes made by a damascene process in integrated magnetic memory devices. The process of the '267 patent, however, is not suitable for forming keepers for a top electrode.

The preferred embodiments of the invention can be understood with reference to the figures. Although only individual magnetic memory structures are shown in the figures, it will be understood that the illustrated individual cells are representative of similar structures that are repeated across a memory array. Figures 1A and 1B show, in cross section, a partially fabricated MRAM cell that will be used as the starting point for describing the embodiments contained herein.

The memory cell includes a bottom electrode structure 10, which further includes a lower conducting line 12 that runs from side to side across the page and is made, preferably, of copper. The

bottom electrode structure 10 typically overlays a semiconductor substrate (not shown). A barrier layer 14 preferably encapsulates the copper line on all four sides along its length. The barrier layer 14 can include a material, such as tantalum (Ta), that prevents the diffusion of copper and is compatible with integrated circuit manufacture. In this cross-sectional view, the copper line is cut near the center along its long axis, so that only the portions of the barrier layer that clad the lower conducting line 12 along an upper surface 18 and a lower surface 20 can be seen. The cladding along one side of the line is above the plane of the page and along the other side of the line is below the plane of the page. In a preferred embodiment (and according to the prior art), the upper surface 18 of the lower conducting line 12 is covered by only the barrier layer 14, but the lower surface 20 and the two side surfaces are further clad by a sandwich structure comprising barrier layer/soft magnetic material/barrier layer, which serves as a magnetic keeper for the lower conducting line 12, in accordance with the teachings of the '267 patent. A "magnetic keeper," as used herein, includes at least a magnetic material layer; in the preferred embodiments the magnetic keeper also includes one or two barrier layers. There is preferably no magnetic material on the top surface of the lower conducting line 12 that faces toward a magnetic memory cell or bit 24 capped with a barrier layer 28 and formed in an insulating layer 26. Magnetic material between the lower conducting line 12 and the bit 24 would interfere with the magnetic field from the lower conducting line 12 acting upon the bit 24.

In Figures 1A and 1B, as well as the embodiments discussed below, the bottom electrode is formed along the lower conducting line 12, which serves as a bit line in the illustrated "cross-point" circuit configurations. In other arrangements, the skilled artisan will readily appreciate that the bit line can be formed above the bit element and the word line below, and that the bit can also be latched to a transistor or diode.

The bit 24 can be any magnetic structure that stores bits of information defined by the direction or polarity of magnetization, including thin ferromagnetic films or more complex layered magnetic thin-film structures, such as tunneling magneto-resistance (TMR) or giant magneto-resistance (GMR) elements.

The preferred magnetic memory cell is a TMR structure. The illustrated TMR structure includes a first ferromagnetic layer 30 followed by an insulating layer 32 and a second ferromagnetic layer 34. A well-known, exemplary TMR structure includes, within the first ferromagnetic layer 30, a series of sub-layers comprising Ta/Ni-Fe/Fe-Mn/Ni-Fe. The insulating layer 32 of the illustrated embodiment includes aluminum oxide, preferably in a thickness between about 0.5 nm and 2.5 nm. The second ferromagnetic layer 34 preferably includes sub-layers, Ni-Fe/Ta. As shown in Figure 1B, the barrier layer 28 preferably overlays the second ferromagnetic layer 34.

The TMR stack can be formed by any suitable method, but is preferably formed as a stack of blanket layers and then patterned into a plurality of cells for the array. The insulating layer 26, preferably silicon nitride or a form of silicon oxide, is then deposited thereon and polished back (e.g., by chemical mechanical planarization) to expose the TMR stack's top surface. Another insulating layer 36, typically comprising a form of silicon oxide, is deposited over the insulating layer 26 and the bit 24. Alternatively, a single insulating layer can take the place of the two illustrated layers 26, 36.

With reference to Figure 1B, a trench 38 is etched into the insulating layer 36 as a first step in using the damascene process to form the top electrode, or word line, for the bit 24. As drawn in Figure 1B, the trench 38, which will contain the word line, runs into and out of the page, perpendicular to the bottom electrode structure 10, and thus traverses several cells in the array. In the illustration of Figure 1B, the bottom of the trench 38 is shown in contact with the barrier layer 28 on the top surface of the bit 24 as a preferred embodiment.

In another arrangement, the trench may be more shallow, leaving a thin portion of the insulating silicon oxide layer between the bottom of the trench and the top of the magnetic cell.

An MRAM, fabricated with a top electrode 40 having no magnetic keeper, is shown in Figure 2. The bottom electrode structure 10 is preferably clad with at least a barrier layer and, more preferably, with the magnetic keeper structure described above with reference to Figure 1A. Using Figure 1B as a starting point, the etched trench 38 preferably has a depth of about 100-300 nm and is about 200 nm in the illustrated embodiments. The width of the trench 38 is preferably about 100-300 nm, and is about 200 nm in the illustrated embodiments. A barrier layer 42 is deposited to line the trench 38. The preferred barrier material is tantalum, although any conductive material that is a good diffusion barrier for confining copper is suitable. The thickness of the barrier layer is preferably about 1-20 nm, more preferably about 2-10 nm and is about 5 nm in the illustrated embodiments. A relatively conductive material 44 is deposited to fill the trench 38 and form the top electrode 40 (along a word line, in the illustrated configuration). The preferred material is copper, but other conductive materials such as aluminum, gold or silver may also be used. The copper may be deposited in a two-step process wherein first a seed layer is deposited by physical vapor deposition and then the trench is filled completely by electroplating. Alternatively, the copper may be deposited completely by physical vapor deposition.

In Figure 2, the top surface 46 of the insulating layer 36 and a top surface 48 of the top electrode 40 have been planarized to remove excess barrier and conductive material and to make the top surface 48 of the top electrode 40 level with the top surface 46 of the insulating layer 36. In the preferred embodiments, the top electrode 40 also includes magnetic keeper structures that help

confine magnetic fields within each cell across the array. The embodiments below employ the structures of Figures 1B or 2 as starting points.

The embodiments that follow have magnetic keeper structures that are multi-layered, including both barrier layers and soft magnetic material layers. Although this is a preferred arrangement, it should be understood that the barrier layer(s) do not have to be present where the magnetic material layer also serves as a diffusion barrier to copper in addition to serving as a magnetic keeper. Thus, the term "magnetic keeper," as used herein, includes at least a magnetic material layer, and preferably also includes one or more barrier layers. Alternative structures include simply a single magnetic material layer as the magnetic keeper or the magnetic material layer and only one barrier layer. The latter arrangement is shown in Figures 6A – 6D.

Patterned Partial Keeper

A relatively simple configuration for a magnetic keeper for a word line is shown in the first embodiment, illustrated in Figures 3A and 3B. This embodiment can be understood using Figure 2 as a starting point. In the illustrated embodiment, a stack 50 of blanket layers is deposited over the planarized top surface as shown in Figure 3A, although it is possible to form this keeper with a magnetic material blanket layer alone. A first layer 52 is a barrier layer. A second layer 54 is a magnetic material that is preferably a soft magnetic material, such as permalloy (Ni-Fe) or cobalt iron (Co-Fe). A third layer 56 is another barrier layer. Preferably, the barrier layers correspond to Ta. The thickness of each layer in the stack is preferably about 1-20 nm, more preferably 2-10 nm and most preferably about 5 nm. The layers in the stack 50 can be deposited by any suitable method. In the illustrated embodiment, the layers are formed by physical vapor deposition all in the same cluster tool.

The stack 50 is patterned and etched using standard photolithography techniques, preferably leaving a patterned partial keeper over the area defining the memory cell. In another arrangement, the keeper is patterned to extend along the top surface of the top electrode 40 that runs into and out of the page as shown in the cross section of Figure 3B. In still another arrangement (and not shown), the blanket stack may be patterned and etched to extend over an entire array, with openings only over vias (not shown) in the insulating layer 36.

The overlying structure is referred to herein as a partial keeper 58 because it does not overlay all external surfaces of the upper conductor or top electrode 40. "External surfaces," as used herein, refers to all surfaces of the top electrode 40 that do not face the bit 24 or TMR stack in the illustrated embodiment.

Self-Aligned Partial Keeper

Figure 4A shows the first step in formation of a self-aligned partial keeper from the top electrode structure of Figure 2, in accordance with a second embodiment. Like reference numerals

are employed for elements corresponding to those of the previous embodiment. A recess 60 is formed in the top surface of the conducting line 44 by a selective etch, which is preferably a wet etch. For example, a solution of glacial acetic acid and nitric acid in a 10:1 (acetic:nitric) ratio will selectively etch copper 44 as compared to the insulating layer 36 and the barrier layer 42. For other materials, the skilled artisan can readily determine a suitable selective chemistry. The depth of the recess 60 is between about 5 nm and 100 nm, more preferably between about 10 nm and 30 nm and most preferably about 15 nm.

Referring to Figure 4B, a magnetic material is deposited into the recess 60. In the illustrated embodiment, the stack 50 of blanket layers is deposited over the recess 60 and the top surface 46 of the insulating layer 36. The illustrated stack 50 includes a first barrier layer 52, a magnetic material layer 54 and a second barrier layer 56. Preferably, the barrier layers 52, 56 correspond to Ta. The magnetic layer preferably includes a soft magnetic material, such as permalloy (Ni-Fe) and more preferably Co-Fe. The thickness of each layer in the stack is preferably about 1-20 nm, more preferably 2-10 nm and most preferably about 5 nm. The layers in the stack 50 can be formed in any suitable manner but are preferably formed by physical vapor deposition all in the same cluster tool.

With reference to Figure 4C, the structure is etched back, preferably planarized, more preferably by chemical-mechanical polishing, which leaves a flat top surface 62 flush with the top surface 46 of the insulating layer 36. The planarization leaves a self-aligned partial keeper 64 within the recess 60 over the upper electrode or top electrode 40.

The self-aligned partial keeper 64 is referred to as such because it is confined to the top electrode 40 without a mask step. The keeper is partial because it covers only one out of three possible external surfaces of the top electrode.

Spacer Keeper

A third embodiment of the current invention is illustrated in Figures 5A-5D. The starting point for this embodiment is the partially fabricated MRAM described earlier with respect to Figure 1B, wherein the trench 38 for the top electrode has been etched. At least a magnetic material layer lines the trench 38. In the illustrated embodiment, the stack 50 of layers, including the magnetic material layer 54 as well as the barrier layers 52, 56 is deposited with good conformity over the top surface 46 and into the trench 38 as shown in Figure 5A. A selective spacer etch is performed to remove the horizontal portions 66, 68, 70 of the stack 50. The selective etch can include an etch with a physical (sputtering) component, such as argon ion milling or a chlorine-based or fluorine-based reactive ion etching, as will be appreciated by the skilled artisan.

Figure 5B shows the remaining portions of the layers 52, 54, 56 along the vertical sidewalls 72 of the trench 38 after application of the spacer etch. Preferably, at least all the soft

magnetic material layer 54 is removed from the bottom of the trench 38 before proceeding, as remaining material can disrupt or block the interaction between the word line magnetic field and the bit 24. While the illustrated embodiment shows all of the stack 50 removed from horizontal portions, thus ensuring complete removal of the magnetic layer 54 from those portions, it will be understood that the spacer etch can also leave part of the lower barrier layer 52 over the bit 24. A spacer keeper 73 is left lining the vertical sidewalls 72.

Referring to Figure 5C, a layer of conductive material 74, preferably copper, is then deposited to fill the trench 38.

Referring to Figure 5D, the conductive material 74 is planarized, preferably by chemical-mechanical polishing, which removes excess conductive material and leaves the conductive material 74 within the trench 38 with external sidewall surfaces covered by the spacer keeper 73, completing the top electrode 40 of the third embodiment. Planarization leaves the top surface 48 of the top electrode 40 flush with the top surface 46 of the insulating layer 36.

Self-Aligned Keeper

A self-aligned keeper 88, in accordance with a fourth embodiment, is described with reference to Figures 6A-6D. This embodiment is similar to the spacer keeper 73 as described above with respect to Figure 5D. The fourth embodiment uses only two layers in the magnetic keeper structure. Alternatively, the self-aligned keeper can be made with the three-layer stack described for embodiments above, or a single layer can serve as both the magnetic layer and barrier function. The starting point for this embodiment is the partially fabricated MRAM described earlier with respect to Figure 1B, wherein the trench 38 for the top electrode has been etched.

With reference to Figure 6A, the barrier layer 52 and the magnetic material layer 54 are deposited with good conformity over the top surface 46 of the insulating layer 36 and into the trench 38. Preferably, the barrier layer 52 corresponds to Ta. The magnetic layer preferably includes a soft magnetic material, such permalloy (Ni-Fe). Co-Fe is particularly preferred for use in this two-layer stack, whereby the magnetic material layer 54 will directly contact copper (see Fig. 6C). A selective spacer etch is performed to remove the horizontal portions 76, 78, 80 of the barrier layer 52 and the magnetic material layer 54. The selective etch comprises an etch with a physical (sputtering) component, such as argon ion milling or a chlorine-based or fluorine-based reactive ion etching, as will be appreciated by the skilled artisan. Preferably, at least all the soft magnetic material layer 54 is removed from the bottom of the trench 38 before proceeding, as remaining material can disrupt or block the interaction between the word line magnetic field and the bit 24.

Figure 6B shows the remaining portions of the layers 52, 54, along the vertical sidewalls 72 of the trench after the selective spacer etch, as well as subsequent via fill and recess steps,

discussed below. While the illustrated embodiment shows all material from layers 52, 54 removed from horizontal portions, thus ensuring complete removal of the magnetic layer 54 from those portions, it will be understood that the spacer etch can also leave part of the barrier layer 52 over the bit 24.

5 As shown in other embodiments, a layer of conductive material 74, preferably copper, is deposited to fill the trench, and the top surface is planarized, preferably by chemical-mechanical polishing. Excess conductive material is removed, leaving conductive material 74 within the trench and barrier 52 and magnetic 54 layers along the vertical sidewalls 72. The conductive material extends along a trench into and out of the page, serving as an upper line 74, comprising a 10 word line in the illustrated arrangement.

A selective etch is performed to create a recess 82 in the top surface of the upper line 74 as shown in Figure 6B. The etch is preferably performed by a wet etching process. For example, a solution of glacial acetic acid and nitric acid in a 10:1 (acetic:nitric) ratio will selectively etch the upper line 74 as compared to the insulating layer 36. Alternatively the recess 82 can be made by 15 extending the previous chemical-mechanical polishing and using an appropriate selective chemistry with the polish. For other materials, the skilled artisan can readily determine a suitable selective chemistry.

With reference to Figure 6C, at least a magnetic material and preferably a second series of blanket layers, comprising the top portion of the magnetic keeper for this embodiment, is deposited 20 over the top surface, filling the recess 82. Preferably, the first layer 54 is a soft magnetic material, such as Co-Fe, and the second layer 52 is a barrier layer, such as a layer of Ta.

Figure 6D shows the structure after chemical-mechanical polishing to remove the excess magnetic keeper material. The upper line 74 is clad along three sides with the magnetic material layer 54 and the barrier layer 52. Advantageously, the magnetic material is formed as a continuous 25 layer 54 around the three sides of the upper line 74. The electrode surface 84 facing the bit 24 has no magnetic material cladding. A top surface 86 of the structure is preferably flush with the top surface 46 of the surrounding insulating layer 36, making it easier to perform further processing.

The self-aligned keeper 88 is referred to as such because it is confined to the upper line 74 without a mask step. This keeper is not called partial because it covers all three surfaces suitable for 30 magnetic keeper cladding.

It will be understood that the fourth embodiment, illustrated in Figures 6A-6D, represents a combination of the second and third embodiments with a modification to two layers in the magnetic keeper structure instead of three. Similarly, the third embodiment can be combined with the first embodiment, thereby also providing keeper material on three external surfaces of the top electrode 35 without blocking magnetic fields between the top electrode and the underlying magnetic bit.

Furthermore, it should be understood that the barrier layer is not necessary to perform the magnetic keeper function and confine the magnetic fields. Alternative structures include simply a single magnetic material layer as the magnetic keeper or the magnetic material layer one or more barrier layers. The invention as described herein in the preferred embodiments provides a method for
5 fabricating a magnetic keeper in a number of structures for a conducting line in a damascene trench, wherein the bottom surface of the trench has no keeper. This has particular application for top electrodes in magnetic memory devices. The keeper localizes the magnetic field surrounding the conducting line so that only the desired or intended magnetic memory cell or bit being addressed is relatively affected by the field. The keeper contains the magnetic flux and directs it toward the
10 magnetic memory structure, thus lowering the effective current density required for writing to the bit. Neighboring bits, which are not addressed, receive relatively less of the undesired magnetic field and electromigration is reduced. This aids in compressing the design of magnetic memory arrays to smaller dimensions without sacrificing functionality.

The presently disclosed embodiments are therefore considered in all respects to be illustrative
15 and not restrictive. The scope of the invention is indicated by the appended claims rather than the foregoing description and all changes that come within the meaning and range of equivalence thereof are intended to be embraced therein.

I CLAIM:

1. A magnetic memory array, comprising:

a series of top electrodes in damascene trenches;

a plurality of top magnetic keepers on at least one outer surface of the top 5 electrodes;

a series of bottom electrodes arranged orthogonally to the top electrodes; and

bit regions sensitive to magnetic fields, where the bit regions are disposed between the top electrodes and the bottom electrodes, where top surfaces of the bit regions are in contact with the top electrodes, and where the bottom surfaces of the bit regions are in 10 contact with the bottom electrodes.

2. The magnetic memory array of Claim 1, wherein bit regions correspond to tunneling magneto-resistance (TMR) bit regions.

3. A magnetic memory device in an integrated circuit comprising:

a bottom electrode over a semiconductor substrate;

15 a bit region sensitive to magnetic fields, where the bit region is formed over the bottom electrode;

a magnetic keeper; and

an upper electrode in a damascene trench formed in an insulating layer, where the upper electrode has a bottom surface facing toward the bit region, a top surface facing 20 away from the bit region, and two side surfaces facing away from the bit region, wherein the top surface of the upper electrode defines a recess that is adapted to accommodate at least a portion of the magnetic keeper.

4. The magnetic memory array of Claim 3, wherein the bit region corresponds to a multi-layer tunneling magneto-resistance (TMR) structure.

25 5. The magnetic memory array of Claim 3, wherein the bit region corresponds to a multi-layer giant magneto-resistance (GMR) structure.

6. The magnetic memory device of Claim 3, wherein a top surface of the bit region is in electrical contact with the upper electrode in the damascene trench.

7. The magnetic memory device of Claim 3, further comprising a barrier material that 30 lines the damascene trench.

8. The magnetic memory device of Claim 7, wherein the barrier material is tantalum.

9. The magnetic memory device of Claim 3, wherein the upper electrode is copper.

10. The magnetic memory device of Claim 3, wherein the magnetic keeper is also in contact with the two side surfaces of the upper electrode.

11. The magnetic memory device of Claim 3, wherein the magnetic keeper comprises a barrier layer and a magnetic layer.

12. The magnetic memory device of Claim 3, wherein the magnetic keeper comprises multiple stacked layers that include a first tantalum layer, a second tantalum layer, and a cobalt-iron (Co-Fe) layer disposed between the first tantalum layer and the second tantalum layer.

13. The magnetic memory device of Claim 3, wherein the recess is between about 5 and 100 nm in depth.

14. The magnetic memory device of Claim 3, wherein the recess is between about 10 and 30 nm in depth.

15. The magnetic memory device of Claim 3 wherein the magnetic keeper further includes holes for corresponding vias that are present in the insulating layer.

16. A magnetic keeper for a top conductor of a magnetic random access memory (MRAM) device, the top conductor having a bottom structure facing toward an underlying magnetic storage element, the magnetic keeper comprising a magnetic layer extending along sidewalls of the top conductor and a barrier layer between a surrounding insulating layer and the magnetic layer, wherein the barrier layer also intervenes between a bottom edge of the magnetic layer and the underlying magnetic storage element.

17. The magnetic keeper of Claim 16, wherein the underlying magnetic storage element comprises a tunneling magneto resistance (TMR) bit structure, and a top surface of the TMR bit structure is in electrical contact with a bottom surface of the top conductor.

18. The magnetic keeper of Claim 16, wherein the top conductor comprises a conductive word line in a damascene trench.

19. The magnetic keeper of Claim 18, wherein the top conductor comprises copper.

20. The magnetic keeper of Claim 18, wherein a depth of the damascene trench is between about 100 and 300 nm.

21. The magnetic keeper of Claim 18, wherein a depth of the damascene trench is between about 180 and 220 nm.

22. The magnetic keeper of Claim 18, wherein a width of the damascene trench is between about 100 and 300 nm.

23. The magnetic keeper of Claim 18, wherein a width of the damascene trench is between about 180 and 220 nm.

24. The magnetic keeper of Claim 16, wherein the barrier layer comprises tantalum, and the magnetic layer comprises cobalt-iron.

25. The magnetic keeper of Claim 24, wherein the barrier layer and the magnetic layer are each between about 1 and 20 nm thick.

26. The magnetic keeper of Claim 24, wherein the barrier layer and the magnetic layer are each between about 2 and 10 nm thick.

27. The magnetic keeper of Claim 16, further comprising a second magnetic layer along a top surface of the top conductor, the top surface facing away from the magnetic storage
5 element, and a second barrier layer over the second magnetic layer.

28. A top conductor in a trench formed in an insulating layer over a magnetic memory bit comprising:

a magnetic material lining layer along each sidewall of the trench;

a top surface of the lining layer sloping downward from an outer edge of the lining
10 layer that is no higher than a top surface of the insulating layer toward an inner edge of the lining layer; and

conductive material filling the trench.

29. The top conductor of Claim 28, wherein the top surface of the outer edge of the lining layer is approximately even with the top surface of the insulating layer.

15 30. The top conductor of Claim 28, wherein the conductive material further covers the top surface of the lining layer along each sidewall of the trench, thereby forming an approximately flat upper surface that is continuous and approximately coplanar with the top surface of the insulating layer.

31. The top conductor of Claim 28, further comprising a first barrier layer between the
20 magnetic material lining layer and each sidewall of the trench, a top surface of the first barrier layer sloping downward from an outer edge of the first barrier layer that is approximately even with the top surface of the insulating layer to an inner edge that is approximately even with the top surface of the magnetic lining layer.

32. The top conductor of Claim 31, further comprising a second barrier layer between
25 the magnetic material lining layer and the conductive material, a top surface of the second barrier layer sloping downward from an outer edge of the second barrier layer that is approximately even with the top surface of the inner edge of the lining layer toward an inner edge of the barrier layer.

33. The top conductor of Claim 31, further comprising a magnetic material top layer across a top surface of the conductive material and in contact with the top surface of the magnetic
30 material lining layer along each sidewall of the trench, an upper surface of the magnetic material top layer extending no higher than the top surface of the insulating layer.

34. The top conductor of Claim 33, wherein the magnetic material top layer forms an approximately flat upper surface that is continuous and approximately coplanar with the top surface of the insulating layer.

35. The top conductor of Claim 33, wherein a top barrier layer is in contact with at least a central portion of the upper surface of the magnetic material top layer, the top barrier layer having an approximately flat upper surface that is approximately coplanar with the top surface of the insulating layer.

5 36. A method of forming a magnetic keeper for a top electrode in a magnetic random access memory (MRAM) device comprising:

depositing an insulating layer over a magnetic storage element;

etching a damascene trench into the insulating layer over the magnetic storage element;

10 filling the trench with a conductive material;

planarizing to remove the conductive material from over the insulating layer and to leave the conductive material within the trench; and

depositing a magnetic material over the conductive material after planarizing.

37. The method of Claim 36, further comprising patterning and etching the magnetic

15 material so that the magnetic material covers at least a top surface of the conductive material.

38. The method of Claim 36, wherein the magnetic material extends over an array of magnetic storage elements, further comprising patterning and etching openings in the magnetic material over contact vias in the insulating layer.

39. The method of Claim 36, further comprising forming a recess in a top surface of

20 the conductive layer after planarizing the conductive material, but before depositing the stacked layers.

40. The method of Claim 39, further comprising selectively etching the conductive material to form the recess.

41. The method of Claim 40, wherein selectively etching comprises wet etching.

25 42. The method of Claim 41, further comprising wet etching with a solution of glacial acetic acid and nitric acid in about a 10:1 (acetic:nitric).

43. The method of Claim 40, further comprising selectively etching with chemical-mechanical polishing.

44. The method of Claim 39, further comprising planarizing to remove the magnetic

30 material from over the insulating layer, but not from within the recess, after depositing the magnetic material.

45. The method of Claim 36, further comprising filling the trench with copper as the conductive material.

46. The method of Claim 45, further comprising depositing a copper seed layer with physical vapor deposition and electroplating copper over the copper seed layer to fill the trench with copper.

47. The method of Claim 36, further comprising forming an initial barrier layer as a trench lining after etching the damascene trench, but before filling the trench with conductive material.

48. The method of Claim 47, further comprising forming a magnetic material layer and then forming a top barrier layer over the initial barrier layer as a complete trench lining.

49. The method of Claim 48, further comprising performing a spacer etch to remove the magnetic material from the bottom of the trench after forming the complete trench lining and before filling the trench.

50. The method of Claim 49, wherein the complete trench lining comprises stacked layers of tantalum/Co-Fe/tantalum.

51. The method of Claim 49, wherein the complete trench lining comprises stacked layers of tantalum/permalloy (Fe-Ni)/tantalum.

52. The method of Claim 48, further comprising using physical vapor deposition to form the complete trench lining.

53. The method of Claim 48, wherein the complete trench lining is deposited in only one cluster tool.

54. A method of forming a magnetic keeper for a top electrode in a magnetic random access memory (MRAM) comprising:

depositing an insulating layer over a magnetic storage element;

etching a damascene trench into the insulating layer over the magnetic storage element;

lining the trench with a magnetic material;

selectively removing the magnetic material from a bottom of the trench; and

filling the trench with a conductive material.

55. The method of Claim 54, wherein lining the trench further comprises forming a first barrier liner layer before lining the trench with the magnetic material, and forming a second barrier liner layer after lining the trench with the magnetic material.

56. The method of Claim 55, wherein the first barrier liner layer is tantalum, the magnetic material is cobalt iron (Co-Fe) and the second barrier liner layer is tantalum.

57. The method of Claim 54, wherein selectively removing the magnetic material from the bottom of the trench comprises a selective etch with a physical etch component.

58. The method of Claim 57, further comprising using argon ion milling to selectively etch.

59. The method of Claim 57, wherein the selective etch is selected from the group consisting of a chlorine-based reactive ion etch and a fluorine-based reactive ion etch.

5 60. The method of Claim 54, further comprising depositing stacked layers of a first barrier layer, a magnetic layer and a second barrier layer on a top surface of the conductive material.

61. The method of Claim 60, further comprising forming a recess in the top surface of the conductive material before the stacked layers are deposited.

10 62. The method of Claim 61, wherein the first barrier layer is tantalum, the magnetic layer is cobalt iron (Co-Fe) and the second barrier layer is tantalum.

63. The method of Claim 62, further comprising planarizing a top surface of the stacked layers.

64. The method of Claim 54, wherein the magnetic storage element is a multi-layer 15 tunneling magneto-resistance (TMR) structure.

65. The method of Claim 64, wherein the TMR structure comprises a first ferromagnetic layer, an insulating layer, and a second ferromagnetic layer.

66. The method of Claim 65, wherein the first ferromagnetic layer includes a series of sub-layers comprising Ta/Ni-Fe/Fe-Mn/Ni-Fe.

20 67. The method of Claim 65, further comprising forming the insulating layer from aluminum oxide.

68. The method of Claim 65, wherein the second ferromagnetic layer comprises sub-layers Ni-Fe/Ta.

69. The method of Claim 54, wherein the conductive material is copper.

25 70. The method of Claim 54, further comprising:

lining the bottom and sidewalls of the trench with a first barrier layer prior to lining the bottom and sidewalls of the trench with the magnetic material;

lining the bottom and sidewalls of the trench with a second barrier layer after lining the bottom and sidewalls of the trench with the magnetic material; and

30 prior to the filling of the trench with a conductive material, selectively removing the first barrier layer, the magnetic material, and the second barrier layer from the bottom of the trench and from a top surface of the insulating layer such that there is substantially no magnetic material at the bottom of the trench and such that the top surface of the insulating layer is substantially flat.

71. The method of Claim 54, further comprising:

lining the bottom and sidewalls of the trench with a first barrier layer prior to lining the bottom and sidewalls of the trench with the magnetic material;

prior to the filling of the trench with a conductive material, selectively removing the first barrier layer and the magnetic material from the bottom of the trench and from a top surface of the insulating layer such that there is substantially no magnetic material at the bottom of the trench and such that the top surface of the insulating layer is substantially flat;

selectively etching a recess in a top surface of the conductive material that fills the trench such that the recess is below a flat level of the top surface of the insulating layer;

depositing a second barrier layer on the top surface of the insulating layer and on the recess in the top surface of the conductive material;

depositing the magnetic material on the second barrier layer; and

planarizing above the insulating layer to remove the second barrier layer and the magnetic material from the top surface of the insulating layer.

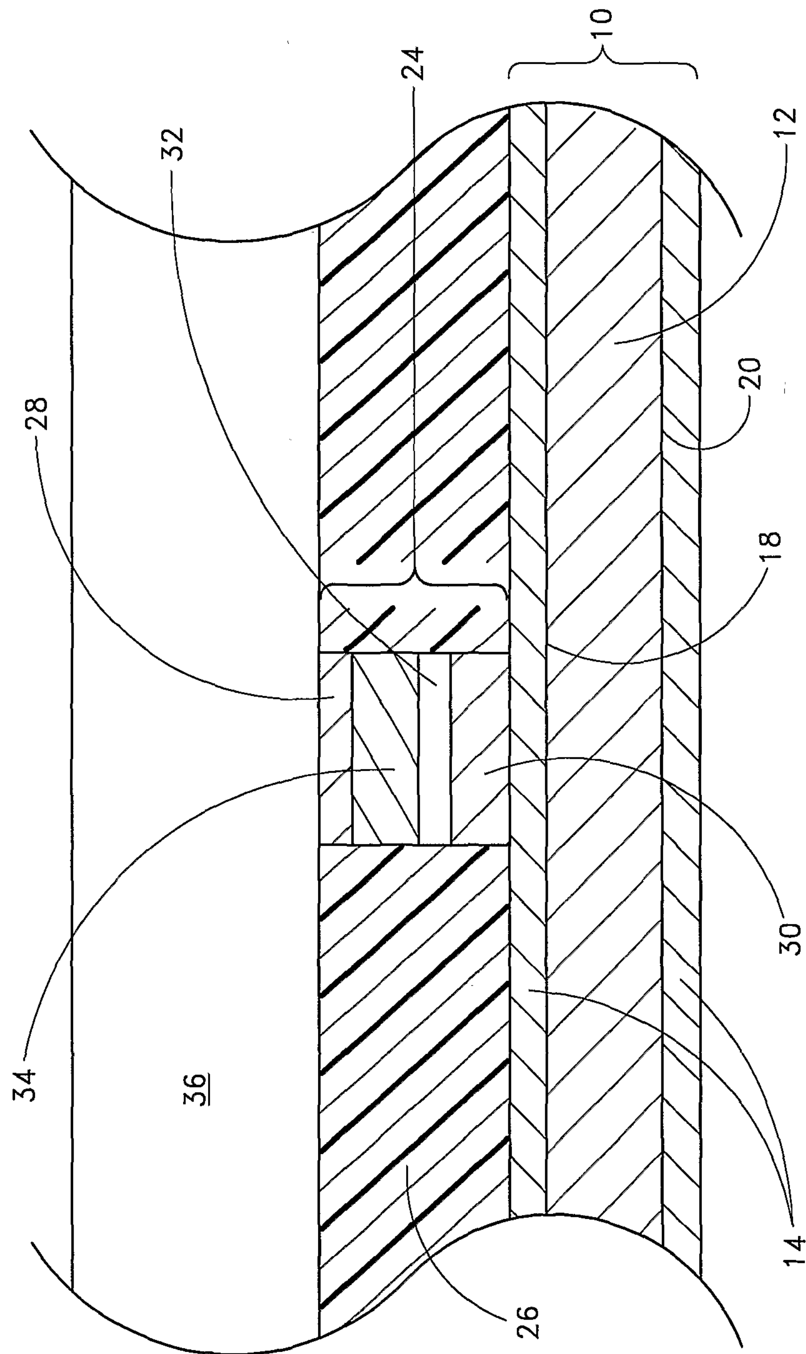

FIG. 1A

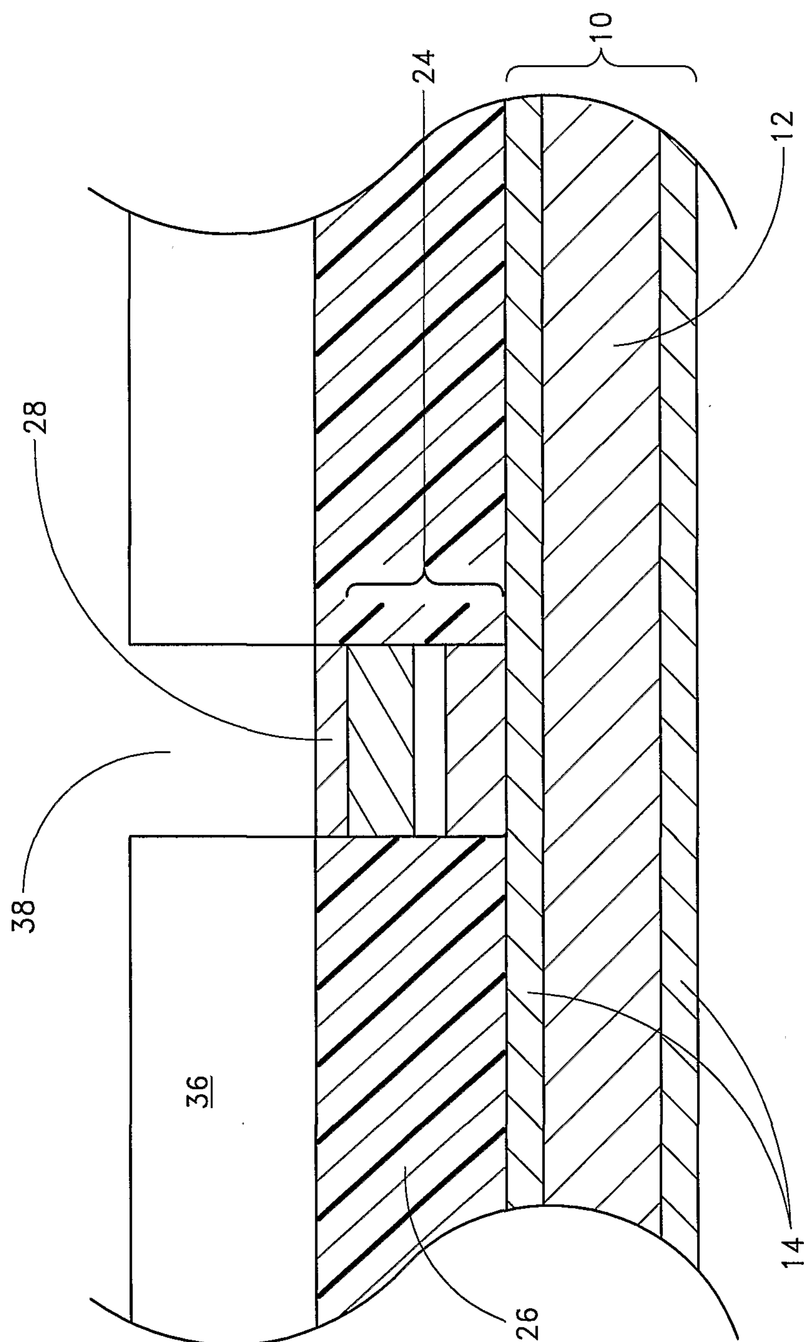

FIG. 1B

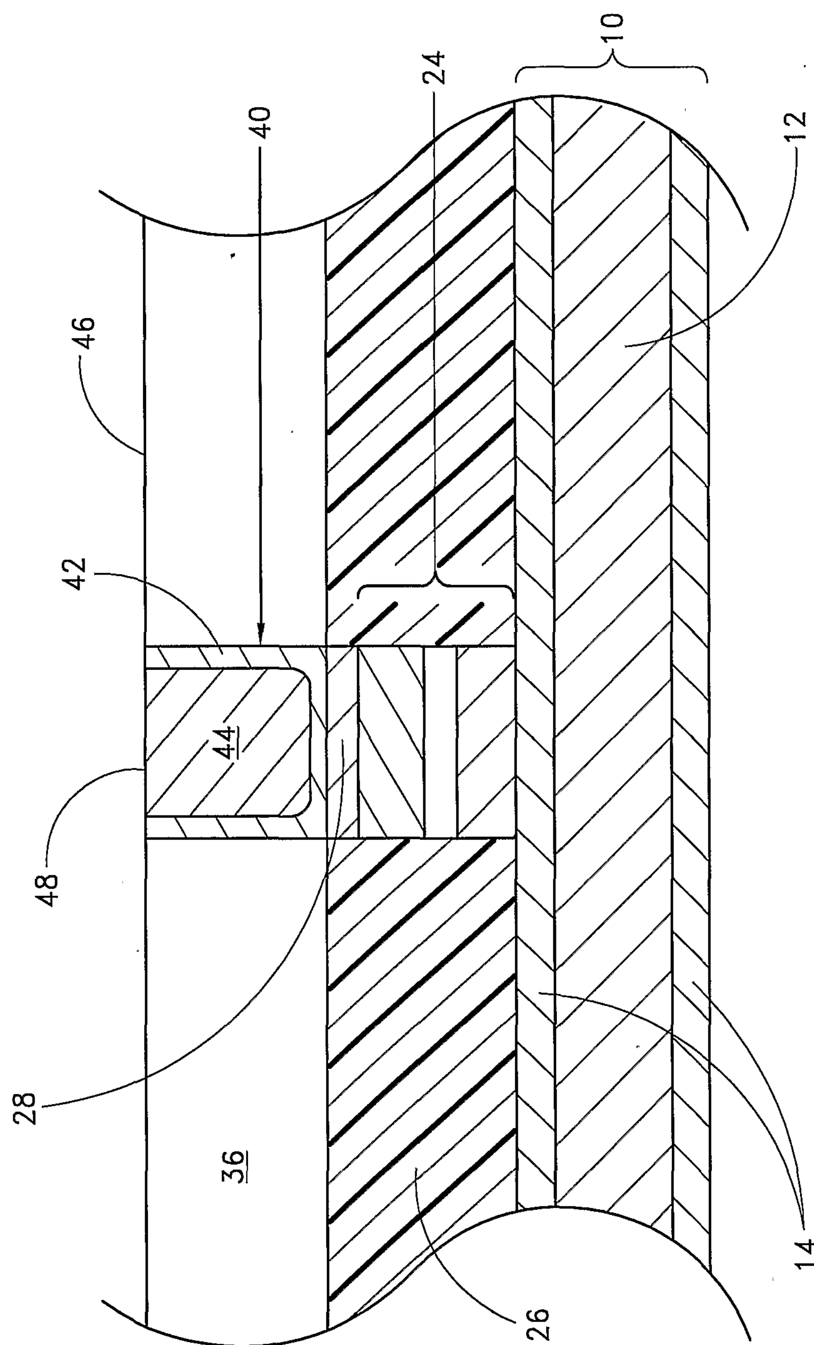

FIG. 2

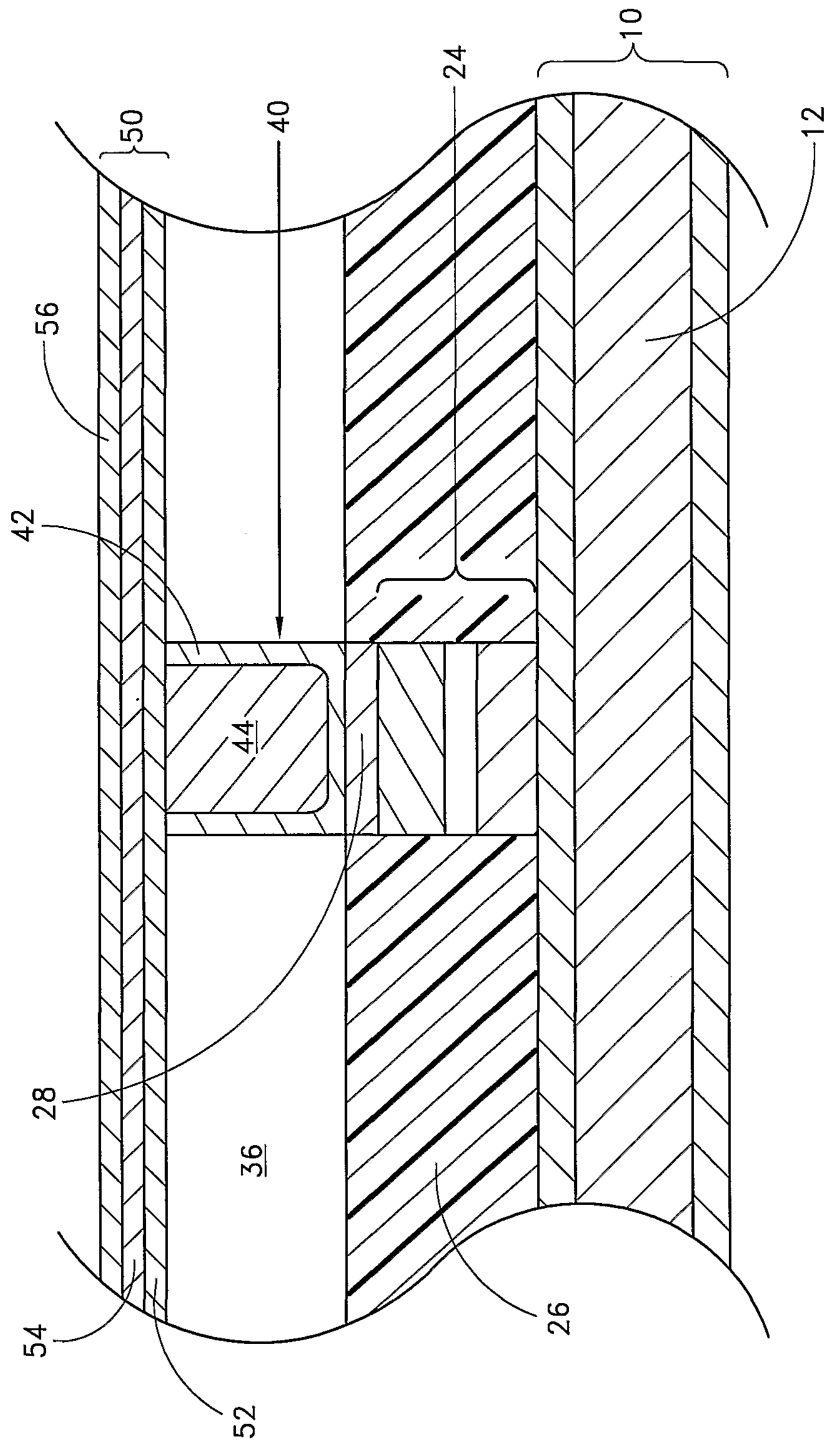

FIG. 3A

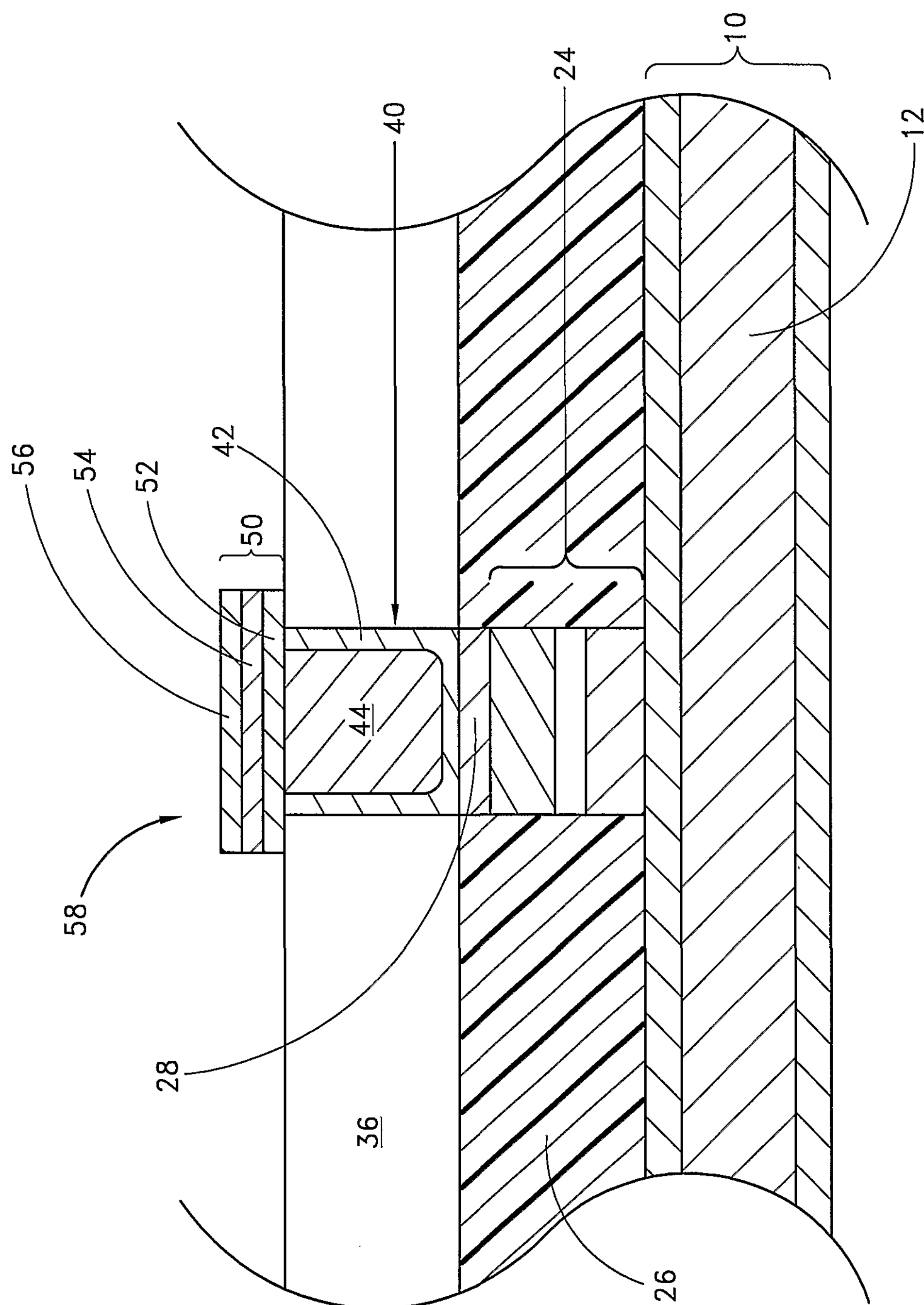

FIG. 3B

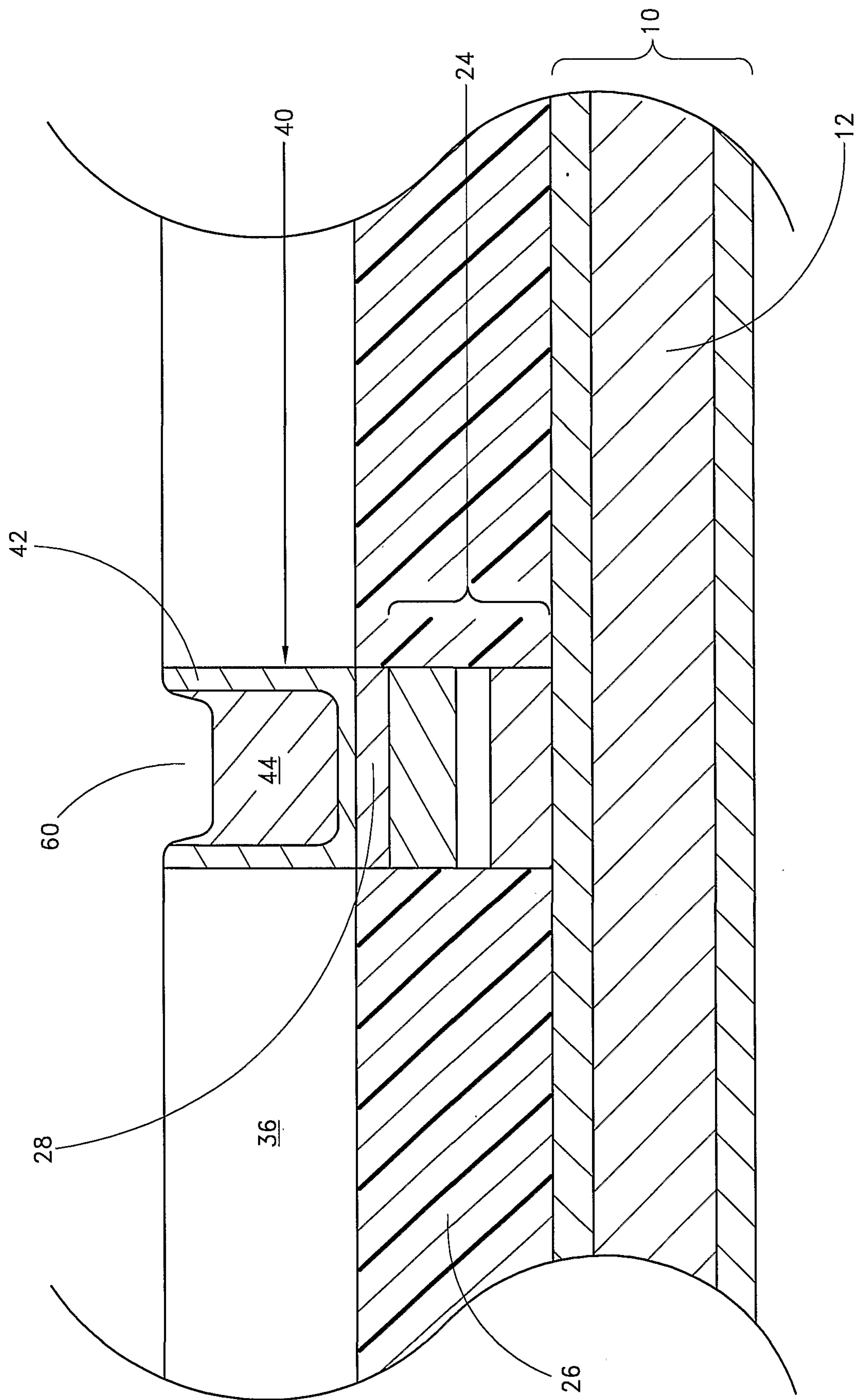

FIG. 4A

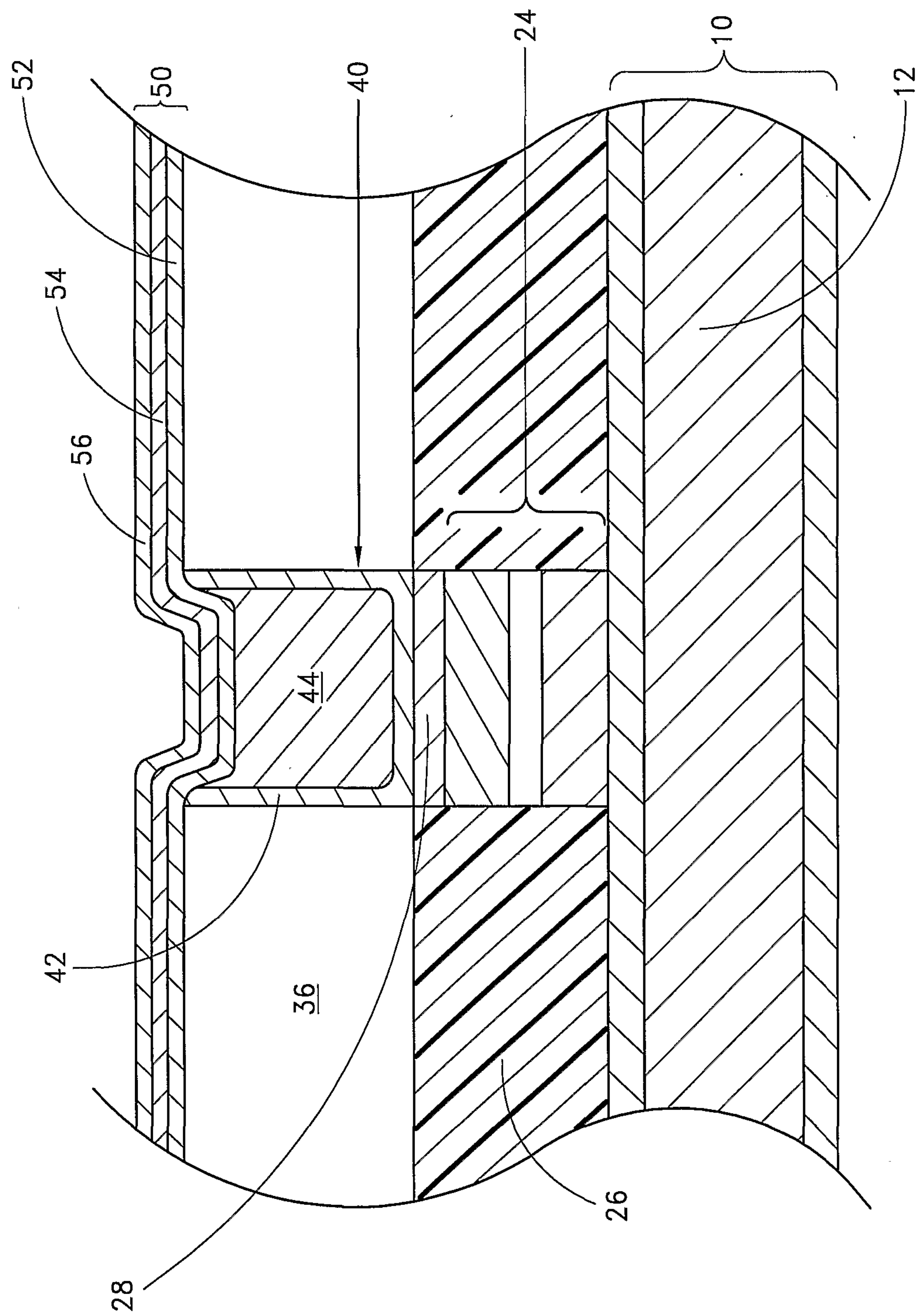

FIG. 4B

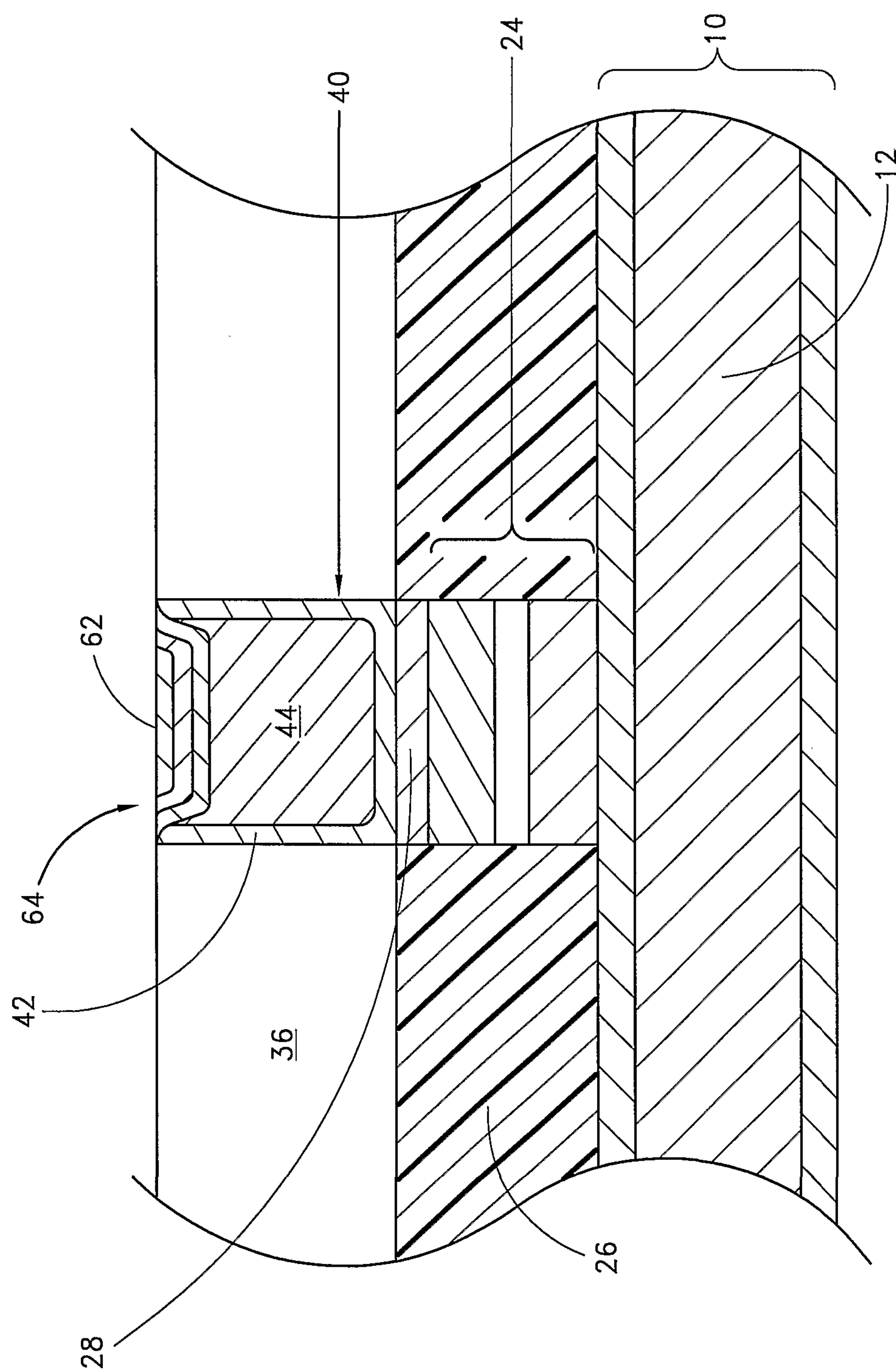

FIG. 4C

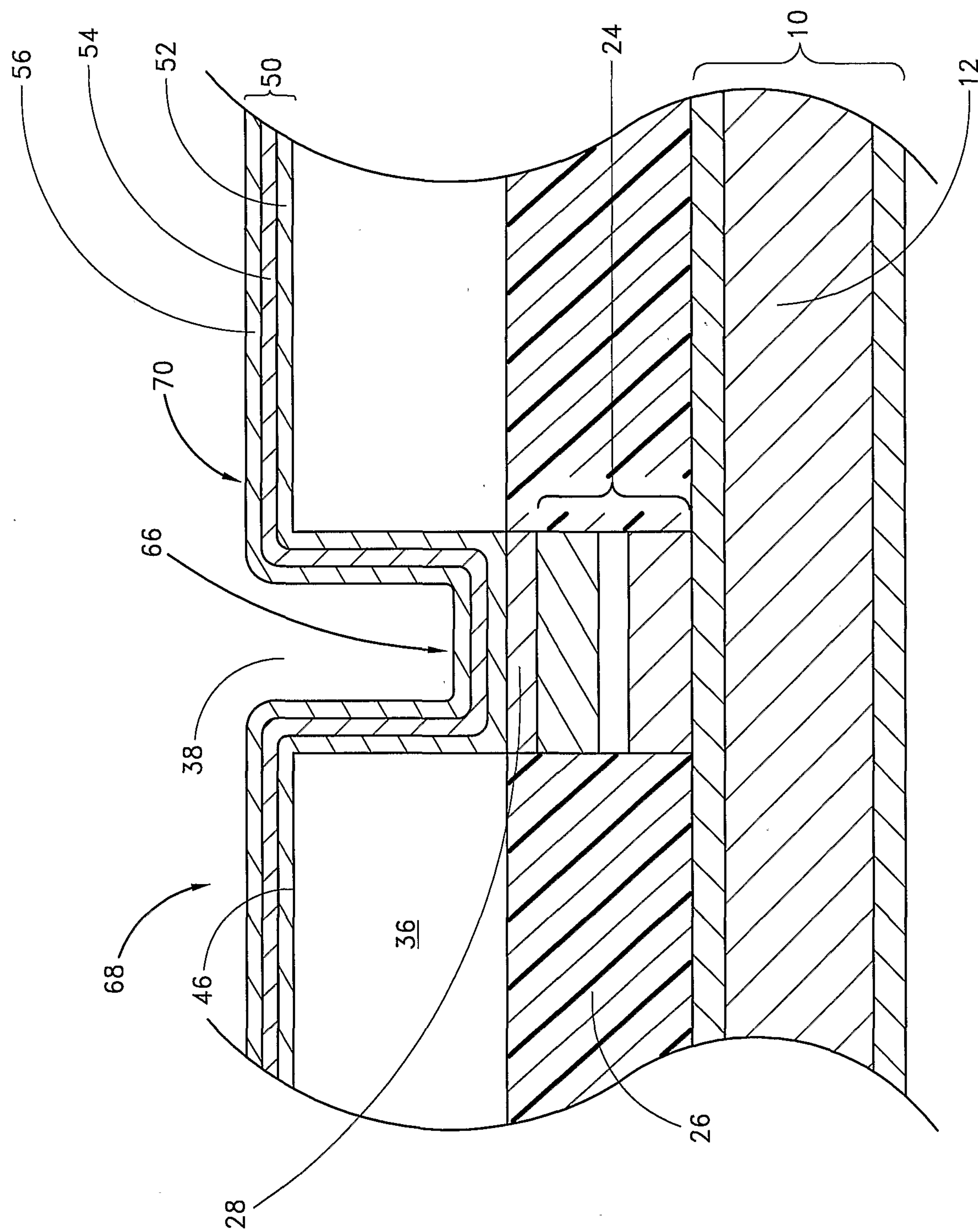

FIG. 5A

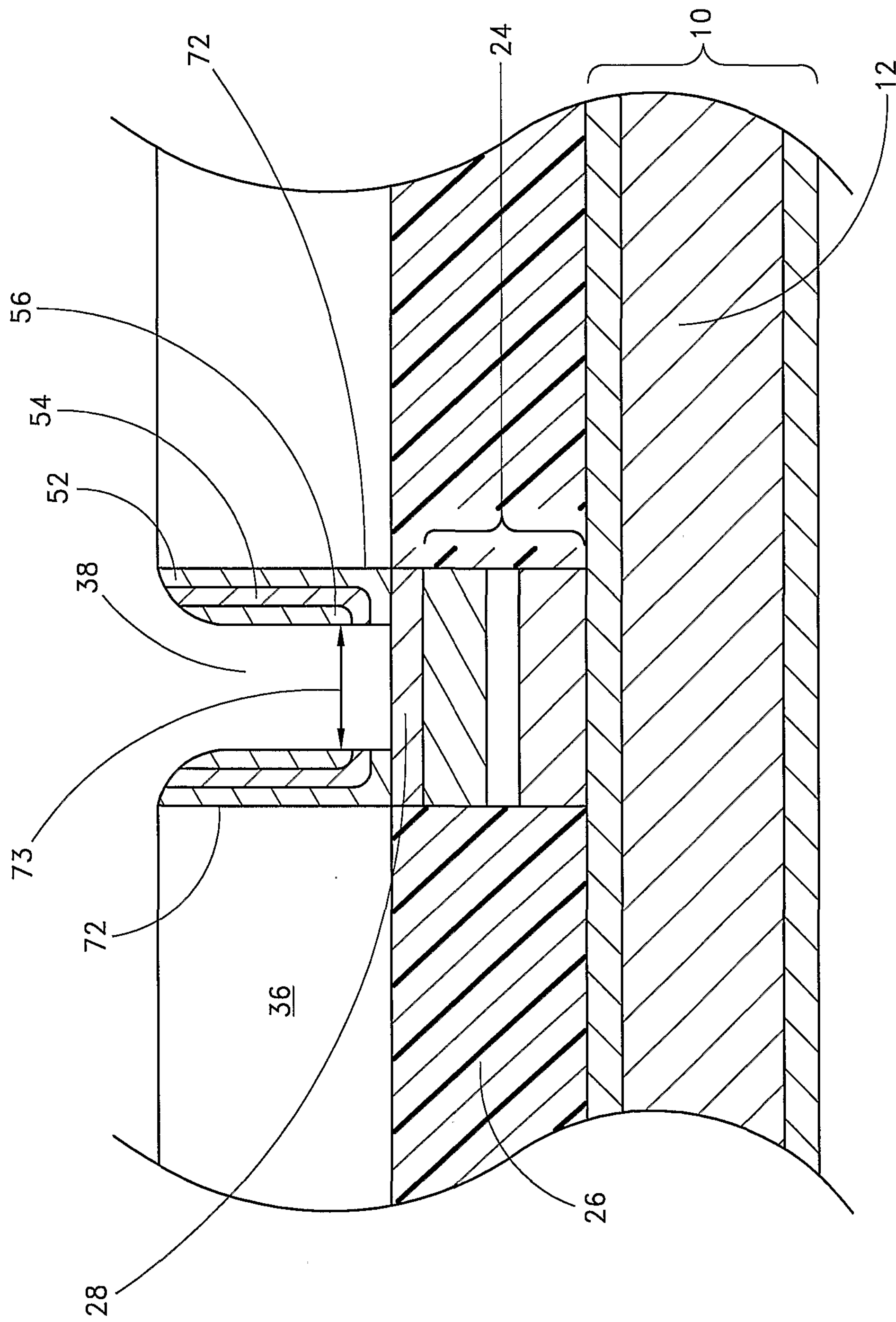

FIG. 5B

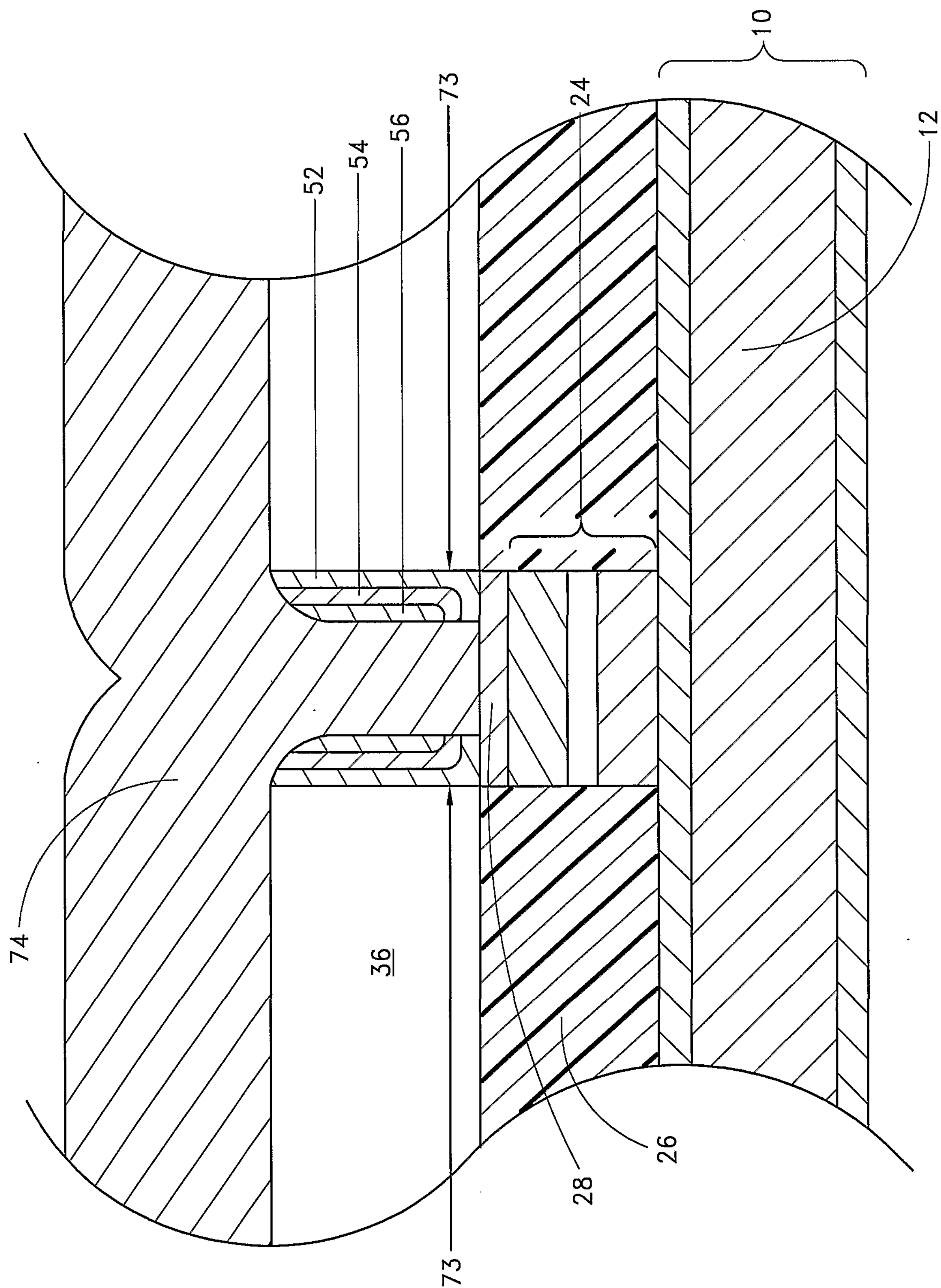

FIG. 5C

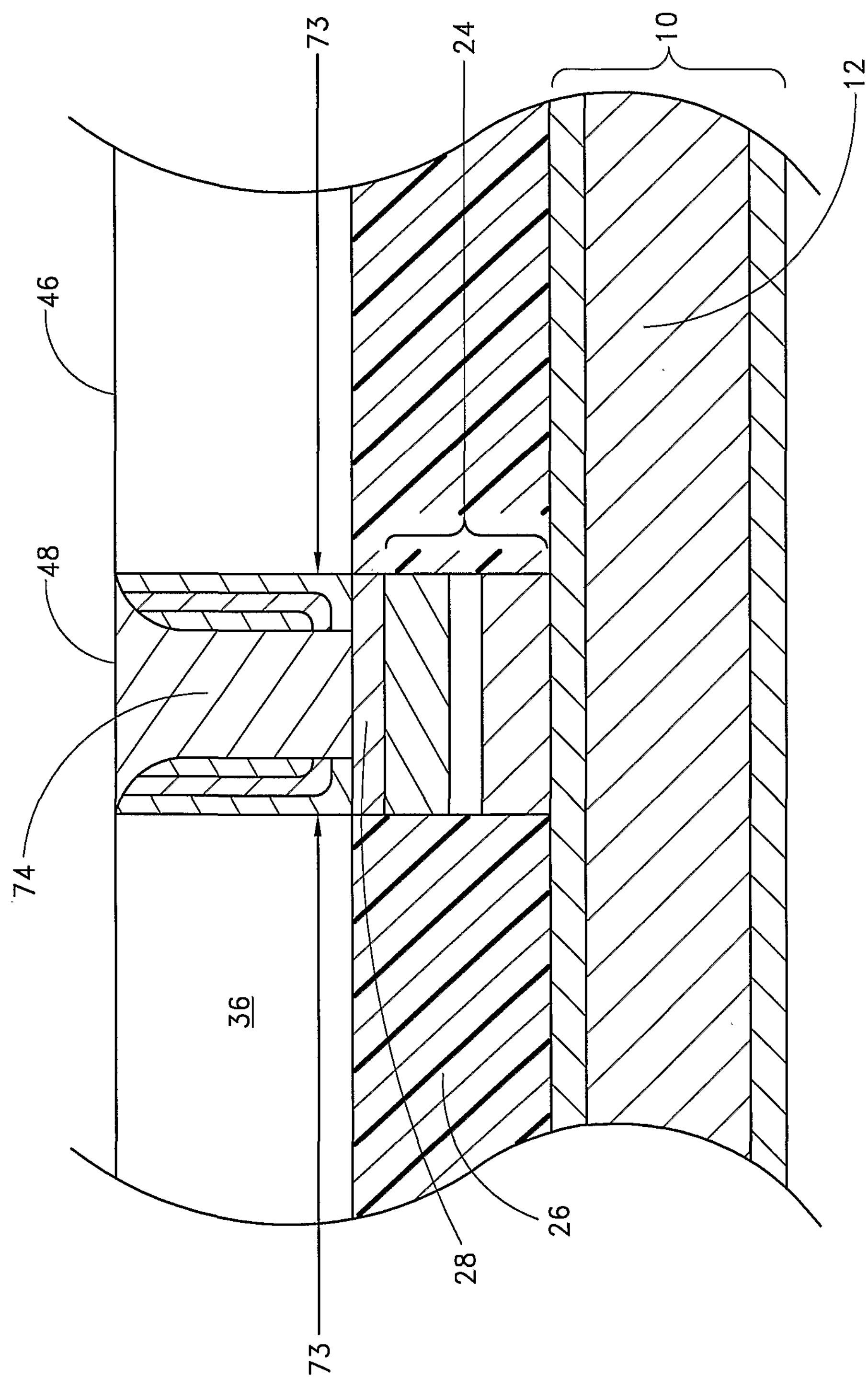

FIG. 5D

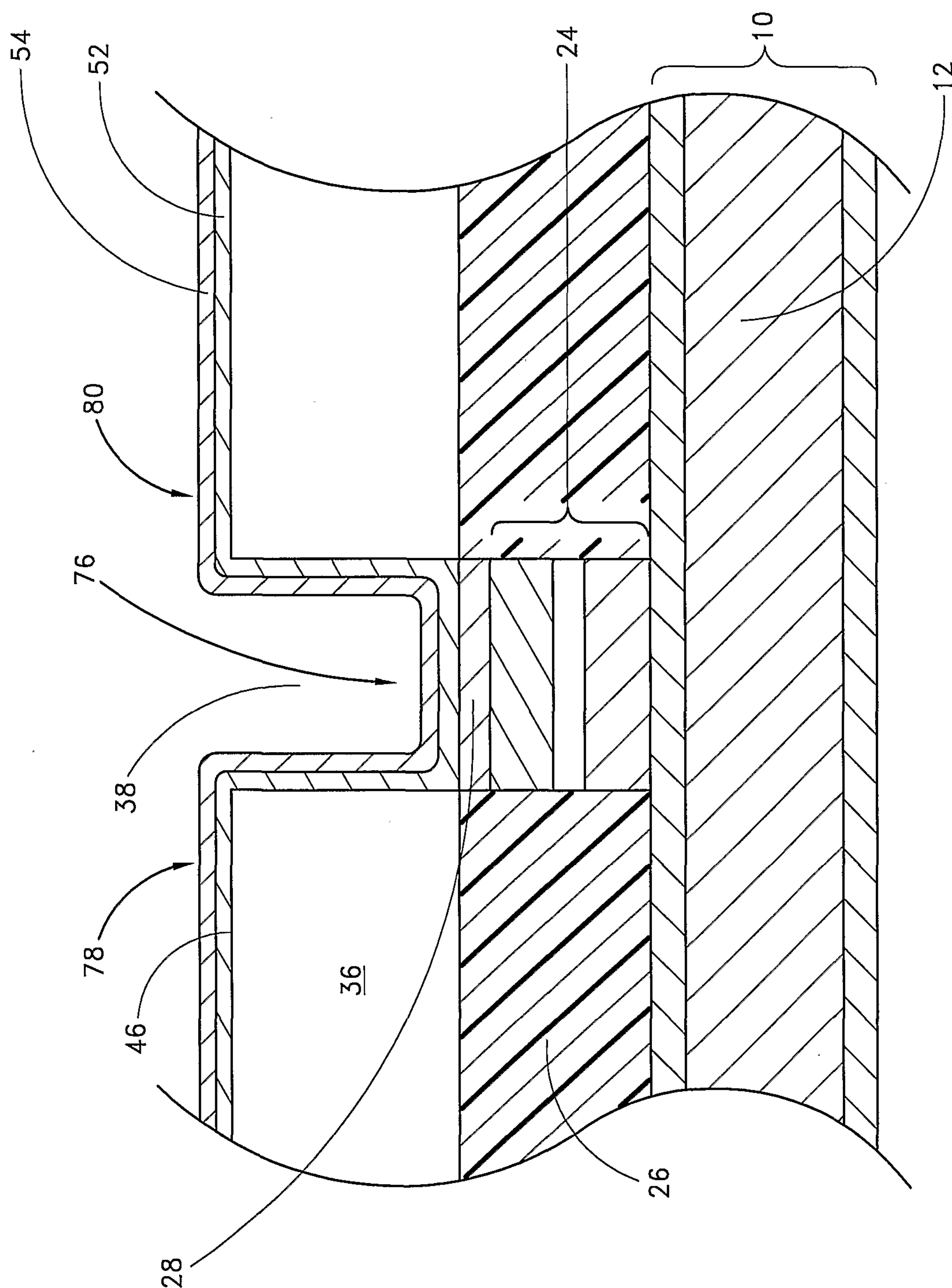

FIG. 6A

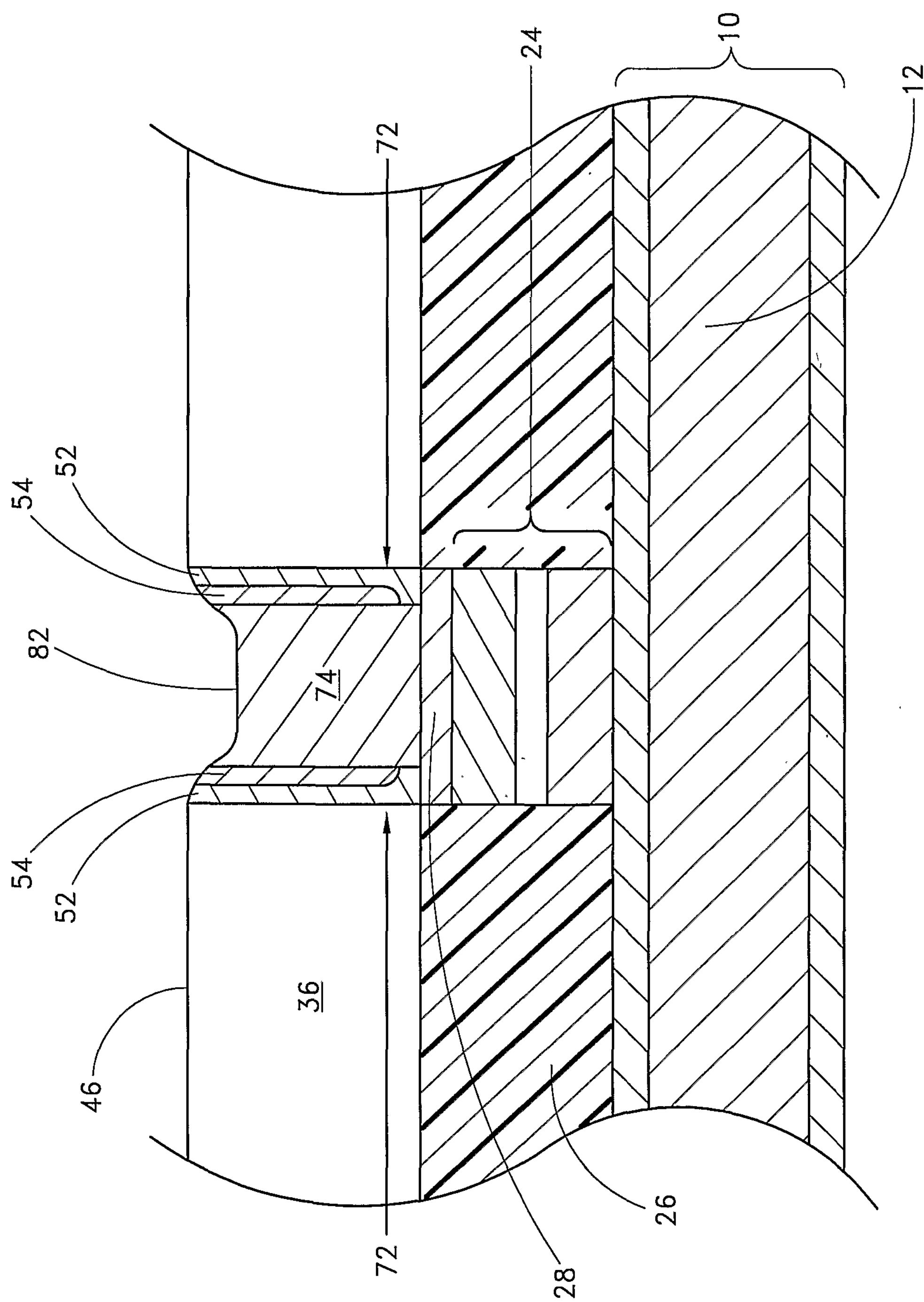

FIG. 6B

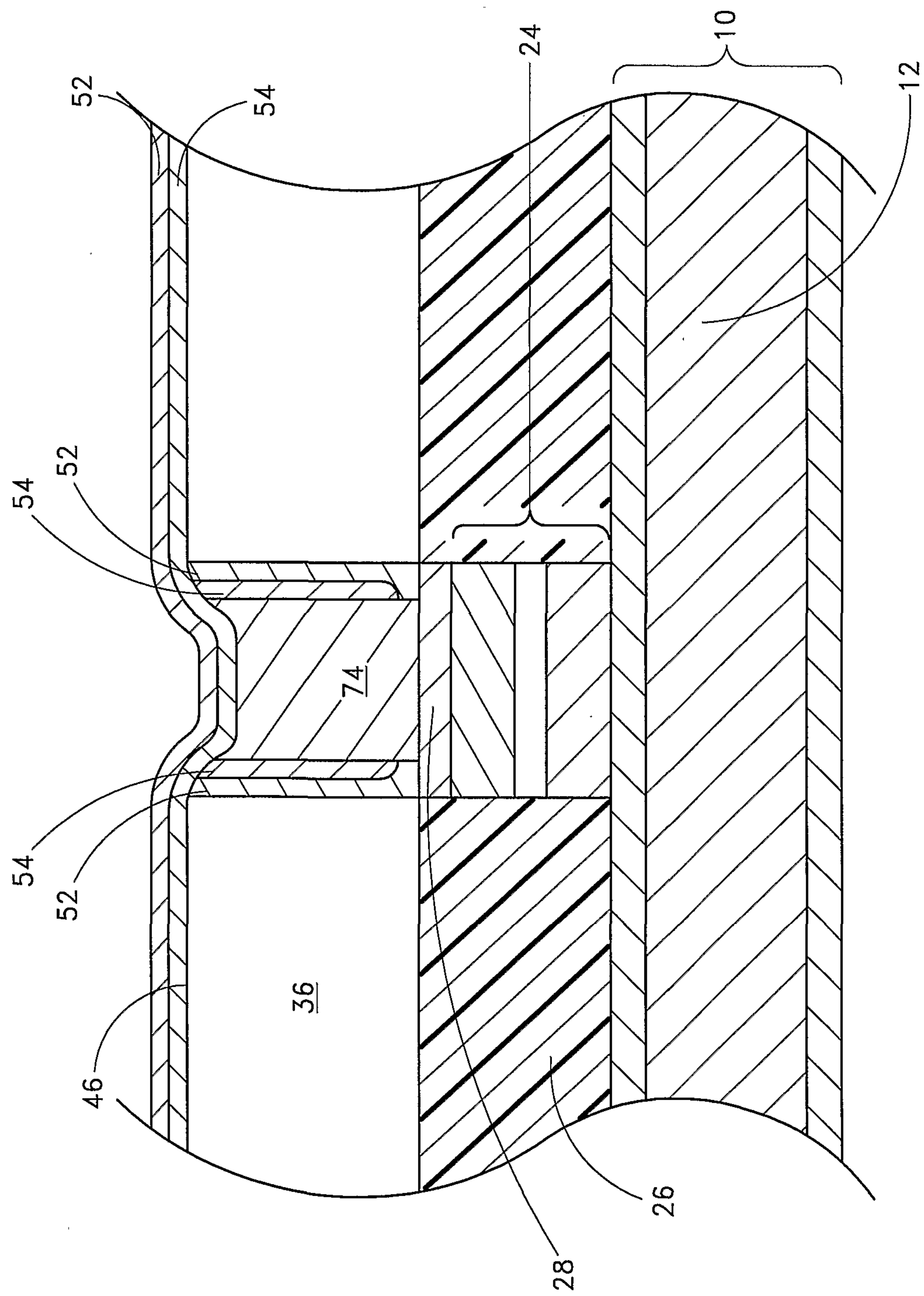

FIG. 6C

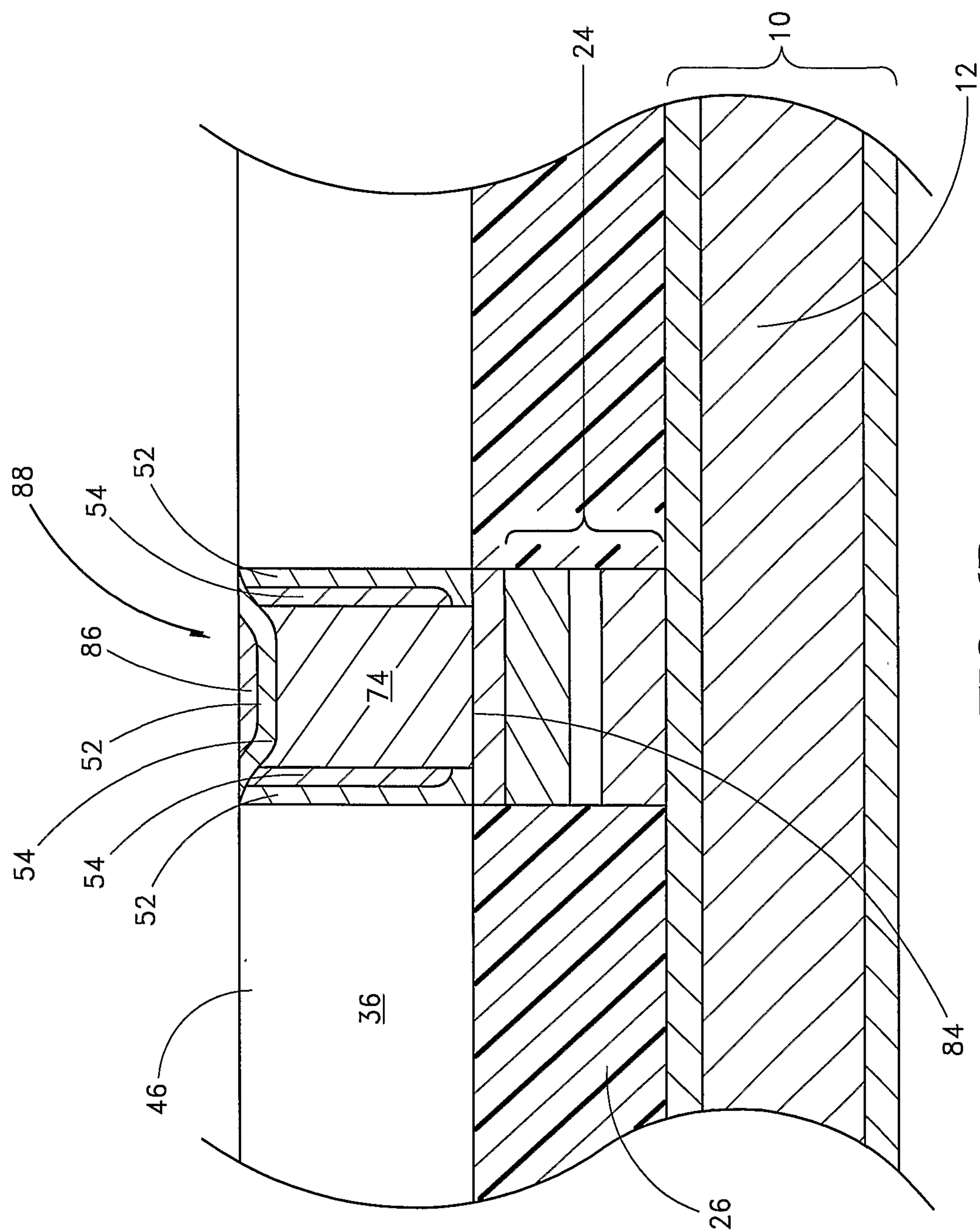

FIG. 6D