(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 October 2011 (20.10.2011)

PCT

(10) International Publication Number
WO 2011/129763 A1

(51) International Patent Classification:
H01L 21/44 (2006.01) *H01L 21/31* (2006.01)

(21) International Application Number:
PCT/SG2010/000145

(22) International Filing Date:
13 April 2010 (13.04.2010)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH** [SG/SG]; 1 Fusionopolis Way #20-10, Connexis, Singapore 138632 (SG).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **CHAI, Tai Chong** [MY/SG]; c/o Institute of Microelectronics, 11 Science Park Road, Singapore Science Park 2, Singapore 117685 (SG). **HO, Soon Wee** [SG/SG]; c/o Institute of Microelectronics, 11 Science Park Road, Singapore Science Park 2, Singapore 117685 (SG). **LIAO, Ebin** [SG/SG]; c/o Institute of Microelectronics, 11 Science Park Road, Singapore Science Park 2, Singapore 117685 (SG). **KHAN, Oratti Navas** [SG/SG]; c/o Institute of Microelectronics, 11 Science Park Road, Singapore Science Park 2, Singapore 117685 (SG). **VAIDYANATHAN, Kripesh** [IN/SG]; c/o Institute of Microelectronics, 11 Science Park Road, Singapore Science Park 2, Singapore 117685 (SG).

(74) Agent: **GOH, Su Lin, Audrey**; Viering, Jentschura & Partner LLP, P.O. Box 1088, Rochor Post Office, Rochor Road, Singapore 911833 (SG).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: AN INTERCONNECT STRUCTURE AND A METHOD OF FORMING THE SAME

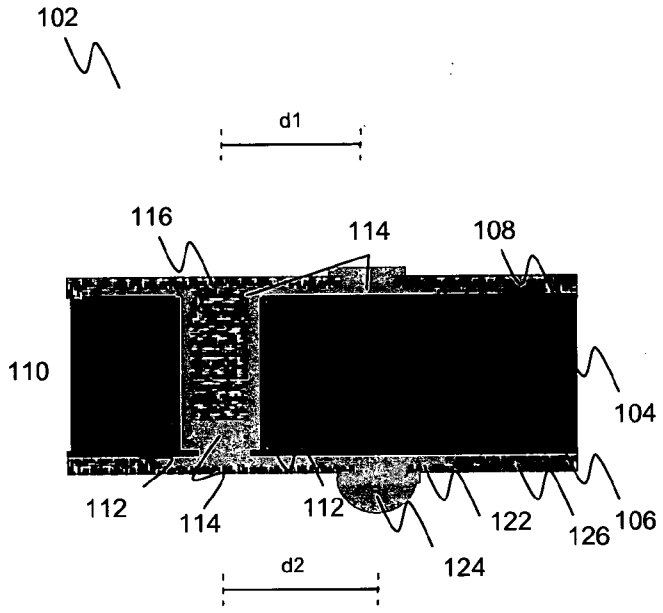


Figure 1

(57) Abstract: In an embodiment, an interconnect structure is provided. The interconnect structure may include a substrate including a bottom surface and a top surface arranged opposite to the bottom surface; a via formed in the substrate, the via including a sidewall; a conductive portion arranged in the via, wherein the conductive portion may have a thickness from the bottom surface to the top surface of the substrate which may be greater than its thickness from the sidewall of the via in a direction normal to the sidewall; and a dielectric portion arranged in the via and at least partially surrounded by the conductive portion. A method of forming an interconnect structure may also be provided.

WO 2011/129763 A1

Published:

— *with international search report (Art. 21(3))*

AN INTERCONNECT STRUCTURE AND A METHOD OF FORMING THE SAME

Technical Field

[0001] Embodiments relate to an interconnect structure and a method of forming the same.

Background

[0002] Three-dimensional (3D) packaging may play a very important role in supporting the demand for continuous miniaturization of products with improved performance, increased functionality and lower cost. Such requirements may require a compact package where multiple chips may be stacked within the same foot print. Through-silicon via (TSV) may be a key technology that may enable vertical inter-chip interconnectivity. It may allow heterogeneous integration of different chips to achieve a new application without the need for a more challenging system-on-chip approach.

[0003] An example may include a TSV with a parylene lining and a polymer dielectric lining for wafer level application. The parylene lining may help to achieve the isolation from a copper via to a silicon substrate. The TSV may also utilize conformal copper plating followed by spin-coated polymer filling for CMOS imaging sensor application. Another example may include a TSV with a polymer via using printing process for the polymer material followed by laser drilling on the polymer via and bottom up copper plating.

[0004] Most of the known TSV may involve a solid copper via structure and there may also be many reported works based on thermal-mechanical modeling for stress analysis of the TSV structure due to a coefficient of thermal expansion (CTE) mismatch between the copper via and silicon substrate. Most of these reported works have shown presence of a high stress concentration at the vicinity of a via corner region and expressed concern on long term reliability of the TSV. To address the reliability concerns, a TSV with tungsten and polysilicon for the electrical connectivity may have been developed. However, such a TSV may not be as well received as compared to copper as the conducting medium in the via due to the ease of process and existing tooling infrastructure.

[0005] Therefore, there is a need for an alternative TSV structure which may result in a compliant structure that may be more forgiven on a CTE induced stress between the silicon substrate and the copper via.

Summary

[0006] In various embodiments, an interconnect structure may be provided. The interconnect structure may include a substrate including a bottom surface and a top surface arranged opposite to the bottom surface; a via formed in the substrate, the via including a sidewall; a conductive portion arranged in the via, wherein the conductive portion may have a thickness from the bottom surface to the top surface of the substrate which may be greater than its thickness from the sidewall of the via in a direction normal to the sidewall; and a dielectric portion arranged in the via and at least partially surrounded by the conductive portion.

Brief Description of the Drawings

[0007] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of various embodiments. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

FIG. 1 shows an interconnect structure according to an embodiment;

FIG. 2 shows a flowchart illustrating a method of forming an interconnect structure according to an embodiment;

FIGs. 3A to 3H show respective cross-sectional views of a method of forming an interconnect structure according to an embodiment; and

FIG. 4 shows a method of forming a dielectric portion in two vias and over at least a portion of a conductive portion which has been formed over a top surface of a substrate according to an embodiment.

Description

[0008] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope

of the invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0009] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration". Any embodiment or design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments or designs.

[0010] An embodiment may provide an interconnect structure. The interconnect structure may include a substrate including a bottom surface and a top surface arranged opposite to the bottom surface; a via formed in the substrate, the via including a sidewall; a conductive portion arranged in the via, wherein the conductive portion may have a thickness from the bottom surface to the top surface of the substrate which may be greater than its thickness from the sidewall of the via in a direction normal to the sidewall; and a dielectric portion arranged in the via and at least partially surrounded by the conductive portion.

[0011] In an embodiment, the via may be formed in the substrate such that the via may extend from the bottom surface to the top surface of the substrate.

[0012] In an embodiment, the via may be formed in the substrate such that the via may include a substantially uniform cross-sectional dimension or a changing cross-sectional dimension as the via extends from the bottom surface to the top surface of the substrate. An example of the via with the changing cross-sectional dimension may be a tapered via.

[0013] In an embodiment, the interconnect structure may include a plurality of vias formed in the substrate depending on user and design requirements. Each of the plurality of vias may be spaced at a same or different distance away from each other. Each of the plurality of vias may include a same or different cross-sectional dimension.

[0014] In an embodiment, the dielectric portion may include a polymer portion.

[0015] In an embodiment, the dielectric portion arranged in the via may form a core portion of the via.

[0016] In an embodiment, the conductive portion may be further disposed over the top surface of the substrate, the conductive portion being configured to connect to a first next layer connection at a first distance away from the via. The first distance may include any distance typically required on an integrated circuit (IC) chip.

[0017] In an embodiment, the first next layer connection may include an under-bump metallization (UBM). The first next layer connection may also include one or more metal lines in combination with the UBM. The number of metal lines depend on the application, for example for high density wiring.

[0018] In an embodiment, the dielectric portion may be further disposed over at least a portion of the conductive portion which may have been disposed over the top surface of the substrate. The dielectric portion may also be disposed over the substrate depending on design and user requirements.

[0019] In an embodiment, the interconnect structure may further include a barrier layer disposed between the substrate and the conductive portion. One purpose of the barrier layer may be to prevent inter-diffusion of the conductive portion onto the substrate. The barrier layer may include a thickness in the range of about 10 nm to about

100 nm, for example about 50 nm. The thickness of the barrier layer may vary depending on the material used. Further, the thickness of the entire barrier layer may not be uniform because the barrier layer may be coated inside a vertical via. One upper side of the barrier layer (or from the bottom surface of the substrate) may be thicker when compared to the lower side of the barrier layer (from the sidewall of the via). It may be critical to ensure a continuous barrier layer between the substrate and the conductive portion to ensure substantially no diffusion of the conductive portion (e.g. copper) into the substrate.

[0020] In an embodiment, the barrier layer may include a material selected from a group consisting of titanium (Ti), titanium nitride (TiN), silicon carbide, silicon oxycarbide, silicon oxide, for example.

[0021] In an embodiment, the interconnect structure may further include a seed layer disposed between the barrier layer and the conductive portion. The seed layer may also serve as a barrier layer and may form a conductive layer to support subsequent copper electro-plating process (i.e. ease any subsequent deposition of the conductive portion).

[0022] In an embodiment, the seed layer may include copper for example. The seed layer may also be of the same material as the subsequent conductive portion to be deposited or electroplated.

[0023] In an embodiment, the interconnect structure may further include a further conductive portion disposed over the bottom surface of the substrate and in electrical connection with the conductive portion in the via, the further conductive portion being configured to connect to a second next layer connection at a second distance away from the via.

[0024] In an embodiment, the second next layer connection may include an under-bump metallization.

[0025] In an embodiment, the first distance may be the same or different from the second distance.

[0026] In an embodiment, the interconnect structure may further include a further dielectric portion disposed over at least a portion of the further conductive portion. The further dielectric portion may also be disposed over the substrate depending on design and user requirements.

[0027] In an embodiment, the dielectric portion may include polymer in dry film format or in liquid form. In the case of dry film, the dry film may be overlaid on the via and this may be follow by compression of the dry film into the via hence filling up the via. In the case of the liquid polymer, the liquid polymer may be spun coated with suitable mechanical properties for spin coating and via filling purpose.

[0028] In an embodiment, the further dielectric portion may be of the same or different material as the dielectric portion.

[0029] In an embodiment, the conductive portion may include a material selected from a group consisting of copper, nickel for example.

[0030] In an embodiment, the further conductive portion may be of the same or different material as the conductive portion.

[0031] In an embodiment, the substrate comprises a material selected from a group consisting of silicon, glass or the equivalent for example. The substrate may be of a semiconductor material.

[0032] An embodiment may provide a method of forming an interconnect structure. The method may include providing a substrate, the substrate including a bottom surface and a top surface arranged opposite to the bottom surface; forming a via in the substrate, the via including a sidewall; forming a conductive portion in the via; wherein the conductive portion may have a thickness from the bottom surface to the top surface of the substrate which may be greater than its thickness from the sidewall of the via in a direction normal to the sidewall; and forming a dielectric portion in the via and at least partially surrounded by the conductive portion.

[0033] In an embodiment, forming the via in the substrate may include forming the via by one or more of a group consisting of lithography and deep reactive-ion etching (DRIE). Any other suitable lithography and etching method may also be used.

[0034] In an embodiment, the method may further include forming a barrier layer over the substrate.

[0035] In an embodiment, the barrier layer may include a material selected from a group consisting of Ti, TiN, silicon carbide, silicon oxycarbide, silicon oxide, for example.

[0036] In an embodiment, the method may further include forming a seed layer over the barrier layer.

[0037] In an embodiment, the seed layer may include a material selected from a group consisting of copper.

[0038] In an embodiment, the method may further include forming the conductive portion over the top surface of the substrate, the conductive portion being configured to connect to a first next layer connection at a first distance away from the via.

[0039] In an embodiment, the first next layer connection may further include an under-bump metallization.

[0040] In an embodiment, forming the conductive portion in the via and forming the conductive portion over the top surface of the substrate may be performed at the same time.

[0041] In an embodiment, forming the conductive portion in the via and forming the conductive portion over the top surface of the substrate may include forming a dry film resist over the substrate; forming an opening in the dry film resist, the opening positioned and sized so as to at least correspond to the via; depositing a conductive layer in the opening; and removing the dry film resist.

[0042] In an embodiment, the conductive layer may be deposited by electroplating, for example copper electroplating.

[0043] In an embodiment, the dielectric portion formed in the via may form a core portion of the via.

[0044] In an embodiment, the method may further include forming the dielectric portion over at least a portion of the conductive portion which may have been formed over the top surface of the substrate.

[0045] In an embodiment, forming the dielectric portion in the via and forming the dielectric portion over at least the portion of the conductive portion which has been formed over the top surface of the substrate may be performed at the same time.

[0046] In an embodiment, forming the dielectric portion in the via and forming the dielectric portion over at least a portion of the conductive portion which has been formed over the top surface of the substrate may include positioning a dry film layered structure

over the substrate; the dry film layered structure may include a dry film dielectric layer; and a dry film lining disposed over the dry film dielectric layer; and applying pressure and heat onto the dry film layered structure to allow the dry film dielectric layer to be formed in the via and over at least the portion of the conductive portion which has been formed over the top surface of the substrate. The dry film dielectric layer is the material to be filled in the via eventually. The dry film lining may be a protection layer arranged on the dry film dielectric layer so as to prevent the dry film dielectric layer from sticking to a pressure chuck table during a thermal compression process. After the via filling may be completed, the dry film lining may be removed easily by peeling the dry film lining away and disposing the dry film lining.

[0047] In an embodiment, forming the via in the substrate may further include forming the via such that the via may extend from the bottom surface to the top surface of the substrate.

[0048] In an embodiment, forming the via such that the via may extend from the bottom surface to the top surface of the substrate may include providing a support substrate; bonding the support substrate to the dielectric portion; and reducing thickness of the substrate from the bottom surface towards the top surface of the substrate such that the via extends from the bottom surface to the top surface of the substrate to expose the conductive portion in the via.

[0049] In an embodiment, reducing thickness of the substrate from the bottom surface towards the top surface of the substrate may include reducing the thickness by one or more of a group consisting of backgrind, planarization, wet etching and dry etching for example.

[0050] In an embodiment, forming the via may further include forming the via such that the via may include a substantially uniform cross-sectional dimension or a changing cross-sectional dimension as the via may extend from the bottom surface to the top surface of the substrate.

[0051] In an embodiment, the method may further include forming a further conductive portion over the bottom surface of the substrate and in electrical connection with the conductive portion in the via, the further conductive portion being configured to connect to a second next layer connection at a second distance away from the via.

[0052] In an embodiment, the second next layer connection may include an under-bump metallization.

[0053] In an embodiment, the method may further include forming a further dielectric portion over at least a portion of the further conductive portion.

[0054] In an embodiment, the method may further include removing the support substrate after forming the further conductive portion and the further dielectric portion.

[0055] In an embodiment, the dielectric portion may include polymer in dry film format or in liquid form.

[0056] In an embodiment, the further dielectric portion may be of the same material as the dielectric portion.

[0057] In an embodiment, the conductive portion may include a material selected from a group consisting of copper, nickel, for example.

[0058] In an embodiment, the further conductive portion may be of the same material as the conductive portion.

[0059] In an embodiment, the substrate may include a material selected from a group consisting of silicon, glass and the equivalent for example.

[0060] In an embodiment, the dielectric portion may include a polymer portion.

[0061] In an embodiment, a novel Through-Silicon Via (TSV) technology may have been developed for a silicon (Si) interposer application. The TSV may replace the solid filled copper (Cu) via with a partial plated copper via for interconnection. Further, polymeric filling inside the via may result in a compliant structure that may be more forgiven on CTE induced stress between Si and Cu via. Thermal-mechanical modeling has shown that more than about 50% shear stress reduction in Si may be possible when a typical 50um diameter TSV with solid filled Cu may be replaced with polymer filled via with no significant impact on electrical performance of the TSV due to skin effect for high frequency interconnection. Thermal modeling may have also shown little or no difference on thermal dissipation for stack chip package utilizing polymer filled via compared to solid Cu via.

[0062] In addition to the novel TSV structure, a new fabrication processes which may result in a simplified TSV fabrication process may be disclosed. A redistribution layer (RDL) may be formed along with partial Cu plating process using a pre-defined dry film resist layer prior to Cu plating. This may allow elimination of a need for Cu overburden removal after Cu plating.

[0063] Further, a novel polymer filling process using a dry film laminated method with simultaneous formation of a dielectric layer may also be established.

[0064] In an embodiment, a novel TSV structure including a partial Cu superfilling which may form a RDL line simultaneously, and polymer dielectric filled inside the

partial Cu plated via may be disclosed. The presence of thinner side wall and polymeric material in the core may provide compliancy to the TSV structure to try to reduce thermal-mechanical stress induced by CTE mismatch between Cu and Si.

[0065] In an embodiment, a method of fabrication of the polymer filled via may also be provided.

[0066] In an embodiment, a novel polymer filled via structure in a silicon substrate or interposer may be disclosed. The TSV may include partial Cu superfilling with thinner sidewall and thicker Cu layer at the bottom of via. At the top side, the partially plated Cu may be connected directly with horizontal Cu line or redistribution layer metallization. The partial plated via may be filled entirely with polymer material which may also form the horizontal dielectric layer on the redistribution metallization. At the end of the redistribution metal layer, there may be an vertical connection to a under-bump metallization (UBM) to form a receiving pad for solder interconnection to other bumped chips. At the bottom side, the partial plated Cu may have a thicker Cu layer to ensure that Cu may be present on the entire via diameter area after via exposure process for good contact with bottom metallization. Again at the end of the metallization layer, there may be a vertical connection to UBM for solder joint interconnection.

[0067] In an embodiment, a fabrication process sequence for the formation of partial Cu superfilling and simultaneously forming horizontal redistribution metallization layer may be disclosed. The process may start with DRIE via etch such as Bosch process, followed by isolation oxide process (or barrier layer), seed layer and dry film resist process to define the electroplating area, including the redistribution metal line. This may be followed by electro-copper-plating (ECP) to form superfilling (for example high

plating rate at bottom of via then the sidewall) resulting in controlled Cu layer thickness at the via bottom. Ideally, a relatively thick Cu (for example 30 um) layer may be electroplated at the via bottom, while a relatively thin Cu (for example 8um) may be desired along the via sidewall. The thick Cu at via bottom may be needed to accommodate the process tolerance of subsequent backside grinding process, which may expose the TSV interconnection from the backside. The thin Cu along the sidewall may be needed to reduce the stress level, which otherwise may be high in the case of fully filled Cu TSV interconnection. To achieve this electroplating thickness control which may be against the natural electrical field and Cu ion concentration distribution in the TSV, specially prepared TSV electroplating chemistry and plating current waveform may be two of the most important factors. The thickness required may depend on subsequent via exposure process capability and via depth variations. For example, for via depth of 200um with +/- 5 % depth variation, and via exposure process variation of +/- 2 um, a Cu layer thickness of at least about 30um may be required to ensure there may be sufficient Cu presence at the via bottom after via exposure.

[0068] After the ECP process, the dry film resist layer and excess seed layer may be removed and the wafer or substrate may be ready for polymer filling process. A dry film dielectric layer of some uniform thickness for polymer filling using a lamination method may be used. To prevent any void being trapped inside the via, the entire wafer and the dry film may be placed inside a vacuum chamber which may include a thermally heated chuck table and be subjected to compression under heat and pressure at the same time. This may allow the dielectric film to become soften and fluidic such that the dielectric film may flow into the via under pressure. Dielectric film thickness may be achieved by

controlling the thermo-compression process, the film thickness, via size and via depth. After via filling may be completed, the whole process of via and RDL formation, and polymer filling may be considered complete. Subsequent processes such as top-side bump formation and bottom-side via exposure and bump formation may follow typical fabrication processes.

[0069] In an embodiment, a unique TSV structure with polymer filling in the core of a partially plated Cu via with thicker bottom layer may be disclosed.

[0070] In an embodiment, a novel dry film dielectric lamination process for polymer filling which may simultaneously form a dielectric layer for the RDL layer may be disclosed.

[0071] In an embodiment, there may be several advantages of the interconnect structure and the method of forming the same. Most of current technology may use a solid filled Cu via which may have a large thermal-mechanical stress at a vicinity of a via corner due to CTE mismatch between Cu and Si. Polymer filled via may have shown a stress reduction by about 57% as compared to a solid filled Cu via.

[0072] In an embodiment, existing TSV technology involving a solid filled Cu via may require a longer process time. The current interconnect stucture and method of forming the same may use partially plated Cu, hence a shorted processing time may be achieved.

[0073] In an embodiment, existing TSV technology involving a solid filled Cu via may required a chemical mechanical polishing (CMP) process for overburden removal. The current interconnect stucture and method of forming the same may not require the CMP process for overburden removal.

[0074] In an embodiment, a polymer filled TSV via structure with thicker bottom metal layer and via core filled with polymer material may be disclosed.

[0075] In an embodiment, a method of fabricating the polymer filled via may be disclosed. The method may achieve a thicker bottom layer inside the via. The method may allow via plating and simultaneously forming RDL layer using patterned dry film resist prior to ECP. The method may also allow dielectric filling in the via. The method of polymer via filling and simultaneously forming dielectric layer on the wafer may be performed using a dielectric film lamination method.

[0076] FIG. 1 shows an interconnect structure 102 according to an embodiment. The interconnect structure 102 may include a substrate 104 including a bottom surface 106 and a top surface 108 arranged opposite to the bottom surface 106; a via 110 formed in the substrate 104, the via 110 including a sidewall 112; a conductive portion 114 arranged in the via 110, wherein the conductive portion 114 may have a thickness from the bottom surface 106 to the top surface 108 of the substrate 104 which is greater than its thickness from the sidewall 112 of the via 110 in a direction normal to the sidewall 112; and a dielectric portion 116 arranged in the via 110 and at least partially surrounded by the conductive portion 114.

[0077] In an embodiment, the conductive portion 114 may include a thickness from the bottom surface 106 to the top surface 108 of the substrate 104 of about twice that of the thickness from the sidewall 112 of the via 110 in a direction normal to the sidewall 112. For example, the ratio of the thickness from the bottom surface 106 to the top surface 108 of the substrate 104 to the thickness from the sidewall 112 may be larger than 1 (i.e. as long as the thickness from the bottom surface 106 to the top surface 108 of the

substrate 104 is larger than the thickness from the sidewall 112). As a further example, the thickness from the bottom surface 106 to the top surface 108 of the substrate 104 may be in a range of about 1 um to about 30 um and the thickness from the respective sidewalls 112 may be in a range of about 1 um to about 10 um. The thickness from the bottom surface 106 to the top surface 108 of the substrate 104 and the thickness from the sidewall 112 may vary according to user and design variations.

[0078] The via 110 may be formed in the substrate 104 such that the via 110 may extend all the way through from the bottom surface 106 to the top surface 108 of the substrate 104. The via 110 may also be formed in the substrate 104 such that the via 110 includes a substantially uniform cross-sectional dimension or a changing cross-sectional dimension as the via 110 extends from the bottom surface 106 to the top surface 108 of the substrate 104. In FIG. 1, the via 110 may be of a substantially uniform cross-sectional dimension as the via 110 extends from the bottom surface 106 to the top surface 108 of the substrate 104. The via 110 may be a cylindrical via. However from the 2D cross-sectional view as shown in FIG. 1, the via 110 may be seen to have two sidewalls 112 (when in fact the two sidewalls 112 are one single integrated sidewall) .

[0079] In an embodiment, the dielectric portion 116 may include a polymer portion. The dielectric portion 116 arranged in the via 110 may form a core portion of the via 110.

[0080] The conductive portion 114 may be further disposed over the top surface 108 of the substrate 104, the conductive portion 114 being configured to connect to the first next layer connection (or first external connection) (not shown) at a first distance away from the via 110. The first distance may be represented by "d1". For example, for a one layer configuration, the first next layer connection may include an under-bump

metallization (UBM). However, it may also be possible to have a multiple layer configuration. Then the first next layer connection may include conductive layers or conductive portions configured for next layer connection.

[0081] The dielectric portion 116 may be further disposed over at least a portion of the conductive portion 114 which has been disposed over the top surface 108 of the substrate 104.

[0082] The interconnect structure 102 may further include a barrier layer (not shown) disposed between the substrate 104 and the conductive portion 114. The barrier layer may include a material selected from a group consisting of Ti, TiN, silicon carbide, silicon oxycarbide, silicon oxide, for example.

[0083] The interconnect structure 102 may further include a seed layer (not shown) disposed between the barrier layer and the conductive portion 114. The seed layer may include copper.

[0084] The interconnect structure 102 may further include a further conductive portion 122 disposed over the bottom surface 106 of the substrate 104 and in electrical connection with the conductive portion 114 in the via 110, the further conductive portion 122 being configured to connect to the second next layer connection or second external connection 124 at a second distance away from the via 110. The second distance may be any suitable distance depending on design and user requirements. The second distance may be represented by "d2". For example, for a one layer configuration, the second next layer connection may include an under-bump metallization (UBM). However, it may also be possible to have a multiple layer configuration. Then the second next layer connection

may include conductive layers or conductive portions configured for next layer connection.

[0085] The interconnect structure 102 may further include a further dielectric portion 126 disposed over at least a portion of the further conductive portion 122. The dielectric portion 116 may include a polymer in dry film format or in liquid form. The further dielectric portion 126 may be of the same material or different material as the dielectric portion 116.

[0086] The conductive portion 114 may include a material selected from a group consisting of copper, nickel, for example. The further conductive portion 122 may be of the same material as the conductive portion 114. The conductive portion 114 and the further conductive portion 122 may be formed such that the conductive portion 114 and the further conductive portion 122 may be one integrated portion.

[0087] The substrate 104 may include a material selected from a group consisting of silicon, glass substrate or the equivalent, for example.

[0088] FIG. 2 shows a flowchart 2000 illustrating a method of forming an interconnect structure 102 according to an embodiment.

[0089] At 2002, the method may include providing a substrate 104, the substrate 104 including a bottom surface 106 and a top surface 108 arranged opposite to the bottom surface 106.

[0090] At 2004, the method may include forming a via 110 in the substrate 104, the via 110 including a sidewall 112.

[0091] At 2006, the method may include forming a conductive portion 114 in the via 110; wherein the conductive portion 114 may have a thickness from the bottom surface

106 to the top surface 108 of the substrate 104 which may be greater than its thickness from the sidewall 112 of the via 110 in a direction normal to the sidewall 112.

[0092] At 2008, the method may include forming a dielectric portion 116 in the via 110 and at least partially surrounded by the conductive portion 114.

[0093] FIGs. 3A to 3H show respective cross-sectional views of a method of forming an interconnect structure 102 according to an embodiment.

[0094] FIG. 3A shows lithography and deep reactive-ion etching (DRIE). In FIG. 3A, the method may include providing a substrate 104, the substrate 104 including a bottom surface 106 and a top surface 108 arranged opposite to the bottom surface 106. The substrate 104 may include a material selected from a group consisting of silicon, for example.

[0095] Two respective vias 110 may be formed in the substrate 104, each of the two vias 110 including respective sidewall 112. Each of the two vias 110 may be formed in the substrate 104 by lithography and deep reactive-ion etching (DRIE) for example a Bosch process. Any other suitable lithography and etching method may also be used. The two vias 110 may be formed in the substrate 104 as blind vias initially.

[0096] FIG. 3B shows barrier layer (not shown) and Cu seed layer 120 deposition. Next in FIG. 3B, the method may include forming a barrier layer over the substrate 104. The barrier layer may be formed over the top surface 108 of the substrate 104 and in the two vias 110 formed in the substate 104. The barrier layer may include a material selected from a group consisting of Ti, TiN, silicon carbide, silicon oxycarbide, silicon oxide, for example.

[0097] The method may further include forming a seed layer 120 over the barrier layer. The seed layer 120 may include copper for example.

[0098] FIGs. 3C to 3E shows the steps involved in the formation of the conductive portion 114 in each of the two vias 110 and over the top surface 108 of the substrate 104. The conductive portion 114 in each of the two vias 110 may include a thickness from the bottom surface 106 to the top surface 108 of the substrate 104 which may be greater than its thickness from the sidewall 112 of each of the two vias 110 in a direction normal to the sidewall 112 within each of the two vias 110. The formation of the conductive portion 114 in each of the two vias 110 and over the top surface 108 of the substrate 104 may be performed at the same time.

[0099] FIG. 3C shows dry film pattern. In FIG. 3C, the formation of the conductive portion 114 may include forming a dry film resist 128 over the substrate 104. An opening 130 or any suitable pattern corresponding to the subsequently formed redistribution (RDL) lines may be formed in the opening 130 of the dry film resist 128, the opening 130 or pattern may be positioned and sized so as to at least correspond to the location and size of the two vias 110 and to form the RDL lines between the two vias 110, and at other location or connection to the next layer as and when desired.

[00100] FIG. 3D shows partial Cu plating. In FIG. 3D, a conductive layer 132 may be deposited in the opening 130. The conductive layer 132 may be deposited by electroplating, for example copper electro-plating. The electroplating or plating process may be modified so to allow superfilling to achieve thicker Cu thickness at the bottom region of the via 110. This may require faster Cu deposition rate at the bottom region of

the via 110 while suppressing the Cu plating rate at the top as well as the sidewall region of the via 110.

[00101] FIG. 3E shows removal of dry film resist 128. In FIG. 3E, the dry film resist 128 may be removed. The dry film resist 128 may be removed by wet etch or dry etch, depending on the type of dry film resist used, and in combination with the type of the seed layer 120.

[00102] After removal of the dry film resist 128, the conductive layer 132 which may have been deposited in each of the two vias 110 and over the top surface 108 of the substrate 104 may form the conductive portion 114.

[00103] FIG. 3F shows polymer portion filling or dielectric portion filling. A dielectric portion 116 may be formed in each of the two vias 110 and over at least a portion of the conductive portion 114 which may have been formed over the top surface 108 of the substrate 104. The dielectric portion 116 formed in each of the two vias 110 may form a respective core portion of each of the two vias 110. The dielectric portion 116 may include a polymer portion.

[00104] The formation of the dielectric portion 116 in each of the two vias 110 and over at least the portion of the conductive portion 114 which may have been formed over the top surface 108 of the substrate 104 may be performed at the same time. An example of the method of formation of the dielectric portion 116 may be described in FIG. 4.

[00105] FIG. 3G shows support substrate bonding and via exposure. Each of the two vias 110 may be formed such that each of the two vias 110 may extend from the bottom surface 106 to the top surface 108 of the substrate 104. The formation of two such vias 110 may include providing a support substrate 134; bonding the support substrate 134 to

the dielectric portion 116; and reducing thickness of the substrate 104 from the bottom surface 106 towards the top surface 108 of the substrate 104 such that each of the two vias 110 extends from the bottom surface 106 to the top surface 108 of the substrate 104 to expose the conductive portion 114 in each of the vias 110.

[00106] In an embodiment, reducing thickness of the substrate 104 from the bottom surface 106 towards the top surface 108 of the substrate 104 may include reducing the thickness by one or more of a group consisting of backgrind, planarization, wet etching and dry etching.

[00107] In an embodiment, forming each of the two vias 110 may further include forming each of the two vias 110 such that each of the two vias 110 may include a substantially uniform cross-sectional dimension or a changing cross-sectional dimension as each of the two vias 110 may extend from the bottom surface 106 to the top surface 108 of the substrate 104.

[00108] FIG. 3H shows bottom metallization and debonding. The method may further include forming a dielectric layer (not shown) on the bottom surface 106 of the substrate 104, and making an opening corresponding to the exposed portion of the conductive portion 114. Then the method may include forming a further conductive portion 122 over the bottom surface 106 of the substrate 104 and in electrical connection with the conductive portion 114 in each of the two vias 110, the further conductive portion 122 being configured to connect to a second next layer connection (not shown) at a second distance away from the two vias 110. In an embodiment, the second next layer connection may include an under-bump metallization.

[00109] In an embodiment, the method may further include forming a further dielectric portion 126 over at least a portion of the further conductive portion 122.

[00110] In an embodiment, the method may further include removing the support substrate 134 after forming the further conductive portion 122 and the further dielectric portion 126. FIG. 3H shows a resultant interconnect structure 102.

[00111] FIG. 4 shows a method of forming a dielectric portion 116 in two vias 110 and over at least a portion of a conductive portion 114 which has been formed over a top surface 108 of a substrate 104 according to an embodiment.

[00112] The method of forming the dielectric portion 116 in the two vias 110 and over at least the portion of the conductive portion 114 which has been formed over the top surface 108 of the substrate 104 may include positioning a dry film layered structure 136 over the substrate 104; the dry film layered structure 136 may include a dry film dielectric layer 138 and a dry film lining 140 disposed over the dry film dielectric layer 138. The method may further include applying pressure and heat onto the dry film layered structure 136 to allow the dry film dielectric layer 138 to be formed in each of the two vias 110 formed in the substrate 104 and over at least the portion of the conductive portion 114 which has been formed over the top surface 108 of the substrate 104.

[00113] In FIG. 4, a dry film dielectric layer 138 of a relatively uniform thickness may be used for dielectric portion 116 or polymer filling using a lamination method. To prevent any voids being trapped inside each of the two vias 110, the entire substrate 104 and the dry film layered structure 136 may be placed inside a vacuum chamber 154 including a thermally heated chuck table 142 and be subjected to compression under heat and pressure by a chuck 158 at the same time. The direction of the compression by the

chuck 158 may be as indicated by the arrows as seen in FIG. 4. The heat and pressure may allow the dry film dielectric layer 138 to soften and to become fluidic such that the molten dry film dielectric layer 138 may be able to flow into each of the two vias 110 under pressure to form the dielectric portion 116. The thickness of the dielectric portion 116 formed in the via 110 may be achieved by controlling the thermo-compression process, the thickness of the dry film dielectric layer 138, the via size and the via depth.

[00114] In an embodiment, besides forming the dielectric portion 116 by dry film dielectric layer 138, it may be possible to form the dielectric portion 116 using liquid dielectric by spin coating. This may be achieved using a suitable liquid dielectric with suitable properties to allow spin coating for via filling.

[00115] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

Claims

What is claimed is:

1. An interconnect structure comprising:

a substrate comprising a bottom surface and a top surface arranged opposite to the bottom surface;

a via formed in the substrate, the via comprising a sidewall;

a conductive portion arranged in the via, wherein the conductive portion has a thickness from the bottom surface to the top surface of the substrate which is greater than its thickness from the sidewall of the via in a direction normal to the sidewall; and

a dielectric portion arranged in the via and at least partially surrounded by the conductive portion.

2. The interconnect structure of claim 1,

wherein the via is formed in the substrate such that the via extends from the bottom surface to the top surface of the substrate.

3. The interconnect structure of claim 2,

wherein the via is formed in the substrate such that the via comprises a substantially uniform cross-sectional dimension or a changing cross-sectional dimension as the via extends from the bottom surface to the top surface of the substrate.

4. The interconnect structure of any one of claims 1 to 3,

wherein the dielectric portion comprises a polymer portion.

5. The interconnect structure of any one of claims 1 to 4,

wherein the dielectric portion arranged in the via forms a core portion of the via.

6. The interconnect structure of any one of claims 1 to 5,

wherein the conductive portion is further disposed over the top surface of the substrate, the conductive portion being configured to connect to a first next layer connection at a first distance away from the via.

7. The interconnect structure of claim 6,

wherein the first next layer connection comprises an under-bump metallization.

8. The interconnect structure of claim 6 or 7,

wherein the dielectric portion is further disposed over at least a portion of the conductive portion which has been disposed over the top surface of the substrate.

9. The interconnect structure of any one of claims 1 to 8, further comprising

a barrier layer disposed between the substrate and the conductive portion.

10. The interconnect structure of claim 9,

wherein the barrier layer comprises a material selected from a group consisting of Ti, TiN, silicon carbide, silicon oxycarbide, silicon oxide.

11. The interconnect structure of claim 9 or 10, further comprising

a seed layer disposed between the barrier layer and the conductive portion.

12. The interconnect structure of claim 11,

wherein the seed layer comprises copper.

13. The interconnect structure of any one of claims 1 to 12, further comprising

a further conductive portion disposed over the bottom surface of the substrate and in electrical connection with the conductive portion in the via, the further conductive portion being configured to connect to a second next layer connection at a second distance away from the via.

14. The interconnect structure of claim 13,

wherein the second next layer connection comprises an under-bump metallization.

15. The interconnect structure of claim 13 or 14, further comprising

a further dielectric portion disposed over at least a portion of the further conductive portion.

16. The interconnect structure of any one of claims 1 to 15,

wherein the dielectric portion comprises a polymer, a dry film dielectric layer.

17. The interconnect structure of claim 15 or 16,

wherein the further dielectric portion is of the same material as the dielectric portion.

18. The interconnect structure of any one of claims 1 to 17,

wherein the conductive portion comprises a material selected from a group consisting of copper, nickel.

19. The interconnect structure of any one of claims 13 to 18,

wherein the further conductive portion is of the same material as the conductive portion.

20. The interconnect structure of any one of claims 1 to 19,

wherein the substrate comprises a material selected from a group consisting of silicon, glass.

21. A method of forming an interconnect structure, the method comprising :

providing a substrate, the substrate comprising a bottom surface and a top surface arranged opposite to the bottom surface;

forming a via in the substrate, the via comprising a sidewall;

forming a conductive portion in the via; wherein the conductive portion has a thickness from the bottom surface to the top surface of the substrate which is greater than its thickness from the sidewall of the via in a direction normal to the sidewall; and

forming a dielectric portion in the via and at least partially surrounded by the conductive portion.

22. The method of claim 21,

wherein forming the via in the substrate comprises forming the via by one or more of a group consisting of lithography and deep reactive-ion etching.

23. The method of claim 21 or 22, further comprising

forming a barrier layer over the substrate.

24. The method of claim 23,

wherein the barrier layer comprises a material selected from a group consisting of Ti, TiN, silicon carbide, silicon oxycarbide, silicon oxide.

25. The method of claim 23 or 24, further comprising

forming a seed layer over the barrier layer.

26. The method of claim 25,

wherein the seed layer comprises copper.

27. The method of any one of claims 21 to 26, further comprising

forming the conductive portion over the top surface of the substrate, the conductive portion being configured to connect to a first next layer connection at a first distance away from the via.

28. The method of claim 27,

wherein the first next layer connection comprises an under-bump metallization.

29. The method of claim 27 or 28,

wherein forming the conductive portion in the via and forming the conductive portion over the top surface of the substrate is performed at the same time.

30. The method of claim 29,

wherein forming the conductive portion in the via and forming the conductive portion over the top surface of the substrate comprises :

forming a dry film resist over the substrate;

forming an opening in the dry film resist, the opening positioned and sized so as to at least correspond to the via;

depositing a conductive layer in the opening; and

removing the dry film resist.

31. The method of claim 30,

wherein the conductive layer is deposited by electroplating.

32. The method of any one of claims 21 to 31,

wherein the dielectric portion formed in the via forms a core portion of the via.

33. The method of any one of claims 27 to 32, further comprising

forming the dielectric portion over at least a portion of the conductive portion which has been formed over the top surface of the substrate.

34. The method of claim 33,

wherein forming the dielectric portion in the via and forming the dielectric portion over the at least a portion of the conductive portion which has been formed over the top surface of the substrate is performed at the same time.

35. The method of claim 34,

wherein forming the dielectric portion in the via and forming the dielectric portion over the at least a portion of the conductive portion which has been formed the top surface of the substrate comprises :

positioning a dry film layered structure over the substrate; the dry film layered structure comprises

a dry film dielectric layer; and

a dry film lining disposed over the dry film dielectric layer;

and

applying pressure and heat onto the dry film layered structure to allow the dry film dielectric layer to be formed in the via and over at least the portion of the conductive portion which has been formed over the top surface of the substrate.

36. The method of any one of claims 21 to 35,

wherein forming the via in the substrate further comprises forming the via such that the via extends from the bottom surface to the top surface of the substrate.

37. The method of claim 36,

wherein forming the via such that the via extends from the bottom surface to the top surface of the substrate comprises :

providing a support substrate;

bonding the support substrate to the dielectric portion; and

reducing thickness of the substrate from the bottom surface towards the top surface of the substrate such that the via extends from the bottom surface to the top surface of the substrate to expose the conductive portion in the via.

38. The method of claim 37,

wherein reducing thickness of the substrate from the bottom surface towards the top surface of the substrate comprises reducing the thickness by one or more of a group consisting of backgrind and planarization.

39. The method of any one of claims 36 to 38,

wherein forming the via further comprises forming the via such that the via comprises a substantially uniform cross-sectional dimension or a changing cross-sectional dimension as the via extends from the bottom surface to the top surface of the substrate.

40. The method of any one of claims 37 to 39, further comprising

forming a further conductive portion over the bottom surface of the substrate and in electrical connection with the conductive portion in the via, the further conductive portion being configured to connect to a second next layer connection at a second distance away from the via.

41. The method of claim 40,

wherein the second next layer connection comprises an under-bump metallization.

42. The method of claim 40 or 41, further comprising

forming a further dielectric portion over at least a portion of the further conductive portion.

43. The method of claim 42, further comprising

removing the support substrate after forming the further conductive portion and the further dielectric portion.

44. The method of any one of claims 21 to 43,

wherein the dielectric portion comprises a polymer, a dry film dielectric layer.

45. The method of any one of claims 42 to 44,

wherein the further dielectric portion is of the same material as the dielectric portion.

46. The method of any one of claims 21 to 45,

wherein the conductive portion comprises a material selected from a group consisting of copper, nickel.

47. The method of any one of claims 40 to 46,

wherein the further conductive portion is of the same material as the conductive portion.

48. The method of any one of claims 21 to 47,

wherein the substrate comprises a material selected from a group consisting of silicon, glass.

49. The method of any one of claims 21 to 48,

wherein the dielectric portion comprises a polymer portion.

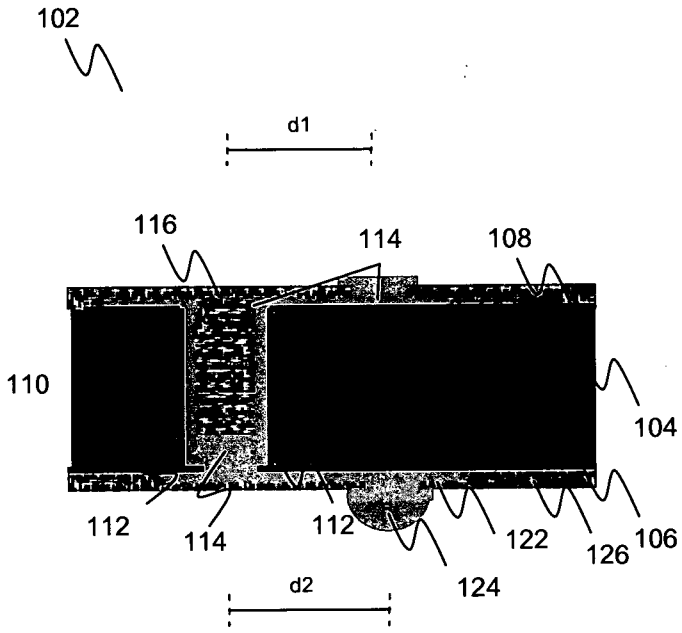


Figure 1

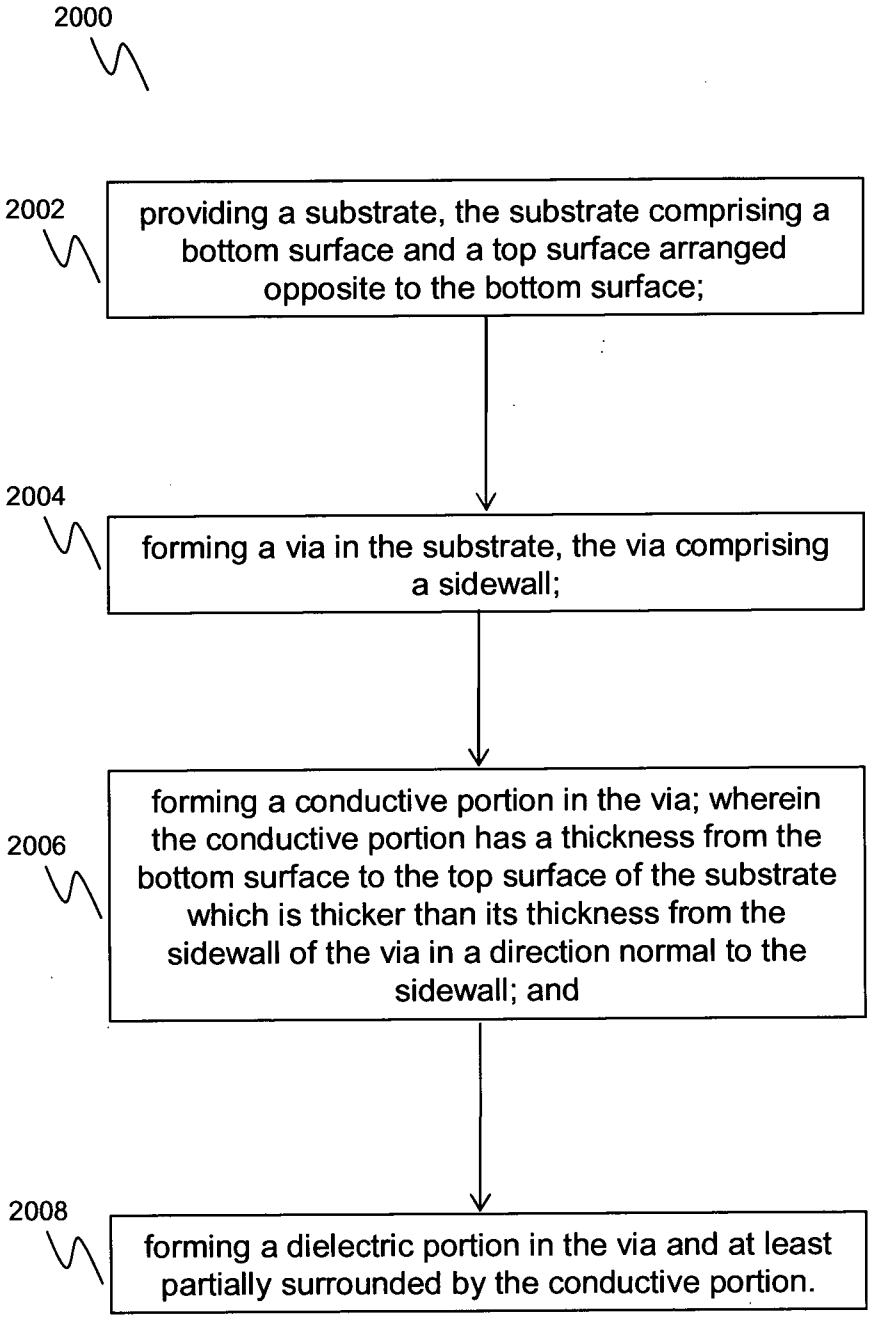

2000
2002
providing a substrate, the substrate comprising a bottom surface and a top surface arranged opposite to the bottom surface;
2004
forming a via in the substrate, the via comprising a sidewall;
2006
forming a conductive portion in the via; wherein the conductive portion has a thickness from the bottom surface to the top surface of the substrate which is thicker than its thickness from the sidewall of the via in a direction normal to the sidewall; and
2008
forming a dielectric portion in the via and at least partially surrounded by the conductive portion.

Figure 2

Figure 3A

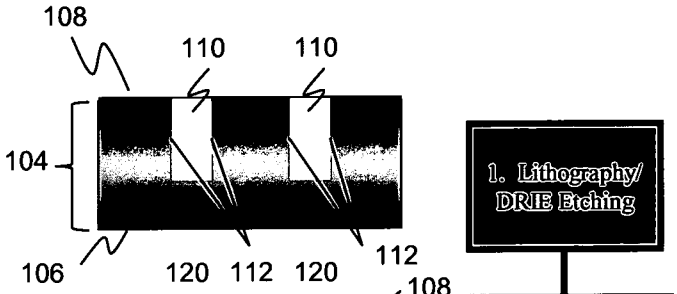


Figure 3B

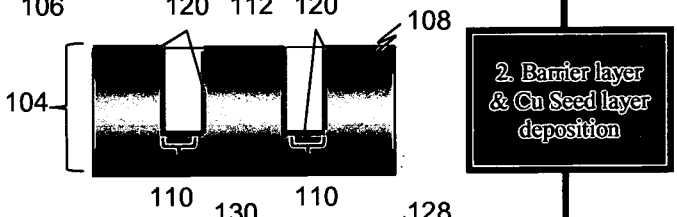


Figure 3C

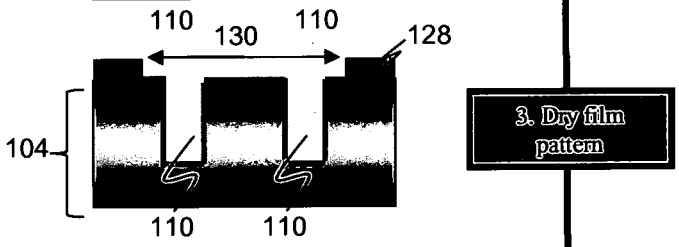


Figure 3D

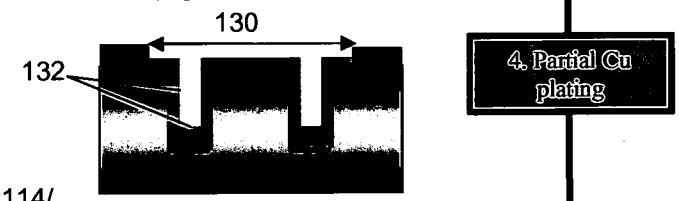


Figure 3E



Figure 3F

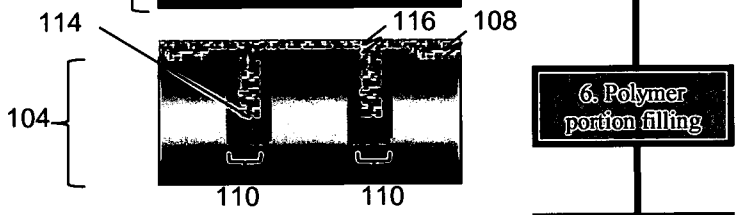


Figure 3G

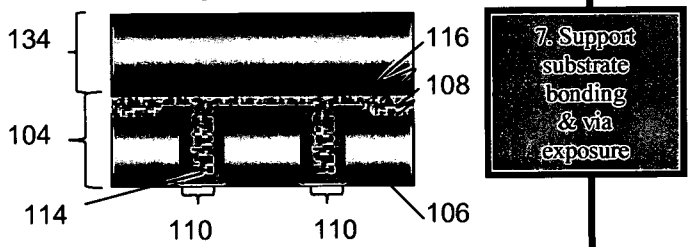
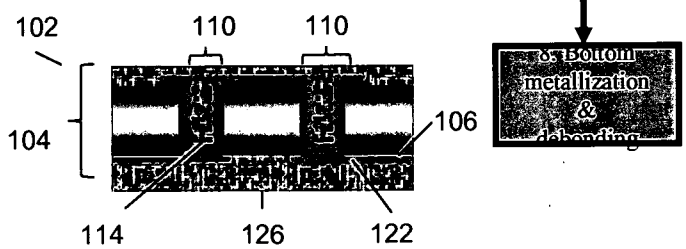


Figure 3H



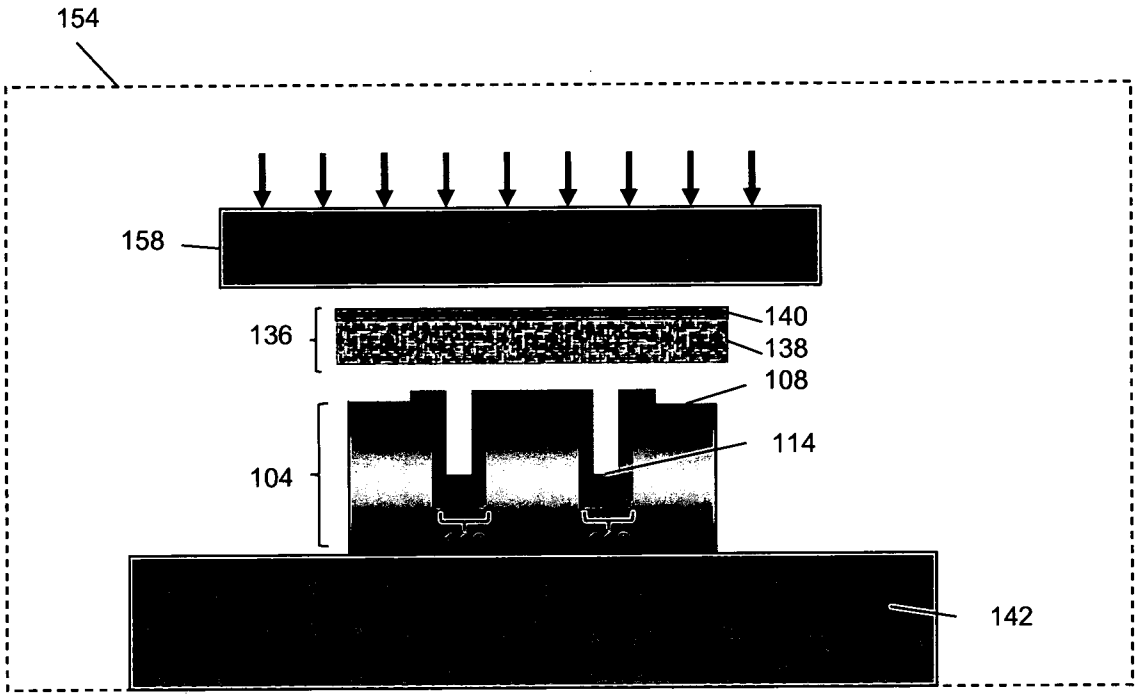


Figure 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2010/000145

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01L 21/44 (2006.01) ***H01L 21/31*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC & WPI: Limit H01L, H05K, H01R & Keywords: wafer, substrate, chip, dice, die, IC, (integrated circuit), contact, interconnect, conduct, electrode, metal, via, hole, aperture, cavity, recess, hollow, groove, TSV, dielectric, oxide, insulator, polymer, barrier, seed, nitride, carbide, coat, layer, film, deposit, dispose, cover, fill or penetrate, Cu or copper, Ni, nickel

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/0259292 A1 (BEYNE ET AL.) 23 December 2004 Paragraphs 0109-0177, Figs. 1A-2H	1-49
A	US 2007/0128868 A1 (HALAHAN ET AL.) 7 June 2007 Whole document	
A	US 5851914 A (HAN ET AL.) 22 December 1998 Whole document	
A	US 2006/0043599 A1 (AKRAM ET AL.) 2 March 2006 Whole document	

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 May 2010	24 MAY 2010
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **JAYATI RAY** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6222 3654

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG2010/000145

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	2004259292	EP	1465246	EP	1519410	US	6908856
US	2007128868	US	2004203224	US	6897148	US	7521360
		US	2005170647				
US	5851914	CN	1170962				
US	2006043599	US	7300857	US	2008111213	US	7683458

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX