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(71) Applicant: **RESEARCH MACHINES LIMITED**
P.O. Box 75 Mill Street
Oxford, OX2 OBW(GB)

(72) Inventor: **Matthews, Anthony John**
24 Heytsbury Gardens Grange Park
Swindon Wilts SN5 6EE(GB)

(74) Representative: **Unwin, Stephen Geoffrey**
S.G. Unwin & Co. 2 North Street
Islip Oxford OX5 2SL(GB)

(54) Generation of raster scan video signals for an enhanced resolution monitor.

(57) The converter circuit (3) provides for the generation of a raster scan video signal to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the circuit (3) comprises: a video timing generator (7) connected to receive timing signals from the video adaptor (1); a multiplexer (11) connected to receive a video output signal from the video adaptor (1); a video line buffer (6) connected to receive the video output signal from the video adaptor (1) and connected to the multiplexer (11); and output means (9) connected to receive a video output signal from the multiplexer (11) for providing a video output signal to an enhanced resolution monitor, and converter circuit (3) being selectively operable in a first mode in which video information from the video adapter (1) is converted by the multiplexer (11) for a high resolution, monochrome display and then provided to the output means (9), and a second mode in which video information for a low resolution, multi-colour display is received by the multiplexer (11) from the video adapter (1) via the buffer (6) such that each pixel of information is read out twice from the buffer (6) and each line of information is read out twice to provide the output means (9) with a video output signal of a low resolution display to be produced on an enhanced resolution monitor.

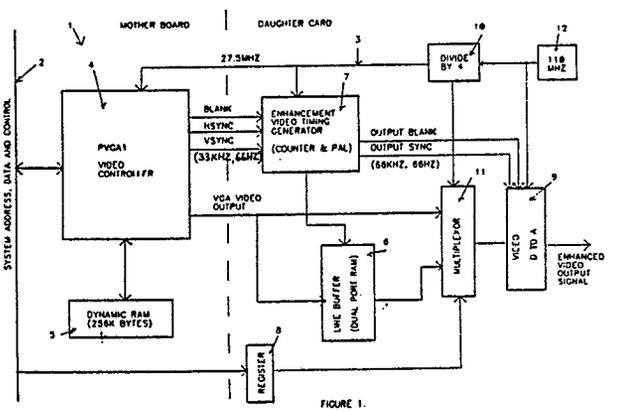


FIGURE 1.

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GENERATION OF RASTER SCAN VIDEO SIGNALS FOR AN ENHANCED RESOLUTION MONITOR

This invention relates to the generation of raster scan video signals for an enhanced resolution monitor in either a high resolution mode or a low resolution mode.

The increasing power of personal computers has led to an interest in providing higher resolution dislay systems, particularly suited to windowing environments, computer aided design and engineering, spread sheets and desk top publishing.

In the past, this area has been catered for by specialised display adaptors typically containing circuitry such as a dedicated video memory to contain the enhanced resolution image and a dedicated video timing signal generator as well as dedicated logic for interfacing the adaptor to the systems bus of the personal computer.

There is also often the requirement to provide compatibility with the native video modes of the personal computer. In the past, this has been achieved by means of a dedicated circuit providing limited capabilities for the display of a normal personal computer video mode on an enhanced resolution monitor or a second display adaptor and monitor to provide compatibility independent from the enhanced resolution display system.

In small computers and data processors, it is particularly important to reduce the complexity and expense of the hardware required to perform such functions and this invention aims to reduce or eliminate the need for the additional expensive circuitry described above and, in one particular arrangement, to provide a plug-in convertor circuit to modify a normal, industry standard video adaptor to operate in accordance with the invention.

According to a first aspect of the invention, there is provided a converter circuit for connection to a video adaptor of a computer to provide for the generation of a raster scan video signal to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the converter circuit comprising: a video timing generator for connecting to receive timing signals from the video adaptor; a multiplexer for connecting to receive a video output signal from the video adaptor; a video line buffer for connecting to receive the video output signal from the video adaptor and connected to the multiplexer; and output means connected to receive a video output signal from the multiplexer for providing a video output signal to an enhanced resolution monitor, the converter circuit being selectively operable in a first mode in which video information from the video adapter is converted by the multiplexer for a high resolution, monochrome display and then provided to the output means, and a second mode in which video information for a low resolution, multi-colour display is received by the multiplexer from the video adaptor via the buffer such that each pixel of information is read out twice from the buffer and each line of information is read out twice to provide the output means with a video output signal of a low resolution display to be produced on an enhanced resolution monitor.

According to a second aspect of the invention, there is provided a video adaptor for a computer for providing a raster scan video signal to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the video adaptor comprising: a video controller for connecting to a system bus of a computer; a video memory connected to the video controller; a video timing generator connected to receive timing signals from the video controller; a multiplexer connected to receive a video output signal from the video controller; a video line buffer connected to receive the video output signal from the video controller and connected to the multiplexer; and output means connected to receive a video output signal from the multiplexer for providing a video output signal to an enhanced resolution monitor, the video adaptor being selectively operable in a first mode in which video information from the video controller is converted by the multiplexer for a high resolution, monochrome display and then provided to the output means, and a second mode in which video information for a low resolution, multi-colour display is received by the multiplexer from the video controller via the buffer such that each pixel of information is read out twice from the buffer and each line of information is read out twice to provide the output means with a video output signal of a low resolution display to be produced on an enhanced resolution monitor.

According to a third aspect of the invention, there is provided a computer having the facility for providing a raster scan video signal to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the computer having a processor responsive to a display request to provide instructions on a system bus to a video adaptor, the video adaptor comprising: a video controller connected to the system bus; a video memory connected to the video controller; a video timing generator connected to receive timing signals from the video controller; a multiplexer connected to receive a video output signal from the video controller; a video line buffer connected to receive the video output signal from the video controller and connected to the multiplexer; and output means connected to receive a video output

signal from the multiplexer for providing a video output signal to an enhanced resolution monitor, the video adaptor being selectively operable in response to instructions received on the system bus in a first mode in which video information from the video controller is converted by the multiplexer for a high resolution, monochrome display and then provided to the output means, and a second mode in which video information for a low resolution, multi-colour display is received by the multiplexer from the video controller via the buffer such that each pixel of information is read out twice from the buffer and each line of information is read out twice to provide the output means with a video output signal of a low resolution display to be produced on an enhanced resolution monitor.

According to a fourth aspect of the invention, there is provided a method of providing a raster scan video signal from a video adaptor of a computer to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the method comprising the steps of: in the first mode, routing video information from the video adaptor for conversion by a multiplexer for a high resolution, monochrome display and then to output means connected to a high resolution monitor and, in the second mode, passing video information for a low resolution, multi-colour display to a buffer and then reading this into the multiplexer, under the control of a video timing generator connected to receive timing signals from the video adaptor, such that each pixel of information is read out twice and each line of information is read out twice so as to provide the output means with a video output signal of a low resolution display to be produced on an enhanced resolution monitor.

Preferred features of the invention will be apparent from the following description and from the subsidiary claims of the specification.

The invention will now be described, merely by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram for explaining the function of an embodiment of the invention;

Figures 2(a)-2(f) show schematic circuit diagrams of parts of the system shown in Figure 1; and

Figure 3 is an assembler listing of the contents of one of the components shown in the Figures 1 and 2.

Figure 1 shows a block diagram of a conventional video adaptor 1 mounted on a mother board and connected to a systems bus 2 of a personal computer (PC). The systems bus 2 carries address, data and control signals and is used by the PC to communicate with input/output (I/O) devices such as the video adaptor 1. The video adaptor 1 is used to provide the primary point for communication of output information to the human operator.

A plug-in converter circuit 3 mounted on a daughter card is connected to the video adaptor 1. As will be described below, this provides for the generation of a raster scan video signal to an enhanced resolution monitor (not shown) in either a first, high resolution mode such as may be needed for the applications mentioned above and a second, low resolution mode for use with the native video modes of the PC. A plug-in video adaptor may also be used rather than mounting it on the mother board.

In the embodiment shown, the video adaptor 1 comprises a video controller 4 such as a PVGA1A device (detailed in 'PVGA1A User Manual' published by Western Digital (Paradise Systems) Corporation, Brisbane, CA). The video controller 4 is configured with 256k bytes of page mode dynamic random access memory (DRAM) 5 such as a Mitsubishi M5M4464 as defined in the recommended applications in the user manual mentioned above.

The converter circuit 3 comprises a video line buffer 6 such as an NEC uPD41101 device (detailed in the 'NEC memory data book' published by NEC Electronics (UK) Ltd. Milton Keynes, UK), a video timing generator 7 implemented using standard FAST series logic devices 74F00, 74F153, 74F163, 74F174 and 74F257 (detailed in 'Fairchild Advanced Schottky TTL' published by Fairchild Semiconductor Ltd., Potter's Bar, Herts, UK) and a PAL16R8A device (detailed in the 'LSI data book' published by Monolithic Memories Incorporated, Santa Clara, CA) and a control register 8 implemented by a Fast series logic device 74F194 (also detailed in 'Fairchild Advanced Schottky TTL').

The convertor circuit 3 also comprises a video digital to analog (D/A) convertor 9, a clock divider 10 and a multiplexer 11 which are implemented together using a Brooktree BT454 device (detailed in 'Brooktree Product Databook' published by Brooktree Corporation, San Diego, California). A 110MHz clock 12 is connected to both the divider 10 and D/A convertor 9. Depending on the type of monitor used, other output means can be used in place of the D/A converter 9.

These components are connected as shown in Figure 1 with the video timing generator 7 connected to receive timing signals from the video controller 4 and connected to control transfer of video data into and out of line buffer 6 and the D/A convertor 9. The multiplexer 11 is connected to route video output signals either directly from the video controller 4 or via the line buffer 6 and to pass signals to the D/A convertor 9. The register 8 is connected to receive instructions from the system bus 2 to control the mode in which the multiplexer 11 and hence the convertor circuit 3 operates.

Software within the PC may control the convertor circuit in one of three modes, a high resolution mode, a low resolution mode and a third optional mode described further below.

In the first, high resolution mode, the full capabilities of the enhanced resolution monitor, eg displaying 1280 x 960 pixels, are used. In this mode, the video adaptor 1 is programmed via the systems bus 2 to output one byte of video information every two 27.5 MHz clocks with a line rate of 66KHz. This programming consists of chaining all memory planes together to form one large, linear bit-map. Consecutive bytes presented at the video output are taken from consecutive memory locations. The built-in video timing generator is programmed to produce 128 bytes per video line at 66kHz with 960 active lines per frame. The line buffer 6 is bypassed using the multiplexer 11 and the eight bits of information are presented one after another to the the D/A convertor 9.

The multiplexer 11 is thus presented with 8 bits of video information at 13.75 MHz (256 colours). The multiplexer 11 converts this first to 4 bits at 27.5 MHz (16 colours) and then 1 bit at 110 MHz (monochrome). The byte is presented so that the first pixel is bit 7, the second pixel is bit 6 and so on to the eighth pixel being the bit 0. This allows an enhanced resolution monochrome (eg black and white) display to be produced on the enhanced resolution monitor without exceeding the limited band width available from the memory 5 and the video controller 4.

It should be noted that all horizontal and vertical SYNC and BLANK signals are derived from the output signals of the video controller 4 using a minimal amount of logic within the video timing generator 7. Also, the sequencing and control of accesses to the memory 5 is controlled by the video controller 4. The enhanced resolution image s also held within the memory 5. None of the above mentioned functions are duplicated on the daughter card so enabling the cost of the system to be considerably reduced compared to prior art systems.

The second, low resolution mode, provides compatibility of the system when using the enhanced resolution monitor with the set of modes supported by the standard video adaptor 1 as would be used when driving a standard video graphics array (VGA) monitor. These modes are detailed in the 'PVGA1A User Manual' mentioned above.

In this mode, the video adaptor 1 presents digital, 16 colour video information along with BLANK and SYNC signals derived from the 110MHz clock 12 divided by the divider 10. However, the video adaptor 1 generates video lines at a rate of 33KHz whereas the enhanced resolution monitor requires video lines at 66kHz. The video timing generator 7 thus synchronises to the BLANK signals from the video adaptor 1 and generates BLANK and SYNC signals at the monitor line rate of 66KkHz. The input and output BLANK signals are used to control the line buffer 6. Each line from the video adaptor 1 is written into the buffer as it arrives (at 33kHz) and the video information is read out at twice the input rate producing two identical lines on the enhanced resolution monitor (at 66kHz) containing the video information produced by the video adaptor 1. Each pixel of information is also read out twice so each line comprises adjacent pairs of identical information.

The video timing generator 7 samples the BLANK signals from the video adapter 1 in the middle of each line to extract the vertical blanking information. It then skews the timing of its BLANK output signal by one line relative to the input signal to ensure that the line buffer 6 is full when the first displayed line is output from the buffer.

The D/A convertor 9 combines the 4 bit (16 colour) display information and the output SYNC and BLANK signals to form a 1 volt peak to peak analog feed signal to the enhanced resolution monitor.

The net result of the above operation is to cause each pixel output from the video adaptor 1 to be displayed as two consecutive pixels on a line and on two consecutive lines, ie as a square of four pixels. This effectively converts the enhanced monitor resolution from 1280 x 960 pixels to 640 x 480 pixels to match the video adapter capabilities in the standard video modes. This allows the PC native video modes to be displayed on the enhanced resolution monitor without exceeding the limited bandwidth available from the memory 5 and video controller 4 and without requiring a second (low resolution) monitor. If the equipment allows, other resolution conversions, eg from one pixel to a 3 x 3 square of pixels, could be similarly performed.

Of course, when a monochrome monitor is used, the different colours in the display can be represented by various shades as well known in the art. References to colours within this specification should be understood to include such different shading.

In the optional third mode mentioned above, the converter circuit 2 on the daughter card is effectively disabled so that the video adaptor can be used to drive directly a standard, low resolution monitor (not shown) with the video adapter 1 operating as normal. In this mode, the video timing generator 7 idles, holding the enhanced resolution monitor blank and generating a 66kHz signal to prevent whistling regardless of the operation of the video adaptor 1.

Figure 2 is a circuit diagram of the components

shown on the daughter card in Figure 1. However, it should be noted that since Figure 1 is a functional representation of the circuit a precise one-to-one relationship does not exist between the boxes shown in Figure 1 and the components shown in Figure 2.

Figure 3 is an assembler listing of the contents of the PAL16R8A device used in the video timing generator 7.

The features of the circuit shown in Figure 2 and of the listing in Figure 3 will be apparent to those skilled in the art in the light of the above description so will not be described further.

As will be appreciated, the arrangement described above eliminates the need for dedicated circuitry to provide an enhanced resolution display by making maximum usage of the facilities provided by a normal, standard PC video adapter together with a minimum amount of logic and special programming.

The arrangement described also reduces or eliminates the dedicated circuitry (or second monitor) required in the prior art to provide compatibility with the native video modes of the PC by utilising the circuitry of the video adapter and converting its output signals for use on an enhanced resolution monitor.

The arrangement described makes use of a lower resolution, higher colour count standard PC video adapter to reduce or eliminate the necessity of using expensive, separate, dedicated video memory and video timing generation for the high resolution image. The logic described allows the number of colours to be converted into the enhanced resolution.

The arrangement also uses a minimum amount of logic to synchronise the video timing generator to the PC video adapter so avoiding the need to provide a separate video timing generator for the high resolution mode.

Although the arrangement described above comprises a plug-in converter circuit for connecting to a standard PC video adapter, it will be appreciated that it would be possible to build a video adapter incorporating the features of the plug-in circuit so as to operate in the manner described above.

Claims

1. A converter circuit (3) for connection to a video adaptor (1) of a computer to provide for the generation of a raster scan video signal to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the converter circuit (3) comprising: a video timing generator (7) for connecting to receive timing signals from the video adaptor (1); a multiplexer (11) for connecting to receive a video output signal from the video adaptor (1); a video line buffer (6) for connecting to receive the video output signal from the video adaptor (1) and connected to the multiplexer (11); and output means (9) connected to receive a video output signal from the multiplexer (11) for providing a video output signal to an enhanced resolution monitor, the converter circuit (3) being selectively operable in a first mode in which video information from the video adapter (1) is converted by the multiplexer (11) for a high resolution, monochrome display and then provided to the output means (9), and a second mode in which video information for a low resolution, multi-colour display is received by the multiplexer (11) from the video adaptor (1) via the buffer (6) such that each pixel of information is read out twice from the buffer (6) and each line of information is read out twice to provide the output means (9) with a video output signal of a low resolution display to be produced on an enhanced resolution monitor.

2. A video adaptor for a computer for providing a raster scan video signal to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the video adaptor comprising: a video controller (4) for connecting to a system bus (2) of a computer; a video memory (5) connected to the video controller (4); a video timing generator (7) connected to receive timing signals from the video controller (4); a multiplexer (11) connected to receive a video output signal from the video controller (4); a video line buffer (6) connected to receive the video output signal from the video controller (4) and connected to the multiplexer (11); and output means (9) connected to receive a video output signal from the multiplexer (11) for providing a video output signal to an enhanced resolution monitor, the video adaptor being selectively operable in a first mode in which video information from the video controller (4) is converted by the multiplexer (11) for a high resolution, monochrome display and then provided to the output means (9), and a second mode in which video information for a low resolution, multi-colour display is received by the multiplexer (11) from the video controller (4) via the buffer (6) such that each pixel of information is read out twice from the buffer (6) and each line of information is read out twice to provide the output means (9) with a video output signal of a low resolution display to be produced on an enhanced resolution monitor.

3. A computer having the facility for providing a raster scan video signal to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the computer having a processor responsive to a display request to provide instructions on a system bus (2) to a video

adaptor (1), the video adaptor (1) comprising: a video controller (4) connected to the system bus (2); a video memory (5) connected to the video controller (4); a video timing generator (7) connected to receive timing signals from the video controller (4); a multiplexer (11) connected to receive a video output signal from the video controller (4); a video line buffer (6) connected to receive the video output signal from the video controller (4) and connected to the multiplexer (11); and output means (9) connected to receive a video output signal from the multiplexer (11) for providing a video output signal to an enhanced resolution monitor, the video adaptor (1) being selectively operable in response to instructions received on the system bus (2) in a first mode in which video information from the video controller (4) is converted by the multiplexer (11) for a high resolution, monochrome display and then provided to the output means (9), and a second mode in which video information for a low resolution, multi-colour display is received by the multiplexer (11) from the video controller (4) via the buffer (6) such that each pixel of information is read out twice from the buffer (6) and each line of information is read out twice to provide the output means (9) with a video output signal of a low resolution display to be produced on an enhanced resolution mintor.

4. A method of providing a raster scan video signal from a video adaptor (1) of a computer to an enhanced resolution monitor in either a first, high resolution mode or a second, low resolution mode, the method comprising the steps of: in the first mode, routing video information from the video adaptor (1) for conversion by a multiplexer (11) for a high resolution, monochrome display and then to output means (9) connected to a high resolution monitor and, in the second mode, passing video information for a low resolution, multi-colour display to a buffer (6) and then reading this into the multiplexer (11), under the control of the video generator (7) connected to receive timing signals from the video adaptor (1), such that each pixel of information is read out twice and each line of information is read out twice so as to provide the output means (9) with a video output signal of a low resolution display to be produced on an enhanced resolution monitor.

5. A converter circuit, video adaptor or computer as claimed in claim 1, 2 or 3 which is operable in a third mode in which the video timing generator (7), multiplexer (11), video line buffer (6) and output means (9) are effectively disabled so that the video adaptor (1) can drive directly a low resolution monitor.

6. A video adaptor as claimed in claim 2 or claim 5 when dependent thereon in which the video controller (4) and video memory (5) are part of an industry standard video adaptor (1) and the video timing generator (7), multiplexer (11), video line buffer (6) and output means (9) comprise a plug-in converter circuit connected thereto.

7. A method as claimed in claim 4 in which the video adaptor (1) comprises a video controller (4) and a video memory (5) and, in the high resolution mode, the sequence and control of accesses to the video memory (5) are controlled by the video controller (4).

8. A method as claimed in claim 7 in which, in the high resolution mode, the enhanced resolution image is held in the video memory (5) of the video adaptor (1).

9. A method as claimed in claim 4, 7 or 8 in which, in the high resolution mode, the multiplexer (11) reduces the word length of the video data received from the video adaptor (1) and increases the rate at which it is presented to the output means (9), eg by converting 8 bits of video data at 13.75 MHz first to 4 bits at 27.5 MHz and then to 1 bit at 110 MHz.

10. A method as claimed in claim 4 or any of claims 7 to 9 in which, in the low resolution mode, the line rate of the video information received by the line buffer (6) is increased by reading it out from the buffer (6) at a higher rate than it is supplied thereto.

11. A method as claimed in claim 4 or any of claims 7 to 10 in which, in both the high and low resolution modes, the timing signals produced by the video timing generator (7) are derived from output signals of the video adaptor (1).

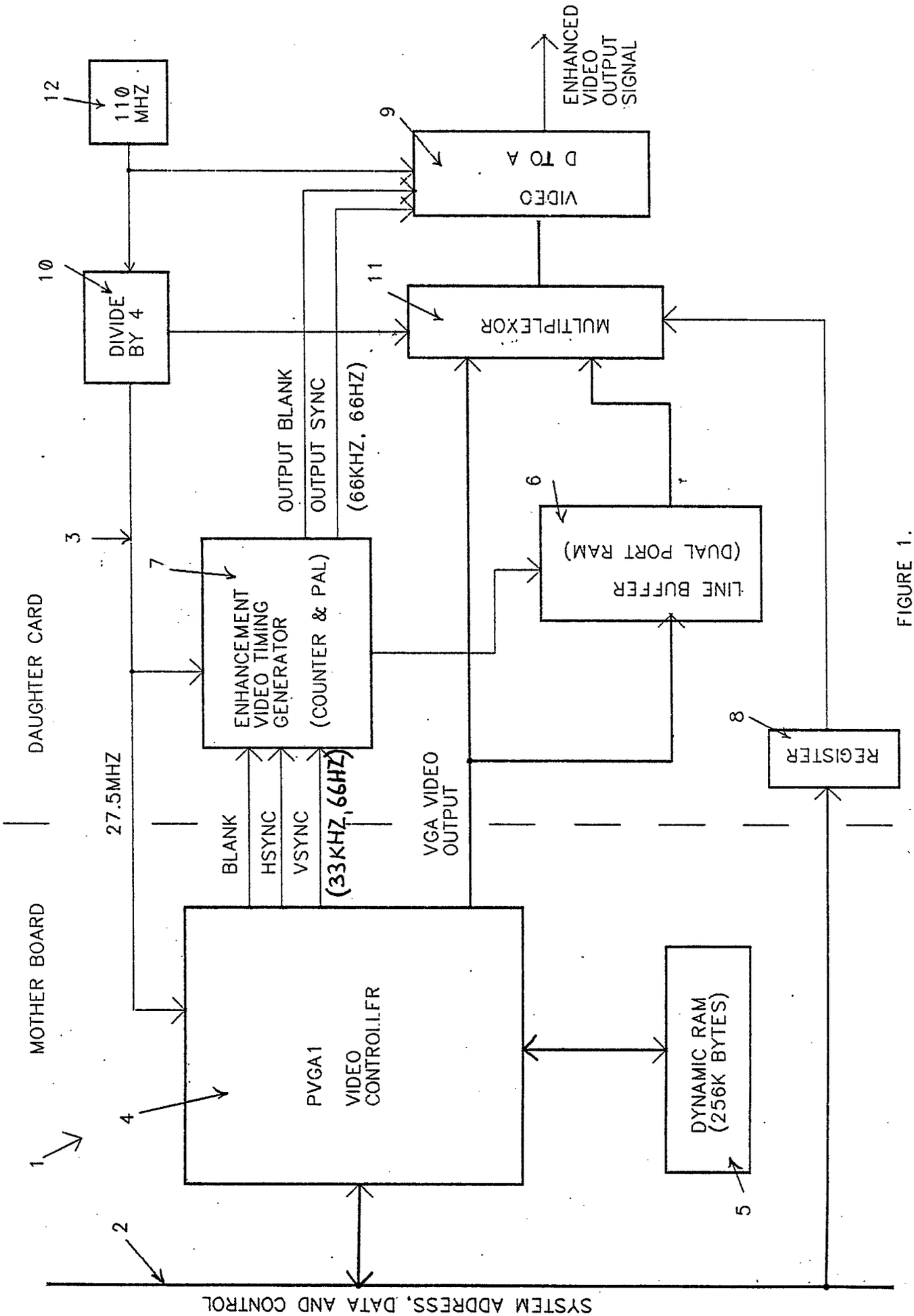

SYSTEM ADDRESS, DATA AND CONTROL
2
MOTHER BOARD
DAUGHTER CARD
1
PVGA1
VIDEO
CONTROLLER
4
DYNAMIC RAM
(256K BYTES)
5
REGISTER
8
LINE BUFFER
(DUAL PORT RAM)
6
ENHANCEMENT
VIDEO TIMING
GENERATOR
(COUNTER & PAL)
7
3
27.5MHZ
BLANK
HSYNC
VSYNC
(33KHZ, 66HZ)
VGA VIDEO
OUTPUT
OUTPUT BLANK
OUTPUT SYNC
(66KHZ, 66HZ)
MULTIPLEXOR
11
DIVIDE
BY 4
10
D TO A
VIDEO
9
110
MHZ
12
ENHANCED
VIDEO
OUTPUT
SIGNAL

FIGURE 1.

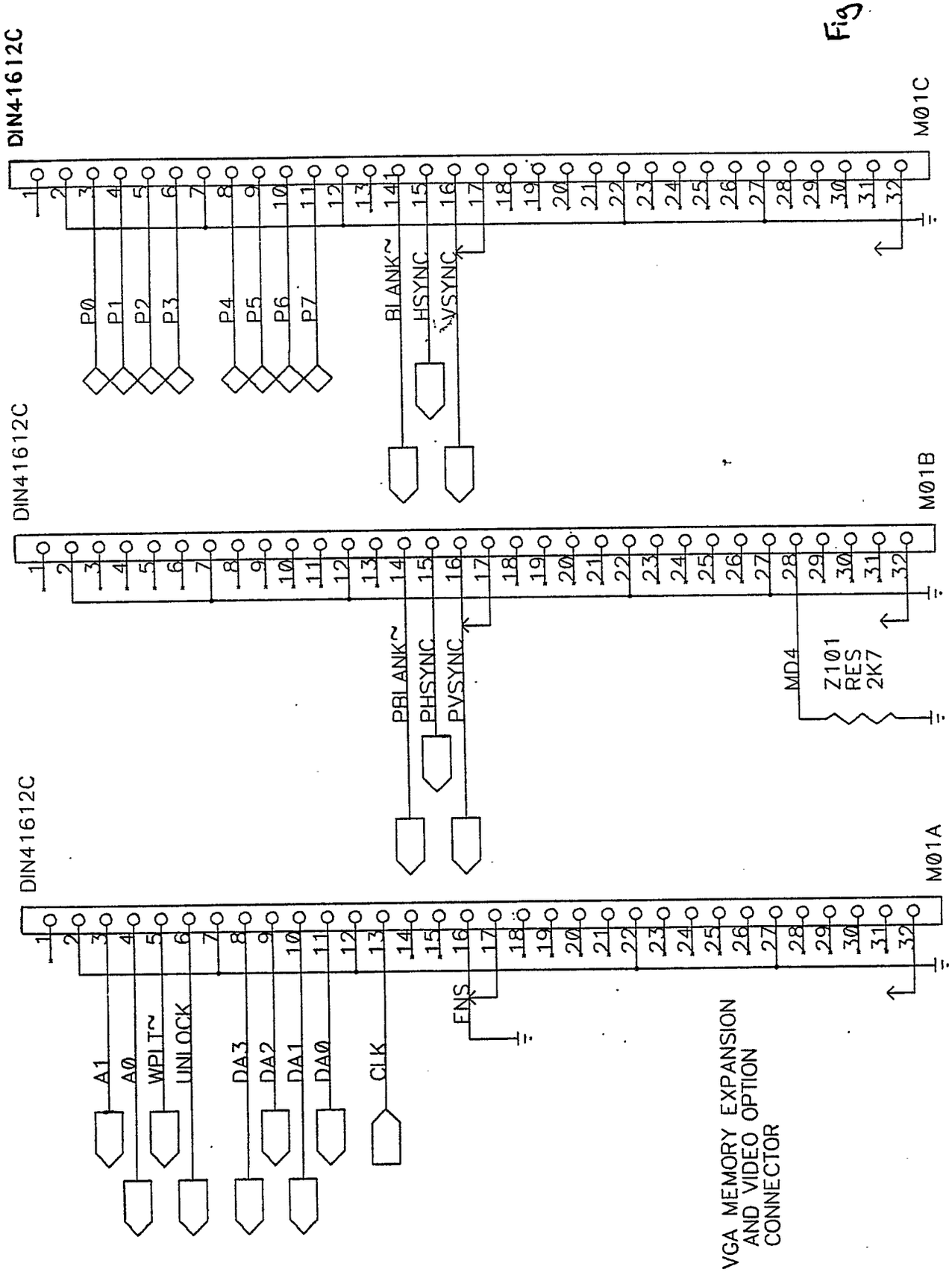

DIN41612C
M01C
P0
P1
P2
P3
P4
P5
P6
P7
BLANK~
HSYNC
VSYNC
DIN41612C
M01B
PBLANK~
PHSYNC
PVSYNC
MD4
Z101
RES
2K7
DIN41612C
M01A
A1
A0
WPLT~
UNLOCK
DA3
DA2
DA1
DA0
CLK
FNS
VGA MEMORY EXPANSION
AND VIDEO OPTION
CONNECTOR

Fig 2(a)

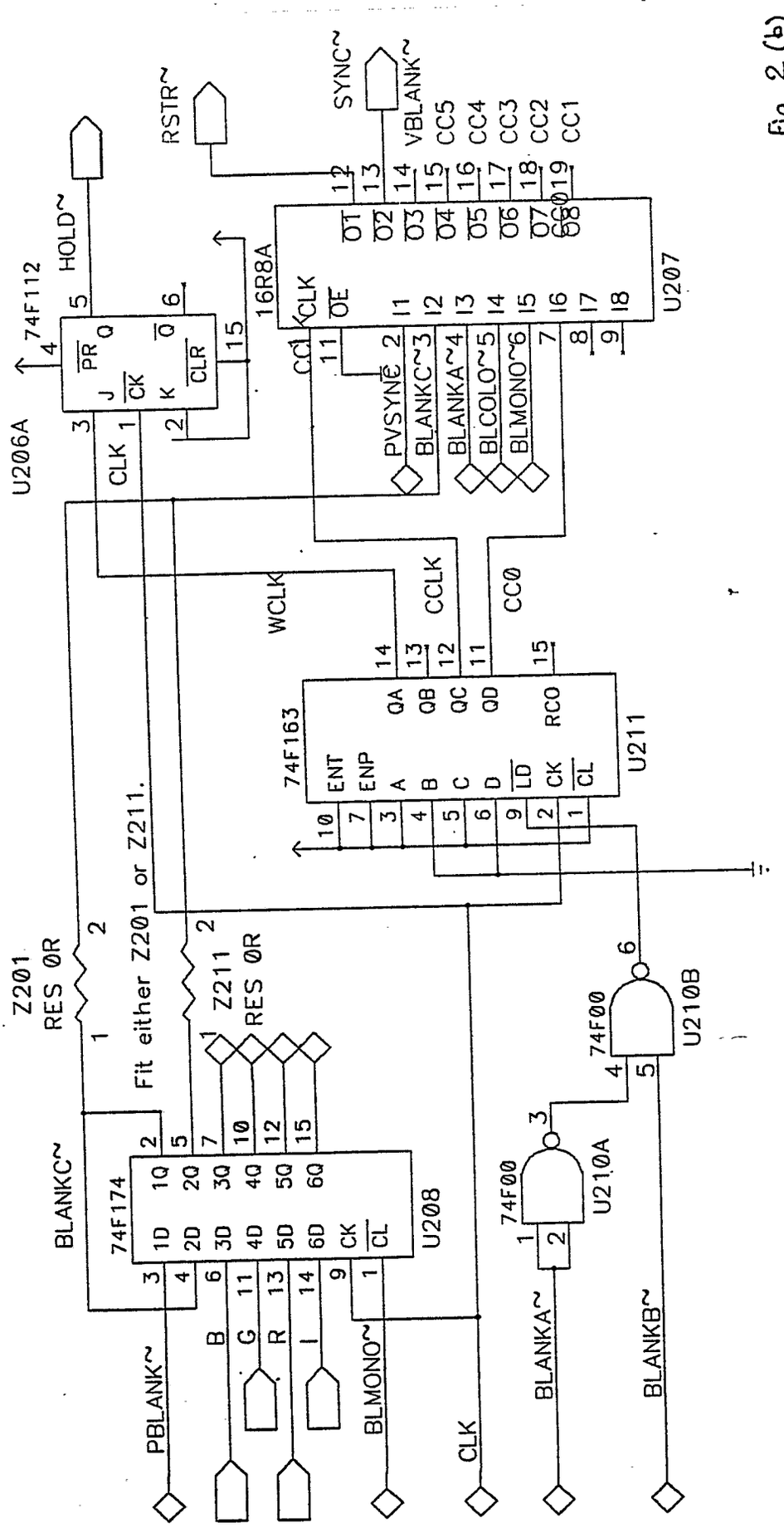

U206A
74F112
HOLD~
RSTR~
SYNC~
VBLANK~
CC5
CC4
CC3
CC2
CC1
16R8A
U207
PVSYNC~
BLANKC~
BLANKA~
BLCOLO~
BLMONO~
WCLK
CCLK
CC0
74F163
U211
Z201
RES 0R
Fit either Z201 or Z211.
Z211
RES 0R
BLANKC~
74F174
U208
PBLANK~
BLMONO~
CLK
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U210A
U210B
BLANKA~
BLANKB~

Fig 2 (b)

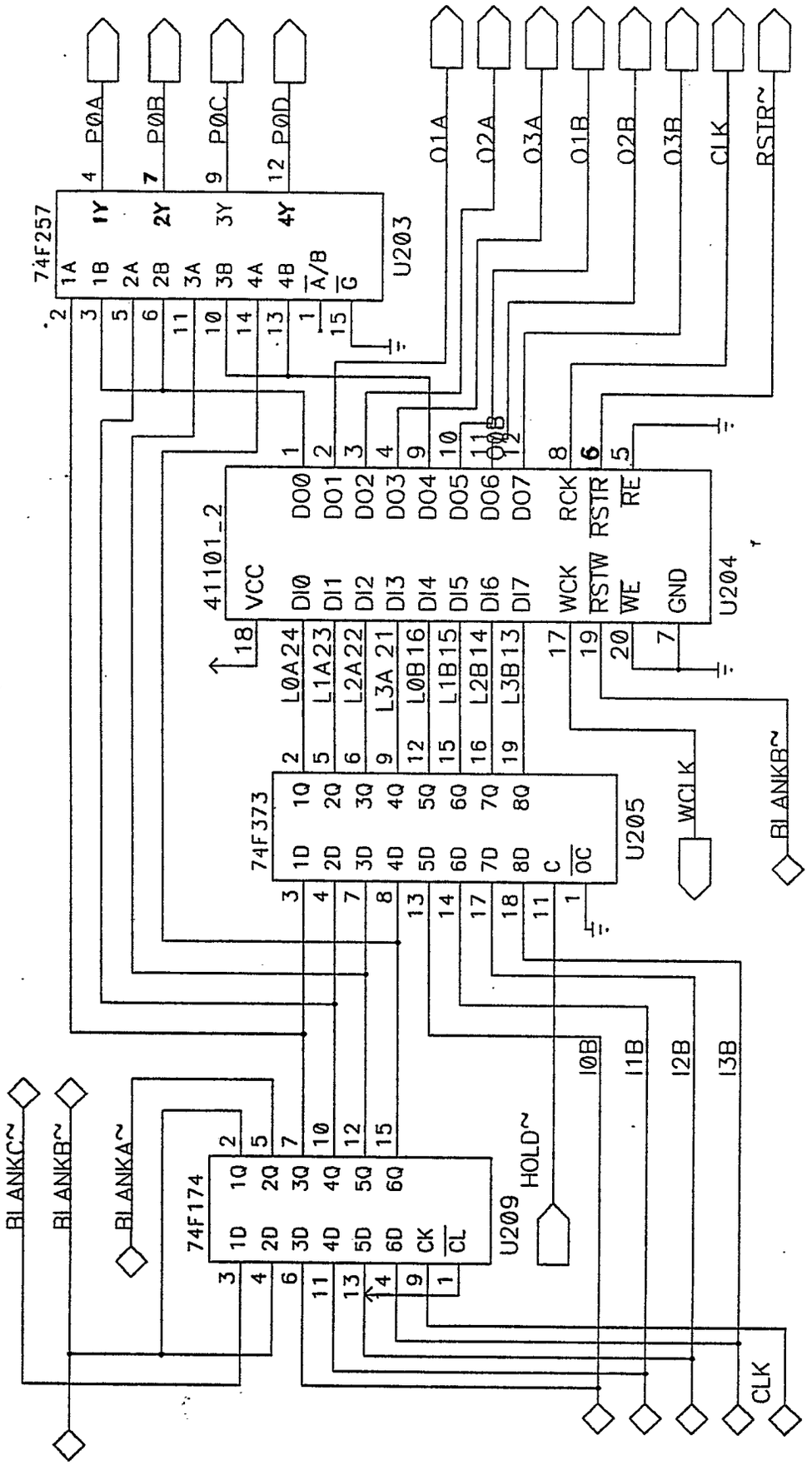

74F257
U203
P0A
P0B
P0C
P0D
Q1A
Q2A
Q3A
Q1B
Q2B
Q3B
CLK
RSTR~
41101_2
U204
74F373
U205
WCLK
BLANKB~
74F174
U209
HOLD~
BLANKC~
BLANKA~
I0B
I1B
I2B
I3B

Fig 2 (c)

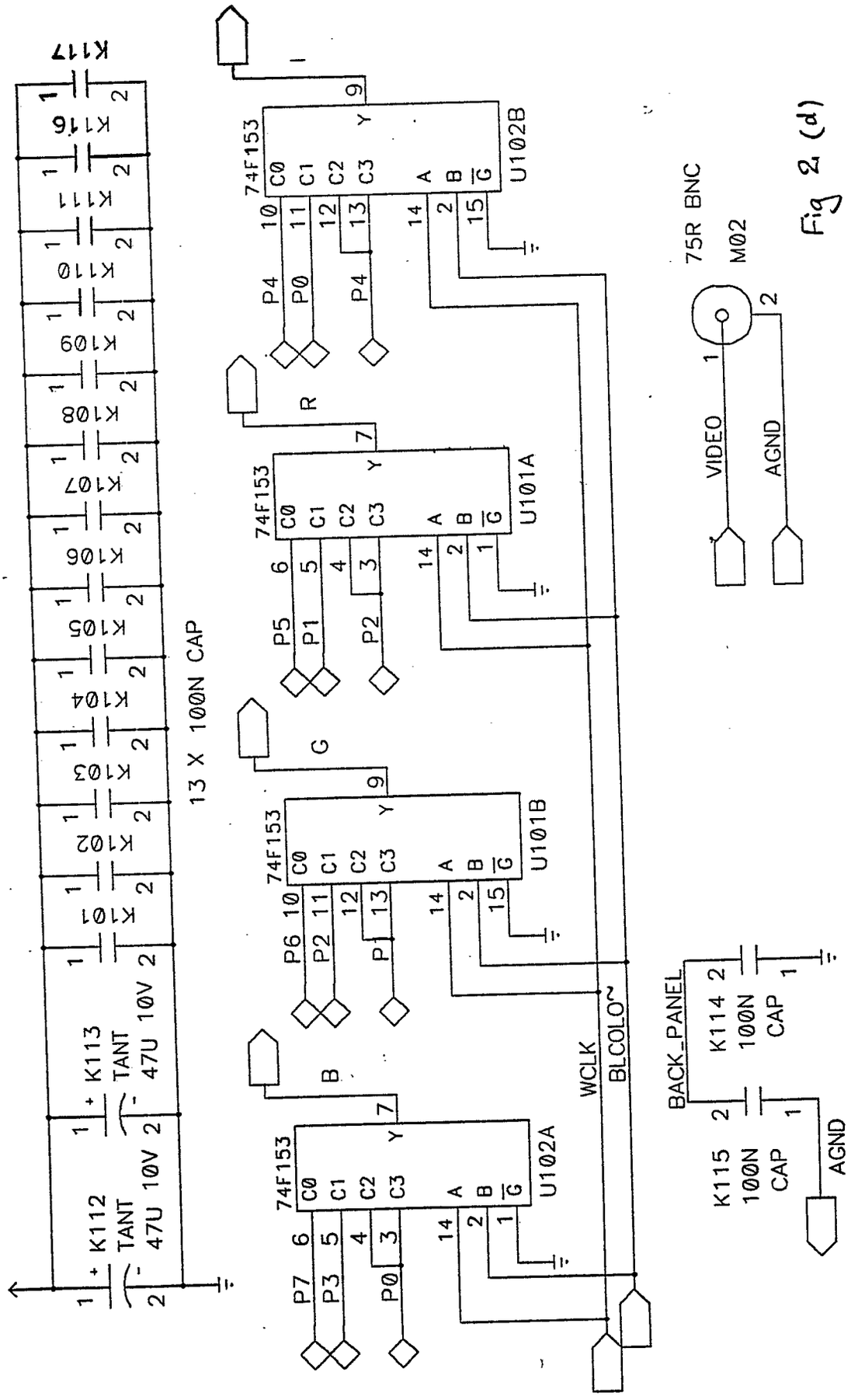

K117
K116
K111
K110
K109
K108
K107
K106
K105
K104
K103
K102
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K113
TANT
47U 10V
K112
TANT
47U 10V
74F153
U102B
U101A
U101B
U102A
P4
P0
P5
P1
P2
P6
P7
P3
P0
R
G
B
WCLK
BLCOLO~
75R BNC
M02
VIDEO
AGND
BACK_PANEL
K114
100N
CAP
K115
100N
CAP
AGND

Fig 2 (d)

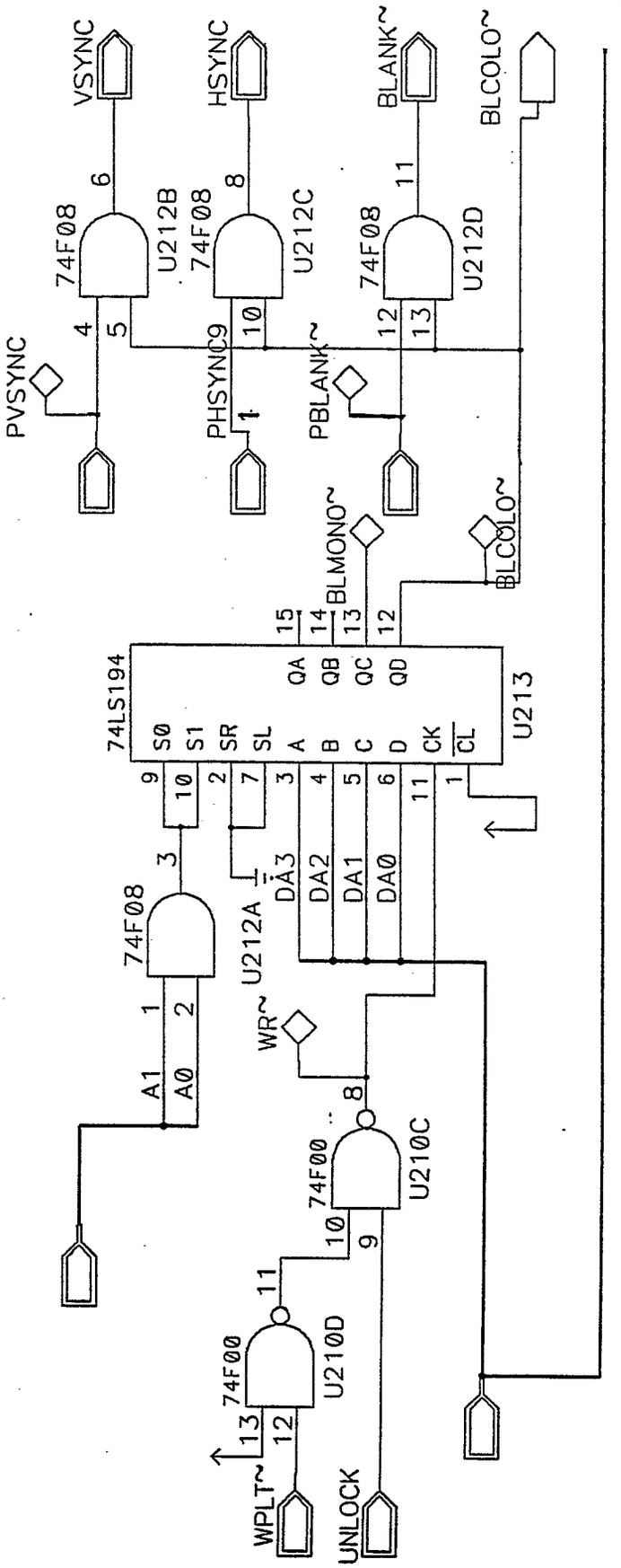

VSYNC
HSYNC
BLANK~
BLCOLO~
74F08
U212B
74F08
U212C
74F08
U212D
PVSYNC
PHSYNC
PBLANK~
BLMONO~
BLCOLO~
74LS194
U213
U212A
74F08
WR~
A1
A0
74F00
U210C
74F00
U210D
WPLT~
UNLOCK

Fig 2 (e)

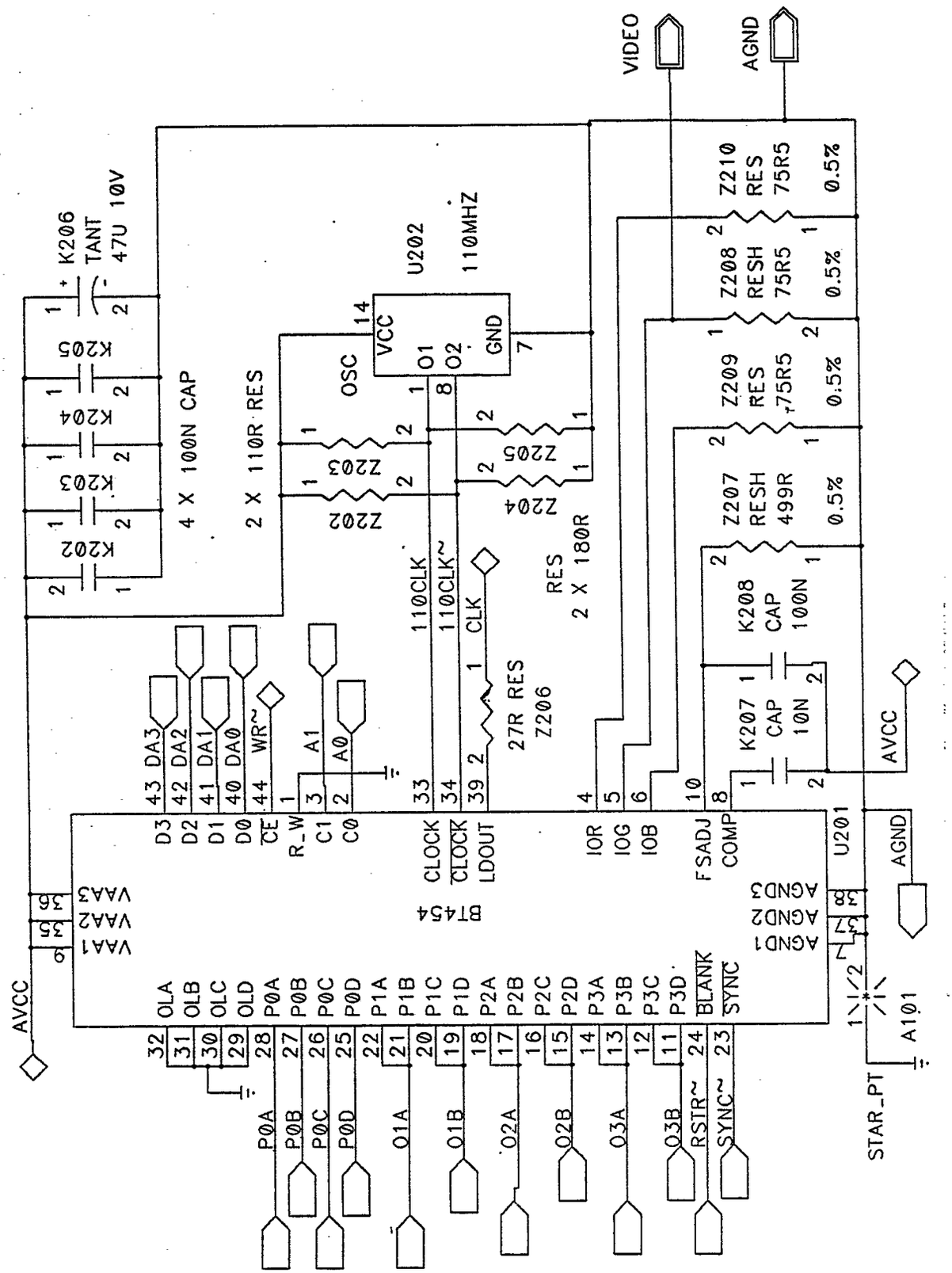

VIDEO
AGND
K206 TANT 47U 10V
4 X 100N CAP
K205
K204
K203
K202
2 X 110R RES
Z203
Z202
OSC
U202
110MHZ
VCC
GND
O1
O2
Z205
Z204
RES 2 X 180R
Z210 RES 75R5 0.5%
Z208 RESH 75R5 0.5%
Z209 RES 75R5 0.5%
Z207 RESH 499R 0.5%
K208 CAP 100N
K207 CAP 10N
AVCC
AGND
27R RES Z206
110CLK
110CLK~
CLK
D3 DA3
D2 DA2
D1 DA1
D0 DA0
CE WR~
R_W A1
C1 A0
C0
CLOCK
CLOCK
LDOUT
IOR
IOG
IOB
FSADJ
COMP
AGND3
AGND2
AGND1
U201
BT454
VAA3
VAA2
VAA1
OLA
OLB
OLC
OLD
P0A
P0B
P0C
P0D
P1A
P1B
P1C
P1D
P2A
P2B
P2C
P2D
P3A
P3B
P3C
P3D
BLANK
SYNC
RSTR~
SYNC~
A101
STAR_PT

Fig 2 (f)

Figure3: Video Timing Generator PAL Assembler Listing.

```
PAL16R8A                                        PAL DESIGN SPECIFICATION
U206
VGA Mono Option Board timing                                        V1.6

CCLK /VSYNC /BLANKC /BLANKA /BLCOLO /BLMONO CC0 NC8 NC9 GND
/OE /RSTR /SYNC /VBLANK /CC5 /CC4 /CC3 /CC2 /CC1 VCC

CC1 :=   /BLANKC * BLANKA                              ; Sync to 63
       + CC1 * /CC0                                    ; count
       + /CC1 * CC0
       + CC5 * CC4 * /CC3 * /CC2 * CC1 * /CC0          ; Reset on 50

CC2 :=   /BLANKC * BLANKA                              ; Sync to 63
       + /CC2 * CC1 * CC0                              ; count
       + CC2 * /CC1
       + CC2 * /CC0
       + CC5 * CC4 * /CC3 * /CC2 * CC1 * /CC0          ; Reset on 50

CC3 :=   /BLANKC * BLANKA                              ; Sync to 63
       + /CC3 * CC2 * CC1 * CC0                        ; count
       + CC3 * /CC2
       + CC3 * /CC1
       + CC3 * /CC0
       + CC5 * CC4 * /CC3 * /CC2 * CC1 * /CC0          ; Reset on 50

CC4 :=   /BLANKC * BLANKA                              ; Sync to 63
       + /CC4 * CC3 * CC2 * CC1 * CC0                  ; count
       + CC4 * /CC3
       + CC4 * /CC2
       + CC4 * /CC1
       + CC4 * /CC0
       + CC5 * CC4 * /CC3 * /CC2 * CC1 * /CC0          ; Reset on 50

CC5 :=   /BLANKC * BLANKA                              ; Sync to 63
       + /CC5 * CC4 * CC3 * CC2 * CC1 * CC0            ; count
       + CC5 * /CC4
       + CC5 * /CC3
       + CC5 * /CC2
       + CC5 * /CC1
       + CC5 * /CC0
       + CC5 * CC4 * /CC3 * /CC2 * CC1 * /CC0          ; Reset on 50

;Latch Blank signal at line centre:

VBLANK :=  /CC5*CC4*/CC3*CC2*/CC1*/CC0 * BLANKC        ; SET (20)
       + VBLANK * CC5                                  ; HOLD (not 20)
       + VBLANK * /CC4
       + VBLANK * CC3
       + VBLANK * /CC2
       + VBLANK * CC1
       + VBLANK * CC0
```

Figure 3 (continued):

```
RSTR :=  CC5 * /CC4 * /CC3 * CC2 * CC1 * /CC0                    ; Set (38)
         + RSTR * /CC5                                           ; Hold:  0-31
         + RSTR * /CC4                                           ;        32-47
         + RSTR * /CC3 * /CC2 * /CC1                             ;        48-49
         + RSTR * VBLANK * /BLCOLO                               ;  vert Blank (LOW RES)
         + RSTR * BLANKC *  BLCOLO                               ;  vert Blank (HIGH
         RES)

SYNC :=  CC5 * /CC4 * /CC3 * CC2 * CC1 * CC0                     ; Set (39)
         + SYNC * /CC5                                           ; Hold (not 35/43): 0-31
         + SYNC * CC5 * CC4                                      ; 48-63
         + SYNC * CC5 * /CC4 * /CC3 * /CC2                       ; 32-35
         + SYNC * CC5 * /CC4 * CC3 * /CC2 * /CC1                 ; 40-41
         + SYNC * CC5 * /CC4 * CC3 * /CC2 * CC1 *  CC0           ; 43
         + SYNC * CC5 * /CC4 * CC3 * CC2                         ; 44-47
         + VSYNC * SYNC * CC5* /CC4 * CC3* /CC2 * CC1 * /CC0 * /BLMONO    ;
         42 (vertical)
```