United States Patent [19]

Buozynski

[11] **3,821,606**

[45] **June 28, 1974**

[54] **POWER SUPPLY FOR GAS DISCHARGE DISPLAY PANEL SYSTEMS**

[75] Inventor: **Leonard M. Buozynski**, Toledo, Ohio

[73] Assignee: **Owens-Illinois**, Toledo, Ohio

[22] Filed: **Oct. 24, 1972**

[21] Appl. No.: **300,285**

[52] **U.S. Cl.** ..... **317/16**, 317/31, 323/22 T

[51] **Int. Cl.** **H02h 3/20**

[58] **Field of Search** ..... 317/31, 20, 16; 323/22 T

[56] **References Cited**

UNITED STATES PATENTS

3,114,873	12/1963	Love	323/22 T
3,397,350	8/1968	Garzon	317/141 S

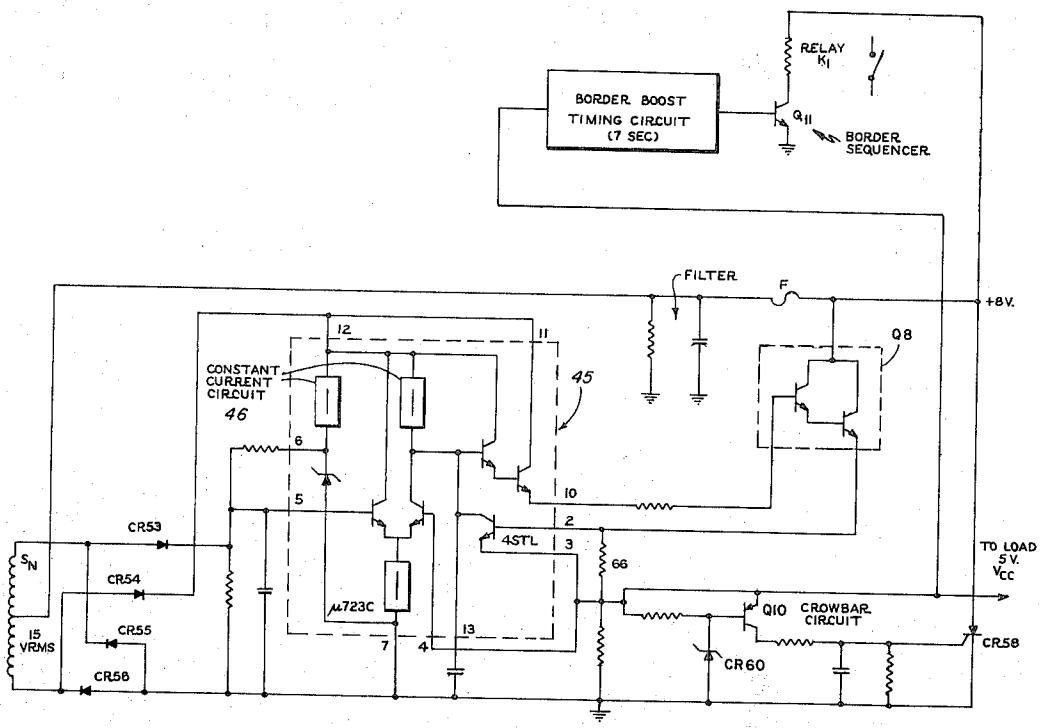
Primary Examiner—James D. Trammell

Attorney, Agent, or Firm—E. J. Holler; Donald Keith Wedding

[57] **ABSTRACT**

There is disclosed a multiple output power supply for supplying direct time potentials to circuits for operating gas discharge panels including sustainer and addressing supplies, border boost and bias supplies. The circuit has reduced power dissipation in sustainer and addressing supplies series pass transistors by phase controlling these devices; a simplified border boosting circuit, and an improved border sequencer. The power supply allows the display panel system to operate in the write mode as soon as the power supply is energized.

3 Claims, 3 Drawing Figures



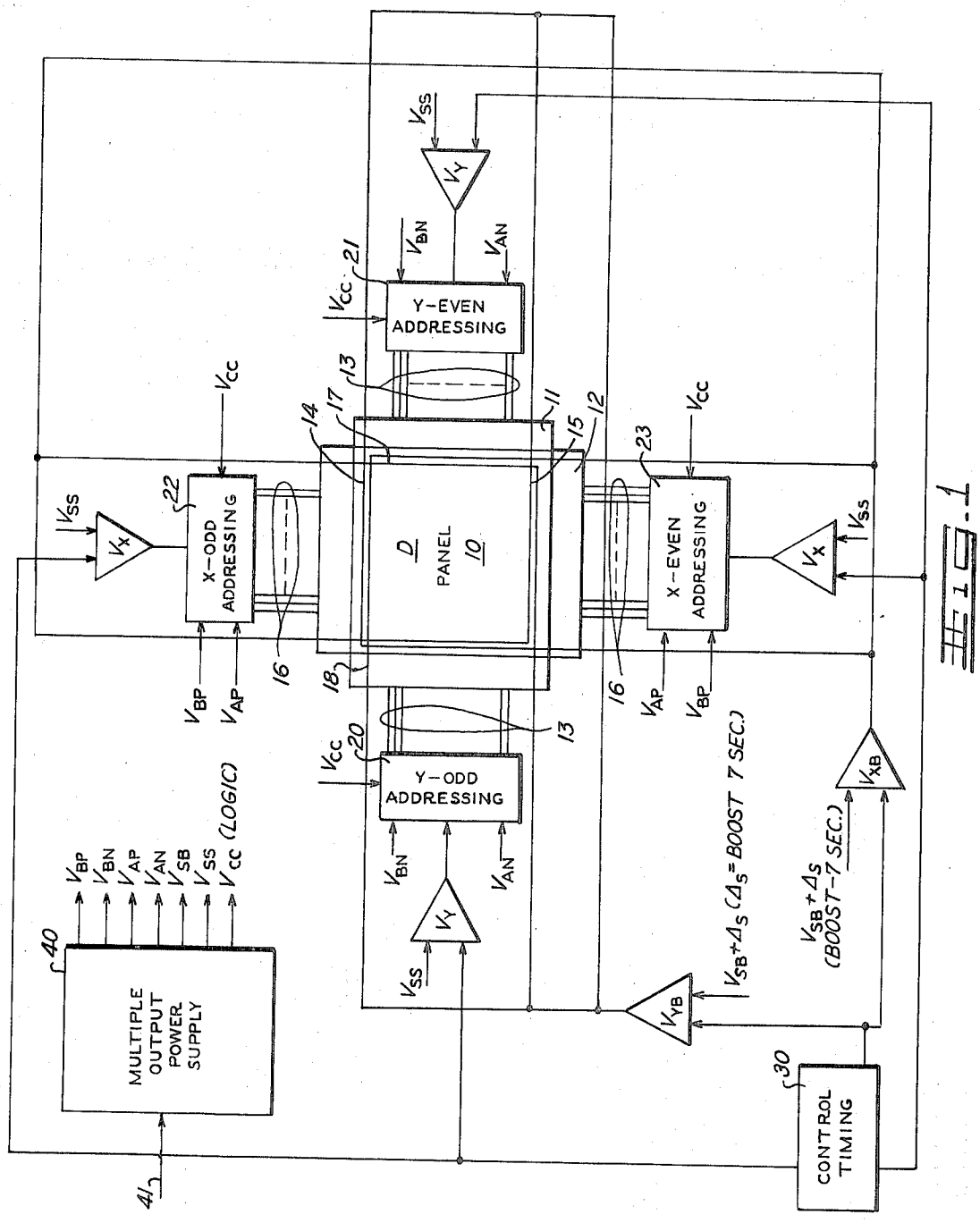

PANEL
10
Y-EVEN ADDRESSING
Y-ODD ADDRESSING
X-ODD ADDRESSING
X-EVEN ADDRESSING
MULTIPLE OUTPUT POWER SUPPLY
CONTROL TIMING
V_{SS}
V_Y
V_{BN}
V_{AN}
V_{CC}
V_X
V_{BP}
V_{AP}
V_{YB}
V_{XB}
$V_{SB}+\Delta_S$ (Δ_S= BOOST 7 SEC.)
$V_{SB}+\Delta_S$ (BOOST-7 SEC.)
V_{CC} (LOGIC)
V_{SB}
10
11
12
13
14
15
16
17
18
20
21
22
23
30
40
41

FIG. 1

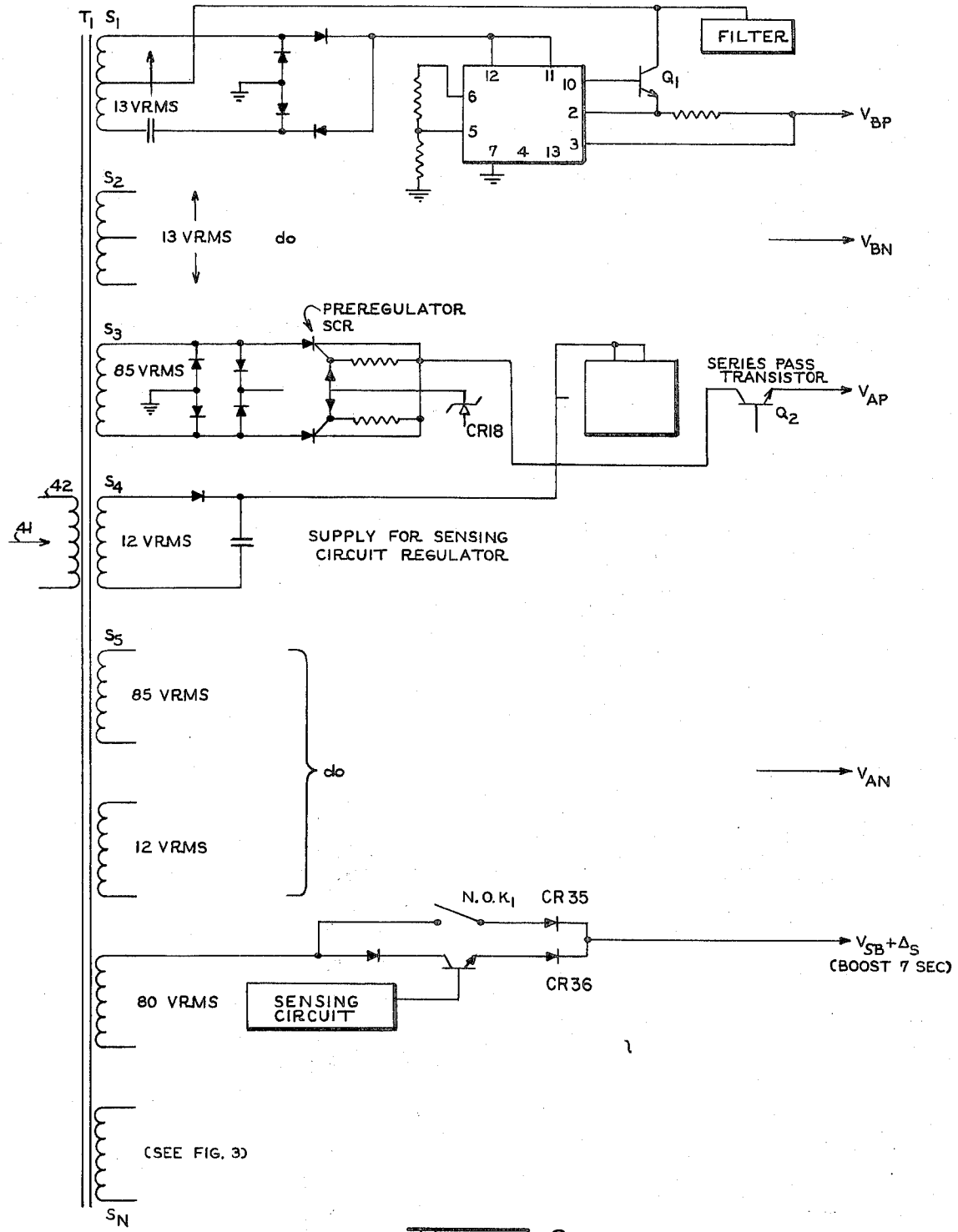

T1 S1
13 VRMS
FILTER
Q1
VBP
S2
13 VRMS
do
VBN
PREREGULATOR SCR
S3
85 VRMS
CR18
SERIES PASS TRANSISTOR
Q2
VAP
42
41
S4
12 VRMS
SUPPLY FOR SENSING CIRCUIT REGULATOR
S5
85 VRMS
do
12 VRMS
VAN
N.O.K1
CR35
CR36
VSB+ΔS
(BOOST 7 SEC)
80 VRMS
SENSING CIRCUIT
(SEE FIG. 3)
SN

FIG. 2

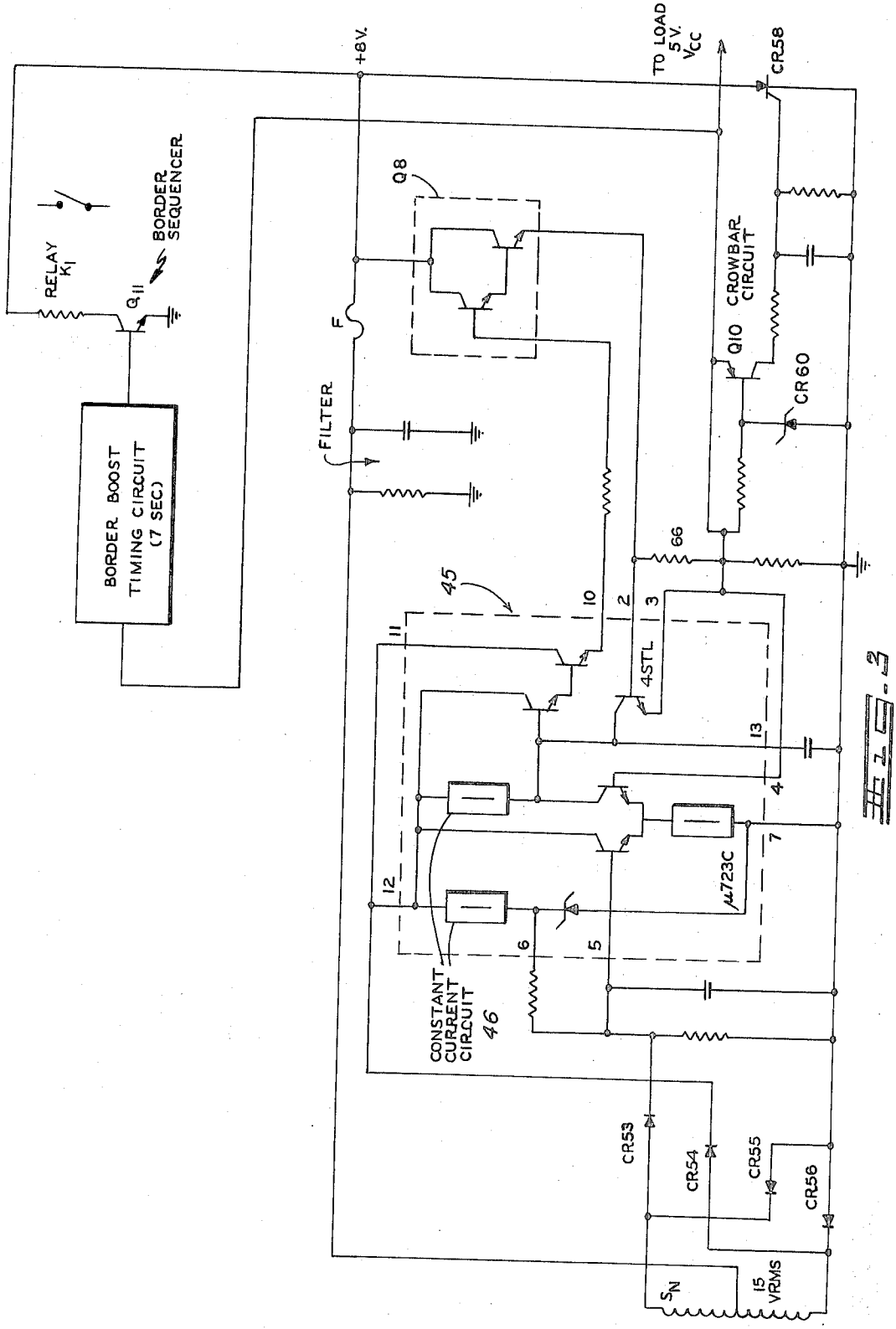

+8V.
TO LOAD
5V.
V_{CC}
CR58
Q8
F
FILTER
RELAY
K_1
BORDER
SEQUENCER
Q_{11}
BORDER BOOST
TIMING CIRCUIT
(7 SEC)
Q10 CROWBAR
CIRCUIT
CR60
66
45
10
2
3
11
4STL
13
4
7
12
μ723C
6
5
CONSTANT
CURRENT
CIRCUIT
46
CR53
CR54
CR55
CR56
S_N
15
VRMS

FIG. 3

POWER SUPPLY FOR GAS DISCHARGE DISPLAY PANEL SYSTEMS

The present invention relates to an improved multiple output power supply system for supplying direct current potentials to various circuits which, in turn, supply operating potentials to gaseous discharge display panels and systems.

Such panels and systems are disclosed in detail in Baker, et al. U.S. Pat. No. 3,499,167, for example. A typical display system supply arrangement is disclosed in Miavecz application Ser. No. 211,371, filed Dec. 23, 1971. In such systems, the power supply is used to provide various voltages for sustainer generators, addressing circuits, border boost and bias supplies. The present invention provides a multiple level power supply which has reduced power dissipation in the sustainer and addressing supplies series pass transistors by use of preregulators to maintain a fixed amount of input-output differential across the pass transistors in the regulator, which reduces power dissipated in the series path transistor. In addition, there is provided a simple border boosting circuit, an improved border sequencer arrangement and the system is adapted to allow the display to operate in the write mode as soon as the power supply is energized.

The invention will be better understood when considered with the following specification and the accompanying drawings wherein:

FIG. **1** is a block diagram of a gaseous discharge display panel and operating potential supply systems, to which the invention has particular utility,

FIG. **2** is a block diagram, partially schematic, illustrating the invention,

FIG. **3** is a circuit diagram illustrating an aspect of the invention for reducing power dissipation in the series pass transistors for the low voltage circuits and the border boost circuit relay.

FIG. **1** illustrates the general environment of the invention and is in part taken from the above-identified Miavecz application. As disclosed in FIG. **1**, a gaseous discharge display panel **10** preferably of the type disclosed in Baker, et al. U.S. Pat. 3,499,167, filled with a neon-argon gas mixture (99.9 percent neon and 0.1 percent argon) as is disclosed in Nolan application Ser. No. 764,577 filed Oct. 2, 1968, and as is further modified by a dielectric or insulative overcoating (not shown) on the dielectric coatings of the aforementioned Baker, et al. patent, which overcast may be a lead oxide of a few hundred angstroms thick. Typically, the discharge gap distance in such panels is selected to be between 4 and 6 mils. The panel **10** is constituted by a row conductor plate **11** and a column conductor plate **12** joined in spaced apart relation by a spacer sealant (not shown) to provide the aforementioned discharge gap distances and a thin gas discharge chamber with the gaseous medium therein.

The row conductor plate **11** carries a row conductor array **13** in the writing or the information display area D and a row border array **14** and **15** at the sides thereof. The column conductor plate **12** may be identical, having a column conductor array **16** in the writing or viewing area of the data display area D and border or side conductors **17** and **18** respectively. (The border conductors are shown as spaced from their respective row and column conductors, but in fabrication of the panel can be one or more end conductors in each array.) As indicated, the addressing circuits **20** and **21** for the row conductors and **22** and **23** for the column conductors, respectively, alternate or odd numbered conductors being driven by the odd addressing circuitry and the even conductors being driven by the even conductor addressing circuits, may be as disclosed in Budzynski U.S. Pat. No. 3,665,401 and, as shown, float upon their respective sustainer sources for these conductors in the panel. The bias voltage supplies VBP and VBN mentioned herein, are for the bias voltage supply **71** the diode switching circuits of FIG. 4A of U.S. Pat. 3,665,401, for example. The control of the sustainers Vx and Vy by control timing circuit **30**, and the panel and circuitry as described, is, for the purposes of this application conventional.

The present invention is directed to improvements in the multiple output power supply **40** shown in FIG. **2.** Alternating current line voltage is applied to the power supply **40** through line **41**, this voltage is supplied to power transformer T1 having a primary winding **42** and multiple secondary windings S1 ... S*n*. Transformer T1 isolates and transforms the line voltage, the transformer voltages being taken off the secondary windings S1 ... SN and routed to the various power supplies.

THE 5-VOLT SUPPLY (*Vcc*) — THE LOW VOLTAGE LOGIC SUPPLY (FIG. 3)

The alternating current voltage from transformer secondary SN is rectified by diodes **CR53, CR54, CR55** and **CR56.** This rectifier serves both as a full wave rectifier and a bridge rectifier with diodes **CR55** and **CR56** being high current diode rectifiers serving as the full wave rectifier for carrying the output current to the load. Diodes CR53 and CR54 are low current devices used for supplying the regulator. Regulator Change Sensor **45** is a conventional commercially available regulator of the integrated circuit type generally known as M723C and is available from Fairchild Industries, Inc. Regulator **45** is shown in detail in FIG. **3** in the large dashed block and it provides an output control voltage whenever there is a variation from a preselected nominal value of 5 volts (established by the Zener diode connected to pin **6.** Series pass transistor **Q8,** which may be constituted by an integrated circuit darlington pair of transistors, receives a control signal from integrated circuit regulator sensor **45.** It will be noted, however, that the regulator sensor itself receives approximately the full voltage of the bridge rectifier which is approximately 12–20 volts, whereas the series pass transistor Q8 receives approximately half this voltage as rectified by full wave rectifiers **CR55** and **CR56.** In this way, since the desired output is approximately 5 volts whereas the regulator circuit **45** requires at least approximately 12 volts for satisfactory operation, only a very small voltage drop is effected in series pass transistor Q8 thus lowering the power dissipation in the series regulating transistor.

As indicated, up to approximately 20 volts are applied to regulator sensor **45** which comprises a comparison amplifier and a reference supply (the Zener and Constant current source **46**). The comparison amplifier continually monitors the difference between the output voltage and the reference voltage. If there is a difference, an error signal is produced; the signal is of such a magnitude and polarity as to change the conduction of series regulation pass transistor **Q8.** This changes the current through the load (the display circuit) until the output voltage equals the reference voltage at **5** of reg-

ulator **45.** A more detailed explanation of the operation of integrated circuit amplifier **45** is available from the manufacturer of this device.

The load and power supply is protected against excessive output current by current limiting. When the current exceeds 4 amps, a 0.50 is dropped across series resistor **66** (on the output of series pass transistor Q8). This voltage is applied to an internal transistor in regulator sensor circuit **45** which is connected between pins **2** and **3** of regulator sensor **45.** This transistor (4STL) controls the output current by limiting the current driving the output transistor **Q8.** The output is effectively limited to about 4 amperes.

The load is also protected for over and under voltage. When an over-voltage or voltage transient appears on the output of the 5-volt supply due to external conditions or internal failues, a conventional crowbar circuit, constituted by CR58 and its associated driving circuitry, energizes (V exceeds 7 volts). This crowbar circuit is conventional and shorts the collector of pass transistor **Q8** to the 5-volt supply which, in turn, causes the fuse F to blow. Under-voltage is detected by diode CR60. When the 5-volt supply exceeds 4.75 volts, transistor **Q10** turns on which, in turn, energizes the sustainer regulator. The 5-volt regulator also energizes the sequencer circuit which turns on the border boost circuit for 7 seconds. The sequence starts when the supply is powered up.

BIAS POSITIVE AND BIAS NEGATIVE (*Vbp* and *Vbn*) SUPPLIES

The bias supplies described earlier herein are identical in operation to the *Vcc* supply and are not described in detail herein. They are indicated generally by the blocks so labeled in FIG. **2** of the drawings.

THE SUSTAINER AND ADDRESSING SUPPLIES (*Vss*, *Van* and *Vap*)

The sustainer and addressing supplies are different from the other units in the sense that the inputs are preregulated by phase control and the regulators are floated above the circuit returns. Each tracking preregulator maintains a fixed minimum input-output differential across the pass transistor (Q2). This circuit operates by holding the controlled rectifier (SCR) gates at some DC (direct current) value (determined by **CR18**) which fires the forward biased silicon controlled rectifiers SCR whenever the ripple voltage on the filter capacitor not shown drops to a level sufficient to exceed the gate to cathode threshold of the silicon controlled rectifiers. This reduces the voltage swing across the pass transistor (Q2) in FIG. **2.**

THE BORDER VOLTAGE SUPPLY (*Vsb*)

The border voltage is added to the sustainer voltage for lighting the border of the display panel **10,** the voltage on border conductors **14** and **17** is boosted above its normal voltage for about seven seconds in the initial turn-on phase to light the border sites. In its normal mode of operation, the border voltage can be 25, 35, or 40 volts above the sustainer voltage and in the booster mode of operation, this voltage is about 90 volts. A higher voltage is required to fire the borders in an initial or turn-on state for display panels. Thus, relay **K1** energizes the high voltage boost circuit for a period of about 7 seconds. This voltage is rectified by diode **CR35.** Diode **CR36** is used to protect the border voltage regulator during the boost mode of operation. The high voltage at the output will back bias **CR36** cutting off this diode. After the boost sequence, the boost voltage drops to zero and diode **CR36** is no longer back biased. Diode **CR36** therefore conducts and the voltage at this output returns to the lower voltage which can be the **25, 35** or **40** volts selected for boosting the sustainer voltage *Vss* to the normal on-state for the border site.

Thus, the invention achieves the objectives of providing a multiple output power supply for gaseous discharge display panels and systems which have the reduced power dissipation in sustainer and addressing supply series pass transistors, a simple border boosting circuit, an improved border sequencing arrangement and a power supply which allows the display system to operate in the write mode as soon as the power supply is energized.

Although the invention has been described in its preferred embodiment, it is clear that the basic principles thereof are applicable to other embodiments obvious to those skilled in the art and it is intended that the claims encompass such other obvious embodiments.

What is claimed is:

1. In a multiple output power supply for supplying multiple level direct current operating potentials to sustainer generators, addressing, logic and border and border boost supplies of a gas discharge display panel having inherent memory, said power supply including a transformer having a primary and multiple secondary windings, multiple recitfier means each connected to a respective secondary winding, multiple filter means each connected to a respective rectifier means, multiple voltage regulator means each connected to a respective filter means, each regulator including a voltage change sensing circuit and a series pass transistor controlled thereby for controlling the output voltage thereof to a load,

the improvement wherein at least one of said direct current voltages is relatively low in magnitude and the voltage required to operate said voltage change or sensing circuit is substantially higher than the desired relatively low voltage output,

the respective transformer for said supply having a center tapped winding with the voltage at said center tap being rectified and applied to the series pass transistor and the higher voltage across said secondary winding being rectified and applied to said voltage change sensing circuit.

2. The invention defined in claim **1** including a relay,

timing means having a selected time of internal operation following energizing thereof connected to said relay for energizing same,

means for energizing said timing means on appearance of said desired low voltage output, said relay having a switch element which shunts the border series pass regulating transistor causing a larger voltage to be applied to the border of said display panel for said selected time interval.

3. The invention defined in claim **1** wherein between at least one of said voltage change sensing circuits and said rectifier means there is connected a preregulator for limiting the voltage swing to be controlled by the pass transistor thereof.

* * * * *

B-12841

PO-1050
(5/69)

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,821,606 Dated June 28, 1974

Inventor(s) LEONARD M. BUDZYNSKI

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

	READS	SHOULD READ
COVER - PAGE 1 Inventor's Name	Leonard M. Buozyński	Leonard M. Budzynski
column 2, line 61	Constant	constant
" 3, " 17	failues	failures
" 4, " 31	recitfier	rectifier

Signed and sealed this 29th day of October 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

B-12841

PO-1050
(5/69)

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,821,606 Dated June 28, 1974

Inventor(s) LEONARD M. BUDZYNSKI

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

	READS	SHOULD READ
COVER - PAGE 1 Inventor's Name	Leonard M. Buozynski	Leonard M. Budzynski
column 2, line 61	Constant	constant
" 3, " 17	failues	failures
" 4, " 31	recitfier	rectifier

Signed and sealed this 29th day of October 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents