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(71) Applicant: OSRAM GMBH [DE/DE]; Marcel-Breuer-Strasse 6, D-80807 München (DE).

(71) Applicant *(for IT only)*: OSRAM S.P.A. - SOCIETA' RIUNITE OSRAM EDISON CLERICI [IT/IT]; Viale dell'Innovazione, 3, I-20126 Milano (IT).

(72) Inventor: ANGELIN, Francesco; Via Vespucci, 16/A, I-31021 Mogliano Veneto (Treviso) (IT).

(74) Agent: MEINDL, Tassilo; Buzzi, Notaro & Antonielli d'Oulx S.r.l., via Maria Vittoria, 18, I-10123 Torino (IT).

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(54) **Title**: ELECTRONIC CONVERTER AND RELATED METHOD OF OPERATING AN ELECTRONIC CONVERTER

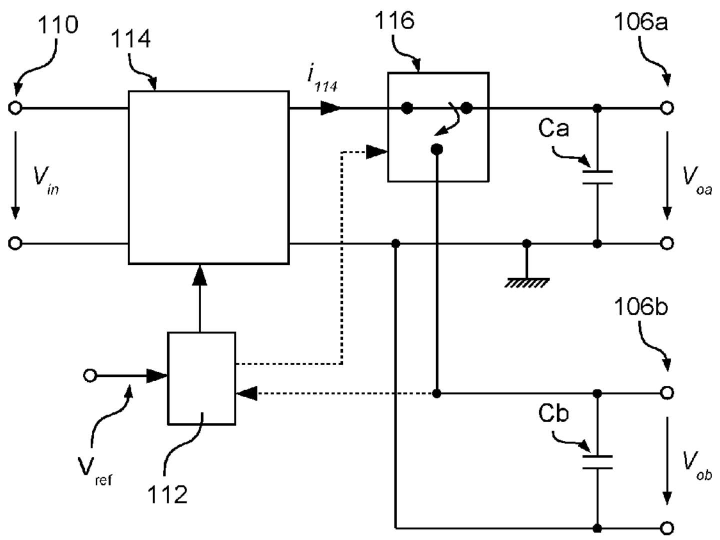

Fig. 7

(57) **Abstract**: There is described an electronic converter (12) comprising - a switching stage (114) comprising at least one electronic switch (S), wherein said switching stage (114) is adapted to provide a current (i_{114}) via a terminal; - a first capacitor (Ca), wherein said first capacitor (Ca) provides a first voltage {V_{oa}). Specifically, converter (12) further comprises: - a second capacitor (Cb), wherein the second capacitor (Cb) provides a second voltage {V_{ob}), - comparison means (1162, D2) configured to detect the difference between the first voltage (V_{oa}) and the second voltage (V_{ob}), and determine a comparison signal which indicates whether this difference is greater than a threshold, and - switching means configured to transfer selectively current (i_{114}) to the first capacitor (Ca) or the second capacitor (Cb) as a function of the comparison signal.

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"Electronic converter and related method of operating an electronic converter"

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Field of the Invention

The description relates to electronic converters.

The description was devised with particular attention paid to the implementation of electronic converters providing a plurality of voltages.

Description of the Related Art

Electronic converters for light sources, comprising e.g. at least one LED (Light Emitting Diode) or other solid-state lighting means, may offer a direct current output. Such current may be steady or vary in time, e.g. in order to adjust the brightness emitted by the light source (so-called dimming function).

Figure 1 shows a possible lighting arrangement comprising an electronic converter 10 and a lighting module 20 including, e.g., at least one LED L.

For instance, Figure 2 shows an example of a lighting module 20 comprising a LED chain, i.e. a plurality of LEDs connected in series. As an example, Figure 2 shows four LEDs L_1, L_2, L_3 and L_4.

Electronic converter 10 usually comprises a control circuit 102 and a power circuit 12 (e.g. an AC/DC or DC/DC switching power supply) which receives at an input a supply signal (e.g. from the mains) and provides at an output, via a power output 106, a voltage V_0. Such a voltage may be steady or vary in time. E.g., control circuit 102 may set, via a reference signal V_{ref} of power circuit 12, the voltage provided at output 106 for feeding lighting module 20. In this case, lighting module 20 may include a current regulator 22, connected in series with light sources L for limiting the current.

Generally speaking, there are known many types of electronic converters, such as for example "*buck*", "*boost*", "*buck-boost*", "*flyback*" or "*forward*" converters. Such converter topologies are well known to the person skilled in the art.

For example, Figure 3 shows the circuit diagram of a flyback converter 12, wherein a lighting module 20 is connected to output 106 of converter 12.

As known, a flyback converter comprises a transformer T with a primary winding T1 and a secondary winding T2, an electronic switch S, such as an n-channel MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), a rectification diode D and an output capacitor C.

Specifically, transformer T may be modelled as an inductor Lm connected in parallel with primary winding T1, which represents the magnetising inductance of transformer T, and an ideal transformer with a given ratio of the numbers of turns 1:n.

In the presently considered example, converter 12 receives at input, via two input terminals 110, a voltage V_{in} and provides at output, via two output terminals 106, a regulated voltage V_o. The person skilled in the art will appreciate that voltage V_{in} may also be obtained from an AC input current, for instance via a rectifier, e.g. a diode-bridge rectifier, and optionally via a filter capacitor.

The first input terminal (positive terminal) is connected to the first terminal of primary winding T1 of transformer T, and the second input terminal (negative terminal) represents a first ground GND_1. On the other hand, the second terminal of primary winding T1 of transformer T is connected via switch S to ground GND_1. Therefore, switch S may be used for activating selectively the current flow through primary winding T1 of transformer T.

In a flyback converter, secondary winding T2 of transformer T is connected via a diode D to an output capacitor C. Specifically, the first terminal of rectification winding T2 is connected to the anode of diode D, and the cathode of diode D is connected to a first output terminal (positive terminal). On the other hand, the second terminal is connected directly to the second output terminal (negative terminal), which represents a second ground GND_2, which due to the insulating effect of transformer T is preferably different from ground GND_1 and therefore is denoted with a different ground symbol.

Finally, capacitor C is connected in parallel with output 106.

As a consequence, when switch S is closed (first operating interval), primary winding T1 of transformer T is connected directly to input voltage V_{in}. This causes an increase of the magnetic flux in transformer T. Therefore, the voltage across secondary winding T2 is negative and diode D is reverse biased. In this condition, output capacitor C provides the energy required by lighting module 20.

On the other hand, when switch S is opened (second operating interval), the energy stored in transformer T is transferred as flyback current to the secondary side.

Typically, both operating intervals are repeated periodically. For example, a converter normally also comprises a driver circuit 112, controlling the switching of switch S as a function of a feedback signal. For example, such driver circuit 112 may be designed for repeating the operating intervals at a fixed frequency, wherein the energy transfer is controlled via a PWM signal, i.e. the durations of the first and of the second time intervals are variable, while the sum of the durations is constant. The person skilled in the art will appreciate that such PWM driving and the control of the durations of the operating intervals are well known and that they can be implemented e.g. via a feedback of the output voltage via an error amplifier. For example, in the case of a voltage control, the duration of the first time interval is increased until the (average) output voltage corresponds to a desired value.

An electronic converter is often required to generate a plurality of voltages. For example, this may be useful for generating a supply for the control circuit 102 and/or for the driver circuit 112.

For example, Figures 4 and 5 show various solutions of multiple output supplies, having e.g. two outputs 106a and 106b, by resorting again e.g. to a flyback topology.

In the diagram of Figure 4, transformer T is provided with two secondary windings T2a and T2b (a winding for each output 106a and 106b). Moreover, on the secondary side for each secondary winding T2a and T2b there is provided a rectification/filter network of a typical flyback converter, respectively including a diode Da/Db and a capacitor Ca/Cb. Therefore, generally speaking, a way to obtain multiple outputs consists in arranging several windings on the same transformer.

The solution according to Figure 5, on the other hand, provides one secondary winding T2 and derives the auxiliary output(s) (e.g. output 106b) from main output 106a via an additional converter 12b.

For example, such converter 12b may be a switching converter, such as e.g. a buck converter. This solution is efficient in energy consumption, but requires a number of additional components. Therefore, it is a costly solution and it is rather bulky, especially with reference to its use for generating an auxiliary low-power supply.

Generally speaking, converter 12b may also be implemented via a linear regulator. This solution is simple and may be implemented easily with a low number of components, but has the drawback of a high dissipation of the linear regulator, so that the possible application field is restricted to situations wherein the voltage difference and the current supplied at output are low.

Object and Summary

The present description aims at overcoming the previously outlined drawbacks. Specifically, the inventor has observed that it would be useful to derive a plurality of outputs at different voltages from one switching converter, without the addition of further magnetic components or the arrangement thereon of multiple plugs, and without the addition of further switching regulators or linear regulators.

According to various embodiments, said object is achieved thanks to an electronic converter having the features set forth in the claims that follow. The claims also concern a related method of operating an electronic converter.

The claims are an integral part of the technical teaching provided herein with reference to the invention.

As previously stated, the present description relates to a converter which provides a plurality of voltages.

In various embodiments, the electronic converter comprises a switching stage with at least one electronic switch which provides a current via a terminal. The other output terminal typically represents a ground. The converter moreover comprises a first and a second capacitor, which may be charged by the current and which respectively provide a first and a second voltage.

In various embodiments, the converter comprises comparison means for detecting the difference between the first and the second voltage. Such comparison means moreover determine a comparison signal indicating whether the difference is greater than a given threshold. For example, the comparison means may be implemented via a comparator, e.g. a comparator with hysteresis or a Zener diode.

In various embodiments, the converter moreover comprises switching means, which are interposed between the terminal providing the current and the capacitors. Specifically, such switching means are provided for transferring selectively the current to the first or to the second capacitor as a function of the comparison signal. For example, the switching means may be implemented via a diode and an electronic switch. Substantially, such a diode guarantees that the first capacitor does not discharge towards the second capacitor. Generally speaking, such a diode may be also implemented as a rectification diode of the switching stage, e.g. the rectification diode of a boost or a flyback converter.

Specifically, in various embodiments, the switching stage provides current pulses, i.e. at given instants the supplied current is equal to zero. In this case, the operation of the switching means is preferably synchronized with such current pulses.

For example, in various embodiments the switching means include a current sensor and a detection circuit, which detects a signal indicating whether the current is equal to zero. In this case, the switching means may transfer selectively the current pulses to the first or to the second capacitor also as a function of such a signal. For example, in various embodiments, the switching means may comprise a latch or a flip-flop, so that a current pulse may be transferred completely to the first capacitor when the voltage difference is smaller than the threshold. On the contrary, a current pulse is transferred completely to the second capacitor when the voltage difference is greater than the threshold.

In other embodiments, the switching means may be implemented via an SCR which is connected between the terminal providing the current pulses and the second capacitor. In this case, the SCR trigger may be driven by a Zener diode, which is connected between the first capacitor and the SCR gate. For example, if the SCR has a low critical rate of rise, every current pulse will be again transferred completely to the first or to the second capacitor.

Brief Description of the Annexed Views

The invention will now be described, by way of non-limiting example only, with reference to the annexed views, wherein:

- Figures 1 to 5 have already been described in the foregoing,
- Figure 6 shows a typical electronic converter with voltage control;
- Figure 7 shows an embodiment of an electronic converter providing two voltages,
- Figures 8 to 11 show details of embodiments of the electronic converter of Figure 7,
- Figure 12 shows a second embodiment of an electronic converter providing two voltages,
- Figures 13 to 15 and 18 show details of embodiments of the electronic converter of Figure 12,
- Figure 16 shows a third embodiment of an

electronic converter providing two voltages, and

- Figure 17 shows a fourth embodiment of an electronic converter providing three voltages.

Detailed Description of Embodiments

In the following description, numerous specific details are given to provide a thorough understanding of the embodiments. The embodiments can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring various aspects of the embodiments.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the possible appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

The headings provided herein are for convenience only and do not interpret the extent of protection or scope of the embodiments.

In the following Figures 6 to 18, the parts, elements or components which have already been described with reference to Figures 1 to 6 are denoted with the same references previously used in such Figures; the description of such previously described elements will not be repeated in the following, so as not to overburden the present detailed description.

As previously stated, the present description provides solutions for generating an auxiliary voltage in a switching converter.

Figure 6 shows the architecture of a general electronic converter which receives at input, via two input terminals 110, a voltage V_{in}, for example a DC voltage, and provides at output, via two output terminals 106, a DC voltage V_O.

In the presently considered embodiment, converter 12 includes a capacitor C providing voltage V_O, i.e. capacitor C is connected (e.g. directly) between both output terminals 106. The converter moreover comprises a switching stage 114, which includes at least an electronic switch, and a driver circuit 112 which drives the at least one electronic switch of stage 114 as a function of output voltage V_o. For example, this sort of arrangement is applicable at least to *buck*, *boost*, *buck-boost*, *Cuk*, *SEPIC*, *ZETA*, *flyback* or *forward* converters.

Generally speaking, switching stage 114 therefore comprises two output terminals (the first terminal providing a current i_{114} and the second terminal representing a ground GND), and current i_{114} charges selectively capacitor C, so that voltage V_o across capacitor C corresponds to a desired value.

For example, driver circuit 112 may be a PWM driver circuit, which increases or decreases the duty cycle of at least one driving signal, until output voltage V_o corresponds (in average) to a desired value. Driver circuit 112 may also include a comparator with hysteresis, which activates or deactivates stage 114 when the output voltage respectively reaches an upper or a lower threshold. The various topologies and the driving thereof are well known to the person skilled in the art, which makes the detailed description thereof unnecessary.

Figure 7 shows a first embodiment of a switching converter which is adapted to generate two voltages. Specifically, in this embodiment too there is provided a switching stage 114 providing a current i_{114}.

In the presently considered embodiment, for every output 106a and 106b there is provided a respective output capacitor Ca and Cb, respectively providing the output voltages V_{oa} and V_{ob}.

In the presently considered embodiment, circuit 12 moreover includes switching means 116, which are interposed between switching stage 114 and the various output capacitors Ca/Cb. Specifically, such switching means 116 are adapted to transfer selectively current i_{114} supplied by stage 114 to either output capacitor Ca or Cb.

For example, in the presently considered embodiment, switching means 116 are implemented by a changeover switch, and driver circuit 112 is adapted to drive the switching of changeover switch 116.

Specifically, in the presently considered embodiment, driver circuit 112 normally keeps the changeover switch in a first position, wherein current i_{114} is transferred to the first branch, i.e. to capacitor Ca. During this step, control circuit 112 may use voltage V_{oa} across capacitor Ca for driving the switching stage 114.

In various embodiments, control circuit 112 simultaneously monitors voltage V_{ob} of the second branch, i.e. to capacitor Cb, and when voltage falls below a given threshold, driver circuit 112 shifts changeover switch 116 to a second position, wherein current i_{114} is transferred to the second branch, thereby charging capacitor Cb again. During this step, control circuit 112 may therefore use voltage V_{ob} across capacitor Ca for driving switching stage 114.

Therefore, in the present embodiment, control circuit 112 should be modified in such a way as to enable the use of two feedback signals. However, control circuits are often implemented via integrated circuits, which makes the modification of such circuits costly.

Therefore, in various embodiments, switching means 116 are configured to control directly the transfer of current i_{114} towards capacitor Ca or capacitor Cb.

Figure 8 shows a first embodiment of switching means 116. Specifically, in the considered embodiment, output 106a is assumed to provide a voltage V_{oa} which is greater than voltage V_{ob} required for output 106b.

In this case, changeover switch 116 may be implemented via a diode D1, such as e.g. a Schottky diode, and an electronic switch 1160, such as a metal-oxide-semiconductor field-effect transistor (MOSFET). Specifically, in the presently considered embodiment, the terminal providing current i_{114} is connected (e.g. directly) to the anode of diode D1, and the cathode of diode D1 is connected (e.g. directly) to a first terminal (positive terminal) of capacitor Ca, associated to output 106a. On the contrary, the second terminal of capacitor Ca is connected (e.g. directly) to ground GND. The terminal which provides current i_{114} is moreover connected, via switch 1160 (e.g. directly) to a first terminal (positive terminal) of capacitor Cb, and the second terminal (negative terminal) of capacitor Cb is connected (e.g. directly) to ground GND.

Therefore, in the presently considered embodiment, diode D1 guarantees that capacitor Ca is not discharged towards capacitor Cb. Such diode D1 may also correspond to a rectification diode of switching stage 114. For example, diode D1 may correspond to diode D shown in Figure 3 for a flyback converter. Such a diode is present, for example, in a boost converter as well.

In the presently considered embodiment, the switching of switch 1160 is driven by a comparator 1162, adapted to compare the difference between voltages V_{oa} and V_{ob} with a threshold TH, i.e:

- when the difference between voltages is smaller than threshold TH, switch 1160 is opened and current i_{114} charges capacitor Ca, increasing voltage V_{oa}, and
- when the difference between voltages is greater than threshold TH, switch 1160 is closed and current i_{114} charges capacitor Cb, increasing voltage V_{ob}.

In various embodiments, comparator 1162 may be a comparator with hysteresis, so as to reduce the switching frequency of switch 1160.

Therefore, in the embodiment, the difference of voltages V_{oa} and V_{ob} is kept substantially constant, and it is sufficient for the converter to perform a voltage control. Generally speaking, driver circuit 112 may drive switching stage 114 as a function of either voltage V_{oa} or voltage V_{ob}. For example, in the presently considered embodiment, driver circuit 112 is adapted to drive switching stage 114 in such a way as to regulate voltage V_{ob}, i.e. the smaller voltage, to the desired value. In this case, voltage V_{oa} is set approximately to $V_{ob} + TH$. Generally speaking, the regulation preferably uses the voltage of the output requiring the higher accuracy.

The previously described embodiment is of very easy implementation; however, it has the drawback that the switching of switch 1160 does not take place at zero current.

In this respect, the inventor has observed that several switching stages 14 have the feature that current i_{114} at the output of switching stage 114 is not continuous but discontinuous, i.e. in some periods it is equal to zero. Such a feature may be intrinsic to the topology of the converter. For example, as described with reference to Figure 3, in a flyback converter the current provided to secondary winding T2 of the transformer is intrinsically discontinuous. The same is true, for example, for a boost or buck-boost converter, wherein energy is transferred to the output capacitor only during one of the switching cycles. On the contrary, in other converters, the discontinuity may derive from the type of driving. For example, the current provided by a buck converter may be discontinuous, if the buck converter is operated in the *Discontinuous Current Mode* (DCM). The person skilled in the art will appreciate that a buck converter typically operates in a discontinuous mode when the load absorbs a low current, and in continuous mode at higher levels of absorbed current.

Therefore, in various embodiments, the operation of circuit 116 is synchronized with the switching of switching stage 114, in such a way as to reduce the switching losses of switch 1160. Generally speaking, such synchronization may be obtained by monitoring the driving signal of stage 114 and/or, as shown in Figure 9, by monitoring a signal identifying current i_{114}.

For example, in the presently considered embodiment, circuit 116 includes a sensor adapted to detect current i_{114} directly at the output of switching stage 112, or to detect another signal identifying such current, e.g. the current flowing through switch 1166.

In the presently considered embodiment, the signal detected by sensor 1166, such as e.g. a shunt resistor, is supplied to a detection circuit 1168 which determines if the detected current is equal to zero.

In this case, the synchronization with current i_{114} may be obtained via a processing circuit 1164, which determines the driving signal for switch 1160 as a function of the signal provided by comparator 1162 and of the signal provided by the detecting circuit 1168.

In the simplest of cases, processing circuit 1164 may be a latch SR. Specifically, in the presently considered embodiment, the signal at the output of comparator 1162 sets latch 1164 to logic level "1" and closes switch 1160 when the voltage difference exceeds threshold TH. On the other hand, the latch is reset when the current detected by circuit 1168 falls to zero again.

In this case, which will be called *split pulse mode* in the following, an initial part of a current pulse is transferred to output 106a, i.e. the output with the greater voltage, and when comparator 1162 detects that the voltage difference exceeds threshold TH, the second part of the current pulse is transferred to output 106b. As a matter of fact, latch 1164 is reset only when the current detected by sensor 1166 falls to zero again.

For example, Figure 10a shows a possible profile of current i_{114}, Figure 10b shows the difference of voltages V_{oa} and V_{ob}, and Figures 10c and 10d respectively show current i_{D1} flowing through diode D1, i.e. the current charging capacitor Ca, and current i_{1160} flowing through switch 1160, i.e. the current charging capacitor Cb.

Specifically, in the presently considered example, there are shown three pulses for current i_{114}:

- the first pulse is transferred completely to capacitor Ca, because the voltage difference is still smaller than threshold TH;

- during the second pulse, the difference between voltages V_{oa} and V_{ob} reaches threshold TH and switch 1160 is closed via latch 1164, and the current is transferred to capacitor Cb from this moment on;

- also the third pulse is transferred completely to capacitor Ca, because the voltage difference is still smaller than threshold TH.

This embodiment offers the advantage that output voltages V_{oa} and V_{ob} have only a reduced ripple, because both capacitors Ca and Cb may be charged at each current pulse. However, this embodiment has the disadvantage that the closing of switch 1160 does not take place at zero current, i.e. only the opening is synchronized with current i_{114}.

For this reason, circuit 1164 may be configured for transferring each current pulse completely to one of capacitors Ca or Cb, which will be named *full pulse mode* in the following. For example, this may obtained via a circuit 1164 which includes a latch D, wherein the signal provided by comparator 1162 is only sampled when current i_{114} is equal to zero, i.e. the signal provided by circuit 1168 may be used as an enablement signal of said latch.

For example, Figure 11a shows a possible profile of current i_{114}, Figure 11b shows the difference between voltages V_{oa} and V_{ob}, and Figures 11c and 11d respectively show current i_{D1} flowing through diode D1, i.e. the current charging capacitor Ca, and current i_{1160} flowing through switch 1160, i.e. the current charging capacitor Cb.

Specifically, also in this example there are shown three pulses for current i_{114}:

- the first pulse is transferred completely to capacitor Ca, because at the beginning of the pulse the difference between voltages V_{oa} and V_{ob} is smaller than threshold TH:

- at the beginning of the second pulse, the difference of voltages V_{oa} and V_{ob} is greater than threshold TH, and the current is transferred to capacitor Cb only;

- also the third pulse is transferred completely to capacitor Ca, because at the beginning of the pulse the difference of voltages V_{oa} and V_{ob} is smaller than threshold TH.

This embodiment offers the advantage that both the closing and the opening of switch 1160 take place at zero current. However, this embodiment has the disadvantage that the output voltages have a higher ripple, which is also visible in figure 11b.

Figure 12 shows a second embodiment of switching means 116, wherein the use of a dedicated latch or flip-flop is not required.

For example, in the presently considered embodiment, switching means 116 are implemented via diode D1, e.g. a Schottky diode, an SCR (Silicon Controlled Rectifier) Q1 and a Zener diode D2.

Specifically, the terminal providing current i_{114} is connected (e.g. directly) to the anode of diode D1, and the cathode of diode D1 is connected (e.g. directly) to a first terminal (positive terminal) of capacitor Ca associated with output 106a. On the other hand, the second terminal of capacitor Ca is connected (e.g. directly) to ground GND. The terminal which provides current i_{114} is moreover connected, via SCR Q1, to capacitor Cb associated to output 106b. Specifically, the terminal providing current i_{114} is connected (e.g. directly) to the anode of SCR Q1, and the cathode of SCR Q1 is connected (e.g. directly) to a first terminal (positive terminal) of capacitor Cb. On the other hand, the second terminal of capacitor Cb is connected (e.g. directly) to ground GND. Finally, the gate of SCR Q1 is connected via Zener diode D2 to the positive terminal of capacitor Ca, associated to output

106a. Specifically, the anode of Zener diode D2 is connected (e.g. directly) to the gate of SCR Q1, and the cathode of Zener diode D2 is connected (e.g. directly) to the cathode of diode D1.

Therefore, in this presently considered embodiment, output 106a provides a voltage V_{oa} which is greater than voltage V_{ob} provided at output 106b, and the difference between the voltages is set via the Zener voltage Vz of diode D2 (and the gate voltage of SCR Q1). As a matter of fact, when a trigger signal is applied to the gate of SCR Q1, i.e. when the difference between voltages V_{oa} and V_{ob} exceeds the Zener voltage Vz of Zener diode D2, SCR Q1 starts conducting. However, conduction is still present when the gate signal ceases, and until the direct current falls below a minimal holding value (the so-called *holding current)*. However, given that current i_{114} is discontinuous, this take place at each pulse of current i_{114}.

As a consequence, when the difference between voltages V_{oa} and V_{ob} exceeds the Zener voltage Vz, SCR Q1 is closed via Zener diode D2 and current i_{114} is transferred to capacitor Cb. Otherwise, current i_{114} is transferred to capacitor Ca.

Therefore, in the presently considered embodiment, Zener diode D2 performs the function of comparator 1162, and SCR Q1 directly implements components 1160, 1164, 1166 and 1168 of Figure 9.

In this respect, Figure 13 shows the typical diagram I-V of a SCR, as a function of current I_G at the gate of the SCR.

Specifically, when directly conducting the SCR has the typical curve of a diode, provided that current I_G reaches a sufficient value, i.e. $I_G >> 0$. On the contrary, when current I_G is smaller, i.e. $I_G > 0$, the triggering takes place anyway, but with a greater voltage V_{AK} between anode and cathode. In the most extreme of cases, with current I_G equal to zero, the triggering takes place when voltage V_{AK} between anode and cathode reaches breakdown voltage V_{BO} of the SCR. Finally, the SCR may also be triggered when the critical rate of rise (dV/dt) is exceeded. As a matter of fact, if the applied voltage rises too rapidly, the SCR may start conducting automatically (so-called spontaneous triggering).

The triggering is maintained until the current flowing through the SCR falls below a holding value I_H (*holding current*). As a consequence, there is no need for the current pulse to fall exactly to zero; on the contrary, it is sufficient for each pulse of current i_{114} to include a portion wherein the current is smaller than holding value I_H of SCR Q1.

On the basis of the features of SCR Q1, there are therefore two operating modes for circuit 116. In the former case, an initial part of a current pulse is transferred to the output having a greater voltage, e.g. output 106a, and when Zener diode D2 triggers SCR Q1, the second part of the current pulse is transferred to the output having a smaller voltage, e.g. output 106b. This operation corresponds therefore to the *split pulse mode*. On the contrary, in the latter case, SCR Q1 is activated via a spontaneous triggering. Therefore, in this case, each current pulse is transferred completely to one of the capacitors Ca or Cb. Therefore, this operation corresponds to the *full pulse mode*.

Split pulse mode

As previously explained, in this case, SCR Q1 is triggered only via the current at the gate of SCR Q1, i.e. triggering is not due to an excessive voltage V_{AK}

or an excessive voltage variation at the anode of SCR Q1.

For example, Figure 14a shows a possible profile of current i_{114}, Figure 14b shows voltage V_{D2} across Zener diode D2, and Figures 14c and 14d respectively show current i_{D1} flowing through diode D1, i.e. the current which charges capacitor Ca, and current i_{Q1} flowing through SCR Q1, i.e. the current which charges capacitor Cb.

Specifically, in the presently considered example, there are shown three pulses for current i_{114}:

- the first pulse is transferred completely to capacitor Ca, because voltage V_{D2} across Zener diode D2 is smaller than voltage V_Z of Zener diode D2;

- during the second pulse, voltage V_{D2} across Zener diode D2 reaches voltage V_Z of Zener diode D2 and SCR Q1 is triggered, and from this moment on the current is transferred to capacitor Cb;

- also the third pulse is transferred completely to capacitor Ca, because voltage V_{D2} across Zener diode D2 is still smaller than voltage V_Z of Zener diode D2.

Therefore, the waveforms substantially correspond to what is shown with reference to Figure 10.

<u>Full pulse mode</u>

On the other hand, in this mode, SCR Q1 is activated by a spontaneous triggering. The spontaneous triggering takes place when to the anode of the SCR a voltage variation is applied which exceeds the critical rate of rise of the SCR. Moreover, as shown in Figure 13, triggering is more likely to occur if current I_G at the gate of the SCR is not equal to zero, i.e. when the difference between V_{oa} and V_{ob} approaches the Zener voltage V_Z of diode D2. Therefore, from a practical point of view, for a given variation of voltage dV/dt the triggering takes place at a voltage $V_z - \Delta$.

For example, Figure 15a shows a possible profile of current i_{114}, Figure 15b shows voltage V_{D2} across Zener diode D2, and Figures 15c and 15d respectively show current i_{D1} flowing through diode D1, i.e. the current which charges capacitor Ca, and current i_{Q1} flowing through SCR Q1, i.e. the current which charges capacitor Cb.

Specifically, in the presently considered example, there are shown three pulses for current i_{114}:

- the first pulse is transferred completely to capacitor Ca because, at the beginning of the pulse, voltage V_{D2} across Zener diode D2 is smaller than voltage $V_z - \Delta$ and the voltage at Zener diode D2 does not reach Zener voltage V_z during the pulse;

- during the second pulse, voltage V_{D2} across Zener diode D2 approaches voltage V_Z of Zener diode D2, specifically it is greater than threshold $V_z - \Delta$, and as a consequence of an abrupt change of voltage at the anode of SCR Q1, SCR Q1 is triggered and the current is transferred to capacitor Cb only;

- also the third pulse is transferred completely to capacitor Ca because, at the beginning of the pulse, voltage V_{D2} across Zener diode D2 is smaller than voltage $V_z - \Delta$ and the voltage at Zener diode D2 does not reach Zener voltage V_z during the pulse.

Therefore, the waveforms substantially correspond to what is shown with reference to Figure 11.

Generally speaking, in order to reduce the ripple in the output voltages, there may also be provided at least one interlink capacitor between the outputs.

For example, Figure 16 shows an embodiment having the addition of a capacitor C3, which is connected between the positive terminal of output 106a and the positive terminal of output 106b.

Such a capacitor C3 therefore performs a capacitive coupling, and therefore each pulse is also transferred partially to the other output. Moreover, capacitor C3 enables an improvement of the output voltage.

Therefore, such an interlink capacitor C3 is particularly useful for the Full Pulse Mode.

As previously stated, on the basis of the critical rate of rise (*dV/dt*) of SCR Q1, switching circuit 116 may behave in two ways.

In this respect, Figure 17 shows a possible embodiment of SCR Q1.

Substantially, an SCR consists in a structure of "pnpn" junctions, wherein:

- the first "p" represents anode A;
- the last "n" represents cathode C, and
- the second "p" represents gate G.

Therefore, as is well known, an SCR may be implemented via two bipolar transistors: a pnp bipolar transistor Q2 and an npn bipolar transistor Q3.

Specifically, in the presently considered embodiment, the emitter of pnp transistor Q2 is connected (e.g. directly) to a terminal which represents anode A of SCR Q1. The base of pnp transistor Q2 is connected to the collector of npn transistor Q3. The collector of pnp transistor Q2 is connected to the base of npn transistor Q3, which is also connected to a terminal representing gate G of SCR Q1. Finally, the emitter of npn transistor Q3 is connected (e.g. directly) to a terminal representing cathode C of SCR Q1.

In various embodiments, the circuit may moreover comprise one or more capacitors connected to the bases of transistors Q2 and Q3, enabling the variation of the critical rate of rise *dV/dt* of SCR Q1. For example, in the presently considered embodiment, a first capacitor

C1 is connected between the emitter of transistor Q2 and the base of transistor Q2, and a second capacitor C2 is connected between the base of transistor Q3 and the emitter of transistor Q3. For example, in an embodiment, such capacitors have a capacitance of a few nF, e.g. 1 - 10 nF, e.g. 4,7 nF.

Generally speaking, the implementation may additionally include further components. For example, in the presently considered embodiment resistors R1 and R4 are provided which are respectively connected to the base of transistors Q2 and Q3. For example, in the presently considered embodiment, resistor R1 is connected between the emitter of transistor Q2 and the base of transistor Q2, and resistor R4 may be connected between the base of transistor Q3 and the emitter of transistor Q3. In the presently considered embodiment, the circuit moreover comprises a resistor R2, connected between the base of transistor Q2 and the collector of transistor Q3, and a resistor R3 connected between the collector of transistor Q2 and the base of transistor Q3.

In various embodiments, the collector of transistor Q2 is also connected to the collector of transistor Q3 via a diode D3, such as e.g. a Schottky diode. Substantially, diode D3 induces most of the current input by emitters to circulate in the collectors and not in the bases. This is due to the fact that BJTs are designed to withstand a base current smaller than the collector current, and a damage would occur without the provision of D3, because the collector currents would equal the base currents. In this way, on the contrary, the base current is limited, also by splitters R1&R2 and R3&R4, so that Vf on the diode with the addition of the diode saturation voltage keeps the arrangement triggered in any case. R2 and R3 have a low value, of around ten Ohm or less, while R1 and R4 determine the triggering current and amount to a few kOhm.

The person skilled in the art will appreciate that the number of outputs may also be increased, by providing a respective circuit 116 for each output.

For example, Figure 18 shows a possible embodiment with three outputs 106a, 106b and 106c, wherein a respective output capacitor Ca, Cb and Cc is associated to each output.

Therefore, in the presently considered embodiment, switching means 116 include a diode for the output with the highest voltage 106a, and for the remaining two outputs respectively an SCR Q1b and Q1c and a Zener diode D2b and D2c, wherein Zener voltage V_z of the respective diode substantially corresponds to the difference between the highest voltage and the desired voltage.

Specifically, in the presently considered embodiment, the terminal providing current i_{114} is connected via SCR Q1b to output capacitor Cb associated to output 106b, and the gate of SCR Q1b is connected via Zener diode D2b to the positive terminal of capacitor Ca associated to output 106a. Similarly, the terminal providing current i_{114} is connected via SCR Q1c to output capacitor Cc associated to output 106c and the gate of SCR Q1c is connected via Zener diode D2c to the positive terminal of capacitor Ca associated to output 106a.

Of course, without prejudice to the principle of the invention, the details and the embodiments may vary, even appreciably, with respect to what has been described herein by way of non-limiting example only, without departing from the extent of protection of the invention as defined by the annexed claims.

CLAIMS

1. Electronic converter (12) comprising:

- a switching stage (114) comprising at least one electronic switch (S), wherein said switching stage (114) is adapted to provide a current (i_{114}) via a terminal;

- a first capacitor (Ca), wherein said first capacitor (Ca) provides a first voltage (V_{oa}),

characterized in that said converter (12) comprises further:

- a second capacitor (Cb), wherein said second capacitor (Cb) provides a second voltage (V_{ob}),

- comparison means (1162, D2) configured to detect the difference between said first voltage (V_{oa}) and said second voltage (V_{ob}), and determine a comparison signal which indicates whether said difference is greater than a threshold (TH; V_Z; V_Z-Δ), and

- switching means (D1, 1160-1168; D1, Q1) configured to transfer selectively said current (i_{114}) to said first capacitor (Ca) or said second capacitor (Cb) as a function of said comparison signal.

2. Electronic converter (12) according to Claim 1, wherein said comparison means (1162) comprise a comparator (1162), such as a comparator with hysteresis, or a Zener diode (D2).

3. Electronic converter (12) according to Claim 1 or Claim 2, wherein said switching means (D1, 1160-1168; D1, Q1) comprise:

- a diode (D1), such as a Schottky diode, connected between said terminal which provides said current (i_{114}) and said first capacitor (Ca), and

- an electronic switch (1160; Q1) connected between said terminal which provides said current (i_{114}) and said second capacitor (Cb).

4. Electronic converter (12) according to any of the previous claims, comprising a driver circuit (112) configured to drive said switching stage (114) as a function of said voltage at said first (Ca) or said second (Cb) capacitor.

5. Electronic converter (12) according to any of the previous claims, wherein said switching stage (114) is configured to provide current pulses (i_{114}) via said terminal.

6. Electronic converter (12) according to any of the previous claims, wherein:

- said switching stage is a buck converter operated in DCM mode, or

- said switching stage is a boost or flyback converter comprising a rectification diode, and wherein said diode (D1) is implemented with said rectification diode.

7. Electronic converter (12) according to Claim 5 or Claim 6, wherein said switching means (D1, 1160-1168) comprise:

- a current sensor (1166) configured to detect a value identifying said current (i_{114});

- a detection circuit (1168) configured to determine a signal which indicates whether said detected current (i_{114}) is equal to zero;

wherein said switching means (D1, 1160-1168) are configured to transfer selectively said current (i_{114}) to said first capacitor (Ca) or said second capacitor (Cb) as a function of said signal which indicates whether said detected current (i_{114}) is equal to zero.

8. Electronic converter (12) according to Claim 7, wherein said switching means (D1, 1160-1168; D1, Q1) comprise a latch (1164), such that:

a) in case said comparison signal indicates that said difference is smaller than said threshold (TH; V_Z; $V_Z-\Delta$), a current pulse (i_{114}) is transferred completely to said first capacitor (Ca); and

b) in case said comparison signal indicates that said difference is greater than said threshold (TH; V_Z; V_Z-Δ), a current pulse (i_{114}) is transferred completely to said second capacitor (Cb).

9. Electronic converter (12) according to Claim 5 or Claim 6, wherein said switching means (D1, Q1) comprise:

- a SCR (Q1), wherein the anode of said SCR (Q1) is connected to said terminal which provides current pulses (i_{114}), and wherein the cathode of said SCR (Q1) is connected to said second capacitor (Cb).

10. Electronic converter (12) according to Claim 9, wherein said switching means (D1, Q1) comprise:

- a Zener diode (D2), wherein the cathode of said Zener diode (D2) is connected to said first capacitor (Ca) and the anode of said Zener diode (D2) is connected to the gate of said SCR (Q1).

11. Electronic converter (12) according to Claim 9 or Claim 10, wherein said SCR (Q1) has a low critical rate of rise, such that each current pulse (i_{114}) is transferred completely to said first capacitor (Ca) or to said second capacitor (Cb).

12. Electronic converter (12) according to any of Claims 9 to 11, wherein said SCR (Q1) is implemented by means of a pnp bipolar transistor (Q2) and a npn bipolar transistor (Q3), wherein said pnp bipolar transistor (Q2) and/or said npn bipolar transistor (Q3) have associated un respective capacitor (C1, C2) for varying said critical rate of rise.

13. Method for operating an electronic converter (12) according to any of the previous claims, comprising the steps of:

- detecting the difference between said first voltage (V_{oa}) and said second voltage (V_{ob}),

- determining a comparison signal which indicated whether said difference is greater than a threshold (TH; V_Z; V_Z-Δ), and
- transferring selectively said current (i_{114}) to said first capacitor (Ca) or said second capacitor (Cb) as a function of said comparison signal.

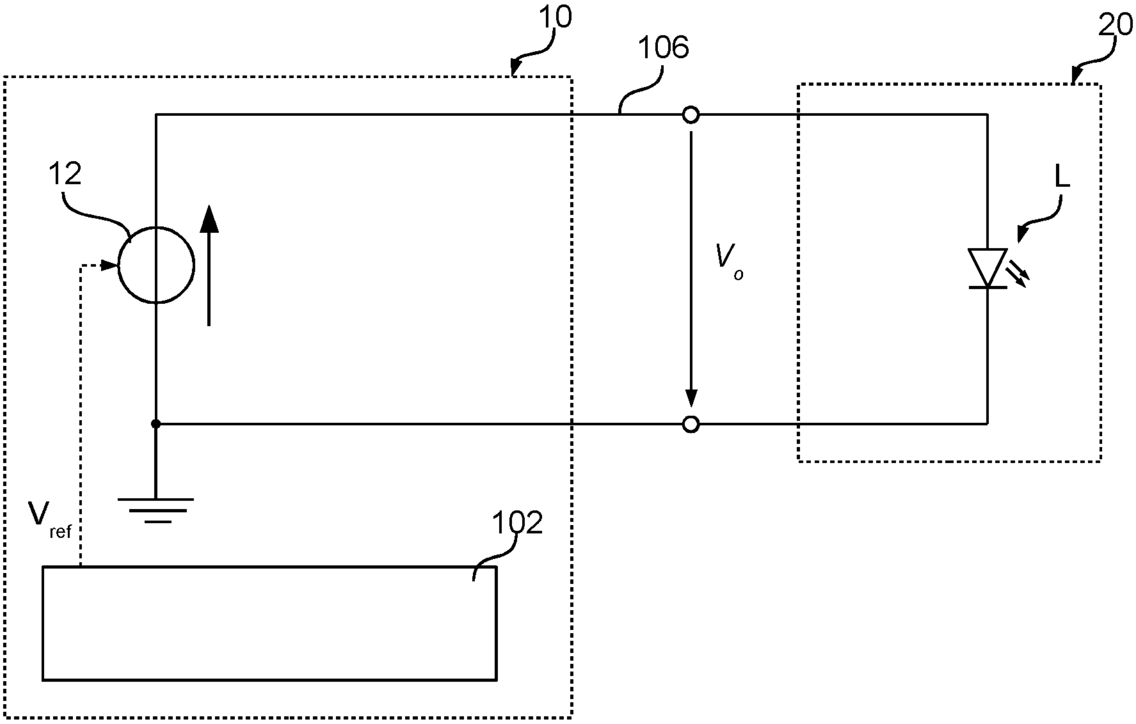


Fig. 1

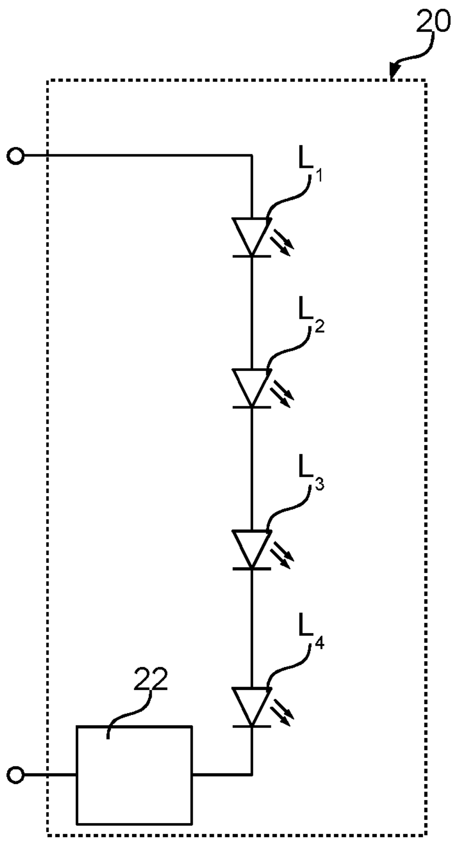


Fig. 2

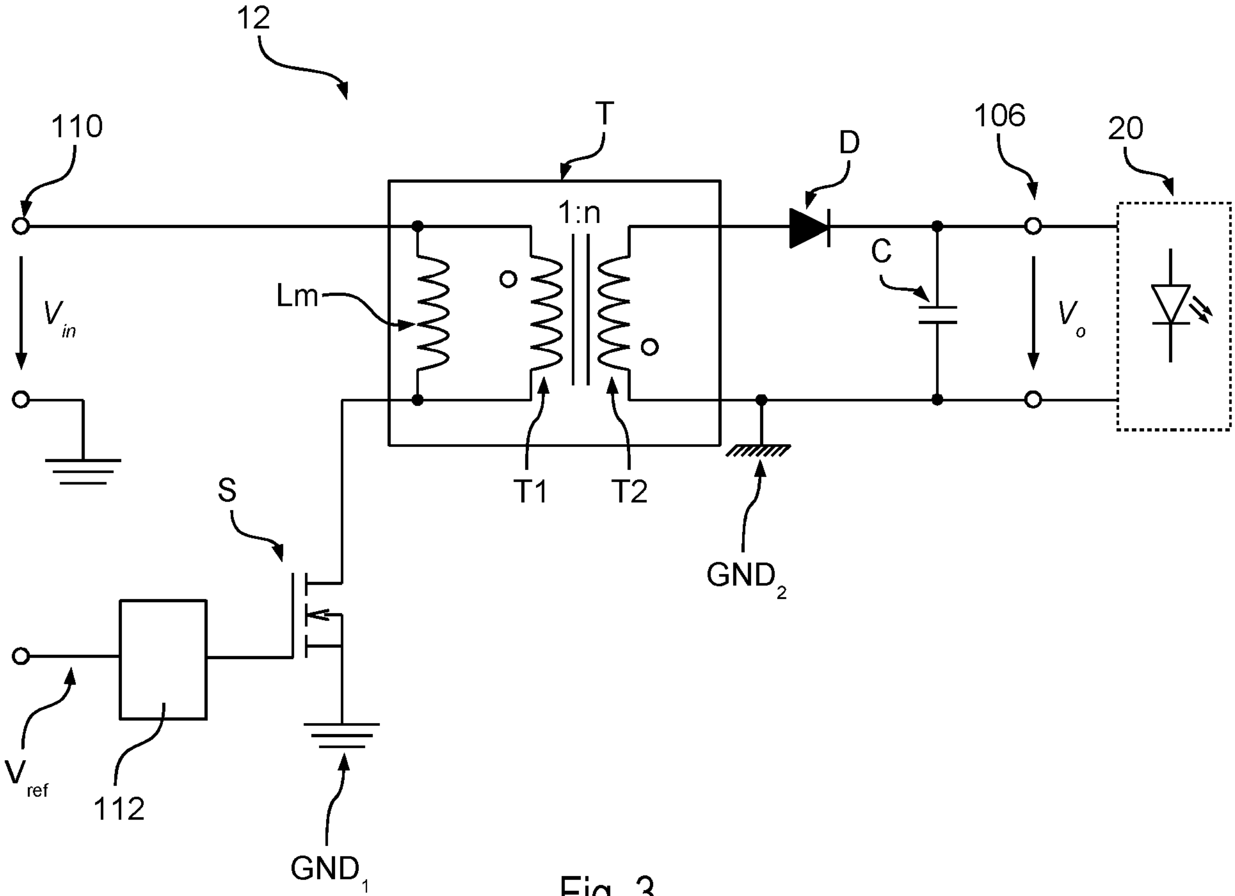

12
110
T
1:n
D
106
20
C
Lm
V_{in}
V_o
T1
T2
S
GND2
V_{ref}
112
GND1

Fig. 3

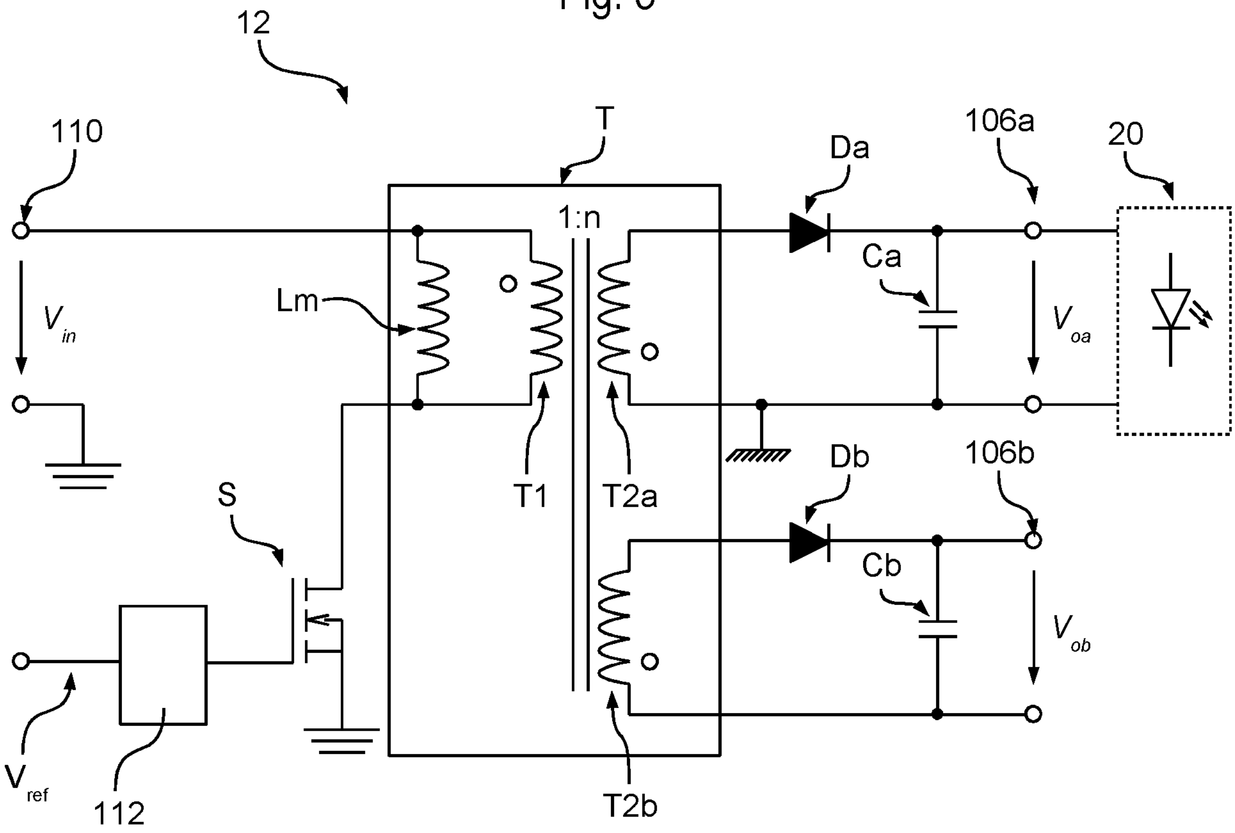

12
110
T
1:n
Da
106a
20
Ca
Lm
V_{in}
V_{oa}
T1
T2a
S
Db
106b
Cb
V_{ob}
V_{ref}
112
T2b

Fig. 4

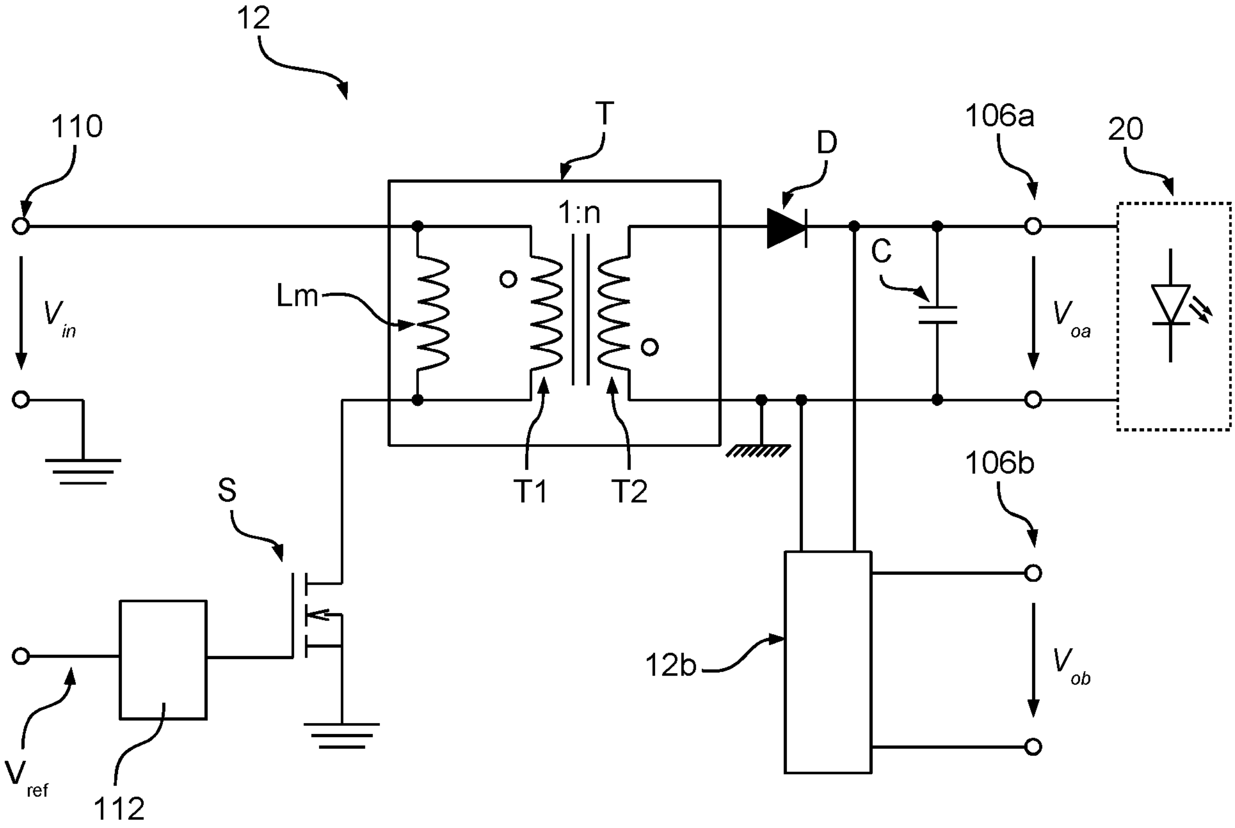
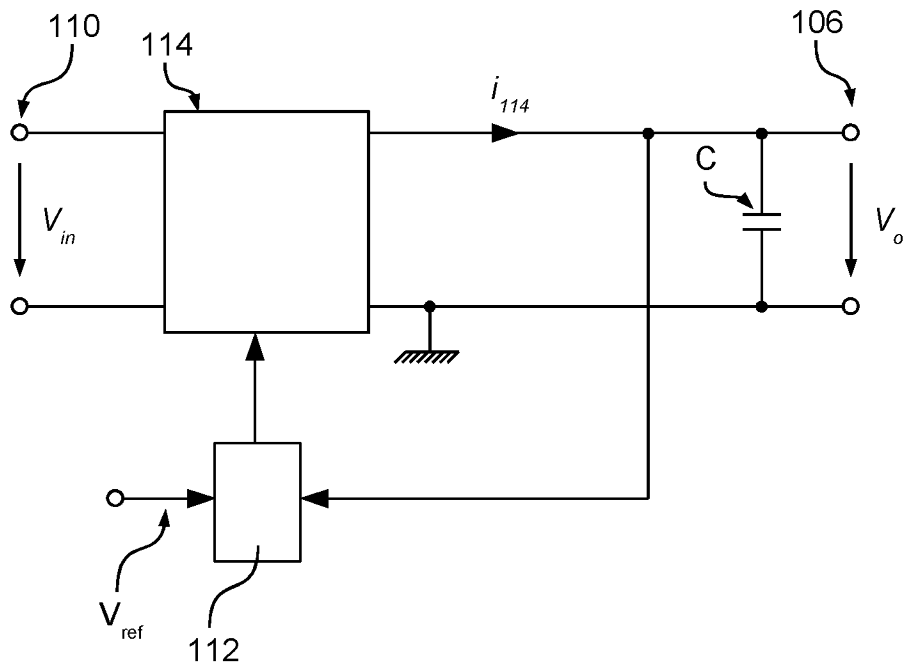

12
110
T
1:n
D
106a
20
C
Lm
V_{in}
V_{oa}
T1
T2
S
106b
12b
V_{ob}
V_{ref}
112

Fig. 5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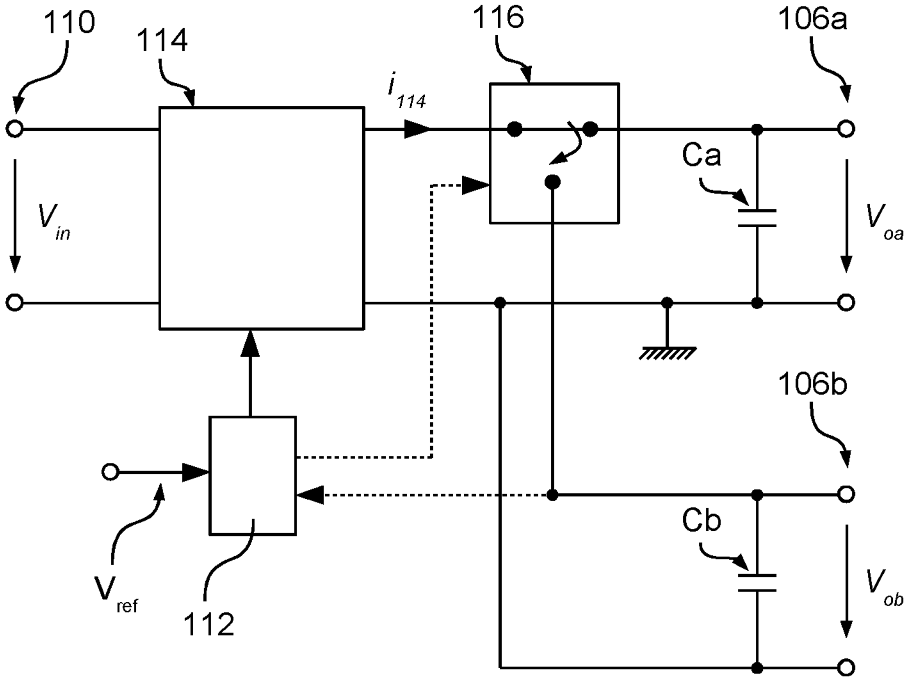
114
i_{114}
106
C
V_{in}
V_o
V_{ref}
112

Fig. 6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116
106a
i_{114}
Ca
V_{in}
V_{oa}
106b
Cb
V_{ob}
V_{ref}
112

Fig. 7

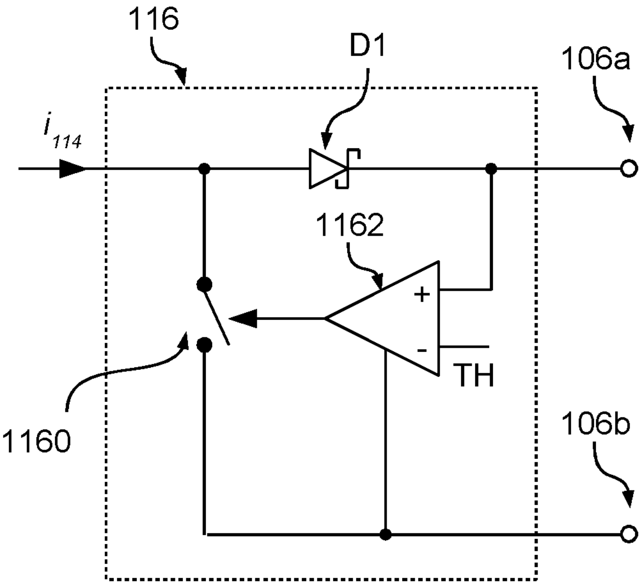
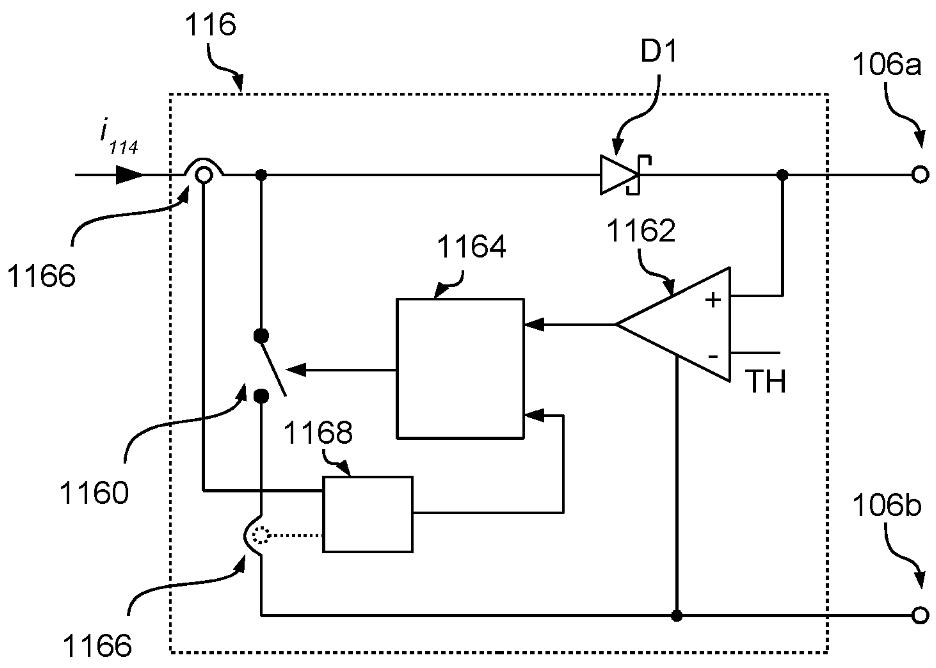
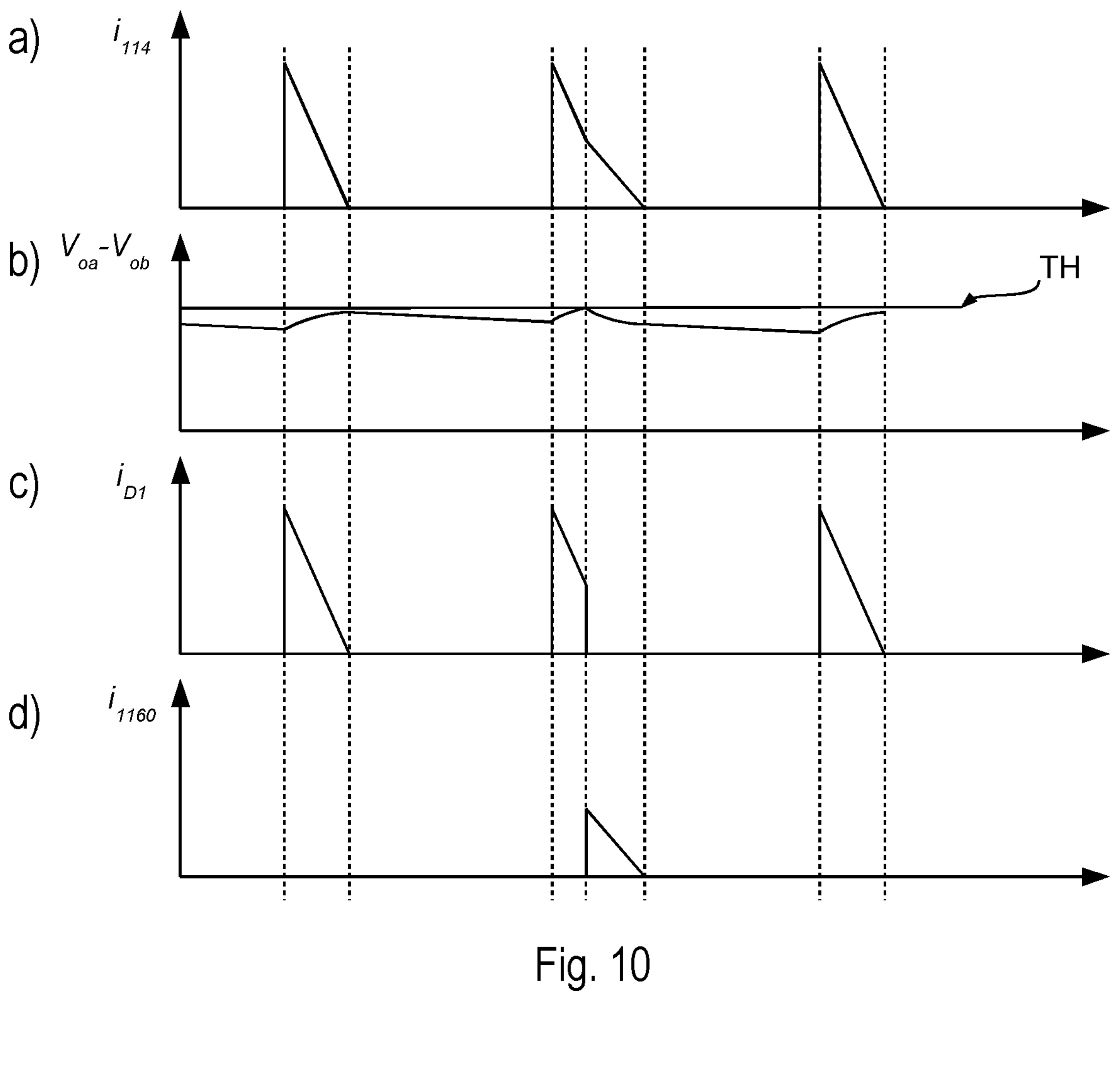

116
D1
106a
i_{114}
1162
+
-
TH
1160
106b

Fig. 8



116
D1
106a
i_{114}
1166
1164
1162
+
-
TH
1160
1168
106b
1166

Fig. 9



a)
i_{114}
b)
$V_{oa}-V_{ob}$
TH
c)
i_{D1}
d)
i_{1160}

Fig. 10

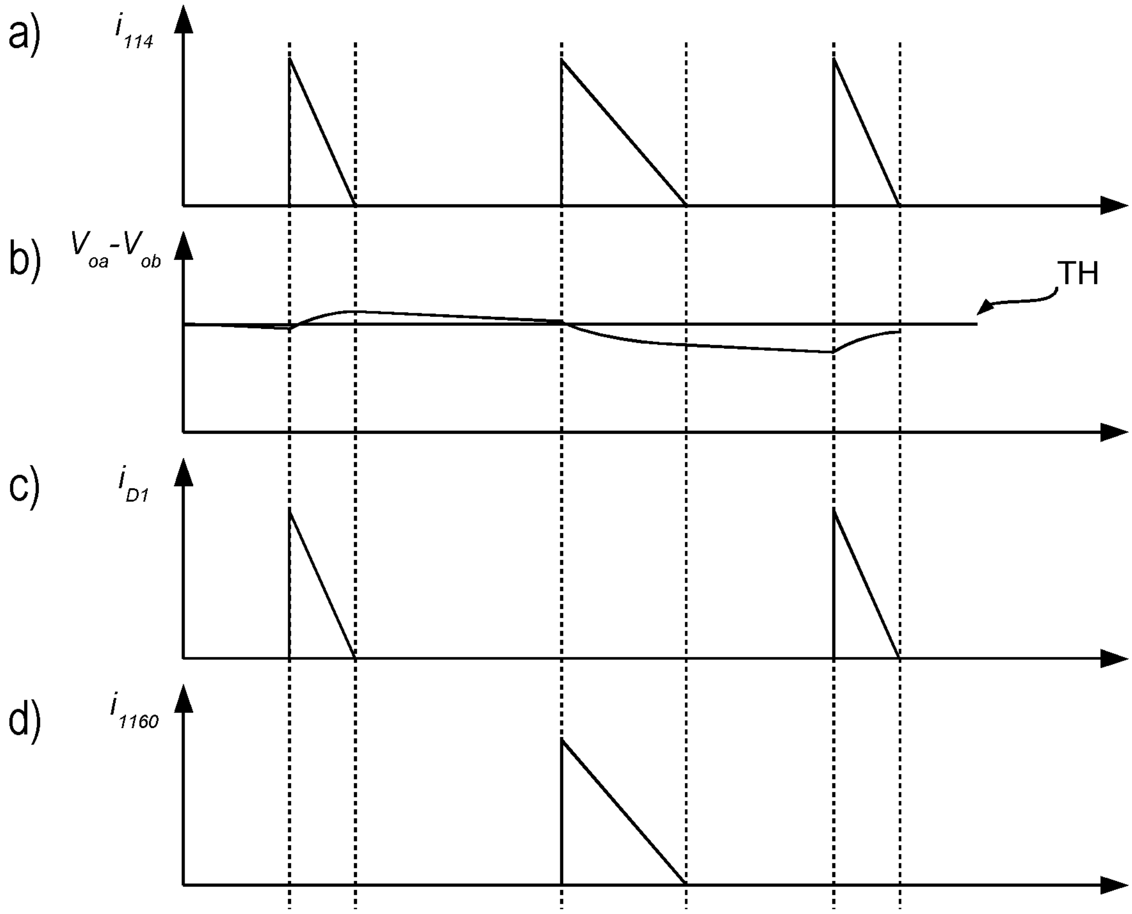

a)
i_{114}
b)
V_{oa}-V_{ob}
TH
c)
i_{D1}
d)
i_{1160}

Fig. 11

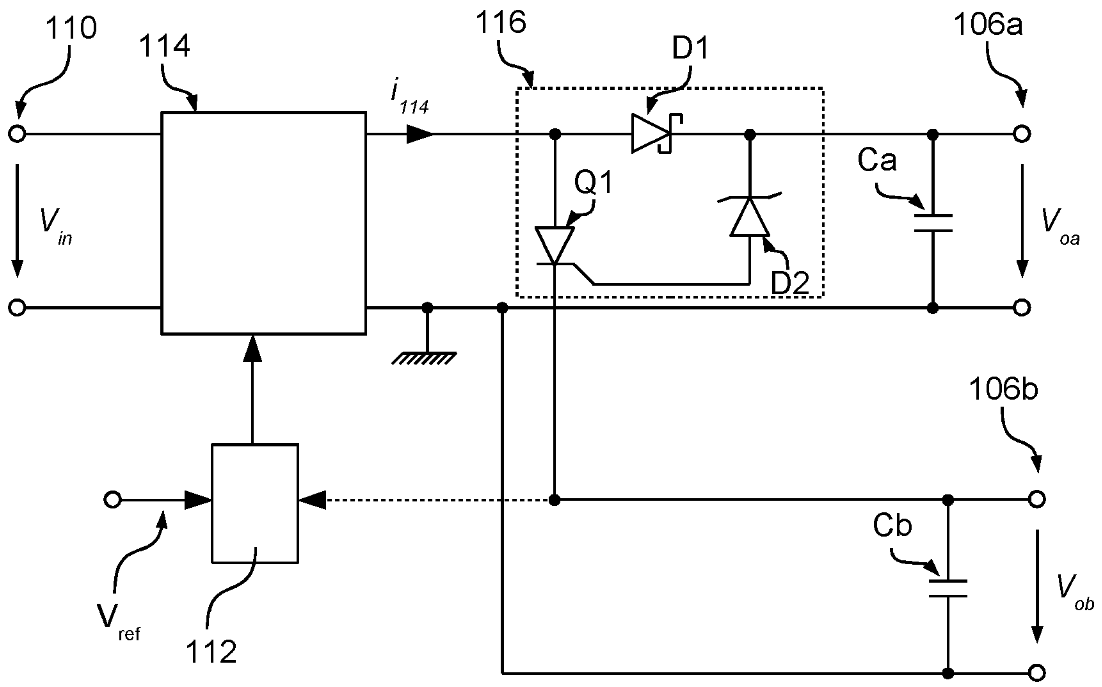

110
114
116
D1
106a
i_{114}
V_{in}
Q1
Ca
V_{oa}
D2
106b
Cb
V_{ob}
V_{ref}
112

Fig. 12

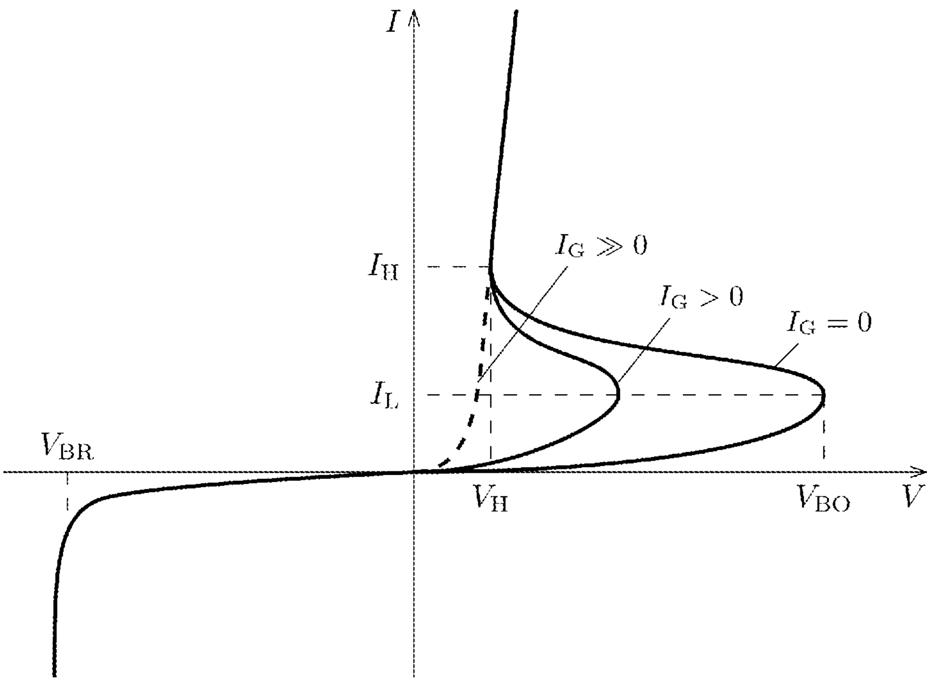


Fig. 13

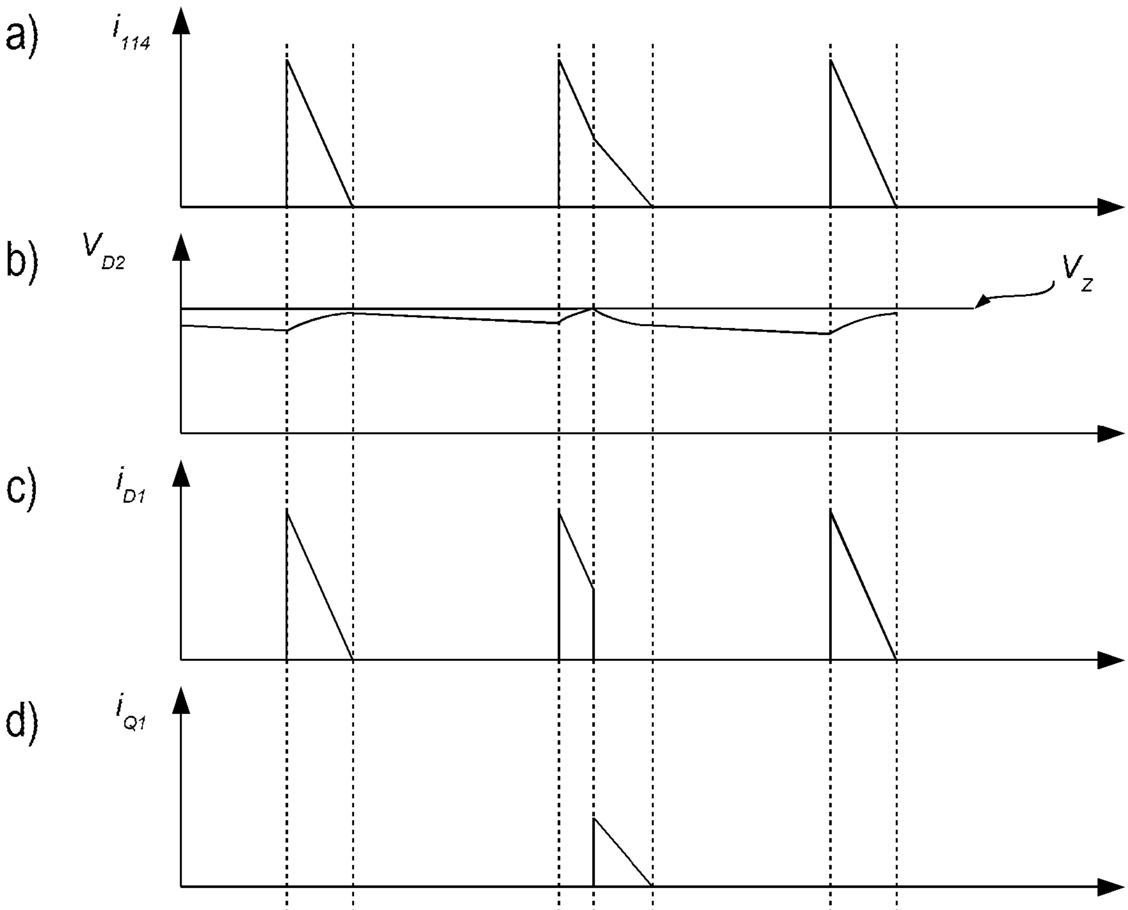


Fig. 14

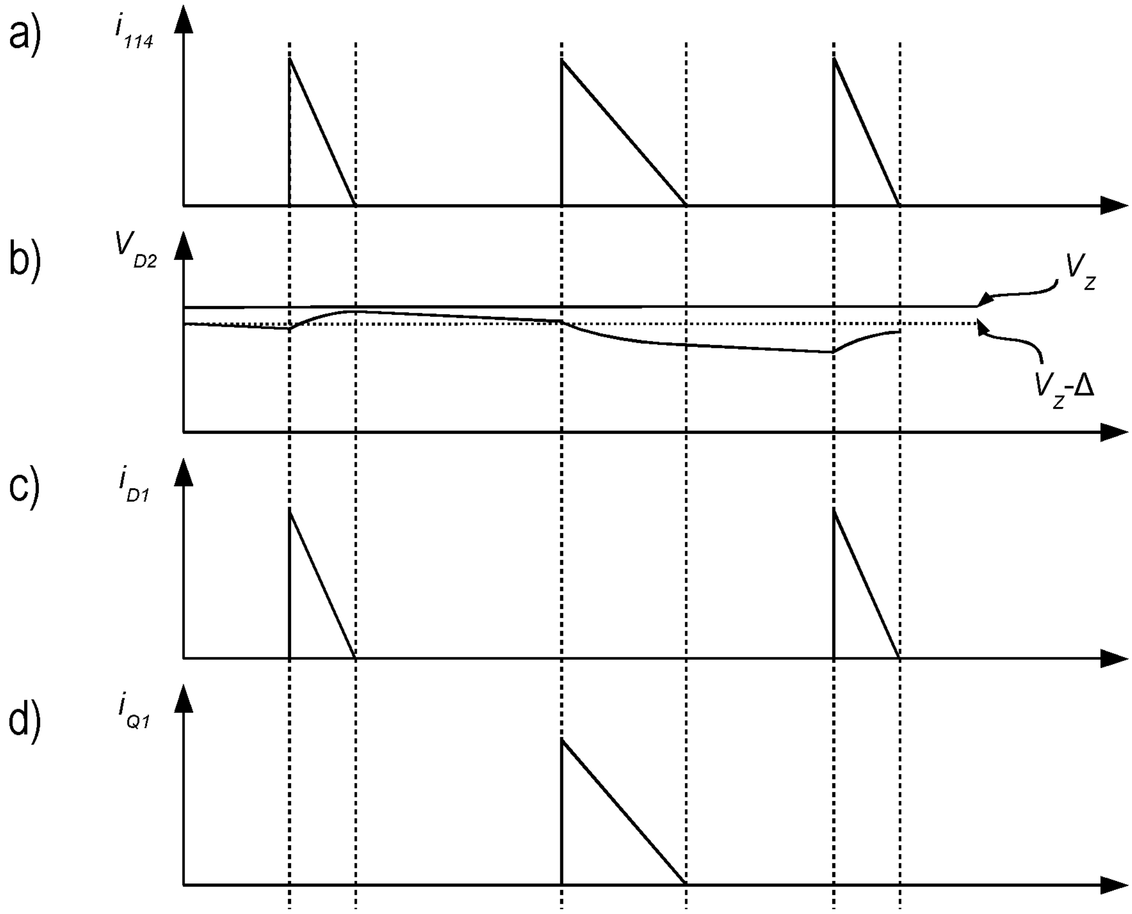

a)
i_{114}
b)
V_{D2}
V_Z
V_Z-Δ
c)
i_{D1}
d)
i_{Q1}

Fig. 15

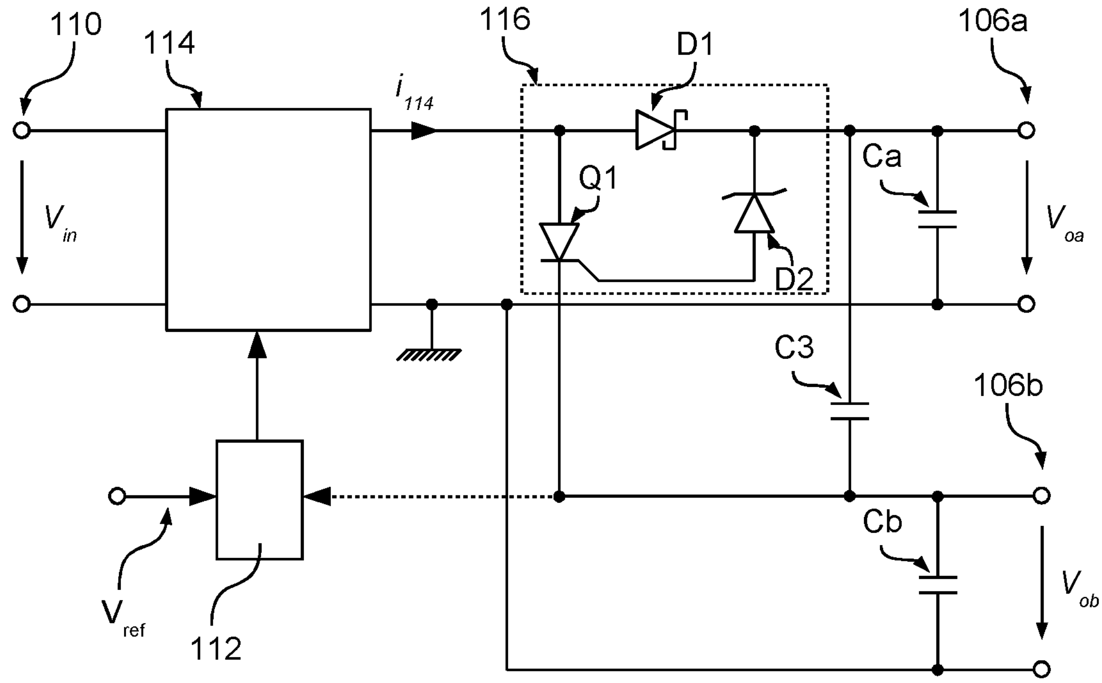

110
114
116
D1
106a
i_{114}
Q1
Ca
V_{in}
V_{oa}
D2
C3
106b
Cb
V_{ob}
V_{ref}
112

Fig. 16

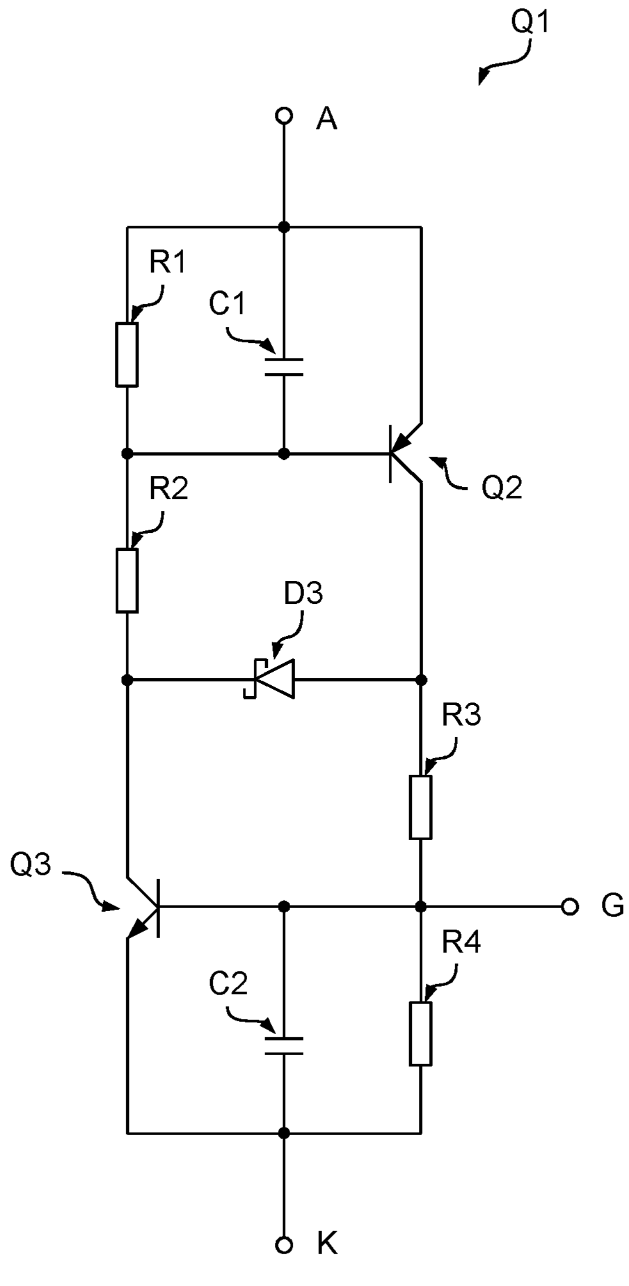
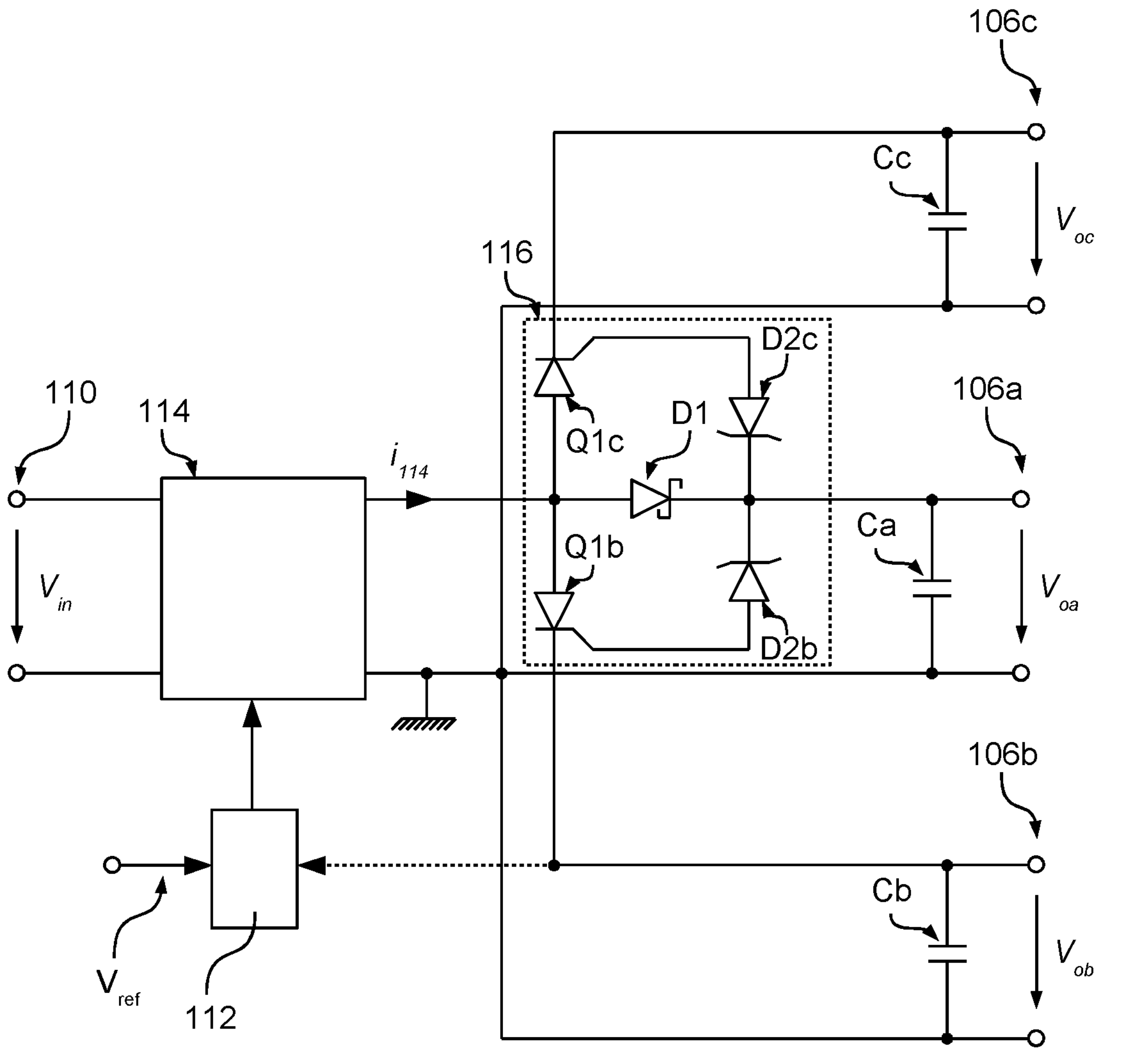


Fig. 17



106c
Cc
V_{oc}
116
D2c
110
114
D1
106a
Q1c
i_{114}
Ca
Q1b
V_{in}
V_{oa}
D2b
106b
Cb
V_{ob}
V_{ref}
112

Fig. 18

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2016/055537

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M3/335 H05B33/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2009/020985 A1 (ADVANCED ANALOGIC TECH INC [US]; WILLIAMS RICHARD K [US]) 12 February 2009 (2009-02-12) page 6; figures 2,3a,3b,3c page 11 - page 13 -----	1-13
X	EP 0 698 959 A1 (SIEMENS AG OESTERREICH [AT]) 28 February 1996 (1996-02-28) column 5, line 20 - line 47; figure 1 sentence 11, paragraph 4 -----	1-13

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 November 2016	17/11/2016

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Taccoen, J

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2016/055537

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