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(54) **Video memory interface circuit.**

(57) A video display circuit (10) receives and stores character code data provided by a processor (12) and supplies character pixel data in the form of a video signal to a video display device (14). The circuit (10) includes a controller chip (16) and four memory chips (18-22), including a character memory chip (18) that stores the character code data received from the processor (12), and a font memory chip (22) that stores the character pixel data, or bit-maps, of each character of the character set. The data output pins (D) of the character memory chip (18) are connected to several of the address pins (A) of the font memory chip (22) to directly select within the font memory chip (22) a block of memory cells containing a character bit-map corresponding to character code data output by the character memory chip (18). Other address pins of the font memory chip (22) are connected to the controller chip (16) and select a row of memory cells within the block of memory cells. The data output pins (D) of the character memory chip (18) are also connected to the controller chip (16) for use in a pure graphics mode in which a portion of a full screen of graphics data is stored in the character memory chip (18).

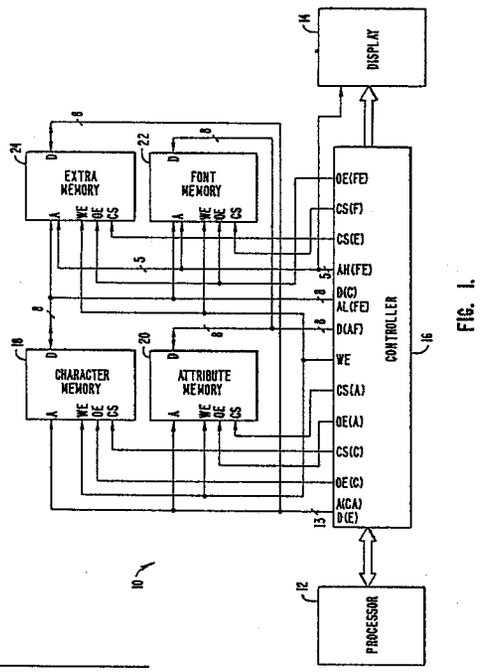


FIG. 1.

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Description

VIDEO MEMORY INTERFACE CIRCUIT

Background of the Invention

Field of the Invention

This invention relates generally to video display circuits, and relates more particularly to a video controller chip and interconnections among the video controller chip and video memory chips.

Description of the Relevant Art

A video display circuit functions as an interface between a processor, which generates data to be displayed, and a video display device, which provides means for visually displaying such data. The video display circuit typically includes two functionally distinct circuits, a video controller and a video memory. The video controller receives data to be displayed from the processor, stores that data in the video memory, and, upon demand, generates a corresponding video signal using data from the video memory to drive the video display device. Changes in the visual display are accomplished by changing the data stored in the video memory.

The video display device such as a cathode ray tube (CRT) or liquid crystal display can be considered as comprising a rectangular array of picture elements, known as pixels, that visually represent the data to be displayed. Each pixel is turned on or turned off according to the video signal. If the pixels are displayed in color, the video signal turns on and off the color components of each pixel. In a raster scan type of video display device, the video signal defines horizontal raster lines (rows of pixels) in a scanning sequence that repetitively covers the display area of the video display device.

Data to be displayed often contains either or both alphanumeric text and graphics display data. Alphanumeric text is typically represented within a computer in two forms: coded and bit-mapped. Associated with each character in the character set is a code and a two-dimensional bit-map. The coded form is used in the processing and memory portions of the computer because the coded form requires far less storage space than does the bit-mapped form. One popular coded form currently in use is ASCII (American Standard Code for Information Interchange), which assigns a seven or eight bit code to each character of the character set.

Within the video display, characters are represented in their bit-mapped form as character pixel data, which defines the on/off states of the pixels that visually represent the characters. The character pixel representation is a two-dimensional bit pattern or map that defines the visual display of the character. The pixel data associated with each character in the character set is stored in a font memory portion of the video memory. The font memory contains character pixel representations for all of the different characters that can be displayed. If the font memory is sufficiently large, alternative pixel representations of the characters can be stored in the font memory to provide a choice of font styles.

Some video display circuits are capable of displaying characters in various optional formats such as underlined, blinking, or inverse video. In such display circuits, attribute codes of the characters to be displayed are stored in an attribute memory portion of the video memory. The attribute codes specify which of the special display options is to be invoked.

To display alphanumeric text, the video controller section of the video display circuit generates a video signal that defines the on/off states of the pixels of the video display device. The video signal contains data that defines the pixels of the character display row by row, with several adjacent rows of pixels defining each row of characters.

To generate the video signal, the video display circuit converts the coded form of each character into its corresponding pixel representation. For each character, the video controller addresses a character memory to read a stored character code, and then uses the character code to address the font memory to read one row of the corresponding character pixel representation. The data read from the font memory defines the video signal. If, for example, the size of each character pixel representation is seven pixels wide by nine pixels high, then each entry into the font memory will yield seven bits of display data that define the states of seven pixels. The video controller repeats this process for each character in the row. When the end of the character row is reached, the video controller returns to the first character in the row and repeats the above process to generate the video signal for the next adjacent row of pixels. In the above example, the video controller will address the font memory nine times for each character because nine rows of pixels are needed to display each row of characters. After a video signal for a complete row of characters has been generated, the video signal for the next row of characters is generated in the same fashion.

If display attributes are used, then the video signal may need to be modified in order to display the characters according to the selected display options. In this case, the video controller must read the character attribute data by addressing the attribute memory each time the character memory is addressed and then transform the character pixel data into the form dictated by the attribute data.

In contrast to the encoded form of character data, graphics display data is usually represented within the processor and the video memory in a pixel or bit-mapped form, wherein the memory cells of the video memory correspond one-to-one with the pixels of the video display device. The processor periodically updates the pixel data stored in the video memory in order to incorporate new graphics display data. To display graphics data, the video controller simply reads the video memory cell by cell. Commonly, several bits of the graphics display data are read in parallel from the video memory into a

high-speed shift register, which shifts the bits out serially to the video display device.

Recent trends in computer design have increased the performance demands on video display circuits. Video display devices with increased pixel resolution and color display capability are increasingly in demand. Such demand increases both the size of the video memory and the data processing bandwidth of the video controller. Another demand is that computers have the capability to display both alphanumeric and graphics data. This complicates the design of the video controller and video memory. Another trend throughout the electronics industry is one of reducing the number of integrated circuit chips necessary to perform a given function in order to reduce cost and size. The overall effect of these trends is to push designers of video display circuits to utilize single chip video controllers coupled to fast access memories in order to fulfill the performance and cost requirements.

The design of a single chip video controller involves much more than simply combining the functions of a multichip video controller into a single chip. Because the cost of a chip is directly related to the number of input/output pins, the chip designer must carefully consider the interconnections between the video controller chip and the processor, the video memory, and the video display device. Assuming that the video memory will consist of more than one chip, the number of pins of the video controller chip needed to interface to the video memory, as well as the performance of the video display circuit, will depend on whether the video memory chips are connected directly or through a bus. In a direct connection, separate address and data pins are allotted for each video memory chip, while in a bus connection, one set of address and data pins are shared among all video memory chips. In a direct memory connection, all of the memory chips can be accessed simultaneously, while in a bus connection, only a single selected memory chip can be accessed at any one time, due to the shared address and data connections. A direct connection allows fast access to all of the video memory chips, but requires dedicated address and data inpuy/output pins for each video memory chip, which significantly increases cost. A bus connection minimzes the number of pins and their associated cost, but degrades the circuit performance because such a connection increases the effective access time to the video memory.

Even if the video memory chips are connected directly, prior art video controllers require two full memory cycles to access each row of the character pixel representation of each alphanumeric character. In the first memory cycle, a memory location in a character memory is accessed and a character code stored at that location is read into a register or a latch by the video controller. In the second memory cycle, the font memory is addressed in part by the character code data read from the character memory, which locates the character pixel representation corresponding to the character, and in part by a row address generated by the video controller, which locates the proper row within the character pixel representation. If a bus connected attribute memory is used, then a third memory cycle would be necessary in order to read the attribute data.

One design approach is to use fast access memory devices to improve the performance by reducing memory access time. Since two or three memory cycles are required, faster memory chips will significantly speed up the performance of the video display circuit. The disadvantage of this approach is the extra cost of such memories.

In addition to alphanumeric display data, the video controller chip designer often must ensure that the controller chip can also handle graphics display data. In this regard, the interconnections between the video controller chip and video memory chips must allow for the efficient transfer of both alphanumeric and graphics display data.

Summary of the Invention

In accordance with the illustrated preferred embodiment, the present invention provides a video display circuit and method for receiving and storing character code data provided by a processor and for supplying character pixel data in the form of a video signal to a video display device. The circuit includes a controller chip for receiving the character code data from the processor and for supplying the character pixel data to the video display device, and also includes memory chips that are coupled to the controller chip. The memory chips include a character memory chip that stores the character code data received from the processor, and a font memory chip that stores the character pixel data, or bit-maps, of each character of the character set. The data output pins of the character memory chip are connected to several of the address pins of the font memory chip as well as to the controller chip. These address pins of the font memory chip are denoted character font address pins, which select within the font memory chip a block of memory cells containing the bit-map of a character when the corresponding character code is supplied to the character font address pins. Other address pins of the font memory chip are denoted row address pins, which are connected to the controller chip and which select a row of memory cells within the selected block of memory cells. The character pixel data stored in the selected font memory chip memory locations is accessed and used to compose the video signal.

The method includes the steps of receiving the character code data from the processor and storing it in the character memory chip, and supplying character pixel data to the video display device from the font memory chip. The step of supplying character pixel data further includes the steps of addressing a memory location in the character memory chip by the controller chip, then supplying the character code data stored at that memory location directly to the character font address pins of the font memory chip by the character memory chip and supplying a row address to the row address pins of the font memory chip by the controller chip, and then supplying to the controller chip the character pixel data stored at the addressed row of the font memory chip.

In a more particularized embodiment, the video display circuit of the present invention further includes an attribute memory chip in which is stored attribute data that specifies certain attributes of the character code data stored in the character memory chip. The address pins of both the character memory chip and the attribute memory chip are connected in common to the controller chip so that both memory chips are addressed simultaneously. The data pins of the attribute memory chip and the data pins of the font memory chip are connected in common to the controller chip to reduce the number of pins of the controller chip.

In another embodiment, a fourth memory chip is coupled to the controller to provide extra memory for storing graphics display data. The address pins of this extra memory chip are connected to the controller chip in common with the address pins of the font memory chip, so that both memory chips are addressed simultaneously. The data pins of the extra memory chip are connected to the controller chip in common with some of the address pins of the character and attribute memory chips in order to reduce the number of pins of the controller chip.

One key feature of the present invention is that the number of input/output pins of the controller chip is reduced due to the overlapping functions served by the address and data pins of the controller chip. Such minimization is important to the development of an economical single chip video controller.

Another key feature is that the font memory chip is directly addressed by the data output signals of the character memory chip. Since the controller chip need not read and store the character code data from the character memory chip prior to addressing the font memory chip, the access time for the character pixel data is reduced from two full memory cycles to somewhere between one and two memory cycles. Such a reduction in the font memory access time allows either increased pixel data rates from a particular type of memory chip or the use of slower and lower cost memory chips while providing the same overall pixel data rate.

Still another key feature is that the video display circuit can operate in both character and graphics modes. In graphics mode, the four memory chips are utilized as a bit-mapped graphics memory. The interconnection between the memory chips and the controller chip provides direct access to the character and attribute memory chips and direct access to the font and extra memory chips.

The features and advantages described in the specification are not all inclusive, and particularly, many additional features and advantages will be apparent to one of ordinary skill in the art in view of the drawings, specification and claims hereof. Moreover, it should be noted that the language used in the specification has been principally selected for readability and instructional purposes, and may not have been selected to delineate or circumscribe the inventive subject matter. For example, although the term "memory chip" is used and illustrated as a single integrated circuit, such use and illustration is not intended to limit the definition of that term to only single integrated circuits or chips. Accordingly, resort to the claims is necessary to determine such inventive subject matter.

Brief Description of the Drawings

Figure 1 is a block diagram illustrating the interconnections of a video display circuit according to the present invention.

Figure 2 is a schematic and block diagram of a controller chip of the video display circuit of Figure 1.

Figure 3 is a diagram of certain memory locations of memory chips of the video display circuit of Figure 1.

Figure 4 is a diagram of a portion of a video display device that is coupled to the video display circuit of Figure 1.

Detailed Description of the Preferred Embodiment

Figures 1 through 4 of the drawings depict various preferred embodiments of the present invention for purposes of illustration only. One skilled in the art will readily recognize from the following discussion that alternative embodiments of the structures and methods illustrated herein may be employed without departing from the principles of the invention described herein.

As illustrated in Figure 1, the preferred embodiment of the present invention is a video display circuit 10 that is operable for receiving and storing character and graphics display data provided by a processor 12 and for supplying character pixel data in the form of a video signal to a video display device 14. The video display circuit 10 includes a controller chip 16 and four memory chips: a character memory chip 18, an attribute memory chip 20, a font memory chip 22, and an extra memory chip 24. The interconnections between the memory chips 18-24 and the controller chip 16 will first be described with reference to Figure 1, followed by a description of the controller chip with reference to Figure 2, and thereafter followed by an explanation of the operation of the video display circuit.

Each of the four memory chips 18-24 is connected to the controller chip 16 via address pins (A), data pins (D), a write enable pin (WE), an output enable pin (OE), and a chip select pin (CS). The address pins of both the character memory chip 18 and the attribute memory chip 20 are connected in common to the controller chip 16 at pins labeled A(CA), (which signifies the address pins for the character and attribute memory chips). The data pins of the character memory chip 18 are connected to the controller chip 16 at D(C), while the data pins of the attribute memory chip 20 are connected to the controller chip at D(AF) (which also connects to the font memory chip 22). Figure 1 indicates the number of signal lines in the address and data connections for memory chips having an 8K x 8 bit configuration, which requires thirteen address lines and eight data lines. Of course, other memory configurations could be substituted. The write enable pins of the character and attribute memory chips are connected in common to the controller chip at WE. The output enable pins of the character and attribute memory chips are individually connected to the controller

chip at OE(C) and OE(A), respectively, while the chip select pins of the character and attribute memory chips are individually connected to the controller chip at CS(C) and CS(A), respectively. The character memory chip 18 and the attribute memory chip 20 are, thus, connected to the controller chip 16 through separate data and control lines and common address lines.

The font memory chip 22 and the extra memory chip 24 are also connected to the controller chip through separate data and control lines and common address lines. Several of the address pins of both the font memory chip 22 and the extra memory chip 24 are connected in common to the data pins of the character memory chip 18 and to the controller chip at AL(FE), (which signifies the low address pins for the font and extra memory chips, and which are the same pins as D(C)). These are the "character font" address pins, which will be discussed in greater detail below. The remaining address pins of the font memory chip 22 and the extra memory chip 24 are connected in common to the controller chip 16 at pins labeled AH(FE) (which signifies the highaddress pins for the font and extra memory chips). These are the "row" address pins, which will also be discussed in greater detail below. The data pins of the font memory chip 22 are connected in common with the data pins of the attribute memory chip 20 to the controller chip 16 at D(AF). The data pins of the extra memory chip 24 are connected in common with some of the address pins of the character and attribute memory chips to the controller chip 16 at D(E) which also serve as some of the A(CA) pins. The write enable pins of the font and extra memory chips are connected in common to the controller chip at WE. The output enable pins of the font and extra memory chips are connected in common to the controller chip at OE(FE) while the chip select pins of the font and extra memory chips are individually connected to the controller chip at CS(F) and CS(E), respectively.

In the illustrated embodiment, which uses 8K x 8 bit memory chips, the interconnections between the controller chip 16 and the memory chips 18-24 are accomplished using forty-two pins of the controller chip: thirteen for the address pins of the character and attribute memory chips and the data pins of the extra memory chip, eight for the data pins of the attribute and font memory chips, eight for the data pins of the character memory chip and the low address pins of the font and extra memory chips, five for the high address pins of the font and extra memory chips, four for the chip select pins, three for the output enable pins, and one for the write enable pin. Additional pins (not shown) of the controller chip 16 are used for interconnections with the processor 12 and the video display device 14.

The circuitry of the controller chip 16 is illustrated schematically in Figure 2. The controller chip 16 serves two basic functions: (1) to provide access by the processor 12 to the memory chips 18-24 for the storage and retrieval of both character and graphics display data, and (2) to generate a video signal that drives the video display device 14 according to the display data stored in the memory chips. The controller chip includes four multiplexers 26, 28, 30 and 32 that selectively connect the processor 12 through a processor interface circuit 34 to the memory chips 18-24. The controller chip also includes a memory address control circuit 36 that defines memory addresses during the generation of the video signal, and a display interface circuit 38 that generates the video signal by converting parallel data bits from the memory chips into a serial stream of data bits in a format compatible with the video display device 14. A memory interface control circuit 40 coordinates the access to the memory chips 18-24 by controlling several latches 42-54, buffers 56-60, and multiplexers 26-32, and by generating the write enable, output enable, and chip select signals.

More specifically, addresses are sent from either the memory address control circuit 36 or the processor interface circuit 34 to the character and attribute memory chips 18 and 20 through multiplexer 30, latch 52, buffer 60, and pins A(CA). Data is sent from the processor interface circuit 34 to the extra memory chip 24 also through multiplexer 30, latch 52, buffer 60, and pins D(E). Data is sent from the processor interface circuit 34 to either the attribute memory chip 20 or the font memory chip 22 through latch 48, buffer 58, and pins D(AF). When necessary, the eight bit low addresses of the font and extra memory chips 22 and 24 may be sent from either the processor interface circuit 34 or the memory address control circuit 36 to the font and extra memory chips through multiplexer 28, latch 44, buffer 56, and pins AL(FE). Data is sent from the processor interface circuit 34 to the character memory chip 18 also through multiplexer 28, latch 44, buffer 56, and pins D(C). The five bit high addresses of the font and extra memory chips 22 and 24 are sent from either the processor interface circuit 34 or the memory address control circuit 36 to the font and extra memory chips through multiplexer 26, latch 42, a buffer 62 and pins AH(FE). Five lines of the video signal may be sent to the video display device 14 through multiplexer 26, latch 42, and buffer 62 via pins AH(FE) of the controller chip (shown in Figure 1) as an alternative route between the display interface circuit 38 and the video display device 14.

Data can also be received by the controller chip 16 from the memory chips 18-24. Data from the character memory chip 18 is received by the controller chip 16 through pins D(C), a buffer 64, and latch 46. Data from the attribute memory chip 20 and the font memory chip 22 is received by the controller chip through pins D(AF), a buffer 66, and latch 50. Data from the extra memory chip 24 is received by the controller chip through pins D(E), a buffer 68, and latch 54. The output pins of the latches 46, 50, and 54 are coupled to the display interface circuit 38 for supplying data thereto for the generation of the video signal, and are coupled to the multiplexer 32 for selectable transmission of data to the processor 12 via the processor interface circuit 34.

The video display circuit 10 operates in two modes: character mode and graphics mode. As one step in character mode operation, character codes and attributes of each character to be displayed are provided to the controller chip 16 by the processor

12 and are stored in the character and attribute memory chips 18 and 20, respectively. To transfer character code data from the processor 12 to the character memory chip 18, the memory interface control circuit 40 activates the write enable signal (WE) and the character memory chip select signal (CS(C)), activates buffers 56 and 60, directs multiplexer 30 to select the address lines from the processor interface circuit 34 for connection to latch 52, and directs multiplexer 28 to select the data-in line from the processor interface circuit for connection to latch 44. To transfer attribute data from the processor to the attribute chip 20, the memory interface control circuit 40 activates the write enable signal (WE) and the attribute chip select signal (CS(A)), activates buffers 58 and 60, and directs multiplexer 30 to select the address lines from the processor interface circuit 34 for connection to latch 52. The attribute data is supplied to the attribute memory chip 20 through the processor interface 34, latch 48, and buffer 58.

The individual bit-maps of the characters of the character set are also provided to the video display circuit 10 by the processor 12, and this font data is stored in the font memory chip 22. To transfer font data from the processor to the font memory chip 20, the memory interface control circuit 40 activates the write enable signal (WE) and the font memory chip select signal (CS(F)), activates buffers 56, 58, and 62 directs multiplexer 26 to select the address lines from the processor interface circuit 34 for connection to latch 42 and directs multiplexer 28 to select the address lines from the processor interface circuit for connection to latch 44. The bit-map data is supplied to the font memory chip 22 through the processor interface 34, latch 48, and buffer 58. Graphics display data is transferred to the extra memory chip 24 in a manner similar to data transfers to the font memory chip 22, except the data passes through the processor interface 34, multiplexer 30, latch 52, and buffer 60.

In addition to the above-described write operations, the controller chip 16 provides the capability for the processor 12 to read the contents of the memory chips 18-24. Read operations are similar to the write operations, but separate buffers 64, 66 and 68 and latches 46, 50 and 54 are used to capture the data from the memory chips. Data is supplied to the processor 12 through multiplexer 32 and the processor interface 34.

As illustrated in Figure 3, each memory cell 74 in the character memory chip 18 has a corresponding memory cell 76 at the same address in the attribute memory chip 20. A character code, which is preferably a one byte ASCII code, is stored in the character memory to represent each character to be displayed. In Figure 3, the hexadecimal value of 31, which is the ASCII code for the numeral "1", is stored in the addressed memory cell of the character memory chip. An attribute code of that character is optionally stored in the attribute memory chip at the same address. The attribute code might indicate, for example, that the displayed character is to be underlinked, blinking, or inverse video. The attribute might also indicate a font selection if several alternative fonts are available in the font memory chip.

The individual bit-maps of the characters of the character set are stored in a block of memory cells 78 in the font memory chip 22. In the example illustrated in Figure 3, the numeral "1" is represented by a sixteen bit by eight bit binary bit-map. Each memory cell contains a value of either one or zero, depending upon whether the corresponding pixel of the visual display is to be illuminated or not. The character bit-map is addressed one row at a time, rather than one memory cell at a time. Each of the sixteen rows of the bit-map contains eight memory cells.

The bit-map data in the font memory chip 22 is addressed by a combination of character code data stored in the character memory chip 18 and a row address supplied by the memory address control circuit 36 of the controller chip 16. The eight bit value stored in the character memory chip directly supplies the low address to the character font address pins of the font memory chip. This eight bit value locates within the font memory the bit-map of the character code stored in the character memory. A four bit row address is supplied by the memory address control circuit 36 of the controller chip 16 to the row address pins of the font memory chip. This four bit value locates a particular row within the bit-map. If one or more alternative fonts are stored in the font memory chip, a font select signal from the controller chip is also supplied to the character font address pins to select the font.

As another step in character mode operation, the video display circuit 10 generates a video signal in the form of character pixel data. The video signal is a serial stream of bits that defines the states of the pixels of the video display device 14 according to the character and attribute data stored in the video screen memory. As shown in Figure 4, the display screen of the video display device can be partitioned into a rectangular array of character blocks 80, which in turn are partitioned into a rectangular array of pixels 82. For example, the video display device might be capable of displaying twenty-five rows of characters, with each row containing eight characters. Each character block has the same number of pixels that are contained in the character bit-maps stored in the font memory chip 22, namely, sixteen rows by eight columns. In this example, the display screen would thus contain a total of 400 rows (25 x 16) by 640 columns (80 x 8) of pixels.

The video display circuit 10 generates the video signal to define horizontal rows, or scan lines, of pixels. Each scan line defines the states of all the pixels in that row, the next scan line defines the states of all the pixels in the next row, and so on. The video signal is a serial stream of bits that define the pixels along a scan direction in each scan line of the video display device. The above-described example requires sixteen scan lines to define each row of characters, and 400 scan lines to define a complete screen of twenty-five rows of characters.

To generate the video signal, the controller chip 16 first addresses the character and attribute memory chips 18 and 20 and then addresses the font memory

chip 22 to read each row in the bit-map of each character to be displayed. Firstly, the memory address control circuit 36 of the controller chip 16 determines the address in the character and attribute memory chips 18 and 20 of a character to be displayed, the memory interface control circuit 40 activates the CS(C) and CS(A) chip select signals and the OE(C) and OE(A) output enable signals, and the memory interface control circuit directs multiplexer 30 to send the address to the address pins of the character and attribute memory chips. The memory address control circuit 36 also determines the current row address, which is supplied to the font memory chip 22 through multiplexer 26. Next, after the attribute and character memory chips have completed a data access cycle, the character memory chip supplies its character code data to the character font address pins of the font memory chip, and the controller chip reads the attribute data supplied to it by the attribute memory chip. The memory interface control circuit 40 then deactivates the attribute memory chip select and output enable signals, CS(A) and OE(A), and activates the font memory chip select and output enable signals, CS(F) and OE(FE). The controller chip then reads the character pixel data for the selected row from the font memory chip, and the display interface circuit 38 converts the character pixel data into the video signal by serializing the data and by processing it according to the selected attributes.

Thus, in character mode, the two access cycles of the character and font memory chips overlap to speed up the performance of the video display circuit 10. The controller chip does not have to read the character code data from the character memory chip and then rebroadcast it to the font memory chip because the character code data goes directly from the data pins of the character memory chip to the character font address pins of the font memory chip. Also, the attribute data from the attribute memory chip and the character pixel data from the font memory chip enters the controller chip through the same pins, thereby reducing the number of pins required to interface the controller chip to the memory chips.

In graphics mode, the processor 12 provides bit-by-bit graphics data to the video display circuit 10, which is then stored in the four memory chips 18-24. To generate the video signal, the controller 16 reads the stored graphics data from each pair of memories, namely the character and attribute memory chips 18 and 20, and the font and extra memory chips 22 and 24. Since each pair of memory chips is coupled to common address lines and separate data lines, the controller chip can read sixteen bits of graphics data per each memory access cycle. In graphics mode, the font memory chip is addressed solely from the controller chip 16, not the character memory chip 18 as in character mode.

An alternative embodiment of the present invention provides an additional interconnection between the controller chip 16 and the video display device 14. As described above, the AH(FE) pins of the controller chip 16 are needed to access the font memory chip 22 only during the second part of the access cycle. During the first part of the access cycle, when the controller chip is accessing the character and attribute memory chips 18 and 20, the five AH(FE) pins may be used for other purposes, such as relaying additional information to the video display device 14. The multiplexer 26 is used to selectively connect certain video signals from the display interface circuit 38 to the AH(FE) pins during the first part of the access cycle and to connect address signals from the memory address control circuit 36 to the AH(FE) pins during the second part of the access cycle. Such multiplexing provides an additional interconnection between the video display circuit 10 and the video display device 14 without increasing the number of pins on the controller chip 16.

From the above description, it will be apparent that the invention disclosed herein provides a novel and advantageous video display circuit and method for receiving and storing character code data provided by a processor and for supplying character pixel data in the form of a video signal to a video display device. As will be understood by those familiar with the art, the invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. For example, each memory chip of the present invention need not be a discrete integrated circuit. The several claimed memory chips could be combined into a single, monolithic memory device having the designated interconnections with the controller chip. On the other hand, each of the claimed memory chips could actually consist of several integrated circuits. Thus, the term "memory chip" is not to be read as limited to only a single, monolithic integrated circuit. More generally, the disclosure of the present invention is intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.

Claims

1. A video display circuit operable for receiving and storing character code data provided by a processor and for supplying character pixel data to a video display device, wherein the character code data specifies which characters are to be visually displayed and the character pixel data defines the pixel representations of the characters, said circuit comprising:

a controller chip for receiving the character code data from the processor, and for supplying the character pixel data to the video display device; and

memory means coupled to said controller chip and operable for storing the character code data of the characters to be displayed in a character memory of said memory means and for storing the character pixel data of all of the characters in a character set in a font memory of said memory means, said character memory including address and data pins connected to said controller chip and being operable for

storing the character code data received from the processor, said font memory being operable for storing in a block of memory cells the character pixel data for each character of the character set, said font memory including character font address pins that select a block of memory cells corresponding to a character whose character code is applied to said character font address pins and including row address pins that select a row of memory cells within said block of memory cells, and wherein data pins and said row address pins of said font memory are connected to said controller chip and said character font address pins of said font memory and said data pins of said character memory are connected in common to said controller chip.

2. A circuit as recited in claim 1 further comprising an attribute memory having address and data pins connected to said controller chip and operable for storing attribute data received from the processor, where the attribute data identifies attributes of characters stored in said character memory at corresponding addresses, wherein said address pins of said attribute memory and said address pins of said character memory are connected in common to said controller chip.

3. A circuit as recited in claim 2 wherein one or more of said data pins of said font memory are connected to said controller chip in common with one or more of said data pins of said attribute memory, and wherein said controller chip further includes enable means for alternatively supplying attribute data to or receiving attribute data from said attribute memory and receiving character pixel data from said font memory.

4. A circuit as recited in claim 1 operable in a character mode for receiving and storing character code data provided by the processor and for supplying character pixel data to the video display device, and operable in a graphics mode for receiving graphics display data provided by the processor, storing the graphics display data in said character and font memories, and supplying the graphics display data to the video display device, wherein said circuit further comprises an extra memory connected to said controller chip through data pins and address pins, and wherein said address pins of said extra memory and said address pins of said font memory are connected in common to said controller chip, said extra memory being operable for storing a portion of the graphics display data provided by the processor and for supplying that graphics display data to said controller chip in parallel with the graphics display data stored in said font memory.

5. A circuit as recited in claim 4 further comprising an attribute memory having data pins connected to said controller chip and having address pins connected in common with said address pins of said character memory to said controller chip, said attribute memory stores attribute data that identifies attributes of characters stored in said character memory at corresponding addresses when said circuit operates in said character mode, and said attribute memory stores the graphics display data provided by the processor and supplies the graphics display data to said controller chip in parallel with the graphics display data stored in said character memory when said circuit operates in said graphics mode.

6. A circuit as recited in claim 5 wherein one or more of said data pins of said extra memory are connected to said controller chip in common with one or more of said address pins of said attribute and character memories, wherein one or more of said data pins of said font memory are connected to said controller chip in common with one or more of said data pins of said attribute memory, and wherein said controller chip further includes enable means for alternatively supplying address data to said address pins of said attribute and character memories and receiving graphics display data from said extra memory, and includes enable means for alternatively supplying data to or receiving data from said data pins of said attribute memory and receiving character pixel data or graphics display data from said font memory.

7. A circuit as recited in claim 1 wherein said font memory further includes a font select address pin connected to said controller chip for selecting alternative blocks of memory cells containing alternative character pixel data for the characters of the character set.

8. A circuit as recited in claim 1 wherein said row address pins of said font memory are connected in common with signal lines coupled to the video display device, and wherein said controller chip includes multiplexing means for alternatively supplying row addresses to said font memory and supplying data to the video display device through said signal lines.

9. A video display circuit operable in a character mode for receiving and storing character code data and attribute data provided by a processor and for supplying corresponding character pixel data to a video display device, and operable in a graphics mode for receiving and storing graphics display data provided by the processor and for supplying the graphics display data to the video display device, wherein the character code data identifies characters to be displayed, the attribute data identifies attributes of the characters to be displayed, the character pixel data specifies pixel representations of the characters to be displayed, and the graphics display data specifies pixel representations of graphics information to be displayed, said circuit comprising:

a controller chip for receiving the character code data and the graphics display data from the processor, and for supplying the character pixel data and the graphics display data to the video display device; and

memory means coupled to said controller chip and operable in the character mode for storing the character code data of the characters to be displayed and the character pixel data of all of the characters in a character set, and operable in graphics mode for storing the graphics display data;

wherein said memory means includes a character memory chip, an attribute memory chip, a font memory chip, and an extra memory chip;

said character memory chip including address and data pins connected to said controller chip, said character memory chip operable in character mode for storing the character code data and operable in graphics mode for storing a portion of the graphics display data;

said attribute memory chip including data pins connected to said controller chip and address pins connected in common with said address pins of said character memory chip to said controller chip, said attribute memory chip operable in character mode for storing attribute data of characters stored in said character memory chip at corresponding addresses, and operable in graphics mode for storing a portion of the graphics display data and supplying the graphics display data to said controller chip in parallel with said character memory chip;

said font memory chip including data pins connected to said controller chip in common with said data pins of said attribute memory chip, including row address pins connected to said controller chip, and including character font address pins connected to said controller chip in common with said data pins of said character memory chip, said font memory chip being operable in character mode for storing in blocks of memory cells the character pixel data for the characters of the character set and operable in graphics mode for storing a portion of the graphics display data, wherein in character mode said character memory chip applies character code data to said character font address pins to select a block of memory cells corresponding to a character code stored in said character memory chip, and wherein said row address pins select a row of memory cells within said block of memory cells;

said extra memory chip including address pins connected to said controller chip in common with said address pins of said font memory chip and data pins connected to said controller chip in common with one or more of said address pins of said attribute and character memory chips, said extra memory chip being operable in graphics mode for storing a portion of the graphics display data and for supplying the graphics display data to said controller chip in parallel with said font memory chip;

and wherein said controller chip further includes enable means for alternatively supplying data to or receiving data from said data pins of said attribute memory ship and supplying data to and receiving data from said data pins of said font memory chip, and includes enable means for alternatively supplying address data to said address pins of said attribute and character memory chips and receiving graphics display data from said extra memory chip.

10. A method for receiving and storing character code data provided by a processor and for supplying character pixel data to a video display device, wherein the character code data identifies characters to be displayed and the character pixel data specifies pixel representations of the characters to be displayed, said method comprising the steps of:

receiving the character code data from the processor by a controller chip and storing the character code data in a character memory; and

supplying character pixel data to the video display device by said controller chip from a font memory that is operabl for storing in blocks of memory cells the character pixel data for the characters of the character set, wherein character code data supplied to character font address pins by said character memory serves to locate the pixel representations of corresponding characters, and wherein a row address supplied to row address pins by said controller chip serves to locate a row within said pixel representations; and

wherein said step of supplying character pixel data includes the steps of addressing a memory location in said character memory by said controller chip, supplying the character code data stored at said memory location directly to said character font address pins of said font memory by said character memory and supplying a row address to said row address pins of said font memory by said controller chip, and then supplying to the controller chip the character pixel data stored in the font memory at the address selected by said controller chip and said character memory.

11. A method for receiving and storing character code data and attribute data provided by a processor and for supplying character pixel data to a video display device, as recited in claim 10, wherein the attribute data identifies attributes of characters stored at corresponding addresses in said character memory, said method further comprising the step of receiving the attribute data from the processor by said controller chip and storing the attribute data in an attribute memory, said attribute memory having address pins connected to said controller chip in common with address pins of said character memory, wherein said step of addressing a memory location in said character memory includes simultaneously addressing a corresponding memory location in said attribute memory, and wherein said step of supplying the character code data includes simultaneously supplying corresponding attribute data to said controller chip.

12. A method as recited in claim 11 wherein one or more data pins of said font memory are

connected to said controller chip in common with one or more data pins of said attribute memory, wherein said step of receiving the attribute data from said controller chip includes supplying a write enable signal to said attribute memory, and wherein said step of supplying character pixel data to said controller chip includes supplying an output enable signal to said font memory.

13. A method for receiving and storing character code data provided by the processor and for supplying character pixel data to the video display device during operation in a character mode, as recited in claim 10, further comprising the steps of receiving graphics display data provided by the processor, storing the graphics display data in said character and font memories and in an extra memory, and supplying the graphics display data to the video display device during operation in a graphics mode, wherein said extra memory includes data pins connected to said controller chip and includes address pins connected to said controller chip in common with said address pins of said font memory, said extra memory being operable for storing a portion of the graphics display data and for supplying the graphics display data to said controller chip in parallel with said font memory.

14. A method for receiving and storing character code data and attribute data provided by a processor and for supplying character pixel data to a video display device during operation in character mode, as recited in claim 13, wherein the attribute data identifies attributes of characters stored at corresponding addresses in said character memory, said method further comprising the step of receiving the attribute data from the processor by said controller chip and storing the attribute data in an attribute memory during operation in character mode, said attribute memory having address pins connected to said controller chip in common with address pins of said character memory, wherein during operation in character mode said step of addressing a memory location in said character memory includes simultaneously addressing a corresponding memory location in said attribute memory and said step of supplying the character code data includes simultaneously supplying corresponding attribute data to said controller chip, and wherein during operation in graphics mode said step of storing the graphics display data includes storing a portion of the graphics display data in said attribute memory and said step of supplying the graphics data includes supplying graphics display data from said attribute memory to said controller chip in parallel with graphics display data from said character memory.

15. A method as recited in claim 10 wherein said step of supplying character pixel data further includes the step of supplying a font select signal to a font select address pin of said font memory for selecting alternative blocks of memory cells containing alternative character pixel data for the characters of the character set.

16. A method for receiving and storing character code data and attribute data provided by a processor and for supplying character pixel data to a video display device during operation in a character mode and for receiving and storing graphics display data provided by the processor and for supplying the graphics display data to the video display device during operation in a graphics mode, wherein the character code data identifies characters to be displayed, the attribute data identifies attributes of the characters to be displayed, the character pixel data specifies pixel representations of the characters to be displayed, and the graphics data specifies pixel representations of graphics information; during operation in character mode said method comprising the steps of;

receiving the character code data by a controller chip and storing the character code data in a character memory chip coupled thereto;

receiving the attribute data by said controller chip and storing the attribute data in an attribute memory chip coupled thereto; and thereafter

simultaneously addressing two corresponding memory locations in said character memory chip and said attribute memory chip by said controller chip, the address pins of said character memory chip and said attribute memory chip being connected in common to said controller chip;

supplying character code data to character font address pins of a font memory chip coupled to said character memory chip and to said controller chip and supplying corresponding attribute data to said controller chip, said character code data being supplied directly to said font memory chip by said character memory chip;

supplying a row address to row address pins of said font memory chip and an output enable signal to said font memory chip by said controllable chip, and

then supplying to the controller chip the character pixel data stored in the font memory chip at the address selected by said controller chip and said character memory chip, the data pins of said font memory chip and said attribute memory chip being connected in common to said controller chip;

and during operation in graphics mode said method comprising the steps of;

receiving the graphics display data by said controller chip;

storing the graphics display data in said character memory chip, said attribute memory chip, and said font memory chip and in an extra memory chip, wherein said extra memory chip includes data pins connected to said controller chip and address pins connected to said controller chip in common with said address

pins of said font memory chip, and thereafter

supplying the graphics display data to the video display device by simultaneously addressing said character memory chip and said attribute memory chip and supplying the graphics display data stored therein in parallel to said controller chip, and by simultaneously addressing said font memory chip and said extra memory chip and supplying the graphics display data stored therein in parallel to said controller chip.

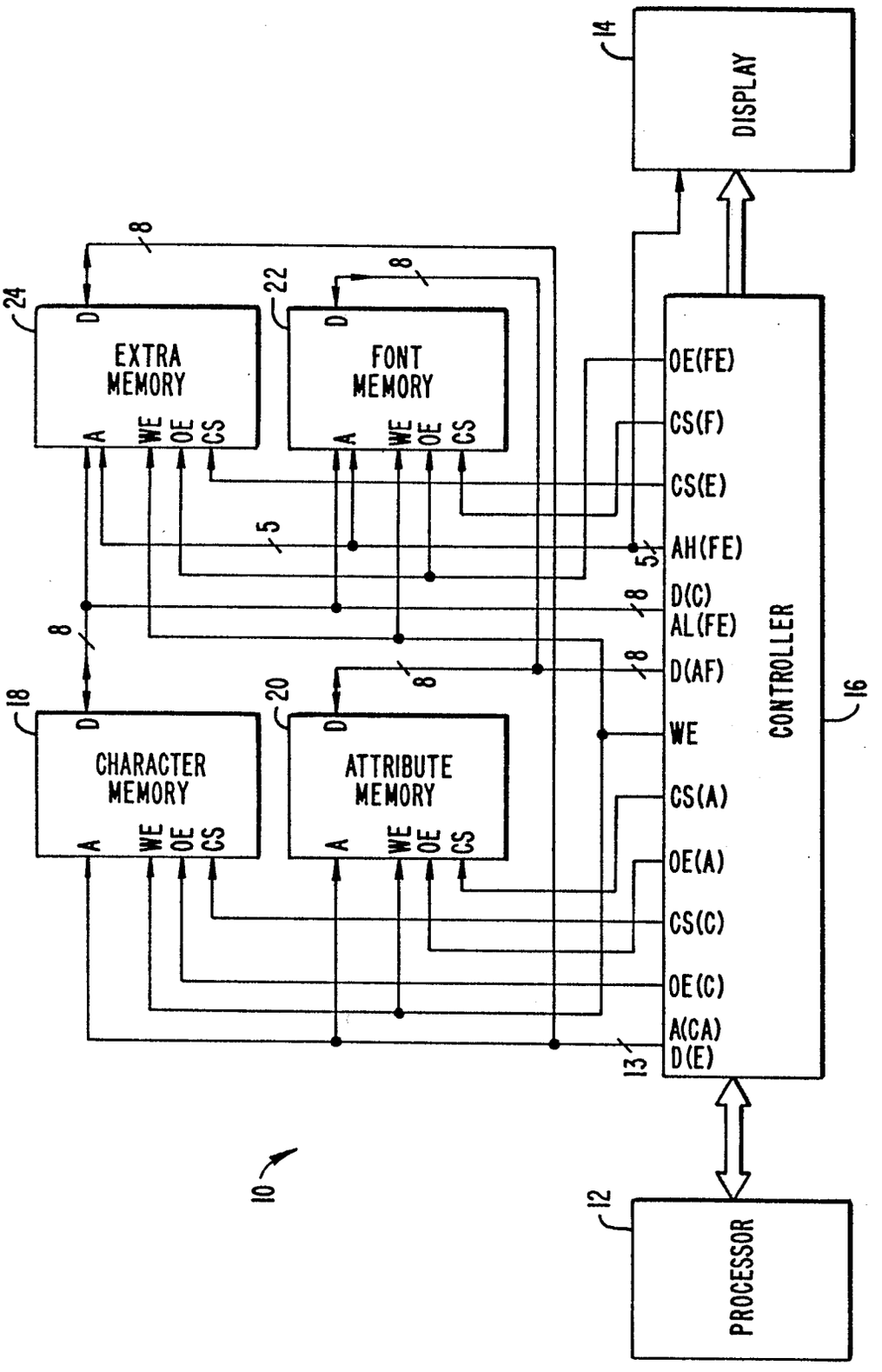

DISPLAY
14
EXTRA MEMORY
24
FONT MEMORY
22
CHARACTER MEMORY
18
ATTRIBUTE MEMORY
20
D
A
WE
OE
CS
8
5
CONTROLLER
16
OE(FE)
CS(F)
CS(E)
AH(FE)
D(C)
AL(FE)
D(AF)
WE
CS(A)
OE(A)
CS(C)
OE(C)
A(CA)
D(E)
13
PROCESSOR
12
10

FIG. 1.

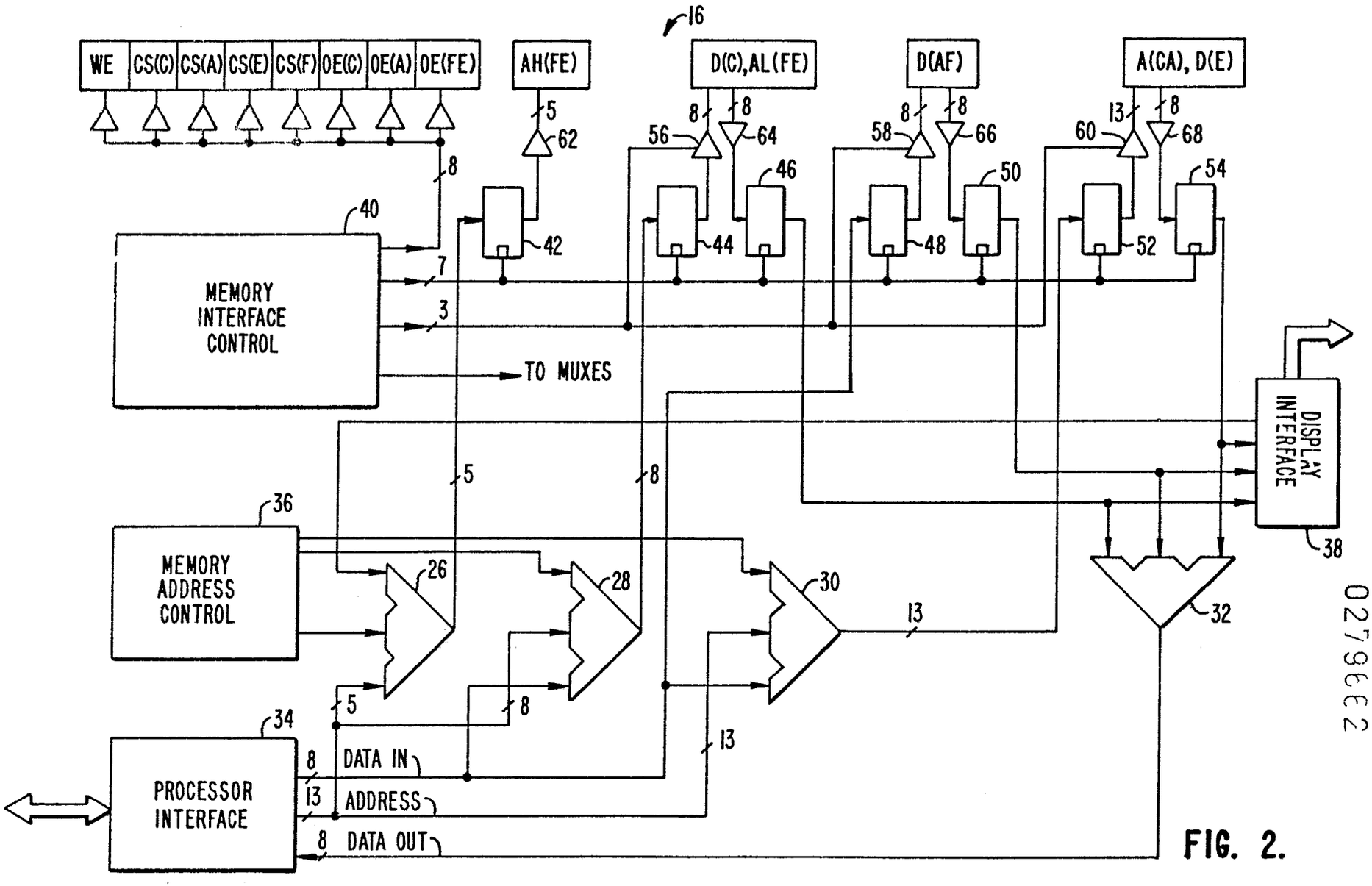


FIG. 2.

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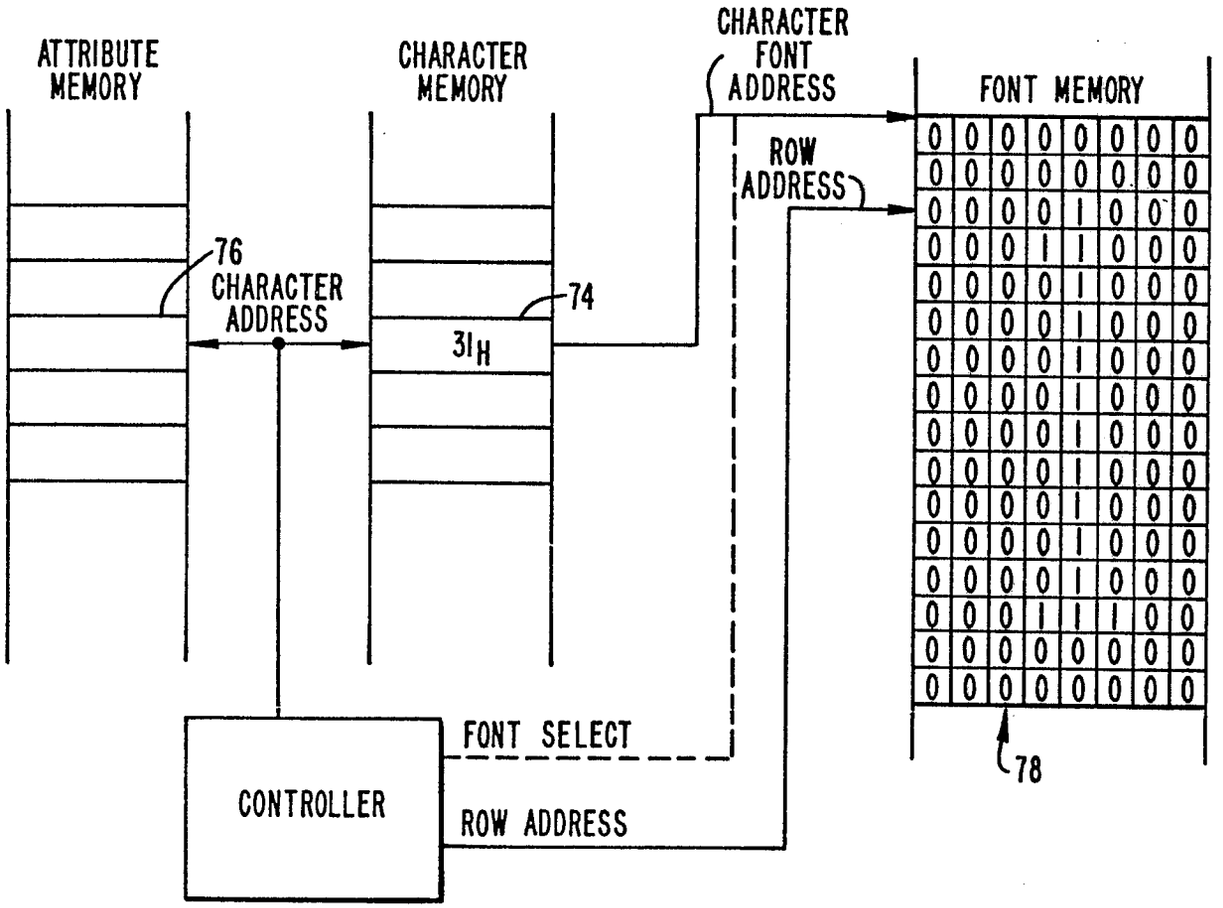

ATTRIBUTE MEMORY
CHARACTER MEMORY
CHARACTER FONT ADDRESS
FONT MEMORY
ROW ADDRESS
76
CHARACTER ADDRESS
74
31H
CONTROLLER
FONT SELECT
ROW ADDRESS
78

FIG. 3.

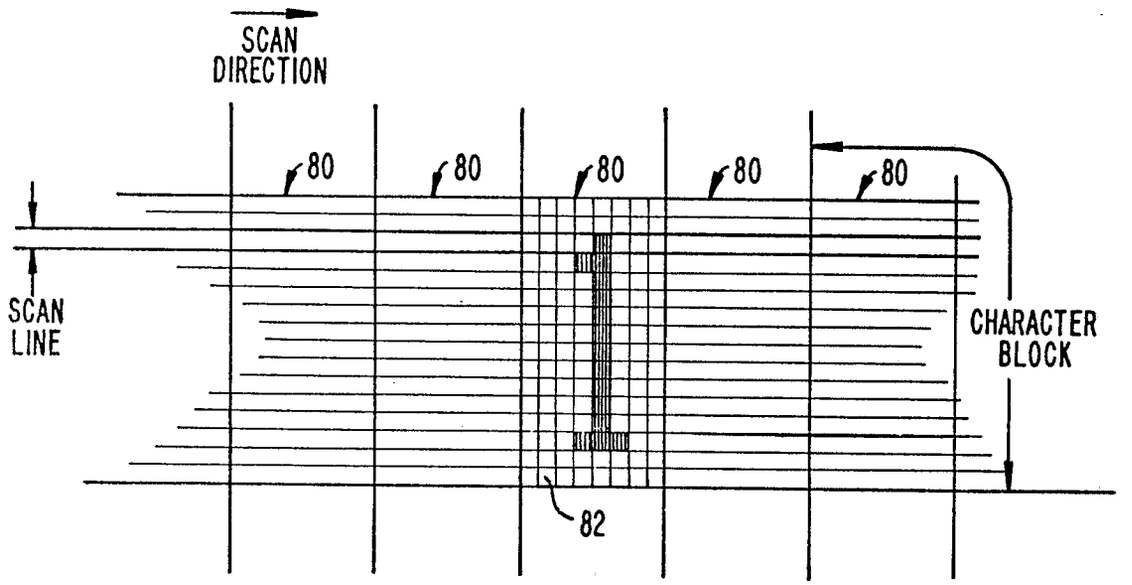

SCAN DIRECTION
80
80
80
80
80
SCAN LINE
CHARACTER BLOCK
82

FIG. 4.