ABSTRACT

A voltage-divider device including an output circuit capable of providing an output voltage from a preselected group of voltages, which output voltage may be set to correspond to a momentary or constant input voltage with respect to ground on a conductor thereof is disclosed. The output circuit includes gate means and clock means coupling the input voltage to an eight bit up down counter in order to produce a digital output representative of the input voltage which digital output is then converted to an output voltage by means of a digital to analog converter. Embodiments of the device providing a visual indication of the setting of the output voltage are disclosed.

3 Claims, 7 Drawing Figures
CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a division of copending application, Ser. No. 394,161, filed Sept. 4, 1973 entitled "TOUCH CONTROLLED VOLTAGE-DIVIDER".

BACKGROUND OF THE INVENTION

This invention relates to devices of the voltage divider type such as the potentiometers used in connection with volume controls for audio amplifiers of various kinds, and more particularly to a voltage-divider device which can be controlled by a momentary or continuous input voltage to provide a corresponding constant output voltage of a preselected group of output voltages.

In the prior art, volume controls have generally included an elongated resistance element having three terminals, one at each end of the resistance element and a third which is adjustable along the resistance element. Thus, if a given voltage difference is established across the resistance element by connecting opposite sides of a voltage source to the terminals at the ends of the resistance element, any desired voltage from that present at one end of the resistance element to that present at the other end of the resistance element may be obtained by proper adjustment of the third terminal along the length of the resistance element.

However, the adjustment of such third terminal according to the prior art required the physical movement of the third terminal along the resistance element usually by rotating a knob and often requiring complicated mechanical linkage between the knob and the third terminal.

It will be understood that the amount of time required to change the setting of a voltage-divider device of the prior art varies directly with the magnitude of the change in setting. It is an object of this invention to provide a voltage-divider device in which any change in setting may be made substantially instantaneously regardless of the magnitude of the change in setting.

SUMMARY OF THE INVENTION

Briefly, a voltage-divider device according to this invention includes means for detecting the presence of a voltage on a conductor thereof connected to one input of a first gate means. A digital clock means is connected to the other input of the first gate means. The conductor of the device is also connected to one input of each of a pair of voltage comparators through means providing a small voltage offset. The output of one of the voltage comparators is connected to one input of a second gate means and the output of the other voltage comparator is connected to one input of a third gate means.

The output of the first gate means is connected to the other input of each of the second and third gate means. The output of the second gate means is connected to the up terminal of a digital up down counter and the output of the third gate means is connected to the down terminal of the digital up down counter. The digital output terminals of the digital up down counter are connected to a digital to analog converter and the output of the digital to analog converter is connected to the other inputs of both of the voltage comparators and provides the output of the device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. 1, a simplified embodiment of the touch controlled voltage-divider device according to this invention is shown.

Referring to FIG. 1, a particular application for the output circuit according to this invention is also shown. An embodiment of the output circuit is shown in block diagram form in the right hand portion of FIG. 1 as connected to particular circuitry including a control element 40 having a resistive element 51.

One end of the resistive element 41 of the control element 40 is connected to a power supply which may provide a positive direct current voltage of 10 volts, for example. The other end of the resistive element 41 is connected to the anode of a germanium diode 50 which may be of the type sold under the designation 1N34, for example. The cathode of the diode 50 is connected to the anode of silicon diode 51 which may be of the type sold under the designation 1N914, for example, and the cathode of which is connected to ground.

Such other end of the resistive element 41 is also connected to the power supply (not shown) which provides a positive direct current voltage of 10 volts through a resistor 52 which may have a value of 10k ohms, for example. Finally, such other end of the control element 41 is connected to the negative input terminal of the voltage comparator A1 through a resistance 53 which may have a value of 3.3 megohms, for example. Thus, it will be seen that a constant reference voltage is present at such one end of the resistive element 41 of the control element 40 which reference voltage is applied to the negative input terminal of the voltage comparator A1. The circuitry of the voltage comparator A1 is such that its negative terminal is connected to ground through a silicon diode. Thus, the series connected germanium diode 50 and silicon diode 51 will insure that such reference voltage is slightly positive with respect to ground.

The conductive element 42 of the control element 40 is connected to ground through resistor R1 which may have a value of 1 megohm, for example. The conductive element 42 of the control element 40 is also connected to the positive input terminal of voltage comparator A1 through a resistor 54 which may have a value of 1 megohm, for example. Finally, the conductive element 42 of the control element 40 is connected to the anode of silicon diode D1 which may be of the type sold under the designation 1N914, for example. Thus, it will be seen that when galvanic contact is established between the conductive element 42 and a point on the resistive element 41 of the control element 40, a voltage corresponding to the point of contact will be developed across resistor R1 and applied to the posi-
tive input terminal of the voltage comparator A1 through the resistor 54. Such voltage will also be applied to the anode of the diode D1.

The cathode of the diode D1 is connected to the positive input terminal of the buffer amplifier A2 through a resistor 55. The cathode of diode D1 is also connected to ground through the capacitor C2 which may have a value of 1 microfarad, for example. According to this embodiment of the invention, the resistor R2 is inherent in the circuitry of the buffer amplifier A2 as indicated by the resistor shown in phantom between the positive input of such buffer amplifier A1 and ground in FIG. 1. The value of the capacitor C2 is selected to provide the desired time constant as discussed hereinabove.

The output of the buffer amplifier A2 which is labeled A in FIG. 1 may be applied to the negative inputs of each of a pair of voltage comparators A5 and A6 which are offset from each other by a small voltage represented in FIG. 1 as ideal generators E1 and E2. A conventional digital clock or oscillator 76 is providing its output connected to one input of a conventional gate 77. The output of the voltage comparator A1, labeled B in FIG. 1, is connected to the other input of the gate 77 and the output of the gate 77 is connected to one of the inputs of each of a pair of gates 78 and 79.

As shown in FIG. 1 the output of the voltage comparator A6 is connected to the other input of the gate 78 and the output of the voltage comparator A5 is connected to the other input of the gate 79. The output of the gate 78 is applied to the "up" terminal of a conventional 8 bit up-down counter 80 and the output of the gate 79 is applied to the "down" terminal of such counter 80.

The output lines 81-88 of the counter 80 are connected to a conventional digital to analog converter 90. The output of the digital to analog converter 90 provides both the output of the device and the positive terminals of the voltage comparators A5 and A6. It will be understood that the digital to analog converter 90 will have a certain minimum output corresponding to a one count of the 8 bit up-down counter 80.

The appearance of a voltage at the inputs A and B, produced by bringing the resistive element 41 of a control element 40 into contact with a conductive element 42 thereof, will open the gate 77 applying the output of the clock 76 to one of the inputs of each of the gates 78 and 79. At the same time the voltage input A will be compared to the voltage output of the digital to analog converter 90. If the voltage at input A is higher than the input of the digital to analog converter 90, the voltage comparator A6 will apply a signal to the other input of gate 78 opening such gate and applying the output of the clock 76 to the up terminal of the 8 bit up-down counter 80. The counter 80 will begin to count in an upward direction thereby raising the output of the digital to analog converter until it equals the voltage input A. At this point the output of voltage comparator A6 will tend to be cut off and voltage comparator A5 will tend to produce an output.

It will be understood that an output from the voltage comparator A5 will open the gate 79, applying the output of the clock 76 to the down terminal of the 8 bit up-down counter 80. Thus, if a lower voltage is subsequently applied to inputs A and B the 8 bit up-down counter 80 will count down to produce an output from the digital to analog converter 90 corresponding to such lower voltage. The offset voltage provided by ideal generators E1 and E2 may be set to correspond to the least significant digit of the 8 bit up-down counter 80.

As soon as the operator's fingers are removed from the control element 40 the voltages at inputs A and B will disappear and the 8 bit up-down counter 80 will remain at a constant count within one or two least significant digits of the count corresponding to the last voltage present at the input A. This in turn will result in a constant voltage output from the digital to analog converter 90 providing a constant voltage output from the device corresponding to the last voltage present at the input A, which output will remain constant until a new voltage setting is established by touching a different point on the control element 40 to apply a different voltage to inputs A and B.

As shown in FIG. 1, the output of the device is also applied to a network of light emitting diodes 48a-48n which may be of the type sold under the LITRONIX trademark and designated 209. The light emitting diodes are preferably arranged in the linearly spaced relationship with respect to each other as indicated. As shown in FIG. 1, the output of the device is applied to each light emitting diode independently through a different one of a plurality of resistors 71a-71n and a different one of a plurality of voltage comparator circuits 72a-72n. It will be understood that each of the voltage comparator circuits 72a-72n is connected to a common power supply (not shown) through a different one of a plurality of resistors 73a-73n, each of which has a different value thus establishing a different comparison voltage associated with each light emitting diode. By proper selection of the resistors 73a-73n the network may be adapted so that the light emitting diodes 48a-48n are turned on, one after another, by the voltage comparator circuits 72a-72n associated therewith as the voltage output of the device increases from its minimum to its maximum value. Similarly, the light emitting diodes will be turned off, one after another, as the voltage output of the device decreases from its maximum to its minimum value. Thus, the voltage output selected by a touch of the finger to the resistive element 41 of the control element 40 bringing a point therealong into contact with the conductive element 42 will cause a corresponding change in the number of consecutive light emitting diodes which are active thereby providing a visual indication of the setting of the device. However, as shown in FIG. 2 the visual indication of the setting of the device may also be conveniently provided by applying the outputs 84-88 of the 8 bit up-down converter 80, corresponding to the five most significant digits, to a conventional 32 bit decoder 91. Each of the 32 outputs of the 32 bit decoder 91 is applied to the base of a different one of a plurality of transistors T1-T32. According to this embodiment of the invention all of the light emitting diodes L1-L32 are connected in series with the cathode of the first light emitting diode L1 being connected to the negative terminal of a power supply (not shown) and the anode of the last light emitting diode L32 connected to the collector of the transistor T32 which has its base connected to the output of the 32 bit decoder 91 corresponding to the most significant digit. The emitters of all of the transistors T1-T32 are connected in parallel to the positive terminal of a voltage supply (not
shown). The collector of the transistor T1 is connected to the anode L1, the collector of the transistor T2 is connected to the anode of L2 and so forth, through transistors T32 and L32. Thus, as shown in FIG. 2 the appearance of an output at any one of the thirty two outputs of the thirty two bit decoder 91 will light up all of the light emitting diodes L1-L32 to the right of such output of the decoder 91.

The arrangement of the light emitting diodes L1-L32 as shown in FIG. 2 in proper sequential spaced relation to the control element 40 will thus provide a visual indication of the setting of such control element. This arrangement of light emitting diodes has the advantage of limiting the current which must be provided by the power supply to that required to light a single light emitting diode.

It is believed that those skilled in the art will adopt the various embodiments of the device disclosed herein to various applications by making obvious modifications therein to suit the particular application. In any event, it is believed that the various embodiments of the device disclosed herein may be adapted for use in any application where conventional voltage-divider devices are now being used without departing from the scope of this invention as set forth in the following claims.

What is claimed is:

1. In a voltage-divider device including means for detecting the presence of a voltage on a conductor of said device with respect to ground:
   a. a first gate means having one of its inputs connected to the output of said means for detecting the presence of a voltage on a conductor of said device;
   b. a digital clock means connected to the other input of said first gate means;
   c. a pair of voltage comparators each having one input thereof connected to said conductor of said device through means providing a small voltage offset;
   d. a second gate means having one input connected to the output of one of said pair of voltage comparators and the other input connected to the output of said first gate means;
   e. a third gate means having one input connected to the output of the other one of said pair of voltage comparators and the other input connected to the output of said first gate means;
   f. a digital up-down counter having its up terminal connected to the output of said second gate means and its down terminal connected to the output of said third gate means; and
   g. a digital to analog converter connected to the digital output terminals of said digital up-down counter, the output of said digital to analog converter being connected to the other inputs of said pair of voltage comparators and providing the output of said device.

2. In a voltage-divider device as claimed in claim 1, a network of light emitting diodes connected to the output of said digital to analog converter and adapted to provide a visual indication of the voltage value of said output of said digital to analog converter.

3. In a voltage-divider device as claimed in claim 1, a digital decoder means having input terminals connected to the digital output terminals of said digital up-down counter and its output terminals connected to visual display means adapted to provide a visual indication of the voltage of said output of said device.
UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,916,327
DATED : October 28, 1975
INVENTOR(S) : STEPHEN H. LAMPEN and WILLIAM E. HEARN

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 3, line 15, after "hereinabove." The following sentence should be inserted:
--The resistor 56 connected between the output of the buffer amplifier A2 and the negative input thereof has a value selected to set the gain of such amplifier at substantially unity which may be 560K ohms, for example.--

Signed and Sealed this Twenty-sixth Day of October 1976

[SEAL]

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks
UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 3,916,327
DATED : October 28, 1975
INVENTOR(S) : STEPHEN H. LAMPEN and WILLIAM E. HEARN

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 3, line 15, after "hereinabove." The following sentence should be inserted:
"The resistor 56 connected between the output of the buffer amplifier A2 and the negative input thereof has a value selected to set the gain of such amplifier at substantially unity which may be 560K ohms, for example."

Signed and Sealed this
Twenty-sixth Day of October 1976

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents and Trademarks