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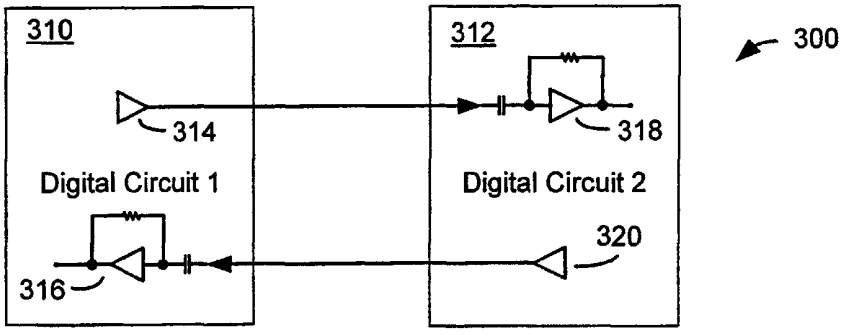
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(54) Title: CAPACITIVELY COUPLED RE-REFERENCING CIRCUIT WITH POSITIVE FEEDBACK



(57) **Abstract:** A circuit and method are disclosed for receiving a digital input signal referenced to arbitrary logic levels, and re-referencing the digital input signal to local logic levels. A re-referencing circuit includes a non-inverting circuit having an input and an output, and a non-inverting transfer characteristic between the input and the output. A capacitive element is connected in series with the non-inverting circuit that capacitively couples the digital input signal to the input of the non-inverting circuit. The re-referencing circuit also includes a resistive element connected between the input and the output of the non-inverting circuit. During operation, rising and falling edges of the digital input signal capacitively couple to the input of the non-inverting circuit and cross a threshold level, causing the non-inverting circuit to change its output state. The voltage at the output of the non-inverting circuit resistively couples back to the input of the non-inverting circuit, where it tends to cause the voltage at the input of the non-inverting circuit to equal the voltage at the output. As the input of the non-inverting circuit has no direct current (DC) connection to the digital input signal, voltage levels at the input of the non-inverting circuit remain referenced to the supply voltages of the non-inverting circuit, regardless of the voltage levels of the digital input signal. A clamping circuit can be used to protect the non-inverting circuit against input voltages having large voltage swings. In addition, an second resistive element can be connected between the input of the non-inverting circuit and a DC level to attenuate feedback from the output of the non-inverting circuit, thereby allowing operation with input signals having small voltage swings.

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CAPACITIVELY COUPLED RE-REFERENCING CIRCUIT WITH POSITIVE FEEDBACK

This invention relates generally to signal re-referencing, and more particularly to logic level re-referencing for digital signals in automatic test systems.

BACKGROUND OF THE INVENTION

Communicating among different portions of a test system customarily involves the use of level translators to re-reference digital signals. Fig. 1 illustrates a conventional technique for conveying digital signals between a first portion 110 and a second portion 112 of a test system. The first and second circuit portions 110, 112 may be physically distant from each other, or they may operate from different power supplies or grounds. Level translators 122 and 124 are connected between the first and second circuit portions 110 and 112. Each level translator receives an input signal from one circuit portion (e.g., from driver 114 or driver 120) and provides a re-referenced output signal to the other circuit portion (e.g., to receiver 116 or 118). Each level translator 122, 124 also receives power and ground from both of the circuits portions 110 and 112.

The purpose of a level translator is to transform an input signal having one set of logic levels into an output signal having another set of logic levels. For example, assume that a digital signal is to be conveyed from TTL logic levels to ECL logic levels. As is known, TTL logic generally uses +5v and ground for powering digital logic, and ECL logic generally uses ground and –5.2v. Logic high and low levels are approximately 4v and 1v, respectively, for TTL, but are approximately –0.8v and –1.8v for ECL. To convey logic signals from TTL to ECL, a level translator respectively transforms high and low logic signals on the TTL side into high and low logic signals on the ECL side.

By applying level translators 122, 124 to the system of Fig. 1, the different portions 110 and 112 of the test system can communicate with each other. They communicate, however, at the expense of increased component count and increased complexity.

When conveying large numbers of signals, such as data or address busses, level translators begin to constitute a significant portion of an overall system design. Level translators take up space that could otherwise be used for performing more substantive operations. They also consume power and cost money. In addition, when level translators are used to transmit signals that have precise timing relationships to

one another, it becomes difficult to maintain equal path delays among the different signals. Circuit board layout becomes particularly complicated.

To overcome the expense and complexity of providing separate level translators, many circuit designs have incorporated level translators within integrated circuits. The level translators then reside within the same physical packages that house the devices that receive the level-translated signals. But because conventional level translators require power and ground connections from both of the circuit portions to which they connect (e.g., circuit portions 110 and 112), the number of power and ground leads that must be provided on the integrated circuit packages grows considerably. The proliferation of power and ground leads reduces the number of leads that are available for conveying other signals, potentially limiting the functional capabilities of the integrated circuits.

What is needed is a way of conveying digital logic signals with less complexity. In particular, what is needed is a way of conveying digital logic between different portions of a system without having to convey as many power and ground connections as are required using current techniques.

SUMMARY OF THE INVENTION

With the foregoing background in mind, it is an object of the invention to convey digital logic between physically distant portions of a system or between different logic families.

Another object is to re-reference digital logic using fewer power supply or ground connections than are used with current techniques.

To achieve the foregoing objects and other objectives and advantages, a logic level re-referencing circuit includes a non-inverting circuit having an input and an output, and a non-inverting transfer characteristic between the input and the output. The logic level re-referencing circuit includes a capacitive element having a first node coupled to the input of the non-inverting circuit and a second node arranged to receive a digital input signal. The digital input signal need not be generated by a device of the same logic family as the non-inverting circuit, and may originate from a source that is physically distant from the non-inverting circuit. The logic level re-referencing circuit further includes a resistive element coupled between the input and the output of the non-inverting circuit. Rising and falling edges of the digital input signal couple through the capacitive element to the input of the non-inverting circuit, where they activate the non-inverting circuit to respectively assume high and low digital logic states. Output states are maintained by feedback through the resistive element.

In accordance with another aspect of the invention, a method for receiving a digital signal includes capacitively coupling rising and falling edges of the digital signal to an input of a non-inverting circuit. The non-inverting circuit has at least one threshold level at the input, and also has an output. The output of the non-inverting circuit respectively assumes high and low states in response to rising and falling edges at the input of a non-inverting circuit crossing the at least one threshold level. The method further includes resistively coupling the output of the non-inverting circuit to the input of the non-inverting circuit, to bias the input of the non-inverting circuit relative to the output.

According to yet another aspect of the invention, a method of constructing a logic level re-referencing circuit for receiving a digital input signal from a source circuit includes obtaining a commercially available non-inverting circuit. The non-inverting circuit has an input and an output, and a non-inverting transfer characteristic between the input and the output. A capacitive element is coupled in series between the input of the non-inverting circuit and the digital input signal. In addition, a resistive element is coupled between the input and the output of the non-inverting circuit. The resulting logic level re-referencing circuit transforms logic levels

referenced to the source circuit into logic levels referenced to the non-inverting circuit.

According to one feature, the non-inverting circuit is a logic gate incorporated within an integrated circuit, for example, an application-specific integrated circuit (ASIC) or a field-programmable gate array (FPGA).

According to still another aspect of the invention, a plurality of logic level re-referencing circuits are incorporated within an integrated circuit. Each logic re-referencing circuit includes a non-inverting circuit having an input and an output, and a non-inverting transfer characteristic between the input and the output. Each re-referencing circuit also includes a capacitive element having a first node coupled to the input of the non-inverting circuit and a second node arranged to receive a digital input signal. Each re-referencing circuit further includes a resistive element coupled between the input and the output of the non-inverting circuit. Rising and falling edges of each digital input signal couple through the capacitive element to the input of the non-inverting circuit, where they activate the non-inverting circuit to respectively assume high and low digital logic states. Output states are maintained by feedback through the resistive element.

Additional objects, advantages, and novel features of the invention will become apparent from a consideration of the ensuing description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood with reference to the accompanying drawings, in which aspects of the prior art and the invention are illustrated as follows:

Fig. 1 is a block diagram of a system in which logic levels are translated between two different portions of a digital system, or between two different families of digital logic, according to conventional techniques;

Fig. 2a is a simplified schematic of an embodiment of a re-referencing circuit according to the invention;

Fig. 2b is a timing diagram of waveforms that can be observed in the re-referencing circuit of Fig. 2a; and

Fig. 3 is a block diagram of a system in which logic levels are translated between two different portions of the system, or between two different families of digital logic, using re-referencing circuits according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Topology and Operation

Fig. 2a illustrates a re-referencing circuit 200 according to the invention. The re-referencing circuit 200 includes a non-inverting circuit 210 having an input 220 and an output 218. The re-referencing circuit 200 also includes a capacitive element 212 coupled between an input node 216 of the re-referencing circuit 200 and the input 220 of the non-inverting circuit 210. The re-referencing circuit further includes a resistive element 214 coupled between the input 220 of the non-inverting circuit 210 and the output 218 of the non-inverting circuit 210.

The re-referencing circuit 200 operates in response to an input signal 250 applied to the input node 216. As shown in Fig. 2b, the input signal 250 has high and low voltage levels established by a source circuit (not shown) from which the input signal originates. If the source circuit is a digital circuit belonging to the HCMOS logic family, for example, a high logic level typically equals +5v and a low logic level typically equals 0v. Therefore, the input signal 250 varies between 0 and 5v. If, however, the source circuit is an analog circuit, the voltage levels of the input signal 250 are based upon the characteristics of the analog circuit and do not necessarily correspond to logic levels of any particular logic family.

Fig. 2b illustrates input and output signals 250 and 252 of the re-referencing circuit 200, as well as examples (254, 256) of signals that may appear at the input 220 of the non-inverting circuit 210. Upon the occurrence of a rising edge of the input signal 250, the edge capacitively couples through the capacitive element 212 and appears at the input 220 of the non-inverting circuit 210. If the capacitively coupled rising edge at the input 220 crosses a high threshold of the non-inverting circuit 210, the non-inverting circuit 210 assumes a high output state. If the non-inverting circuit 210 is a digital circuit, the output signal 252 has as a voltage level commensurate with the normal high output voltage level of the logic family to which the non-inverting circuit 210 belongs. If the non-inverting circuit 210 is an analog circuit, the output level depends upon the particularities of the analog circuit.

When the output signal 252 goes high, a current is fed back through the resistive element 214 to the input 220 of the non-inverting circuit 210. The current from the output 218 tends to drive the input 220 of the non-inverting circuit 210 to the same voltage as the output 218 of the non-inverting circuit 210. With the input and output of the non-inverting circuit having substantially equal voltages, the logic re-referencing circuit maintains a stable state, even if the input signal 250 is disconnected.

Upon the occurrence of a falling edge of the input signal 250, a similar sequence of events takes place, although with opposite polarity. The falling edge capacitively couples through the capacitive element 212 and appears at the input 220 of the non-inverting circuit 210. If the capacitively coupled falling edge crosses a low threshold of the non-inverting circuit 210, the non-inverting circuit 210 assumes a low output state. Current feeds back through the resistive element 214, tending to drive the input 220 of the non-inverting circuit to a voltage that substantially equals the voltage at the output. A stable state is established, and that state is maintained until the logic re-referencing circuit 200 subsequently responds to a rising edge on the input signal 250. The stable state is maintained, even if the input signal is disconnected.

As shown in Fig. 2b, the input and output signals 250 and 252 appear to have equal voltage swings. The voltage swings of the input and output signals need not be the same, however. If the voltage swing of the input signal 250 is greater than the voltage swing of the output signal 252, the voltage at the input 220 of the non-inverting circuit 210 may appear like the signal 254. Positive edges of the input signal 250 cause the signal 254 to exceed the highest level of the output signal 252. Likewise, falling edges of the input signal 250 cause the signal 254 to exceed, in the negative direction, the lowest level of the output signal 252. After each transition, the signal 254 tends to return to the voltage of the output signal 252, as feedback through the resistive element 214 tends to equalize the input and output voltages of the non-inverting circuit 210.

If, however, the voltage swing of the input signal 250 is less than the voltage swing of the output signal 252, the voltage at the input 220 of the non-inverting circuit 210 may appear like the signal 256. Positive edges of the input signal 250 cause the signal 256 to rise to a value lower than the highest level of the output signal 252. Falling edges of the input signal 250 cause the signal 256 fall to a value higher than the lowest level of the output signal 252. Over time, feedback tends to cause the signal 256 to return to the voltage of the output signal 252.

The threshold level, or levels, of the non-inverting circuit 210 significantly affect the operation of the logic re-referencing circuit 200. For example, if the non-inverting circuit 210 has a single threshold for high low transitions, the capacitively coupled input signal (e.g., waveforms 254, 256) must cross that threshold to induce both high and low logic states. If the high and low thresholds are different, the non-inverting circuit 210 only goes high in response to rising edges crossing the high threshold, and only goes low in response to falling edges crossing the low threshold level.

DC voltage levels of the input signal 250 relative to the output signal 252 are substantially irrelevant to the operation of the re-referencing circuit 200. DC voltage levels of the input signal 250 are not applied to the non-inverting circuit 210, but rather are maintained across the capacitive element 212. Thus, the logic re-referencing circuit 200 behaves substantially the same way for input signals that vary between 0 and 5v as it does for those that vary between 10 and 15v, or between–10 and –5v.

Component Characteristics

The non-inverting circuit 210 has an input and an output, and a non-inverting transfer characteristic between the input and the output. The gain of the non-inverting circuit 210 should usually be at least one, to ensure that the output signal 252 can reach sufficient levels to meet input requirements of any downstream components. Preferably, the gain of the non-inverting circuit 210 is high, so that the particular amplitudes of the input and output signals 250, 252 need not be considered when constructing the re-referencing circuit 220.

The non-inverting circuit 210 can take a variety of forms. It can be implemented in either analog or digital form, as long as it is capable generating a digital output signal in response to an input signal crossing a threshold. For example, the non-inverting circuit 210 can be implemented using an analog differential amplifier. The non-inverting input of the differential amplifier carries the capacitively coupled input signal (from the input 220), and the inverting input of the differential amplifier receives a reference level. Capacitively coupled edges from the input signal 250 that cross the reference level cause the differential amplifier to change its output state.

When implemented in digital form, the non-inverting circuit 210 may constitute a single logic gate. A buffer can be used, an OR gate, an AND gate, or any other gate having a non-inverting transfer characteristic between an input and an output. If a logic gate has one or more unused inputs, the unused inputs should be connected in a manner that enables non-inverting operation of the logic gate between the input and the output.

Inverting logic gates can also be used to constitute the non-inverting circuit 210, as long as they are combined in ways that yield an overall non-inverting transfer characteristic. Gates with multiple outputs, for example differential outputs, can also be used, provided that the output that is connected to the resistive element 214 carries an output signal 252 that is non-inverting relative to the input signal 250.

Preferably, the capacitive element 112 is a discrete capacitor or a capacitor fabricated within an integrated circuit. The capacitive element should be chosen to reduce to an acceptable level the effects of stray input capacitance at the input 220 of

the non-inverting circuit 210. Typically, this means setting the capacitive element 112 to a capacitance at least five times greater than the input capacitance of the non-inverting circuit 210. For example, if the input 220 of the non-inverting circuit 210 has a stray capacitance of 3 picofarads, the capacitive element 212 should be chosen to have a capacitance of at least 15 picofarads. This is merely a rule of thumb. If very large input signals are expected, some attenuation of input edges can be tolerated, and smaller values of capacitance can be used.

Preferably, the resistive element 114 is a discrete resistor or a resistor fabricated within an integrated circuit. The resistive element 114 should be chosen to reduce to an acceptable level the effects of input bias current of the non-inverting circuit 210. An approximate way of ensuring this is to set the resistance of the resistive element 114 to less than twice the output voltage swing of the non-inverting circuit 210 divided by the maximum expected input bias current. For example, if the voltage swing at the output of the non-inverting circuit 210 is 5v and the maximum input bias current is 1 microampere, the resistive element 114 should typically have a resistance no greater than about 2 * 5v / 1 microampere = 10 Megaohms. If for some reason it is desired to use even larger values of resistance, additional care should be taken to ensure that the effects of input bias current do not interfere with the ability of input edges to cross threshold.

The resistive element 114 should also be large enough to prevent excessive attenuation of the input signal 250. The resistive element 114 combines with the capacitive element 112 to form a parasitic voltage divider, which can attenuate the input signal 250. Attenuation is reduced to negligible levels by selecting a resistance much greater than the impedance of the capacitive element 112 at the highest relevant frequencies of the input signal. For example, if the capacitance of the capacitive element 112 is 15 picofarads and the highest relevant frequency component of the input signal 250, including edge transitions, is 100 MHz, the impedance of the capacitive element 112 is about 100 ohms ($1 / 2*\pi*F*C$). To ensure that the resistive element 114 does not significantly attenuate edges of the input signal 250, the resistance of the resistive element 114 should be at least five times greater than this value, or at least 500 ohms.

The values of the resistive and capacitive elements 112 and 114 should also be chosen so that the time constant (R*C) formed by these elements exceeds the propagation delay of the non-inverting circuit. If an input edge trails off before the output of the non-inverting circuit 210 changes state, the circuit may momentarily glitch to a new state, but then immediately return to the old state, thus failing to track the input.

Commercial logic gates typically include built-in circuits to protect their inputs from damage arising from electro-static discharge (ESD). We have recognized that ESD circuits can also be used to protect the non-inverting circuit 210 from large voltage swings of the input signal 250, while maintaining normal operation of the re-referencing circuit 200.

ESD circuits vary, but commonly include a resistor connected in series with the input of a logic gate and a pair of clamping diodes connected between the input of the logic gate and the positive and negative supplies. One diode has an anode connected to the input of the gate and a cathode coupled to the more positive supply. The other diode has a cathode connected to the input of the gate and an anode connected to the more negative supply.

If excessive voltages appear at the input terminal, current flows through the resistor, through one of the clamping diodes, and into one of the supplies. The input of the gate thus remains within one diode drop of the gate's supplies, regardless of input voltage. No damage occurs and normal operation continues. If the non-inverting circuit 210 does not have an ESD circuit, protection circuitry like the kind described above can be added externally.

System-Level Design

Fig. 3 illustrates a system 300 that uses the re-referencing circuit 200. A first circuit portion 310 communicates with a second circuit portion 312 by sending and receiving digital signals. Specifically, a driver 314 within the first circuit portion 310 sends an electrical signal to a receiver 318 within the second circuit portion 312, and a driver 320 within the second circuit portion 312 sends an electrical signal to a receiver 316 within the first circuit portion 310. The system 300 uses a re-referencing circuit 200 for each of the receivers 316 and 318, in place of the receivers 112, 116, which were used in Fig. 1.

The system 300 of Fig. 3 does not require explicit level translators. Rather, level translating functions are provided internally to the receivers 316, 318. Moreover, the system 300 of Fig. 3 does not require additional power or ground connections.

Because fewer signals need to be routed between the first and second circuit portions 310 and 312, layout of circuit boards tends to be much simpler for the system 300 than for the prior system of Fig. 1. Furthermore, incorporation of the re-referencing circuit 200 within an integrated circuit can be accomplished without adding power supply or ground terminals to the integrated circuit package. The terminals that would otherwise be used to convey additional power and ground signals are thus free to convey signals that allow the integrated circuit to perform more substantive functions.

For truly transparent operation, the entire re-referencing circuit 200, including the non-inverting circuit 210, the capacitive element 212, the resistive element 214, and any protection circuitry, is incorporated within an integrated circuit. The input signal 250 is then received by the re-referencing circuit 200 via a single input terminal of the integrated circuit, in the same way that signals are received that do not require re-referencing.

Alternatives

Having described one embodiment, numerous alternative embodiments or variations can be made. For example, the re-referencing circuit 200 has been described for use with signals from distant portions of a system or from different logic families. The re-referencing circuit 200 is not limited, however, to these applications. Rather, it can be used for receiving all digital input signals of a circuit, regardless of whether the signals need to be re-referenced. Thus, the re-referencing circuit 200 can be a default digital receiver, able to accept a wide range of input signals. Integrated circuits can be constructed using the re-referencing circuit 200 as a default input receiver for receiving all digital input signals.

According to another variation, a re-referencing circuit can be constructed from readily available components. By adding an off-the-shelf capacitive element 212 and an off-the-shelf resistive element 114 to a pre-existing, commercially available non-inverting circuit 210, a re-referencing circuit can be readily constructed.

According to another variation, the capacitive element 112 can be located near the source circuit, which originates the input signal 250, rather than being located close to the non-inverting circuit 210.

As described above, the voltage swing of the input signal 250 of the re-referencing circuit 200 must be large enough to cross the threshold of the non-inverting circuit 210. According to another variation of the invention, this limitation is overcome using a re-referencing circuit 400, shown in Fig. 4. The re-referencing circuit 400 is similar to the re-referencing circuit 200, except that it includes a second resistive element 410 coupled between the input 220 of the non-inverting circuit 210 and DC level 412. The DC level 412 is preferably set to a value that approximately equals the threshold voltage of the non-inverting circuit 210. Feedback from the output of the non-inverting circuit 210 thus tends to drive the input 220 of the non-inverting circuit 210 to a level between the output voltage and the threshold voltage.

With the steady-state value of the input 220 closer to threshold, input signals with smaller voltage swings can still cross threshold. Although the second resistive element 410 attenuates the feedback from the output of the non-inverting circuit 410, it does not substantially attenuate the input signal 250. Thus, the re-referencing circuit 400 can be used to translate signals from logic families having small swings to

logic families having large swings. For example, by setting the DC level to 2.5v and setting the second resistive element 410 to one-fourth the resistance of the resistive element 114, the re-referencing circuit 400 can effectively translate ECL levels (1v swing) to HCMOS levels (5v swing). The circuit still operates for input signals having large voltage swings. Because the DC level 412 can be derived from the power supplies of the non-inverting circuit 210, no additional power supply connections are needed to realize the re-referencing circuit 400. The advantages of requiring only a single input terminal are therefore preserved.

In accordance with yet another variation, the re-referencing circuit 200 can be used to re-reference digital signals that have greater than two discrete logic levels. According to this variation, the non-inverting circuit 210 is provided with multiple input threshold levels and can generate multiple output levels. The output level of the non-inverting circuit 210 depends upon the level of the capacitively coupled input signal 254, 256 with respect to the input threshold voltages. Edges of the input signal 250 couple through the capacitive element 212 and cause the signal at the input 220 of the non-inverting circuit 210 to cross one or more of the threshold levels. The output of the non-inverting circuit is then caused to assume a state that corresponds to the input level. Feedback through the resistive element 214 tends to hold the input in its current state. That state is maintained even if the input signal is disconnected, until another edge of the input signal 250 occurs and crosses a threshold.

It should be understood, therefore, that the invention may be practiced in a variety of different ways, and should be limited only by the spirit and scope of the appended claims.

What is claimed is:

1. A logic level re-referencing circuit for receiving a digital input signal, comprising:

a non-inverting circuit having an input and an output, and a non-inverting transfer characteristic between the input and the output;

a capacitive element having a first node coupled to the input of the non-inverting circuit and a second node arranged to receive the digital input signal; and

a resistive element coupled between the input of the non-inverting circuit and the output of the non-inverting circuit,

wherein the logic level re-referencing circuit is constructed and arranged to couple rising and falling edges of the digital input signal through the capacitive element to the input of the non-inverting circuit, whereupon the rising and falling edges activate the non-inverting circuit to respectively assume high and low digital states.

2. The logic level re-referencing circuit of claim 1, manufactured within an integrated circuit.

3. The logic level re-referencing circuit of claim 1, wherein the capacitive element includes a capacitor integrated within an integrated circuit.

4. The logic level re-referencing circuit of claim 1, wherein the resistive element includes a resistor integrated within an integrated circuit.

5. The logic level re-referencing circuit of claim 1, wherein the non-inverting circuit is a commercially available non-inverting circuit, to which the resistive element and the capacitive element are attached to form the logic level re-referencing circuit.

6. The logic level re-referencing circuit of claim 1, wherein the non-inverting circuit has an input bias current and an output voltage swing, and the resistive element has a resistance less than twice the output voltage swing divided by the input bias current.

7. The logic level re-referencing circuit of claim 6, wherein

the capacitive element has an impedance that varies with frequency,

the digital input signal has a highest frequency component, and

the resistive element has a resistance at least five times greater than the impedance of the capacitive element at the highest frequency component of the digital input signal.

8. The logic level re-referencing circuit of claim 6, wherein the non-inverting circuit has an input capacitance, and the capacitive element has a capacitance at least five times greater than the input capacitance of the non-inverting circuit.

9. The logic level re-referencing circuit of claim 8, wherein the non-inverting circuit has a setup time, and a product of the resistance of the resistive element and the capacitance of the capacitive element exceeds the setup time of the non-inverting circuit.

10. The logic level re-referencing circuit of claim 8, wherein the non-inverting circuit has a propagation delay from the input of the non-inverting circuit to the output of the non-inverting circuit, and a product of the resistance of the resistive element and the capacitance of the capacitive element exceeds the propagation delay through the non-inverting circuit.

11. The logic level re-referencing circuit of claim 1, wherein the non-inverting circuit has an input capacitance, and the capacitive element has a capacitance at least five times greater than the input capacitance of the non-inverting circuit.

12. The logic level re-referencing circuit of claim 1, further comprising a protection circuit coupled to the input of the non-inverting circuit, for protecting the non-inverting circuit from large input voltages.

13. The logic level re-referencing circuit of claim 12, wherein the protection circuit is an ESD protection circuit.

14. The logic level re-referencing circuit of claim 1, wherein the resistive element is a first resistive element, and further comprising:

a second resistive element coupled between the input of the non-inverting circuit and a DC level, wherein the second resistive element forms a voltage divider with the first resistive element to attenuate a feedback voltage from the output of the non-inverting circuit.

15. The logic level re-referencing circuit of claim 14, wherein the DC level approximately equals a threshold voltage of the non-inverting circuit.

16. A method for receiving a digital signal, comprising:

capacitively coupling rising and falling edges of the digital signal to an input of a non-inverting circuit,

the non-inverting circuit further having at least one threshold level at the input of the non-inverting circuit,

the output of the non-inverting circuit changing its state responsive to the rising and falling edges at the input of the non-inverting circuit crossing the at least one threshold level; and

resistively coupling the output of the non-inverting circuit to the input of the non-inverting circuit to tend to maintain the input of the non-inverting circuit at a substantially same level as the output.

17. The method of claim 16, wherein the at least one threshold level is substantially the same level for both rising and falling edges.

18. The method of claim 16, wherein the at least one threshold level includes a rising threshold level and a falling threshold level, wherein the rising threshold level is more positive than the falling threshold level.

19. The method of claim 16, further comprising resistively coupling the input of the non-inverting circuit to a DC level, to attenuate a feedback signal from the output of the non-inverting circuit.

20. The method of claim 16, wherein the DC level approximately equals an input threshold voltage of the non-inverting circuit.

21. The method of claim 16, further comprising clamping the input of the non-inverting circuit to power supply connections of the non-inverting circuit, to protect the input of the non-inverting circuit from excessive voltages.

22. A method of constructing a logic level re-referencing circuit for receiving an incoming digital signal, comprising:

obtaining a commercially available non-inverting circuit having a non-inverting characteristic between an input and an output of the non-inverting circuit;

coupling a capacitive element in series between the incoming digital signal and the input of the non-inverting circuit; and

coupling a resistive element between the input of the non-inverting circuit and the output of the non-inverting circuit, thereby re-referencing the incoming digital signal to levels of the non-inverting circuit.

18. The method of claim 17, wherein the non-inverting circuit is incorporated within an integrated circuit.

19. The method of claim 18, wherein the integrated circuit is an application-specific integrated circuit (ASIC).

20. The method of claim 18, wherein the integrated circuit is a field-programmable gate array (FPGA).

21. A plurality of logic level re-referencing circuits incorporated within an integrated circuit, each of the plurality of logic re-referencing circuits comprising:

a non-inverting circuit having an input and an output, and a non-inverting transfer characteristic between the input and the output;

a capacitive element having a first node coupled to the input of the non-inverting circuit and a second node arranged to receive a digital input signal; and

a resistive element coupled between the input of the non-inverting circuit and the output of the non-inverting circuit,

wherein the logic level re-referencing circuit is constructed and arranged to couple rising and falling edges of the digital input signal through the capacitive element to the input of the non-inverting circuit, whereupon the rising and falling edges activate the non-inverting circuit to respectively assume high and low digital states.

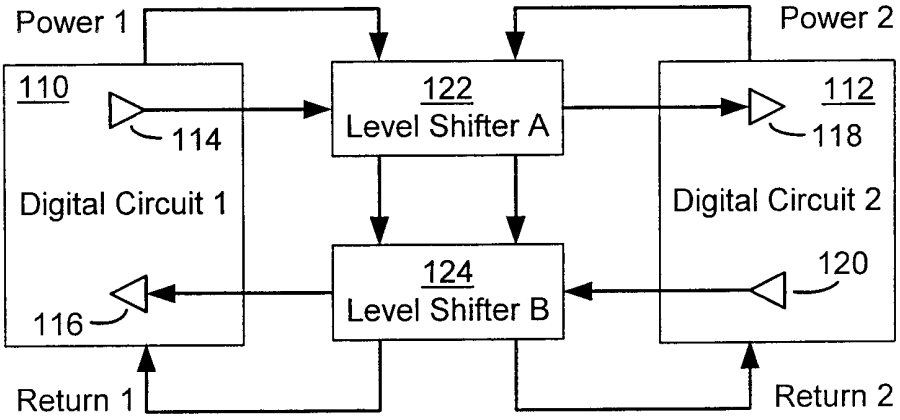


FIG. 1
(Prior Art)

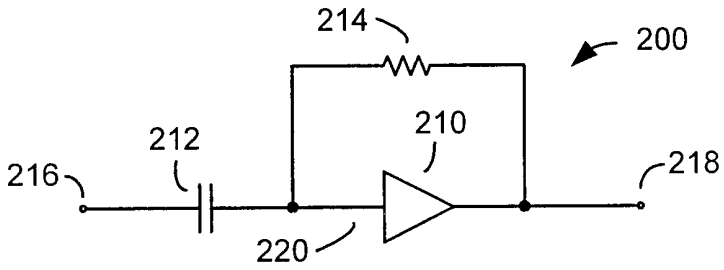


FIG. 2a

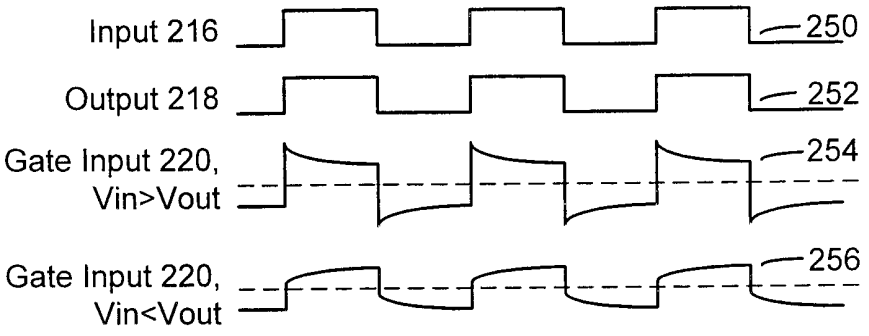


FIG. 2b

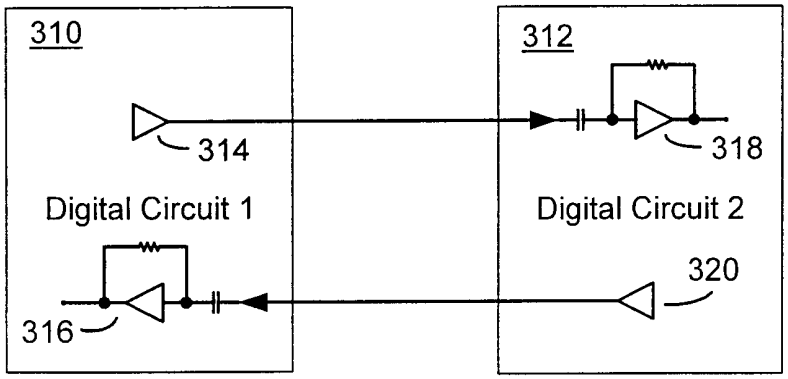

310
312
300
314
318
Digital Circuit 1
Digital Circuit 2
320
316

FIG. 3

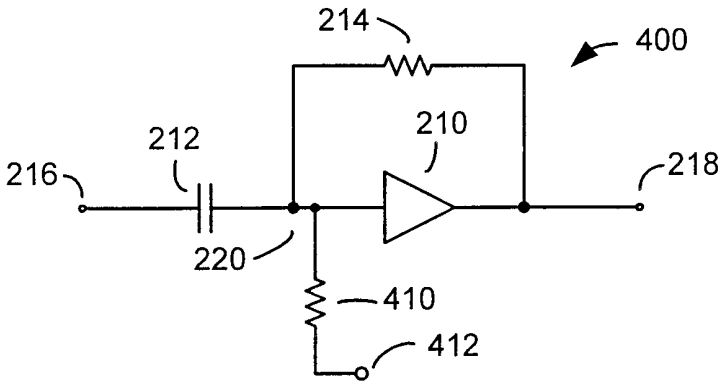

214
400
210
212
216
218
220
410
412

FIG. 4