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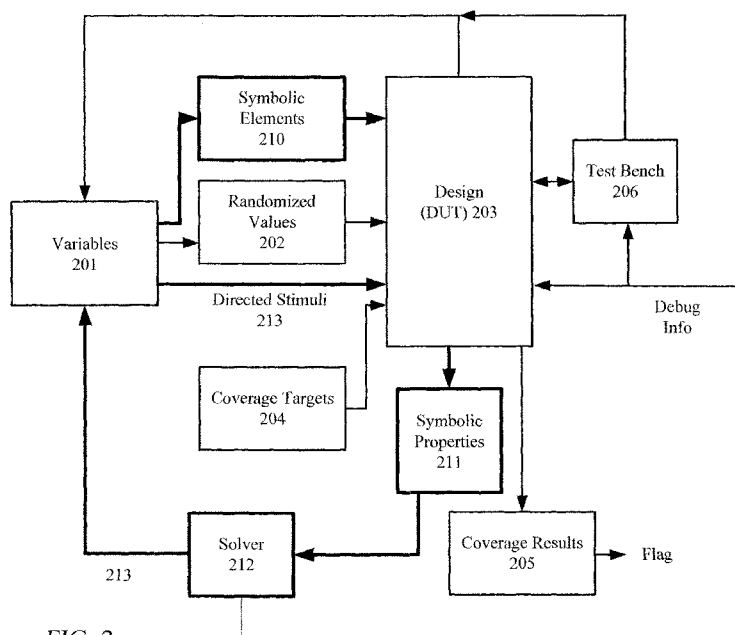
(54) **Title:** ACCELERATING COVERAGE CONVERGENCE USING SYMBOLIC PROPERTIES

FIG. 2

(57) **Abstract:** ABSTRACT In a method for increasing coverage convergence during verification of a design for an integrated circuit, multiple simulation runs can be performed. Symbolic variables and symbolic expressions can be generated for the variables and the variable expressions in the hardware code of the design and a test bench. Exemplary hardware code can include the hardware description language (HDL) code and/or the hardware verification language (HVL) code. Symbolic properties, which are derived from propagating the symbolic variables and symbolic expressions through the design and the test bench during the multiple simulation runs, can be collected. Coverage information from the multiple simulation runs can be analyzed to identify coverage points to be targeted. At this point, for each identified coverage point, the constraints resulting from the collected symbolic properties can be solved to generate directed stimuli for the design. These directed stimuli can increase the coverage convergence.

ACCELERATING COVERAGE CONVERGENCE USING SYMBOLIC
PROPERTIES

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to techniques for verifying the correctness of an integrated circuit design, and in particular to accelerating coverage convergence using symbolic properties.

Related Art

[0002] Integrated circuit designs have increasingly higher complexity. This complexity makes determining the correctness of the design both difficult and resource intensive. To verify the correctness of a design, a verification tool typically applies stimuli to the design under verification (DUV). In general, many stimuli and simulation runs are needed to achieve a reasonable coverage of the behavior of the DUV. The simulation outputs of the DUV can be compared to expected outputs to determine whether the design is providing the desired functionality.

[0003] Coverage is a key metric that measures the quality and project completeness in the functional verification of the design. Types of coverage targets can be characterized as either functional coverage targets or code coverage targets. In a functional coverage target, a user wants some scenario to happen in the design. For example, the user wants signal A to have

value X at the same time that signal B has value Y. In contrast, the code coverage target can include branch (if, case) statement, and line coverage. These types of coverage targets are well known and therefore not described in further detail.

[0004] Note that conventional simulations cannot generate such scenario information - hence the need for the user to specify coverage targets in a test bench. For example, FIG. 1 illustrates a conventional environment for a verification tool with an open loop, coverage convergence technique. In this environment, variables 101 of the hardware description language (HDL) code (typically in a register transfer level (RTL) format) of a design 103 are identified. In one embodiment, variables 101 are the input variables of design 103. In another embodiment, variables 101 are the input variables of specific starting points in design 103. After identification, randomized values 102 (i.e. stimuli) for variables 101 can be generated.

[0005] These randomized values 102 as well as user-provided coverage targets 104 can be provided to design 103 for simulation. In one embodiment, these simulations can be performed using a test bench 106 and design 103 is then typically referred to as a device-under-test (DUT). In another embodiment, the randomized values 102 can also be generated by test bench 106. The simulation results can be analyzed using functional verification and then provided to the user as coverage results 105.

[0006] Conventional functional verification uses constrained random simulation, which enables users to go from 0 to 80-90% coverage by automatically creating

thousands of tests (i.e. different stimuli). However, getting the remaining 10-20% coverage is a very time consuming and difficult manual process. Typically, this process requires that verification engineers work with design engineers to analyze the coverage obtained so far, identify coverage holes, determine the reasons for not reaching the missing coverage targets, and write new tests to hit the missing targets and achieve coverage convergence. Unfortunately, this coverage convergence phase of verification can take up to 30% of the overall chip development cycle.

[0007] Previous techniques for automatically reaching the missing coverage targets have encountered severe scalability problems and require extensive modifications to existing verification tools. One such technique relies on randomly changing paths based on symbolic properties with the goal of executing new, previously unexplored branches in the code.

[0008] Therefore, a need arises for a coverage convergence technique that can automatically increase the number of reached coverage targets. This technique should scale to any size design and require minimal modifications to existing verification tools.

SUMMARY OF THE INVENTION

[0009] A method for increasing coverage convergence during verification of a design for an integrated circuit is provided. In this method, multiple simulation runs are performed. Symbolic variables and symbolic expressions can be generated for the variables and the variable expressions in the hardware code of the design and a test bench. Exemplary hardware code includes the

hardware description language (HDL) code and/or the hardware verification language (HVL) code. Symbolic properties, which are derived from propagating the symbolic variables and symbolic expressions through the design and the test bench during the multiple simulation runs, can be collected. Coverage information from the multiple simulation runs can be analyzed to identify coverage points to be targeted. At this point, for each identified coverage point, the constraints resulting from the collected symbolic properties can be solved to generate directed stimuli for the design. These directed stimuli can increase the coverage convergence.

[0010] The directed stimuli can be used in a simulation to verify the expected coverage convergence. In one embodiment, debugging information can be provided to a user when a coverage target is not hit. In another embodiment, when an amount of data associated with storing of the symbolic properties exceeds a predetermined threshold, collecting of the symbolic properties can be either limited or restarted with less data being collected. In the latter case, the information collected can be leveraged to identify a narrower scope for symbolic property generation so that full data can then subsequently be collected within this limited scope, thereby decreasing the chance of exceeding the predetermined threshold.

[0011] In yet another embodiment, random simulation or random constrained simulation can be performed on the hardware code to increase the number of collected symbolic properties. In yet another embodiment, when a coverage target cannot be hit, one or more new paths through the design can be suggested.

[0012] A computer-readable medium storing computer-executable instructions for increasing coverage convergence during verification of a design for an integrated circuit is also provided. These computer-executable instructions, when executed by a computer, can perform the above-described steps.

[0013] This coverage convergence technique can advantageously solve the problem of the slow, manual coverage convergence phase of verification. Notably, this technique is applicable to designs at the block level up to full chip designs of any size.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 illustrates a conventional environment for a verification tool with an open loop, coverage convergence technique.

[0015] FIG. 2 illustrates an exemplary environment for a verification tool with a closed loop, coverage convergence technique.

[0016] FIG. 3 illustrates a flowchart of an exemplary coverage convergence technique that uses symbolic properties to generate stimulus vectors that can achieve high coverage targets.

[0017] FIG. 4 illustrates an exemplary generation of symbolic variables and expressions from conventional code.

[0018] FIG. 5 illustrates an exemplary execution using standard randomized values for variables versus using symbolic properties.

[0019] FIG. 6 illustrates a simplified representation of an exemplary digital ASIC design flow, which provides the context for the coverage convergence technique using symbolic properties.

DETAILED DESCRIPTION OF THE DRAWINGS

[0020] FIG. 2 illustrates an improved environment for a verification tool, which can leverage symbolic properties to achieve higher and faster coverage convergence than conventional tools. In this environment, variables 201 of the hardware code of a design 203 and a test bench 206 can be identified. Exemplary hardware code can include hardware description language (HDL) code and/or hardware verification language (HVL) code. In one embodiment, variables 201 can include the input variables of design 203. In another embodiment, variables 201 can include the input variables of specific starting points in design 203. After identification, randomized values 202 (i.e. stimuli) can be generated for variables 201 (called constrained random verification).

[0021] These randomized values 202 as well as user-provided coverage targets 204 can be provided to design 203 for simulation. In one embodiment, these simulations can be performed using a test bench 206 and design 103 is then typically referred to as a device-under-test (DUT). In another embodiment, the randomized values 202 can also be generated by test bench 206. In yet another embodiment, coverage targets 204 can be entered via test

bench 206. The simulation results can be analyzed using functional verification and then provided to the user as coverage results 205.

[0022] Note that the verification tool performs many simulation runs, each run with new values for variables 201 (also called legal inputs for the test). As simulations are performed during those multiple runs, the verification tool accumulates information to evaluate the feasibility of reaching coverage targets. Coverage targets can be reached by executing the simulation code using the generated values of the variables to create a certain condition or certain combinations of conditions in the design, as specified by coverage targets 204. Thus, coverage results 205 effectively determine whether the desired conditions were created.

[0023] When the desired conditions are not created by constrained random verification, it is extremely difficult for the user to manually generate directed tests (i.e. assign specific values to the variables) and/or manipulate constraints to achieve those desired conditions. Therefore, in one embodiment, after constrained random verification is run for a predetermined period and coverage results 205 still indicate less than full coverage convergence (which typically occurs for any large, complex design), a flag can be generated. This flag can trigger the generation of symbolic variables and expressions.

[0024] In accordance with one aspect of an improved coverage convergence technique, the accumulated intelligence from propagated symbolic variables and expressions through the design and the test bench can

advantageously provide a suggested mapping of actual values to variables to achieve target coverage. This accumulated intelligence can be characterized as symbolic properties, wherein a symbolic property is a factual statement about the expected or assumed behavior of a symbolic variable or expression. In one embodiment, when such mapping is not possible, then the verification tool can indicate why and provide enough information to generate some actionable feedback, i.e. a modification of one or more constraints and/or design elements, to minimize coverage non-convergence.

[0025] Note that one reason that target coverage cannot be achieved is because of a bug. Therefore, in one embodiment, actionable feedback generated by solver 212 may include debugging information, which can be provided to design (DUT) 203 and test bench 206. Debugging information may include constraint modifications. For example, a constraint may be loosened when too tight (e.g. a variable value set to 5-10 should instead be set to 0-10) or vice versa. Debugging information may also include modified sequential code. For example, the sequential code in the test bench or in the design may have some statements that change the stimulus to an extent that the target coverage is not achieved.

[0026] In one embodiment, after flag generation, variables in the hardware code, the test bench code, or the constraints can be analyzed to generate symbolic variables and symbolic expressions, i.e. symbolic elements 210. Solving these symbolic expressions in a solver 211, after propagation through design 203 and test bench 206, can increase and accelerate coverage

convergence and aid in coverage debug. Specifically, by combining hardware code simulation, coverage analysis, symbolic simulation, and constraint solving, a coverage convergence technique can be developed that can achieve higher and faster coverage convergence and at the same time provide relevant information to aid coverage debugging.

[0027] FIG. 3 illustrates an exemplary coverage convergence technique 300 that uses symbolic properties. Step 301 of technique 300 can run a conventional random simulation or random constrained simulation on the hardware description language (HDL) code of the design. In step 302, using a test bench, the simulator can test the design by using the randomized inputs described above. Notably, during these simulations, the symbolic variables and symbolic expressions are propagated through paths of the design and the test bench. The collected symbolic properties derived from this propagation can advantageously facilitate determining the relationship between the sampled signals (as identified from coverage analysis) and the random inputs (specifically, the variables) that control them. In general, the symbolic variables have a functional relationship to a generated random input (e.g. added to or subtracted from the random input), and the symbolic expressions are built from symbolic variables. Collecting the symbolic properties effectively traces the paths followed by the simulation.

[0028] FIG. 4 illustrates the pseudo code for a simple conventional simulation 401 as well as symbolic variables and expressions 402 that correspond to the variables and the variable expressions of simulation 401. In simulation 401, "a" and "b" are random value variables,

which in the design are used to construct the variable expression "c = (a + b)". In this example, symbolic variables <1> and <2> are created (to correspond to variables "a" and "b"), thereby allowing the following symbolic expressions to be generated: symbol<3>=<1>-<2>. Note that the display commands allow a user to look at the output of the simulation in order to better understand what took place. The "#" are delays in Verilog, e.g. #5 means the simulator should suspend execution of the current thread for 5 time units. The branch conditions show how the symbolic elements can be leveraged to take a particular branch, which may be the coverage target. In this case, if the symbolic expression <4> can be made equal to the value "1" then that particular branch can be entered and the coverage target associated with that branch would be reached.

[0029] The generated symbolic expressions can be sent to a solver, which can then determine a value that will likely result in a "true" condition based on symbolic properties. For example, if the user would like the value of "c" to be "1", then the solver can determine that symbol<1> must be equal to symbol<2> in order for symbol<4> (and by extension, "c") to be "1". Note that a conventional simulator cannot track the effect of the specific variables or variable expressions. As an add-on to a conventional verification tool including a simulator, the symbolic variables and symbolic expressions can advantageously allow tracing of design paths as they propagate through the design during simulations.

[0030] In one preferred embodiment, the symbolic properties are collected only for the paths taken by the

simulator and not other branches from the path. This limited collection can advantageously minimize the required memory resources to implement the coverage convergence technique with only minimal precision loss. This path tracing can be done at every step of the simulation.

[0031] Referring back to FIG. 3, step 303 can accumulate information regarding the results of these simulations for coverage analysis. Analyzing the coverage information, as well as the propagated symbolic properties and further analysis can be performed at each simulation step to identify intermediate coverage points that the simulator needs to target. In other words, the simulation of a design may include millions of steps with multiple symbolic elements (i.e. symbolic variables and/or symbolic expressions) being propagated to specific parts of the design and test bench during different steps. In one embodiment, the analysis can include processing of these symbolic elements as they arrive at specific parts of the design and the test bench. In another embodiment, the analysis can include accumulating these symbolic elements and then processing them at a later point in time. As indicated above, the symbolic properties, which are derived from propagation of the symbolic elements through the design and the test bench, allows the solver to suggest directed values (FIG. 2, directed stimuli 205) to replace the randomized inputs for the input variables. Such directed stimuli have a high probability in resulting in the desired conditions in the design. In one embodiment, step 303 can provide the user with a listing of the statements (i.e. lines of code) that were executed and contributed to the coverage result.

[0032] In one embodiment, an optional step 304 can further limit the symbolic property collection and symbolic variable/expression propagation based on exceeding a predetermined threshold. Note that this collection and propagation reduction is in addition to the path-specific reduction performed as part of step 302. In one embodiment, if the amount of collected information for symbolic properties or symbolic elements exceeds the predetermined threshold, then the simulator can selectively drop some collected symbolic property information or even eliminate certain symbolic elements. This dropping can be done arbitrarily or can incorporate some intelligent heuristics such as ranking the various symbolic variables according to their contribution to the collected symbolic properties or minimizing the size of the collected symbolic properties. In one embodiment, the user can be notified of any dropped information, with the option of re-inserting this collected information into the simulation to increase precision (although probably impacting system performance). In another embodiment, symbolic property collection can be restarted with less data being collected. In this case, the information collected can be leveraged to identify a narrower scope for symbolic property generation so that full data can then subsequently be collected within this limited scope, thereby decreasing the chance of exceeding the predetermined threshold.

[0033] For each identified coverage target, step 305 can solve the constraints resulting from the collected symbolic properties to generate directed stimuli to reach that coverage target. In step 306, if the coverage target cannot be hit, then debugging information can be

provided to the user explaining why the coverage target cannot be hit. Optionally, or in addition to step 306, if the coverage target cannot be hit, then step 307 can suggest new paths that can potentially hit the coverage target.

[0034] Step 308 can perform standard simulation with the directed values for inputs to the design (in this loop, with no symbolic variables, symbolic expressions, or random variables) to validate the results. In other words, step 308 ensures that the stimuli generate the desired conditions (i.e. the user scenarios happen) in the design. In one embodiment, an optional step 309 can repeat simulation iterations with different randomized inputs, different starting points in the design (e.g. computed in previous simulation iterations), or on different unexplored paths of the design.

[0035] FIG. 5 illustrates an exemplary execution using standard randomized values for variables versus using the symbolic properties described above. Specifically, block 501 represents some SystemVerilog code, which could describe a portion of a design. Block 502 represents one execution of that code using randomized values for variables. As noted, the result of this execution is "FALSE" and therefore the coverage point is not hit. Block 503 represents the generation of the symbolic expressions and properties. The generated symbolic properties (shown in the dotted box) can be sent to a solver 505, which generates solution 506. That is,

a = 7;
b = 3;
c = 10;
d = 4;

```
(4 ==4)? e = 10 : e = 18;  
if (10 ==10)
```

Because solution 506 is "TRUE", the coverage point is hit. Thus, as seen from above, the use of symbolic properties can result in significantly faster coverage convergence than using conventional randomized values for variables.

[0036] The coverage convergence technique described above can provide significant advantages over conventional techniques. For example, the coverage convergence technique using symbolic properties can provide faster, machine-assisted coverage convergence. The coverage convergence technique using symbolic properties can also provide faster, machine-assisted coverage debug. Moreover, the coverage convergence technique using symbolic properties can provide the user with hints to modify sections of code or constraints to improve coverage. The coverage convergence technique using symbolic properties can also advantageously scale with large design sizes significantly better than comparable technologies, such as formal analysis. The coverage convergence technique using symbolic properties can also advantageously leverage existing verification infrastructures and widely deployed methodologies.

[0037] FIG. 6 illustrates a simplified representation of an exemplary digital ASIC design flow, which provides the context for the coverage convergence technique described above. At a high level, the process starts with the product idea (step 600) and is realized in an EDA software design process (step 510). When the design is finalized, it can be taped-out (event 640). After tape out, the fabrication process (step 650) as well as

packaging and assembly processes (step 660) can occur, thereby resulting in finished chips (result 670).

[0038] The EDA software design process (step 610) is actually composed of a number of steps 612-630, shown in linear fashion for simplicity. In an actual ASIC design process, the particular design might have to go back through steps until certain tests are passed. Similarly, in any actual design process, these steps may occur in different orders and combinations. This description is therefore provided by way of context and general explanation rather than as a specific, or recommended, design flow for a particular ASIC.

[0039] A brief description of the components steps of the EDA software design process (step 610) will now be provided. In system design (step 612), the designers can describe the functionality that they want to implement, perform what-if planning to refine functionality, check costs, etc. Hardware-software architecture partitioning can occur at this stage. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Model Architect, Saber, System Studio, and DesignWare® products.

[0040] In logic design and functional verification (step 614), the VHDL or Verilog code for modules in the system is written and the design is checked for functional accuracy. More specifically, the design is checked to ensure that it produces the correct outputs. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include VCS, VERA, DesignWare®, Magellan, Formality, ESP and LEDA products. In one embodiment, the above-described coverage convergence

technique can be implemented in the VCS tool, which is run during step 614.

[0041] In synthesis and design for test (step 616), the VHDL/Verilog code is translated to a netlist. The netlist can be optimized for the target technology. Additionally, the design and implementation of tests to permit checking of the finished chip occurs. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Design Compiler®, Power Compiler, Tetramax, and DesignWare® products.

[0042] In netlist verification (step 618), the netlist is checked for compliance with timing constraints and for correspondence with the VHDL/Verilog source code. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Formality, PrimeTime, and VCS products. In one embodiment, the samples-based, multi-corner static timing analysis can be used in step 218.

[0043] In design planning (step 620), an overall floorplan for the chip is constructed and analyzed for timing and top-level routing. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Astro and IC Compiler products.

[0044] In physical implementation (step 622), the placement (positioning of circuit elements) and routing (connection of the same) can occur. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include the Astro and IC Compiler products.

[0045] In analysis and extraction (step 624), the circuit function is verified at a transistor level, which in turn permits what-if refinement. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include AstroRail, PrimeRail, Primetime, and Star RC/XT products.

[0046] In physical verification (step 626), various checking functions are performed to ensure correctness for manufacturing, electrical issues, lithographic issues, and circuitry. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include the Hercules product.

[0047] In resolution enhancement (step 628), geometric manipulations of the layout can be performed to improve manufacturability of the design. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include Proteus, ProteusAF, and PSMGen products.

[0048] In mask data preparation (step 630), the "tape-out" data for production of masks can be lithographically used to produce the integrated circuit chips. Exemplary EDA software products from Synopsys, Inc. that can be used at this step include the CATS(R) family of products.

[0049] The coverage convergence technique described above can be implemented advantageously in one or more computer programs that execute on a programmable system including at least one programmable processor coupled to receive data and instructions from, and to transmit data and instructions to, a data storage system, at least one input device, and at least one output device. Each computer program can be implemented in a high-level

procedural or object-oriented programming language, or in assembly or machine language if desired; and in any case, the language can be a compiled or interpreted language. Suitable processors include, by way of example, both general and special purpose microprocessors, as well as other types of micro-controllers. Generally, a processor will receive instructions and data from a read-only memory and/or a random access memory. Generally, a computer will include one or more mass storage devices for storing data files; such devices include magnetic disks, such as internal hard disks and removable disks, magneto-optical disks, and optical disks. Storage devices suitable for tangibly embodying computer program instructions and data include all forms of non-volatile memory, including by way of example semiconductor memory devices, such as EPROM, EEPROM, and flash memory devices, magnetic disks such as internal hard disks and removable disks, magneto-optical disks, and CDROM disks. Any of the foregoing can be supplemented by, or incorporated in, application-specific integrated circuits (ASICs).

[0050] A detailed description of one or more embodiments of the invention is provided above along with accompanying figures that illustrate the principles of the invention. The invention is described in connection with such embodiments, but the invention is not limited to any embodiment. The scope of the invention is limited only by the claims and the invention encompasses numerous alternatives, modifications and equivalents. Numerous specific details are set forth in the above description in order to provide a thorough understanding of the invention. These details are provided for the purpose of example and the invention may be practiced according to the claims without some or all of these specific details.

For the purpose of clarity, technical material that is known in the technical fields related to the invention has not been described in detail so that the invention is not unnecessarily obscured.

CLAIMS

1. A method for increasing coverage convergence during verification of a design for an integrated circuit, the method comprising:

- performing multiple simulation runs;
- generating symbolic variables and symbolic expressions for variables and variable expressions, respectively, in hardware code of the design and a test bench;

- collecting symbolic properties derived from the symbolic variables and symbolic expressions being propagated through the design and the test bench during the multiple simulation runs;

- analyzing coverage information from the multiple simulation runs to identify coverage points to be targeted; and

- using a computer, for each identified coverage point, solving constraints resulting from collected symbolic properties to generate directed stimuli for the design, the directed stimuli increasing the coverage convergence.

2. The method of Claim 1, further including performing one of random simulation and random constrained simulation on the hardware code.

3. The method of Claim 1, further including providing debugging information to a user when a coverage target is not hit.

4. The method of Claim 1, further including using the directed stimuli in a simulation and verifying expected coverage convergence.

5. The method of Claim 1, further including limiting the symbolic properties when an amount of data associated with storing of the symbolic properties exceeds a predetermined threshold.

6. The method of Claim 1, further including suggesting new paths through the design when a coverage target cannot be hit.

7. A computer-readable medium storing computer-executable instructions for increasing coverage convergence during verification of a design for an integrated circuit, which when executed by a computer performs steps comprising:

- performing multiple simulation runs;
- generating symbolic variables and symbolic expressions for variables and variable expressions, respectively, in hardware code of the design and a test bench;

- collecting symbolic properties derived from the symbolic variables and symbolic expressions being propagated through the design and the test bench during the multiple simulation runs;

- analyzing coverage information from the multiple simulation runs to identify coverage points to be targeted; and

- for each identified coverage point, solving constraints resulting from collected symbolic properties to generate directed stimuli for the design, the directed stimuli increasing the coverage convergence.

8. The computer-readable medium of Claim 7, further including performing one of random simulation and random

constrained simulation on the hardware code.

9. The computer-readable medium of Claim 7, further including providing debugging information to a user when a coverage target is not hit.

10. The computer-readable medium of Claim 7, further including using the directed stimuli in a simulation and verifying expected coverage convergence.

11. The computer-readable medium of Claim 7, further including limiting the symbolic properties when an amount of data associated with storing of the symbolic properties exceeds a predetermined threshold.

12. The computer-readable medium of Claim 7, further including suggesting new paths through the design when a coverage target cannot be hit.

13. A system for increasing coverage convergence during verification of a design for an integrated circuit, the system including a processor configured to perform steps comprising:

- performing multiple simulation runs;
- generating symbolic variables and symbolic expressions for variables and variable expressions, respectively, in hardware code of the design and a test bench;

- collecting symbolic properties derived from the symbolic variables and symbolic expressions being propagated through the design and the test bench during the multiple simulation runs;

- analyzing coverage information from the multiple simulation runs to identify coverage points to be

targeted; and

for each identified coverage point, solving constraints resulting from collected symbolic properties to generate directed stimuli for the design, the directed stimuli increasing the coverage convergence.

14. The system of Claim 13, further including performing one of random simulation and random constrained simulation on the hardware code.

15. The system of Claim 13, further including providing debugging information to a user when a coverage target is not hit.

16. The system of Claim 13, further including using the directed stimuli in a simulation and verifying expected coverage convergence.

17. The system of Claim 13, further including limiting the symbolic properties when an amount of data associated with storing of the symbolic properties exceeds a predetermined threshold.

18. The system of Claim 13, further including suggesting new paths through the design when a coverage target cannot be hit.

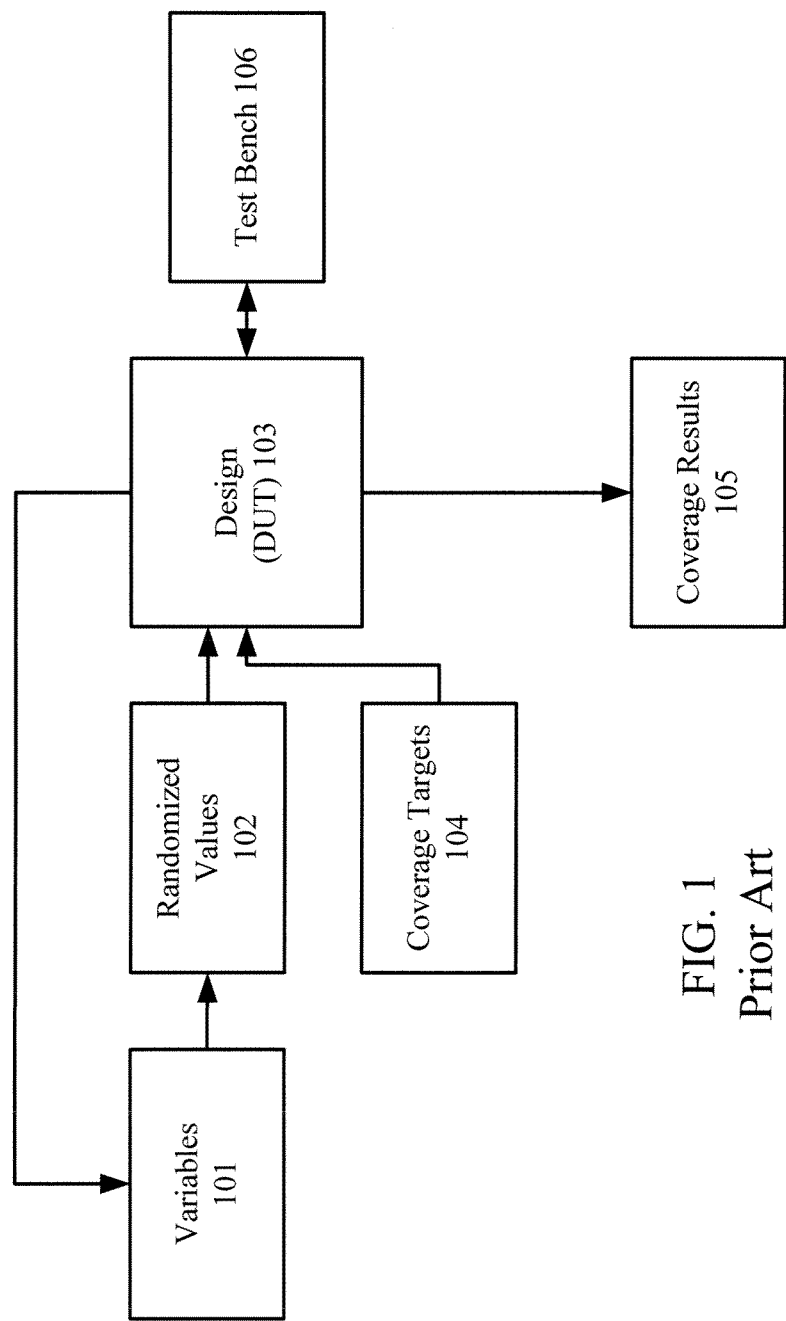


FIG. 1
Prior Art

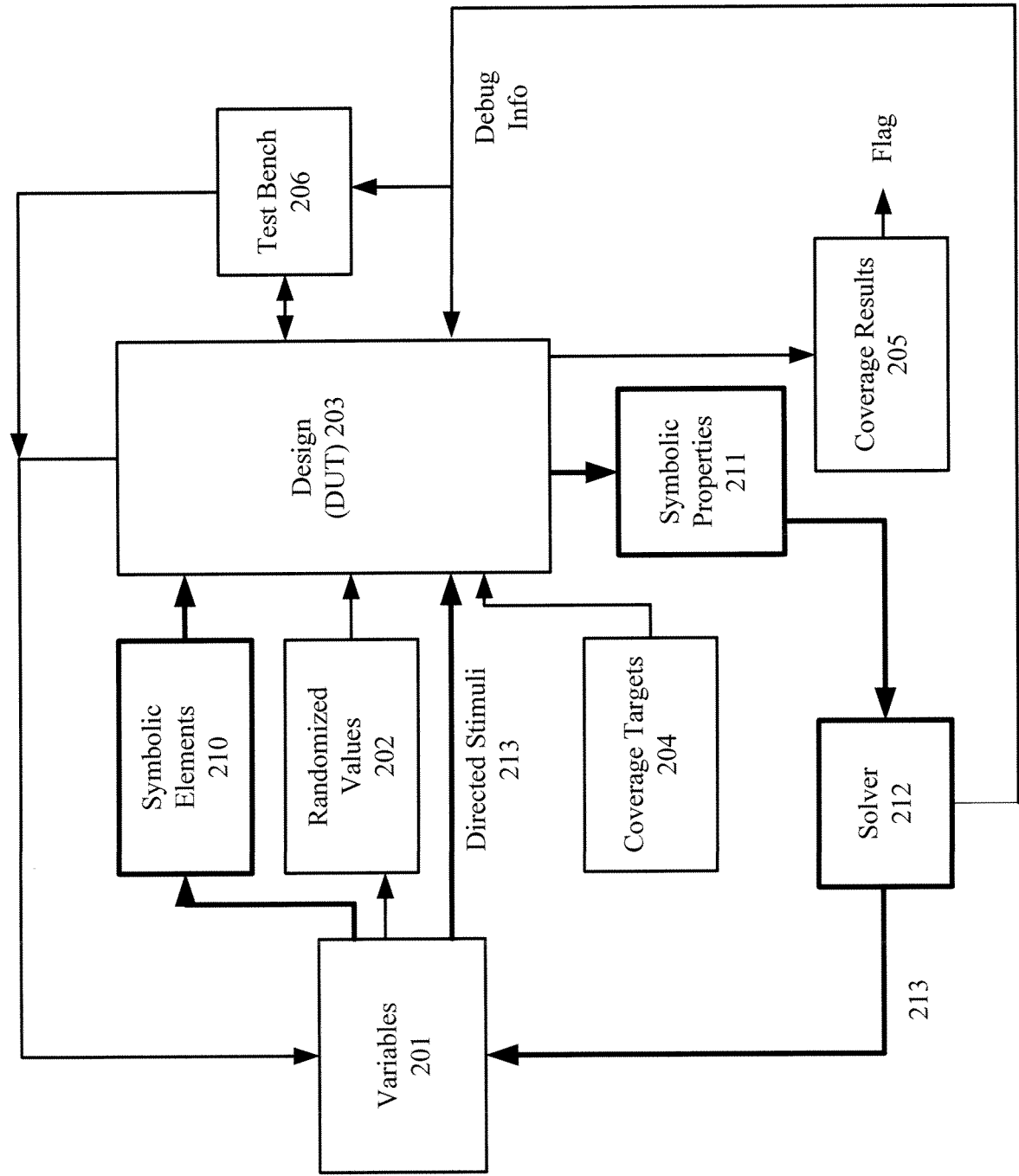


FIG. 2

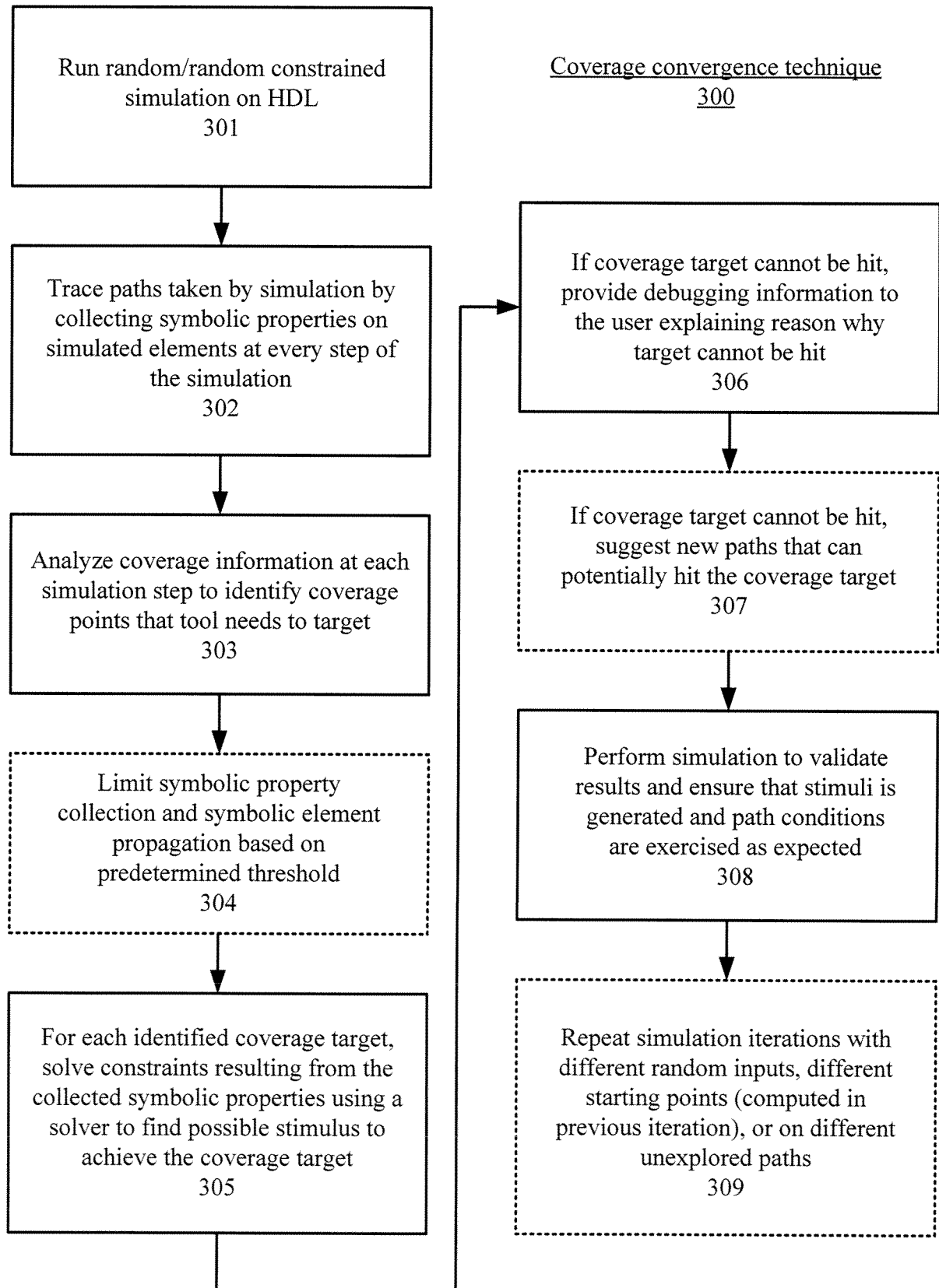


FIG. 3

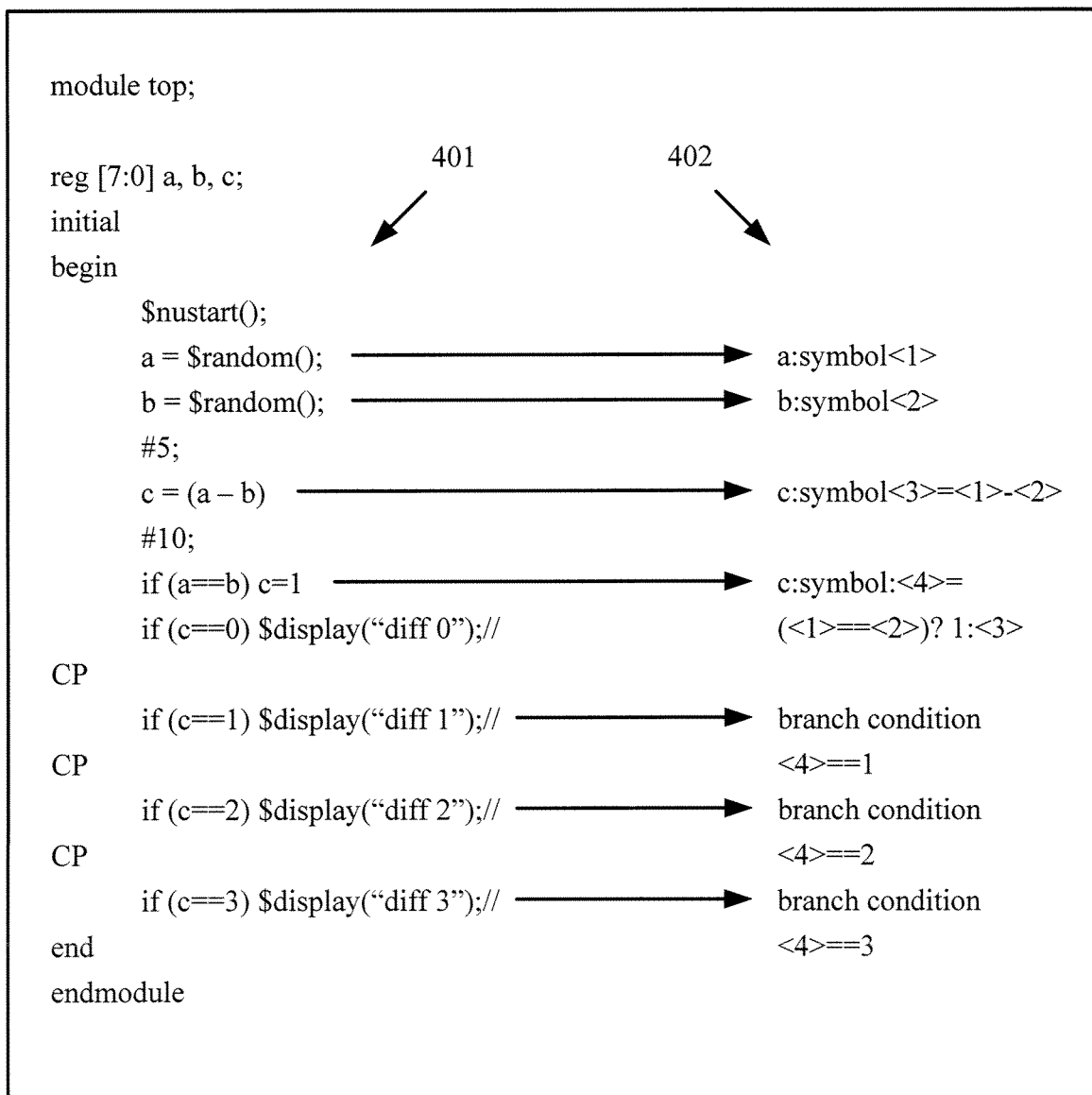


FIG. 4

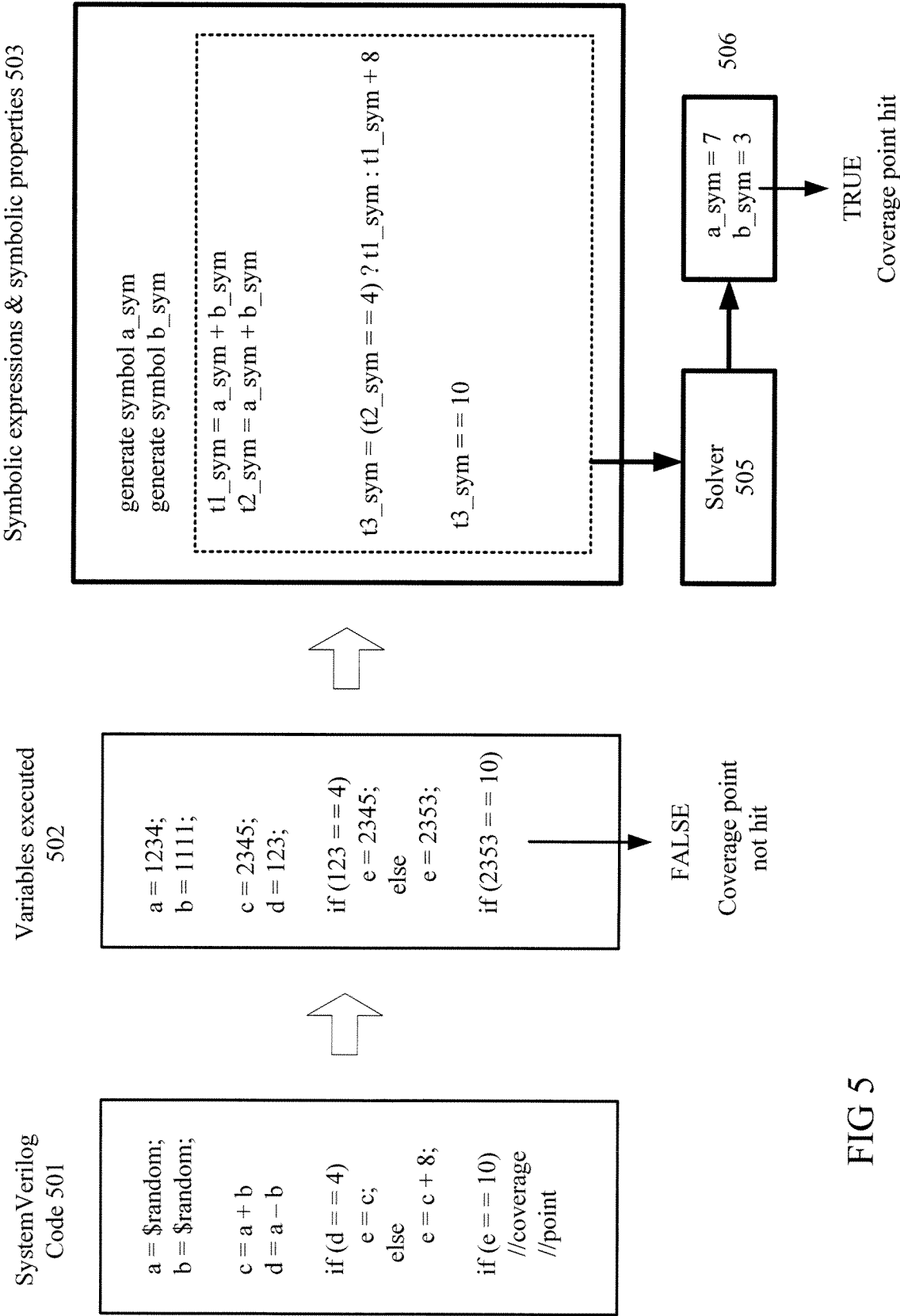


FIG 5

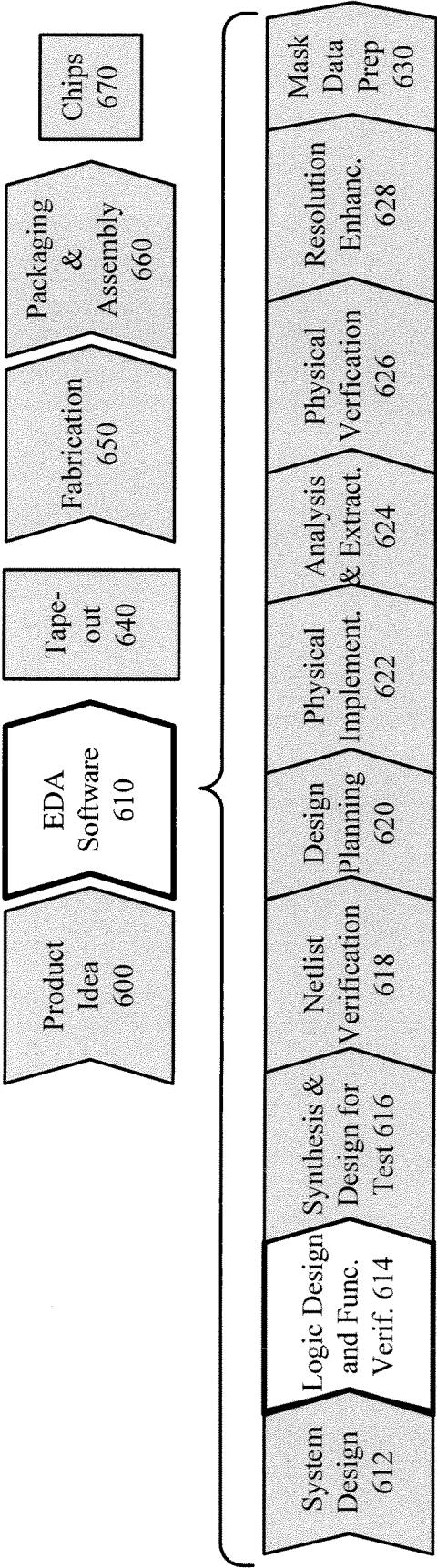


FIG. 6

A. CLASSIFICATION OF SUBJECT MATTER**G06F 17/50(2006.01)i, G06F 9/455(2006.01)i, G06F 11/36(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 17/50; G11B 27/00; G06F 11/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: coverage, verification, design, integrated circuit and increase.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005-0278576 A1 (AMIR HEKMATPOUR) 15 December 2005 See abstract; pages 1-10; claims 1-26; and figures 1-7.	1-18
A	WO 2005-109257 A2 (CADENCE DESIGN SYSTEMS, INC. et al.) 17 November 2005 See abstract; claims 1-20; and figures 1-24.	1-18
A	WO 2008-134215 A1 (INTERNATIONAL BUSINESS MACHINES CO.) 06 November 2008 See abstract; claims 1-30; and figures 1-4.	1-18



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

27 APRIL 2012 (27.04.2012)

Date of mailing of the international search report

04 MAY 2012 (04.05.2012)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2012/027589

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