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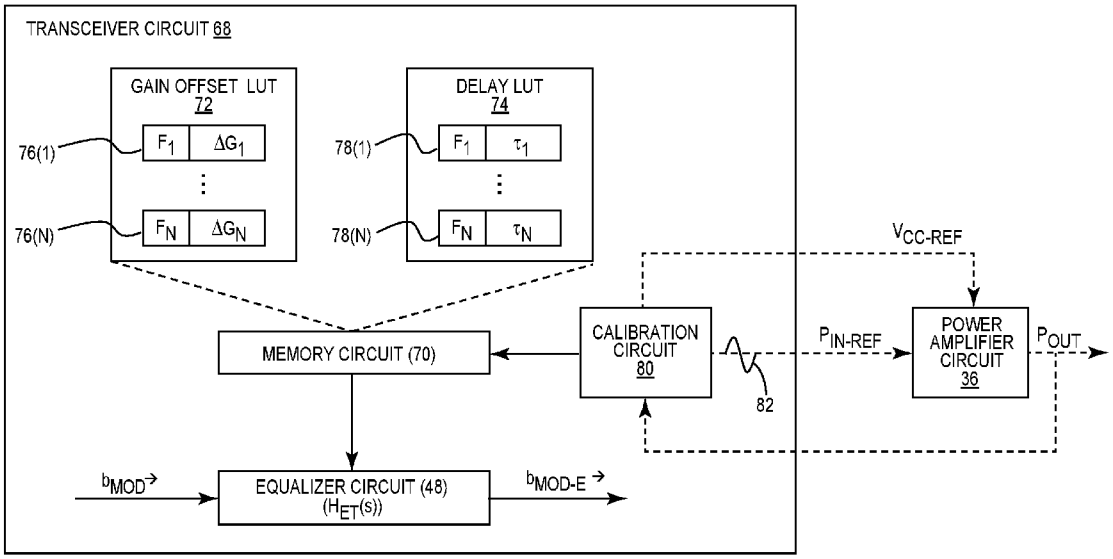

FIG. 5

(57) Abstract: A transceiver circuit (68) generates a radio frequency (RF) signal from a time-variant modulation vector and a power amplifier circuit (36) amplifies the RF signal based on a modulated voltage. The transceiver circuit (68) is configured to apply an equalization filter to the time¬ variant modulation vector to thereby compensate for a voltage distortion filter created at the output stage of the power amplifier circuit (36). In embodiments disclosed herein, a calibration circuit can be configured to calibrate the equalization filter across multiple frequencies within a modulation bandwidth of the power amplifier circuit (36) to generate a gain offset LUT (72) and a delay LUT (74). As a result, the equalization filter can be dynamically adapted to reduce undesired instantaneous excessive compression and/or spectrum regrowth resulting from the voltage distortion filter across the modulation bandwidth of the power amplifier circuit (36).

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[Continued on next page]

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EQUALIZATION FILTER CALIBRATION IN A TRANSCEIVER CIRCUIT

Related Applications

[0001] This application claims the benefit of provisional patent application serial number 63/245,139, filed September 16, 2021, provisional patent application serial number 63/303,531, filed January 27, 2022, and U.S. patent application serial number 17/737,300, filed May 5, 2022, the disclosures of which are hereby incorporated herein by reference in their entireties.

Field of the Disclosure

[0002] The technology of the disclosure relates generally to a transmission circuit that transmits a radio frequency (RF) signal modulated in a wide modulation bandwidth.

Background

[0003] Mobile communication devices have become increasingly common in current society for providing wireless communication services. The prevalence of these mobile communication devices is driven in part by the many functions that are now enabled on such devices. Increased processing capability in such devices means that mobile communication devices have evolved from being pure communication tools into sophisticated mobile multimedia centers that enable enhanced user experiences.

[0004] The redefined user experience relies on a higher data rate offered by advanced fifth generation (5G) and 5G new radio (5G-NR) technologies, which typically transmit and receive radio frequency (RF) signals in millimeter wave spectrums. Given that the RF signals are more susceptible to attenuation and interference in the millimeter wave spectrums, the RF signals are typically amplified by state-of-the-art power amplifiers to help boost the RF signals to higher power before transmission.

[0005] Envelope tracking (ET) is a power management technology designed to improve operating efficiency and/or linearity performance of the power

amplifiers. In an ET power management circuit, a power management integrated circuit (PMIC) is configured to generate a time-variant ET voltage based on a time-variant voltage envelope of the RF signals, and the power amplifiers are configured to amplify the RF signals based on the time-variant ET voltage. Understandably, the better the time-variant ET voltage is aligned with the time-variant voltage envelope in time and amplitude, the better the performance (e.g., efficiency and/or linearity) that can be achieved at the power amplifiers. However, the time-variant ET voltage can become misaligned from the time-variant voltage envelope in time and/or amplitude due to a range of factors (e.g., group delay, impedance mismatch, etc.). As such, it is desirable to always maintain good alignment between the time-variant voltage and the time-variant voltage envelope and across a wide modulation bandwidth.

Summary

[0006] Embodiments of the disclosure relate to equalization filter calibration in a transceiver circuit. The transceiver circuit generates a radio frequency (RF) signal(s) from a time-variant modulation vector and a power amplifier circuit(s) amplifies the RF signal(s) based on a modulated voltage and provides the amplified RF signal(s) to a coupled RF front-end circuit (e.g., filter/multiplexer circuit). Notably, when the power amplifier circuit(s) is coupled to the RF front-end circuit, an output reflection coefficient (e.g., S_{22}) of the power amplifier circuit(s) can interact with an input reflection coefficient (e.g., S_{11}) of the RF front-end circuit to create a voltage distortion filter on an output stage of the power amplifier circuit(s), which can cause unwanted distortion in the RF signal(s). In this regard, the transceiver circuit is configured to apply an equalization filter to the time-variant modulation vector to thereby compensate for the voltage distortion filter at the output stage of the power amplifier circuit(s). In embodiments disclosed herein, a calibration circuit can be configured to calibrate the equalization filter across multiple frequencies within a modulation bandwidth of the power amplifier circuit to generate a gain offset lookup table (LUT) and a delay LUT. As a result, the equalization filter can be dynamically adapted to

reduce undesired instantaneous excessive compression and/or spectrum regrowth resulting from the voltage distortion filter across the modulation bandwidth of the power amplifier circuit.

[0007] In one aspect, a transceiver circuit is provided. The transceiver circuit includes a memory circuit. The transceiver circuit also includes a calibration circuit. The calibration circuit is coupled to a power amplifier circuit. The calibration circuit is configured to determine and store a gain offset LUT in the memory circuit to correlate multiple calibrated frequencies within a modulation bandwidth of the power amplifier circuit with multiple gain offsets, respectively. The calibration circuit is also configured to determine and store a delay offset LUT in the memory circuit to correlate the multiple calibrated frequencies with multiple delay factors, respectively.

[0008] In another aspect, a method for calibrating an equalization filter in a transceiver circuit is provided. The method includes determining and storing a gain offset LUT to correlate a plurality of calibrated frequencies within a modulation bandwidth with a plurality of gain offsets, respectively. The method also includes determining and storing a delay offset LUT to correlate the plurality of calibrated frequencies with a plurality of delay factors, respectively.

[0009] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0010] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0011] Figure 1A is a schematic diagram of an exemplary existing transmission circuit, wherein an unwanted voltage distortion filter may be created on a power amplifier circuit when the power amplifier circuit is coupled to a radio frequency (RF) front-end circuit;

[0012] Figure 1B is a schematic diagram providing an exemplary illustration of an output stage of the power amplifier circuit in Figure 1A;

[0013] Figure 2 is a schematic diagram of an exemplary equivalent model providing an exemplary illustration of the unwanted voltage distortion filter created by a coupling between the power amplifier circuit and the RF front-end circuit 14 in Figure 1A;

[0014] Figure 3 is a schematic diagram of an exemplary transmission circuit configured to compensate for the unwanted voltage distortion filter in the existing transmission circuit of Figure 1A based on an equalization filter;

[0015] Figures 4A-4C are graphic diagrams providing exemplary illustrations as to why the equalization filter in Figure 3 must be calibrated across a modulation bandwidth of the transmission circuit;

[0016] Figure 5 is a schematic diagram of an exemplary transceiver circuit that can be configured according to embodiments of the present disclosure to calibrate the equalization filter across a modulation bandwidth of the transmission circuit of Figure 3;

[0017] Figure 6 is a flowchart of an exemplary calibration process that can be employed by the transceiver circuit of Figure 5 to calibrate the equalization filter;

[0018] Figure 7 is a flowchart of an exemplary process that can be employed by the transceiver circuit of Figure 5 to determine a gain offset lookup table (LUT) as part of the calibration process of Figure 6;

[0019] Figures 8A-8B are graphic diagrams illustrating impacts of the equalization filter calibration as performed based on the processes of Figures 6 and 7;

[0020] Figure 9 is a flowchart of an exemplary process that can be employed by the transceiver circuit of Figure 5 to determine a gain offset LUT according to an alternative embodiment of the present disclosure; and

[0021] Figure 10 is a flowchart of an exemplary process that can be employed by the transceiver circuit of Figure 5 to determine a delay LUT as part of the calibration process of Figure 6.

Detailed Description

[0022] The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0023] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0024] It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element

is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

[0025] Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

[0026] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0027] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0028] Embodiments of the disclosure relate to equalization filter calibration in a transceiver circuit. The transceiver circuit generates a radio frequency (RF) signal(s) based on a time-variant modulation vector and a power amplifier circuit(s) amplifies the RF signal(s) based on a modulated voltage and provides the amplified RF signal(s) to a coupled RF front-end circuit (e.g., filter/multiplexer circuit). Notably, when the power amplifier circuit(s) is coupled to the RF front-end circuit, an output reflection coefficient (e.g., S_{22}) of the power amplifier

circuit(s) can interact with an input reflection coefficient (e.g., S_{11}) of the RF front-end circuit to create a voltage distortion filter on an output stage of the power amplifier circuit(s), which can cause unwanted distortion in the RF signal(s). In this regard, the transceiver circuit is configured to apply an equalization filter to the time-variant modulation vector to thereby compensate for the voltage distortion filter at the output stage of the power amplifier circuit(s). In embodiments disclosed herein, a calibration circuit can be configured to calibrate the equalization filter across multiple frequencies within a modulation bandwidth of the power amplifier circuit to generate a gain offset lookup table (LUT) and a delay LUT. As a result, the equalization filter can be dynamically adapted to reduce undesired instantaneous excessive compression and/or spectrum regrowth resulting from the voltage distortion filter across the modulation bandwidth of the power amplifier circuit.

[0029] Before discussing the transceiver circuit and the calibration process according to the present disclosure, starting at Figure 5, a brief discussion is first provided to help explain why there is a need to calibrate an equalization filter used in an existing transmission circuit for suppressing an unwanted voltage distortion filter.

[0030] Figure 1A is a schematic diagram of an exemplary existing transmission circuit 10, wherein an unwanted voltage distortion filter $H_{IV}(s)$ presented to a power amplifier circuit 12 can cause a memory distortion in the power amplifier circuit 12 when the power amplifier circuit 12 is coupled to an RF front-end circuit 14. Notably, in the unwanted voltage distortion filter $H_{IV}(s)$, "s" is a notation of Laplace transform.

[0031] The existing transmission circuit 10 includes a transceiver circuit 16, an ETIC 18, and a transmitter circuit 20, which can include an antenna(s) (not shown) as an example. The transceiver circuit 16 is configured to generate an RF signal 22 having a time-variant input power P_{IN} and provide the RF signal 22 to the power amplifier circuit 12. The transceiver circuit 16 is also configured to generate a time-variant target voltage V_{TGT}, which tracks the time-variant input power P_{IN} of the RF signal 22. The ETIC 18 is configured to generate a

modulated voltage V_{CC} that tracks the time-variant target voltage V_{TGT} and provides the modulated voltage V_{CC} to the power amplifier circuit 12. Accordingly, the power amplifier circuit 12 can amplify the RF signal 22 to a time-variant output power P_{OUT} as a function of a time-variant output voltage V_{OUT}. The power amplifier circuit 12 then provides the amplified RF signal 22 to the RF front-end circuit 14. The RF front-end circuit 14 may be a filter circuit that performs further frequency filtering on the amplified RF signal 22 before providing the amplified RF signal 22 to the transmitter circuit 20 for transmission.

[0032] Figure 1B is a schematic diagram providing an exemplary illustration of an output stage 24 of the power amplifier circuit 12 in Figure 1A. Common elements between Figures 1A and 1B are shown therein with common element numbers and will not be re-described herein.

[0033] The output stage 24 can include at least one transistor 26, such as a bipolar junction transistor (BJT) or a complementary metal-oxide semiconductor (CMOS) transistor. Taking the BJT as an example, the transistor 26 can include a base electrode B, a collector electrode C, and an emitter electrode E. The base electrode B is configured to receive a bias voltage V_{BIAS} and the collector electrode C is configured to receive the modulated voltage V_{CC}. The collector electrode C is also coupled to the RF front-end circuit 14 and configured to output the amplified RF signal 22 at the output voltage V_{OUT}. In this regard, the output voltage V_{OUT} can be a function of the modulated voltage V_{CC}. Understandably, the power amplifier circuit 12 will operate with good efficiency and linearity when the time-variant modulated voltage V_{CC} is aligned with the time-variant input power P_{IN}.

[0034] Figure 2 is a schematic diagram of an exemplary equivalent model 28 providing an exemplary illustration of the voltage distortion filter $H_{IV}(s)$ created by a coupling between the power amplifier circuit 12 and the RF front-end circuit 14 in the existing transmission circuit 10 of Figure 1A. Elements in Figures 1A and 1B are referenced in Figure 2 without being re-described herein.

[0035] In the equivalent model 28, V_{PA} and Z_{PA} represent the output stage 24 of the power amplifier circuit 12 and an inherent impedance of the power

amplifier circuit 12, respectively, and Z_{11} represents an inherent impedance associated with an input port of the RF front-end circuit 14. Herein, V_{OUT} represents an output voltage associated with the RF signal 22 before the power amplifier circuit 12 is coupled to the RF front-end circuit 14, and V'_{OUT} represents an output voltage associated with the RF signal 22 after the power amplifier circuit 12 is coupled to the RF front-end circuit 14. Hereinafter, the output voltages V_{OUT} and V'_{OUT} are referred to as "non-coupled output voltage" and "coupled output voltage," respectively, for distinction.

[0036] A Laplace transform representative of the coupled output voltage V'_{OUT} can be expressed in equation (Eq. 1) below.

$$V'_{OUT}(s) = \frac{V_{OUT}(s)*[1- T_{PA}(s)]*[1+ T_I(s)]}{2*[1- T_{PA}(s)*T_I(s)]} = V_{OUT}(s)*H_{IV}(s) \qquad \text{(Eq. 1)}$$

$$H_{IV}(s) = \frac{[1- T_{PA}(s)]*[1+ T_I(s)]}{2*[1- T_{PA}(s)*T_I(s)]}$$

[0037] In the equation (Eq. 1) above, $\boldsymbol{T}_{PA}(s)$ represents a reflection coefficient looking back into the output stage 24 of the power amplifier circuit 12 and $\boldsymbol{T}_I(s)$ represents a reflection coefficient looking into the RF front-end circuit 14. Notably, $\boldsymbol{T}_{PA}(s)$ and $\boldsymbol{T}_I(s)$ are complex filters containing amplitude and phase information. In this regard, the $\boldsymbol{T}_{PA}(s)$, the $\boldsymbol{T}_I(s)$, and, therefore, the voltage distortion filter $H_{IV}(s)$ are dependents of such factors as modulation bandwidth, RF spectrum, and/or voltage standing wave ratio (VSWR).

[0038] The equation (Eq. 1) shows that the coupled output voltage V'_{OUT} will be altered from the non-coupled output voltage V_{OUT} by the voltage distortion filter $H_{IV}(s)$ when the power amplifier circuit 12 is coupled to the RF front-end circuit 14. As a result, the coupled output voltage V'_{OUT} may become misaligned from the modulated voltage V_{CC}, thus causing unwanted distortion in the RF signal 22.

[0039] Notably, it is possible to modify the modulated voltage V_{CC} to compensate for the voltage distortion filter $H_{IV}(s)$ to thereby reduce or eliminate

the difference between the non-coupled output voltage V_{OUT} and the coupled output voltage V'_{OUT}. As a result, it is possible to reduce undesired instantaneous excessive compression and/or spectrum regrowth resulting from the voltage distortion filter $H_{IV}(s)$.

[0040] In this regard, Figure 3 is a schematic diagram of an exemplary transmission circuit 30 configured to compensate for the unwanted voltage distortion filter $H_{IV}(s)$ in the existing transmission circuit 10 of Figure 1A based on an equalization filter $H_{ET}(s)$. The transmission circuit 30 is configured to transmit an RF signal 32 modulated in a wide range of modulation bandwidths. In a non-limiting example, the RF signal 32 can be modulated in a modulation bandwidth of 200 MHz or higher and transmitted in a millimeter wave RF spectrum.

[0041] The transmission circuit 30 includes a transceiver circuit 34, a power amplifier circuit 36, and an ETIC 38. The power amplifier circuit 36 is coupled to a transmitter circuit 40 via an RF front-end circuit 42. In a non-limiting example, the RF front-end circuit 42 can include one or more of a filter circuit and a multiplexer circuit (not shown). The filter circuit may be configured to include a filter network, such as an acoustic filter network with a sharp cutoff frequency. The power amplifier circuit 36 may be identical to or functionally equivalent to the power amplifier circuit 12 in Figure 1B. As such, the power amplifier circuit 36 may also include the output stage 24 as in the power amplifier circuit 12.

[0042] The transceiver circuit 34 includes a signal processing circuit 44 and a target voltage circuit 46. The signal processing circuit 44 is configured to generate the RF signal 32 from a time-variant modulation vector $b_{MOD}^{\rightarrow}$. The time-variant modulation vector $b_{MOD}^{\rightarrow}$ may be generated by a digital baseband circuit (not shown) in the transceiver circuit 34 and includes both in-phase (I) and quadrature (Q) components. The target voltage circuit 46 is configured to detect a time-variant amplitude envelope $\sqrt{I^2+Q^2}$ of the RF signal 32 from the time-variant modulation vector $b_{MOD}^{\rightarrow}$. Accordingly, the target voltage circuit 46 can generate a modulated target voltage V_{TGT} based on the detected time-variant amplitude envelope $\sqrt{I^2+Q^2}$.

[0043] The ETIC 38 is configured to generate a modulated voltage V_{CC} based on the modulated target voltage V_{TGT} and provide the modulated voltage V_{CC} to the power amplifier circuit 36. The power amplifier circuit 36, in turn, amplifies the RF signal 32 to an output voltage V_{OUT} based on the modulated voltage V_{CC} for transmission via the RF front-end circuit 42 and the transmitter circuit 40.

[0044] As previously described, the output voltage V_{OUT} is a function of the modulated voltage V_{CC}. In this regard, it is possible to reduce or even eliminate the difference between the non-coupled output voltage V_{OUT} and the coupled output voltage V'_{OUT} by generating the modulated voltage V_{CC} to compensate for the voltage distortion filter $H_{IV}(s)$. Given that the ETIC 38 is configured to generate the modulated voltage V_{CC} based on the modulated target voltage V_{TGT}, it is thus possible to reduce or even eliminate the difference between the non-coupled output voltage V_{OUT} and the coupled output voltage V'_{OUT} by generating the modulated target voltage V_{TGT} to compensate for the voltage distortion filter $H_{IV}(s)$.

[0045] In this regard, the transceiver circuit 34 further includes an equalizer circuit 48. The equalizer circuit 48 is configured to apply the equalization filter $H_{ET}(s)$ to the time-variant modulation vector $b_{MOD}^{\rightarrow}$ prior to the target voltage circuit 46 generating the modulated target voltage V_{TGT}. In an embodiment, the equalization filter $H_{ET}(s)$ can be described by equation (Eq. 2) below.

$$H_{ET}(s) = H_{IQ}(s) * H_{PA}(s) * H_{IV}(s) \qquad \text{(Eq. 2)}$$

[0046] In the equation (Eq.2) above, $H_{IQ}(s)$ represents a transfer function of the signal processing circuit 44 and $H_{PA}(s)$ represents a voltage gain transfer function of the power amplifier circuit 36. In this regard, the equalization filter $H_{ET}(s)$ is configured to match a combined signal path filter that includes the transfer function $H_{IQ}(s)$, the voltage gain transfer function $H_{PA}(s)$, and the voltage distortion filter $H_{IV}(s)$.

[0047] In an embodiment, the equalizer circuit 48 applies the equalization filter $H_{ET}(s)$ to the time-variant modulation vector $b_{MOD}^{\rightarrow}$ to generate an equalized time-

variant modulation vector $b_{MOD\text{-}E}^{\rightarrow}$ and provides the equalized time-variant modulation vector $b_{MOD\text{-}E}^{\rightarrow}$ to the target voltage circuit 46. The target voltage circuit 46, in turn, detects the time-variant amplitude envelope $\sqrt{I^2+Q^2}$ from the equalized time-variant modulation vector $b_{MOD\text{-}E}^{\rightarrow}$ and generates the modulated target voltage V_{TGT} based on the detected time-variant amplitude envelope $\sqrt{I^2+Q^2}$. Since the modulated target voltage V_{TGT} is generated from the equalized time-variant modulation vector $b_{MOD\text{-}E}^{\rightarrow}$, the modulated target voltage V_{TGT}, and therefore the modulated voltage V_{CC}, will be able to compensate for the voltage distortion filter $H_{IV}(s)$, which is created on the output stage 24 of the power amplifier circuit 36 by coupling the power amplifier circuit 36 with the RF front-end circuit 42.

[0048] In an embodiment, the target voltage circuit 46 includes an amplitude detector circuit 50, an ET LUT circuit 52, and a digital-to-analog converter (DAC) 54. The amplitude detector circuit 50 is configured to detect the time-variant amplitude envelope $\sqrt{I^2+Q^2}$ from the equalized time-variant modulation vector $b_{MOD\text{-}E}^{\rightarrow}$. The ET LUT circuit 52, which can include an isogain LUT (not shown) correlating the time-variant amplitude envelope $\sqrt{I^2+Q^2}$ with various level of voltages, is configured to generate a time-variant digital target voltage V_{DTGT} based on the detected time-variant amplitude envelope $\sqrt{I^2+Q^2}$. The DAC 54 is configured to convert the time-variant digital target voltage V_{DTGT} into the modulated target voltage V_{TGT} and provide the modulated target voltage V_{TGT} to the ETIC 38.

[0049] In an embodiment, the signal processing circuit 44 can include a memory digital predistortion (mDPD) circuit 56 and a modulator circuit 58. The mDPD circuit 56 is configured to receive the time-variant modulation vector $b_{MOD\text{-}E}^{\rightarrow}$ and digitally pre-distort the time-variant modulation vector $b_{MOD\text{-}E}^{\rightarrow}$ to generate a pre-distorted time-variant modulation vector $b_{MOD\text{-}DPD}^{\rightarrow}$. The modulator circuit 58 is configured to generate the RF signal 32 from the pre-distorted time-variant modulation vector $b_{MOD\text{-}DPD}^{\rightarrow}$ and provide the RF signal 32 to the power amplifier circuit 36.

[0050] As mentioned earlier, the RF signal 32 may be modulated in a wide range of modulation bandwidth. Herein, a modulation bandwidth refers to a range of RF frequencies that the RF signal 32 may be modulated onto and/or the transmission circuit 30 is configured to handle. For example, if the RF signal 32 can be modulated between 2554 MHz and 2654 MHz, the modulation bandwidth will then be 100 MHz and a center frequency (F_C) of the modulation bandwidth will be at 2604 MHz. Accordingly, any other frequencies within the modulation bandwidth will be regarded as non-center frequencies (F_{NC}) (2554 MHz $\leqq F_{NC} <$ 2604 MHz and 2604 MHz $< F_{NC} \leqq$ 2654 MHz). Hereinafter, the modulation bandwidth of the RF signal 32 is referred to interchangeably as the modulation bandwidth of the transmission circuit 30.

[0051] In this regard, the equalization filter $H_{ET}(s)$ needs to suppress the voltage distortion filter $H_{IV}(s)$ across the entire modulation bandwidth. However, as the isogain LUT in the ET LUT circuit 52 is typically determined based on a center frequency within the modulation bandwidth, the isogain LUT in the ET LUT circuit 52 may not be able provide a constant isogain for all other frequencies within the modulation bandwidth. Accordingly, the equalization filter $H_{ET}(s)$ must be calibrated to ensure that the isogain LUT determined based on the center frequency can provide a constant isogain across all the frequencies within the modulation bandwidth.

[0052] Figures 4A-4C are graphic diagrams providing exemplary illustrations as to why the equalization filter $H_{ET}(s)$ in Figure 3 must be calibrated across a modulation bandwidth of the transmission circuit 30. Common elements between Figures 4A-4C are shown therein with common element numbers and will not be re-described herein.

[0053] Figure 4A illustrates a center-frequency LUT 60 corresponding to a center frequency F_C within the modulation bandwidth of the transmission circuit 30 and a non-center-frequency LUT 62 corresponding to a non-center frequency F_{NC} within the modulation bandwidth of the transmission circuit 30.

[0054] Figure 4B illustrates a center-frequency gain 64 provided by the center-frequency LUT 60 and a non-center-frequency gain 66 provided by the

non-center-frequency LUT 62. As illustrated, the center-frequency LUT 60 can provide a 30 dB constant gain when the RF signal 32 is modulated at the center frequency F_C and has the input power P_{IN} between -25 dBm and 3 dBm for the center frequency F_C. The non-center-frequency LUT 62, on the other hand, can provide a 29 dB constant gain when the RF signal 32 is modulated at the non-center frequency F_{NC} and has the input power P_{IN} between -25 dBm and 4 dBm. In this regard, if the ET LUT circuit 52 employs both the center-frequency LUT 60 and the non-center-frequency LUT 62, it will be possible to achieve constant gains when the RF signal 32 is modulated at both the center frequency F_C and the non-center frequency F_{NC}.

[0055] However, when the ET LUT circuit 52 employs only the center-frequency LUT 60, the non-center-frequency LUT 62 would not be able to maintain the 29 dB constant gain at the non-center-frequency F_{NC}. As illustrated in Figure 4C, the center-frequency LUT 60 in Figure 4A provides a varying gain from 29.4 dB to 30.5 dB between -25 dBm and +2 dBm but does not provide 29 dB constant gain when the RF signal 32 is modulated at the non-center-frequency F_{NC}. Hence, it is desirable to calibrate the equalization filter $H_{ET}(s)$ to ensure that the center-frequency LUT 60 can provide a constant gain across center and non-center frequencies within the modulation bandwidth of the RF signal 32.

[0056] In this regard, Figure 5 is a schematic diagram of an exemplary transceiver circuit 68 that can be configured according to embodiments of the present disclosure to calibrate the equalization filter $H_{ET}(s)$ across a modulation bandwidth of the transmission circuit of Figure 3. Common elements between Figures 3 and 5 are shown therein with common element numbers and will not be re-described herein. In an embodiment, the transceiver circuit 68 may be employed in the transmission circuit 30 to replace the transceiver circuit 34.

[0057] In an embodiment, the transceiver circuit 68 includes a memory circuit 70. The memory circuit 70, which can include such storage circuits as random-access memory (RAM), flash storage, solid-state disk (SSD), as an example, is configured to store a gain offset LUT 72 and a delay LUT 74. In a non-limiting

example, the gain offset LUT 72 includes multiple gain offset entries 76(1)-76(N), each configured to correct a respective one of multiple calibrated frequencies F_1-F_N within the modulation bandwidth with a respective one of multiple gain offsets ΔG_1-ΔG_N. Herein, the calibrated frequencies F_1-F_N include all the non-center frequencies (F_{NC}) and the center frequency (F_C) within the modulation bandwidth. In another non-limiting example, the delay LUT 74 includes multiple delay entries 78(1)-78(N), each configured to correlate a respective one of the calibrated frequencies F_1-F_N with a respective one of multiple delay factors τ_1-τ_N.

[0058] In an embodiment, the transceiver circuit 68 can be configured to include a calibration circuit 80, which can be a field-programmable gate array (FPGA), as an example. Although the calibration circuit 80, as illustrated herein, is provided inside the transceiver circuit 68, it should be appreciated that the calibration circuit 80 can be separated from the transceiver circuit 68 but coupled to the transceiver circuit 68 via, for example, a general-purpose input/output (GPIO) interface. As discussed below, the calibration circuit 80 can be configured to determine and populate the gain offset LUT 72 and the delay LUT 74 such that the equalization filter $H_{ET}(s)$ can be calibrated to cause the ET LUT circuit 52 to provide a constant gain across all the calibrated frequencies F_1-F_N based on, for example, the center-frequency LUT 60 in Figure 4A.

[0059] The calibration circuit 80 may be configured to calibrate the equalization filter $H_{ET}(s)$ based on a process. In this regard, Figure 6 is a flowchart of an exemplary calibration process 200 that can be employed by the calibration circuit 80 in the transceiver circuit 68 of Figure 5 to calibrate the equalization filter $H_{ET}(s)$.

[0060] Herein, the calibration circuit 80 is first configured to determine and store the gain offset LUT 72 that includes the gain offset entries 76(1)-76(N), with each of the gain offset entries 76(1)-76(N) configured to correlate a respective one of the calibrated frequencies F_1-F_N within the modulation bandwidth with a respective one of the gain offsets ΔG_1-ΔG_N (step 202). Next, the calibration circuit 80 is configured to determine and store the delay LUT 74 that includes the delay entries 78(1)-78(N), with each of the delay entries 78(1)-78(N) configured

to correlate a respective one of the calibrated frequencies F_1-F_N with a respective one of the delay factors τ_1-τ_N (step 204).

[0061] In an embodiment, the calibration circuit 80 may determine and store the gain offset LUT 72 (step 202) in the memory circuit 70 based on a process. In this regard, Figure 7 is a flowchart of an exemplary process 206 that can be employed by the calibration circuit 80 in the transceiver circuit 68 of Figure 5 to determine the gain offset LUT 72 as part of the calibration process 200 of Figure 6. Elements in Figure 5 are referenced in conjunction with the discussion of Figure 7 and will not be re-described herein.

[0062] Herein, the calibration circuit 80 is configured to determine a minimum reference voltage $V_{CC\text{-}REF}$ and a minimum reference input power $P_{IN\text{-}REF}$ based on an efficiency target, a noise target, and/or a linearity target of the power amplifier circuit 36 (step 208). In other words, the minimum reference voltage $V_{CC\text{-}REF}$ and the minimum reference input power $P_{IN\text{-}REF}$ can be determined empirically to achieve a desired trade-off between the efficiency target, the noise target, and/or the linearity target of the power amplifier circuit 36. Although the calibration circuit 80 is configured herein to determine a minimum reference input power $P_{IN\text{-}REF}$, it should be appreciated that it is also possible to replace the input power $P_{IN\text{-}REF}$ with a corresponding output power.

[0063] The calibration circuit 80 then determines a reference frequency F_{REF} among the calibrated frequencies F_1-F_N within the modulation bandwidth of the power amplifier circuit 36 (step 210). In a non-limiting example, the reference frequency F_{REF} can be the center frequency F_C among the calibrated frequencies F_1-F_N.

[0064] Next, the calibration circuit 80 determines a reference target voltage ($V_{TGT\text{-}REF}$) based on an expected root-mean-square (RMS) of the modulated voltage V_{CC} (e.g., 2.5 V) to be provided to the power amplifier circuit 36 for amplifying the RF signal 32 in the transmission circuit 30 of Figure 3 (step 212).

[0065] Next, the calibration circuit 80 selects a calibrated frequency F_i among the calibrated frequencies F_1-F_N within the modulation bandwidth (step 214). The calibration circuit 80 then determines a respective gain G_i of the power amplifier

circuit 36 when the power amplifier circuit 36 amplifies a test signal 82 that is generated at the selected calibrated frequency F_i and in the minimum reference input power P_{IN-REF} based on the minimum reference voltage V_{CC-REF} (step 216). Notably, the test signal 82 may be generated by the calibration circuit 80 or a separate signal generator (not shown). In a non-limiting example, the calibration circuit 80 can measure an output power P_{OUT} of the power amplifier circuit 36 and determine the respective reference gain G_{REF} based on the measured output power P_{OUT} and the determined minimum reference input power P_{IN-REF}. Subsequently, the calibration circuit 80 can determined a respective modulated voltage V_{CCj} ($1 \leqq j \leqq M$) and a respective input power P_{INj} ($1 \leqq j \leqq M$) that can cause the power amplifier circuit 36 to have the respective gain G_i when amplifying the RF signal 32 at the selected calibrated frequency F_i (step 218). Herein, M may be identical to or different from N. Accordingly, the calibration circuit 80 can store the respective modulated voltage V_{CCj} and the respective input power P_{INj} in a temporary voltage LUT (not shown) in the memory circuit 70 (step 220). The calibration circuit 80 is configured to repeat steps 214-220 for each of the calibrated frequencies F_1-F_N.

[0066] With continuing reference to Figure 7, the calibration circuit 80 again selects a calibrated frequency F_i ($1 \leqq i \leqq N$) among the calibrated frequencies F_1-F_N within the modulation bandwidth (step 222). The calibration circuit 80 then determines a respective adjusted input power $P_{IN-ADJi}$ ($1 \leqq i \leqq N$) relative to an input power P_{INj} ($1 \leqq j \leqq M$) in the temporary voltage LUT associated with a modulated voltage V_{CCj} that is equal to the reference target voltage $V_{TGT-REF}$ (step 224). Subsequently, the calibration circuit 80 determines a respective gain offset ΔG_i ($1 \leqq i \leqq N$) between a respective adjusted input power at the reference frequency F_{REF} and the respective adjusted input power $P_{IN-ADJi}$ at the selected calibrated frequency F_i (step 226). The calibration circuit 80 then stores the selected calibrated frequency Fi in association with the respective gain offset ΔG_i in the gain offset LUT 72 (step 228). Notably, the calibration circuit 80 is configured to repeat steps 222-228 for each of the calibrated frequencies F_1-F_N.

[0067] With reference back to Figure 5, for each of the calibrated frequencies F_1-F_N, the equalizer circuit 48 is configured to generate the equalization filter HET(s) based on the gain offset LUT 72 and apply the equalization filter $H_{ET}(s)$ to the time-variant modulation vector $b_{MOD}^{\rightarrow}$ to generate the equalized time-variant modulation vector $b_{MOD\text{-}E}^{\rightarrow}$. Figures 8A-8B are graphic diagrams illustrating an impact of the equalization filter calibration as performed based on the process 200 of Figure 6 and the process 206 of Figure 7.

[0068] Figure 8A illustrates a center-frequency LUT 84 corresponding to a center frequency F_C among the calibrated frequencies F_1-F_N and a non-center-frequency LUT 86 corresponding to a non-center frequency F_{NC} among the calibrated frequencies F_1-F_N. Notably, both the center-frequency LUT 84 and the non-center-frequency LUT 86 are both based on the same minimum reference voltage $V_{CC\text{-}REF}$ and the same minimum reference input power $P_{IN\text{-}REF}$. The center-frequency LUT 84 will be stored in the ET LUT circuit 52 in the transmission circuit 30 for generating the time-variant digital target voltage V_{DTGT} from the detected time-variant amplitude envelope $\sqrt{I^2+Q^2}$. The non-center-frequency LUT 86, on the other hand, is not stored in the ET LUT circuit 52 and can be seen as a "virtual" LUT. The equalization filter $H_{ET}(s)$ can use a corresponding gain offset ΔG_i ($1 \leqq i \leqq N$) of the non-center frequency F_{NC} to superimpose the non-center-frequency LUT 86 on the center-frequency LUT 84. As can be visualized in Figure 8A, it is equivalent to left-shifting the non-center-frequency LUT 86 to overlap with the center-frequency LUT 84. As a result, as illustrated in Figure 8B, a center-frequency gain 88 and a non-center-frequency gain 90 are both relatively constant.

[0069] In an embodiment, the calibration circuit 80 may determine and store the gain offset LUT 72 (step 202) in the memory circuit 70 based on an alternative process. In this regard, Figure 9 is a flowchart of an exemplary process 230 that can be employed by the calibration circuit 80 in the transceiver circuit 68 of Figure 5 to determine the gain offset LUT 72 according to another embodiment of the present disclosure. Elements in Figure 5 are referenced in conjunction with the discussion of Figure 9 and will not be re-described herein.

[0070] Herein, the calibration circuit 80 is configured to determine a reference voltage $V_{CC\text{-}REF}$ and a reference input power $P_{IN\text{-}REF}$ based on an efficiency target and/or a noise target of the power amplifier circuit 36 (step 232). In other words, the reference voltage $V_{CC\text{-}REF}$ and the reference input power $P_{IN\text{-}REF}$ can be determined empirically to achieve a desired trade-off between the efficiency target and the noise target of the power amplifier circuit 36. Although the calibration circuit 80 is configured herein to determine a reference input power $P_{IN\text{-}REF}$, it should be appreciated that it is also possible to replace the reference input power $P_{IN\text{-}REF}$ with a corresponding reference output power.

[0071] The calibration circuit 80 then determines a reference frequency F_{REF} among the calibrated frequencies F_1-F_N within the modulation bandwidth of the power amplifier circuit 36 (step 234). In a non-limiting example, the reference frequency F_{REF} can be the center frequency F_C among the calibrated frequencies F_1-F_N.

[0072] Next, the calibration circuit 80 determines a reference target voltage ($V_{TGT\text{-}REF}$) based on an expected RMS of the modulated voltage V_{CC} (e.g., 2.5 V) to be provided to the power amplifier circuit 36 for amplifying the RF signal 32 in the transmission circuit 30 of Figure 3 (step 236).

[0073] Next, the calibration circuit 80 selects a calibrated frequency F_i among the calibrated frequencies F_1-F_N within the modulation bandwidth (step 238). The calibration circuit 80 determines a respective gain G_i ($1 \leqq i \leqq N$) of the power amplifier circuit 36 when the power amplifier circuit 36 amplifies the test signal 82 that is generated at the selected calibrated frequency F_i and in the reference input power $P_{IN\text{-}REF}$ based on the reference voltage $V_{CC\text{-}REF}$ (step 240).

[0074] The calibration circuit 80 then adjusts the respective gain G_i based on a determined compression gain G_{CMP} to determine a compressed reference gain $G_{REF\text{-}CMP}$ (step 242). Notably, the calibration circuit 80 may determine compression gain G_{CMP} empirically to achieve a desired linearity target of the power amplifier circuit 36.

[0075] The calibration circuit 80 then determines a respective modulated voltage V_{CCj} ($1 \leqq j \leqq M$) and a respective input power P_{INj} ($1 \leqq j \leqq M$) that will

cause the power amplifier circuit 36 to have the compressed reference gain $G_{REF-CMP}$ when amplifying the test signal 82 at the selected calibrated frequency F_i (step 244). Herein, M may be identical to or different from N. Accordingly, the calibration circuit 80 can store the respective modulated voltage V_{CCj} and the respective input power P_{INj} in a temporary voltage LUT (not shown) in the memory circuit 70 (step 246). The calibration circuit 80 is configured to repeat steps 238-246 for each of the calibrated frequencies F_1-F_N.

[0076] With continuing reference to Figure 9, the calibration circuit 80 selects a calibrated frequency F_i ($1 \leqq i \leqq N$) among the calibrated frequencies F_1-F_N within the modulation bandwidth (step 248). The calibration circuit 80 then determines a respective adjusted input power $P_{IN-ADJi}$ ($1 \leqq i \leqq N$) relative to an input power P_{INj} ($1 \leqq j \leqq M$) in the temporary voltage LUT associated with a modulated voltage V_{CCj} ($1 \leqq j \leqq M$) that is equal to the reference target voltage $V_{TGT-REF}$ (step 250).

[0077] Subsequently, the calibration circuit 80 determines a respective gain offset ΔG_i ($1 \leqq i \leqq N$) between a respective adjusted input power at the reference frequency F_{REF} and the respective adjusted input power $P_{IN-ADJi}$ at the selected calibrated frequency F_i (step 252). The calibration circuit 80 then stores the selected calibrated frequency Fi in association with the respective gain offset ΔG_i in the gain offset LUT 72 (step 254). Notably, the calibration circuit 80 is configured to repeat steps 248-254 for each of the calibrated frequencies F_1-F_N.

[0078] In an embodiment, the calibration circuit 80 may determine and store the delay LUT 74 (step 204) in the memory circuit 70 based on a process. In this regard, Figure 10 is a flowchart of an exemplary process 256 that can be employed by the transceiver circuit 68 of Figure 5 to determine the delay LUT 74 as part of the calibration process 200 of Figure 6. Elements in Figure 5 are referenced in conjunction with the discussion of Figure 10 and will not be re-described herein.

[0079] Herein, the calibration circuit 80 first determines an arbitrary delay offset Δt (step 258). Next, the calibration circuit 80 selects a calibrated frequency

F_i ($1 \leqq i \leqq N$) among the calibrated frequencies F_1-F_N within the modulation bandwidth (step 260). The calibration circuit 80 then determines an arbitrary delay factor τ (step 264). The calibration circuit 80 then measures a pair of output powers P_{OUT1}, P_{OUT2} of the power amplifier circuit 36 when the power amplifier circuit 36 amplifies the test signal 82 that is generated at the selected calibrated frequency F_i and delayed by $\tau \pm \Delta t$, respectively (step 264).

[0080] The calibration circuit 80 checks whether the pair of output powers P_{OUT1} and P_{OUT2} are equal (step 266). In an embodiment, the calibration circuit 80 may treat the pair of output powers P_{OUT1} and P_{OUT2} as being equal if a difference between the pair of output powers P_{OUT1} and P_{OUT2} is smaller than a predefined threshold.

[0081] If the pair of output powers P_{OUT1} and P_{OUT2} are equal, the calibration circuit 80 stores the selected calibrated frequency F_i in association with arbitrary delay factor τ in the delay LUT 74 (step 268). Otherwise, the calibration circuit 80 will return to step 262 and determine a new arbitrary delay factor τ. The calibration circuit 80 may adjust (e.g., increase) the predefined threshold in case the pair of output powers P_{OUT1} and P_{OUT2} remain unequal after several iterations. Notably, the calibration circuit 80 is configured to repeat steps 260-268 for each of the calibrated frequencies F_1-F_N.

[0082] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A transceiver circuit comprising:
a memory circuit; and
a calibration circuit coupled to a power amplifier circuit and configured to:
determine and store a gain offset lookup table (LUT) in the memory circuit to correlate a plurality of calibrated frequencies within a modulation bandwidth of the power amplifier circuit with a plurality of gain offsets, respectively; and
determine and store a delay offset LUT in the memory circuit to correlate the plurality of calibrated frequencies with a plurality of delay factors, respectively.

2. The transceiver circuit of claim 1, wherein each of the plurality of gain offsets is determined relative to a reference frequency within the modulation bandwidth.

3. The transceiver circuit of claim 2, wherein the reference frequency corresponds to a center frequency of the modulation bandwidth.

4. The transceiver circuit of claim 1, wherein the calibration circuit is further configured to:
determine a minimum reference voltage and a minimum reference input power;
determine a reference frequency among the plurality of calibrated frequencies within the modulation bandwidth;
determine a reference target voltage based on an expected root-mean-square (RMS) of a modulated voltage to be provided to the power amplifier circuit for amplifying a radio frequency (RF) signal; and
for each of the plurality of calibrated frequencies:

determine a respective gain of the power amplifier circuit that amplifies a test signal generated at the calibrated frequency and in the determined minimum reference input power based on the determined minimum reference voltage;

determine a respective modulated voltage and a respective input power that cause the power amplifier circuit to have the respective gain when amplifying the test signal at the calibrated frequency; and

store the respective modulated voltage in association with the respective input power in a temporary voltage LUT.

5. The transceiver circuit of claim 4, wherein the calibration circuit is further configured to determine the minimum reference voltage and the minimum reference input power based on a trade-off between one or more of:

an efficiency target of the power amplifier circuit;

a noise target of the power amplifier circuit; and

a linearity target of the power amplifier circuit.

6. The transceiver circuit of claim 4, wherein, for each of the plurality of calibrated frequencies, the calibration circuit is further configured to:

determine a respective adjusted input power relative to an input power in the temporary voltage LUT associated with a modulated voltage that is equal to the reference target voltage;

determine a respective one of the plurality of gain offsets between a respective adjusted input power at the reference frequency and the respective adjusted input power at the calibrated frequency; and

store the respective calibrated frequency in association with the respective one of the plurality of gain offsets in the gain offset LUT.

7. The transceiver circuit of claim 1, wherein the calibration circuit is further configured to:

determine a reference voltage and a reference input power;

determine a reference frequency among the plurality of calibrated frequencies within the modulation bandwidth;

determine a reference target voltage based on an expected root-mean-square (RMS) of a modulated voltage to be provided to the power amplifier circuit for amplifying a radio frequency (RF) signal; and

for each of the plurality of calibrated frequencies:

determine a respective gain of the power amplifier circuit that amplifies a test signal generated at the calibrated frequency and in the determined reference input power based on the determined reference voltage;

adjust the respective gain based on a determined compression gain to determine a compressed gain;

determine a respective modulated voltage and a respective input power that will cause the power amplifier circuit to have the compressed gain when amplifying the test signal at the calibrated frequency; and

store the respective modulated voltage and the respective input power in a temporary voltage LUT.

8. The transceiver circuit of claim 7, wherein the calibration circuit is further configured to determine the reference voltage and the reference input power based on a trade-off between one or more of:

an efficiency target of the power amplifier circuit; and

a noise target of the power amplifier circuit.

9. The transceiver circuit of claim 7, wherein, for each of the plurality of calibrated frequencies, the calibration circuit is further configured to:

determine a respective adjusted input power relative to an input power in the temporary voltage LUT associated with a modulated voltage that is equal to the reference target voltage;

determine a respective one of the plurality of gain offsets between a respective input power at the reference frequency and the respective input power at the calibrated frequency; and

store the calibrated frequency in association with the respective one of the plurality of gain offsets in the gain offset LUT.

10. The transceiver circuit of claim 1, wherein, for each of the plurality of calibrated frequencies, the calibration circuit is further configured to:

determine an arbitrary delay factor;

measure a pair of output powers of the power amplifier circuit when amplifying a test signal generated at the respective calibrated frequency and delay by the arbitrary delay factor minus an arbitrary delay offset and the arbitrary delay factor plus the arbitrary delay offset; and

store the respective calibrated frequency in association with the arbitrary delay factor in the delay LUT in response to the pair of output powers being equal.

11. The transceiver circuit of claim 10, wherein the calibration circuit is further configured to:

determine a new arbitrary delay factor in response to the pair of output powers being unequal;

measure a new pair of output powers of the power amplifier circuit when amplifying the test signal generated at the respective calibrated frequency and delay by the new arbitrary delay factor minus the arbitrary delay offset and the new arbitrary delay factor plus the arbitrary delay offset; and

store the respective calibrated frequency in association with the new arbitrary delay factor in the delay LUT in response to the pair of output powers being equal.

12. A method for calibrating an equalization filter in a transceiver circuit comprising:

determining and storing a gain offset lookup table (LUT) to correlate a plurality of calibrated frequencies within a modulation bandwidth with a plurality of gain offsets, respectively; and

determining and storing a delay offset LUT to correlate the plurality of calibrated frequencies with a plurality of delay factors, respectively.

13. The method of claim 12, further comprising determining each of the plurality of gain offsets relative to a reference frequency within the modulation bandwidth.

14. The method of claim 13, further comprising selecting a center frequency of the modulation bandwidth as the reference frequency.

15. The method of claim 12, further comprising:

determining a minimum reference voltage and a minimum reference input power;

determining a reference frequency among the plurality of calibrated frequencies within the modulation bandwidth;

determining a reference target voltage based on an expected root-mean-square (RMS) of a modulated voltage to be provided to a power amplifier circuit for amplifying a radio frequency (RF) signal; and

for each of the plurality of calibrated frequencies:

determining a respective gain of the power amplifier circuit that amplifies a test signal generated at the calibrated frequency and in the determined minimum reference input power based on the determined minimum reference voltage;

determining a respective modulated voltage and a respective input power that cause the power amplifier circuit to have the

respective gain when amplifying the test signal at the calibrated frequency; and

storing the respective modulated voltage in association with the respective input power in a temporary voltage LUT.

16. The method of claim 15, further comprising, for each of the plurality of calibrated frequencies:

determining a respective adjusted input power relative to an input power in the temporary voltage LUT associated with a modulated voltage that is equal to the target voltage;

determining a respective one of the plurality of gain offsets between a respective adjusted input power at the reference frequency and the respective adjusted input power at the calibrated frequency; and

storing the respective calibrated frequency in association with the respective one of the plurality of gain offsets in the gain offset LUT.

17. The method of claim 12, further comprising:

determining a reference voltage and a reference input power;

determining a reference frequency among the plurality of calibrated frequencies within the modulation bandwidth;

determining a reference target voltage based on an expected root-mean-square (RMS) of a modulated voltage to be provided to a power amplifier circuit for amplifying a radio frequency (RF) signal; and

for each of the plurality of calibrated frequencies:

determining a respective gain of the power amplifier circuit that amplifies a test signal generated at the calibrated frequency and in the determined reference input power based on the determined reference voltage;

adjusting the respective gain based on a determined compression gain to determine a compressed reference gain; and

determining a respective modulated voltage and a respective input power that will cause the power amplifier circuit to have the compressed reference gain when amplifying the test signal at the calibrated frequency; and

store the respective modulated voltage and the respective input power in a temporary voltage LUT.

18. The method of claim 17, further comprising, for each of the plurality of calibrated frequencies:

determining a respective adjusted input power relative to an input power in the temporary voltage LUT associated with a modulated voltage that is equal to the target voltage;

determining a respective one of the plurality of gain offsets between a respective input power at the reference frequency and the respective input power at the calibrated frequency; and

storing the respective calibrated frequency in association with the respective one of the plurality of gain offsets in the gain offset LUT.

19. The method of claim 12, further comprising, for each of the plurality of calibrated frequencies:

determining an arbitrary delay factor;

measuring a pair of output powers of a power amplifier circuit when amplifying a test signal generated at the respective calibrated frequency and delay by the arbitrary delay factor minus an arbitrary delay offset and the arbitrary delay factor plus the arbitrary delay offset; and

storing the respective calibrated frequency in association with the arbitrary delay factor in the delay LUT in response to the pair of output powers being equal.

20. The method of claim 19, further comprising:

determining a new arbitrary delay factor in response to the pair of output powers being unequal;

measuring a new pair of output powers of the power amplifier circuit when amplifying the test signal generated at the respective calibrated frequency and delay by the new arbitrary delay factor minus the arbitrary delay offset and the new arbitrary delay factor plus the arbitrary delay offset; and

storing the respective calibrated frequency in association with the new arbitrary delay factor in the delay LUT in response to the pair of output powers being equal.

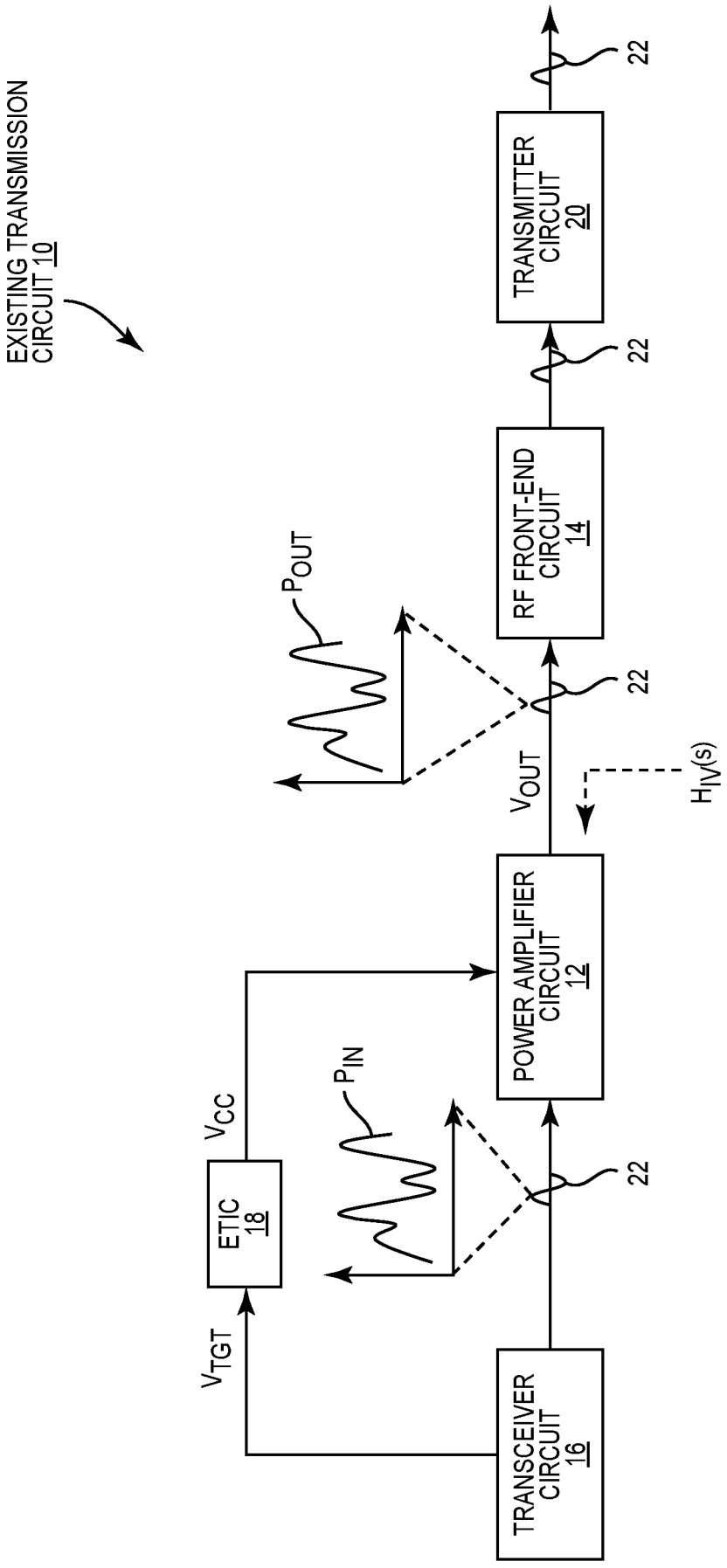

FIG. 1A
(RELATED ART)

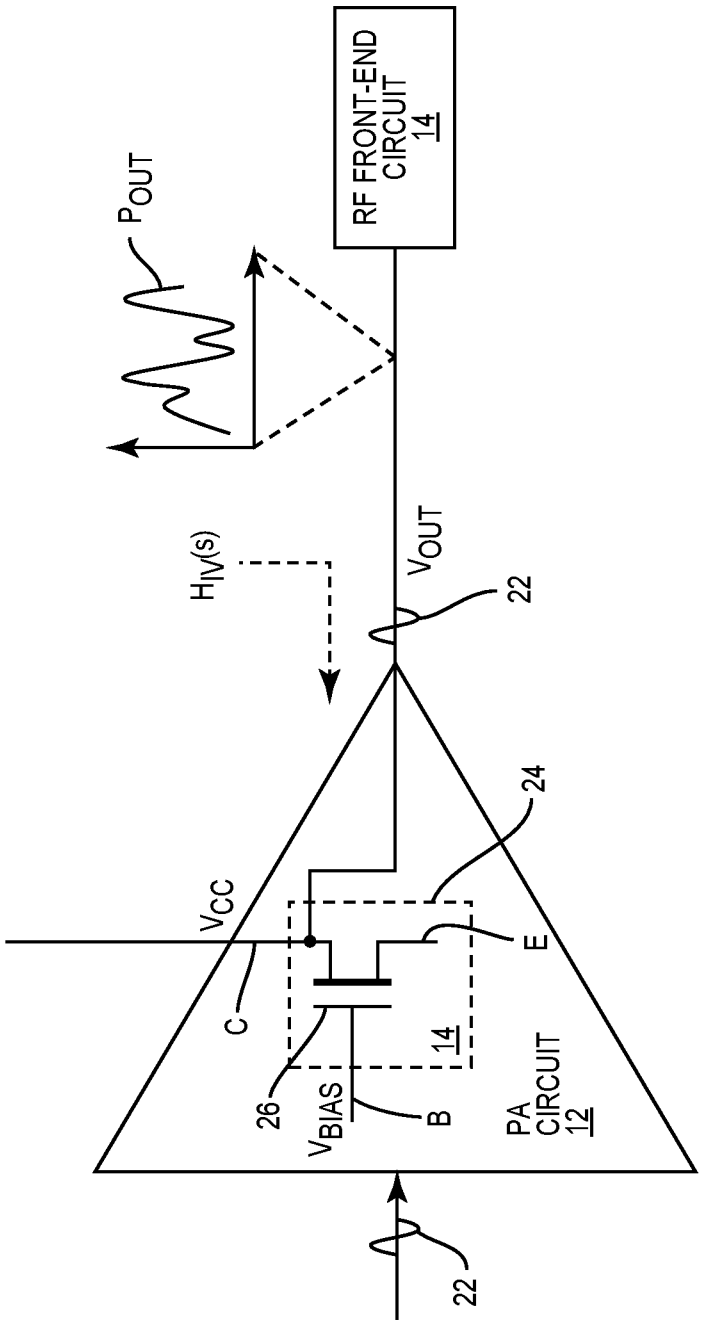

FIG. 1B
(RELATED ART)

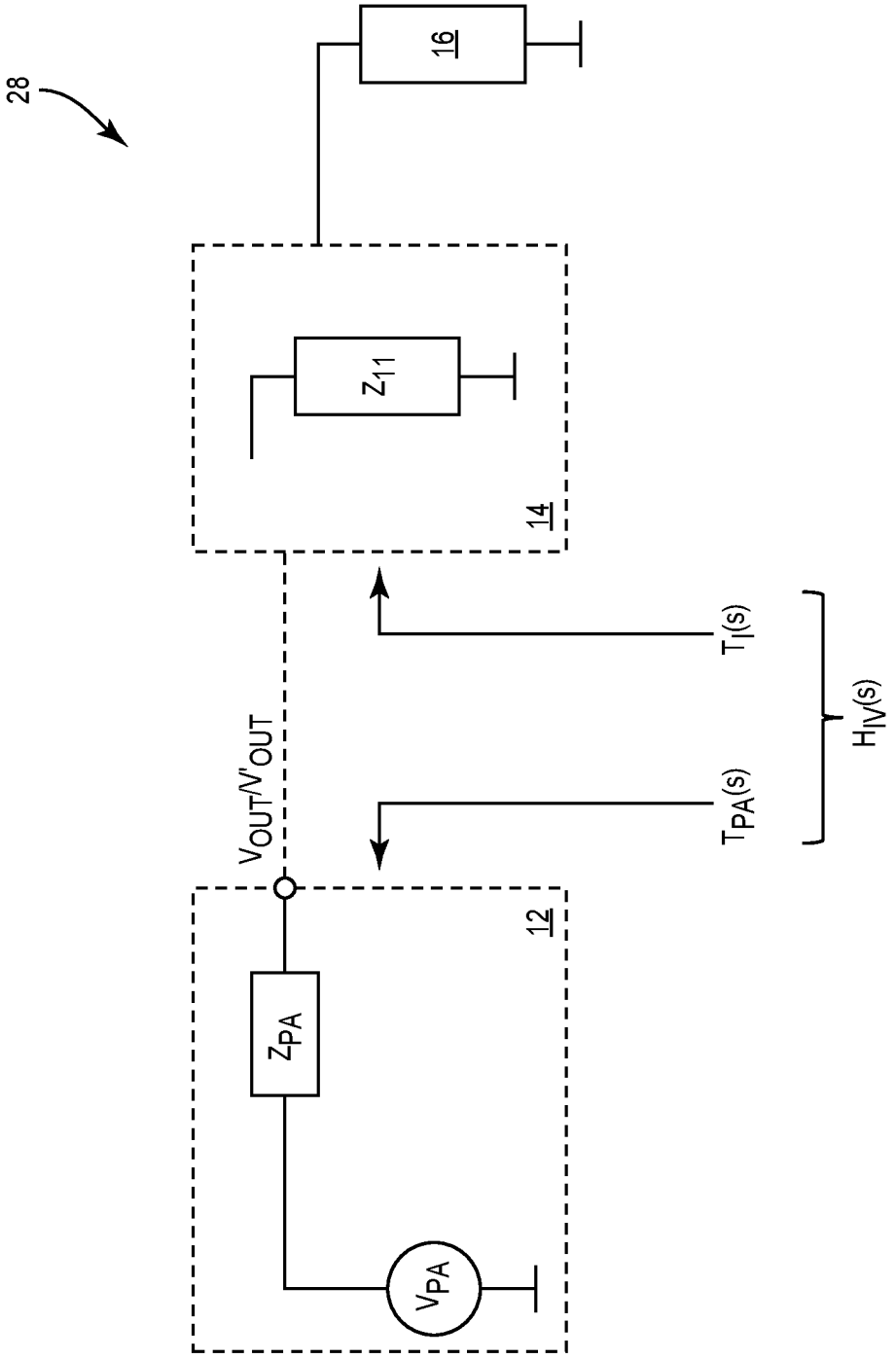

FIG. 2
(RELATED ART)

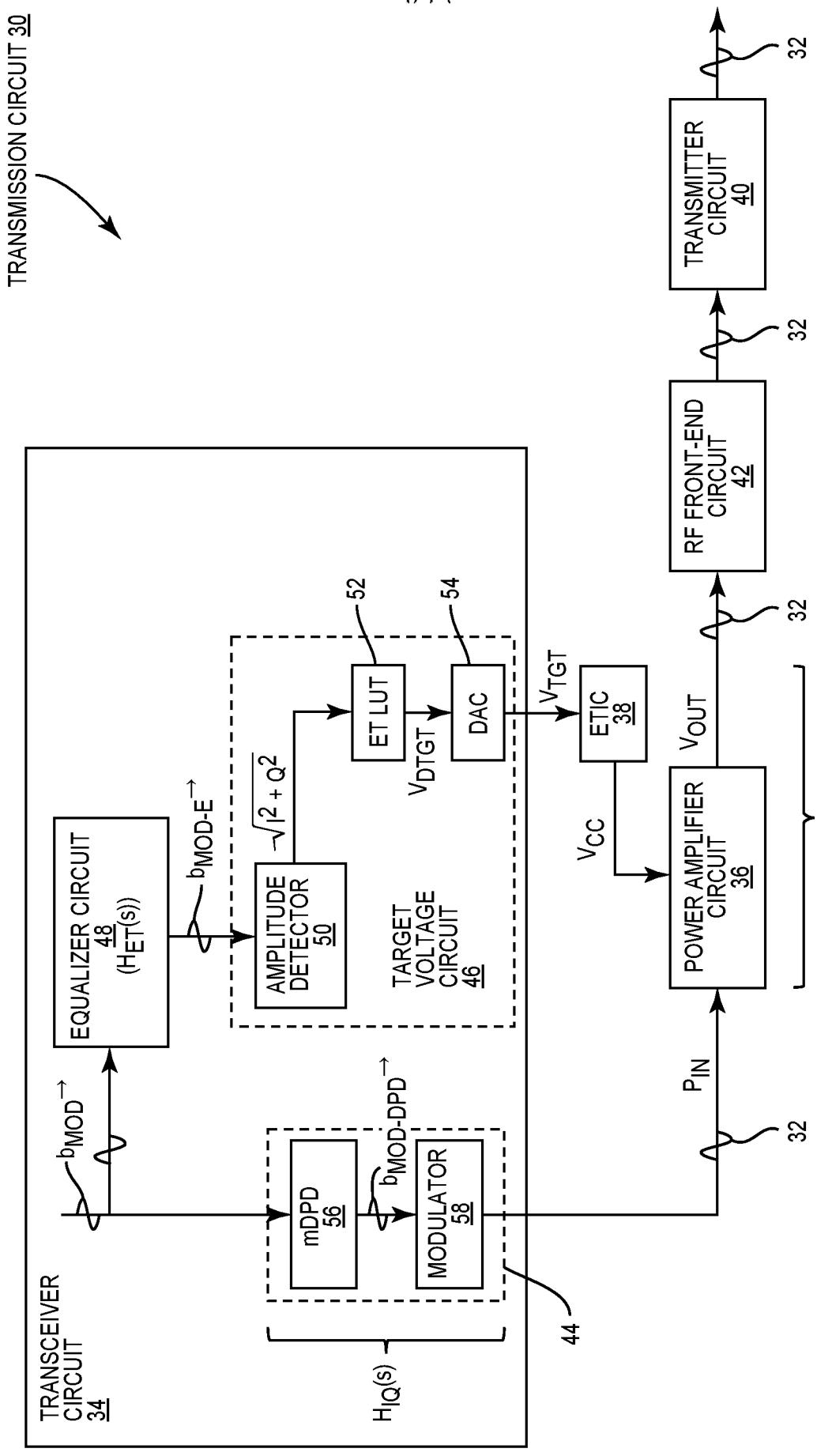

FIG. 3
(RELATED ART)

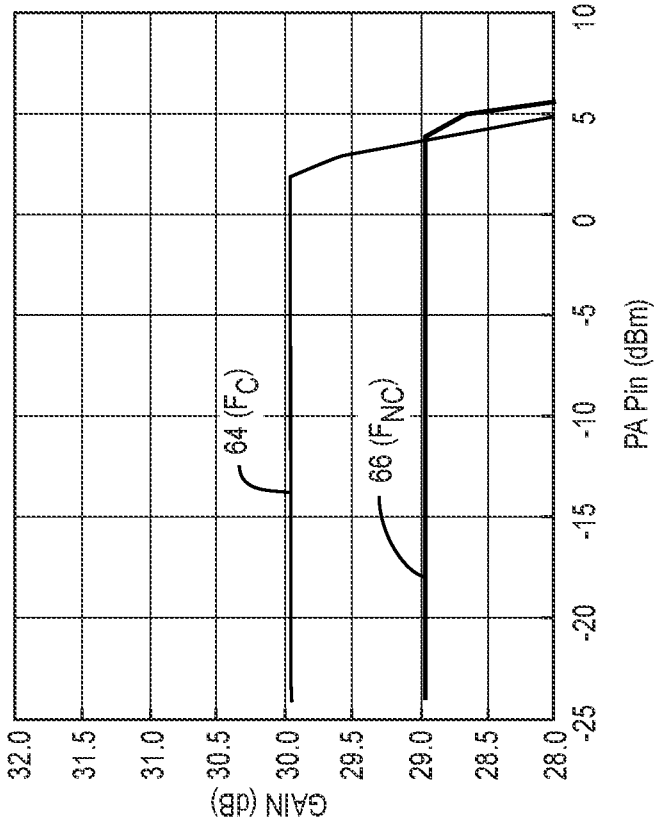

FIG. 4B
(RELATED ART)

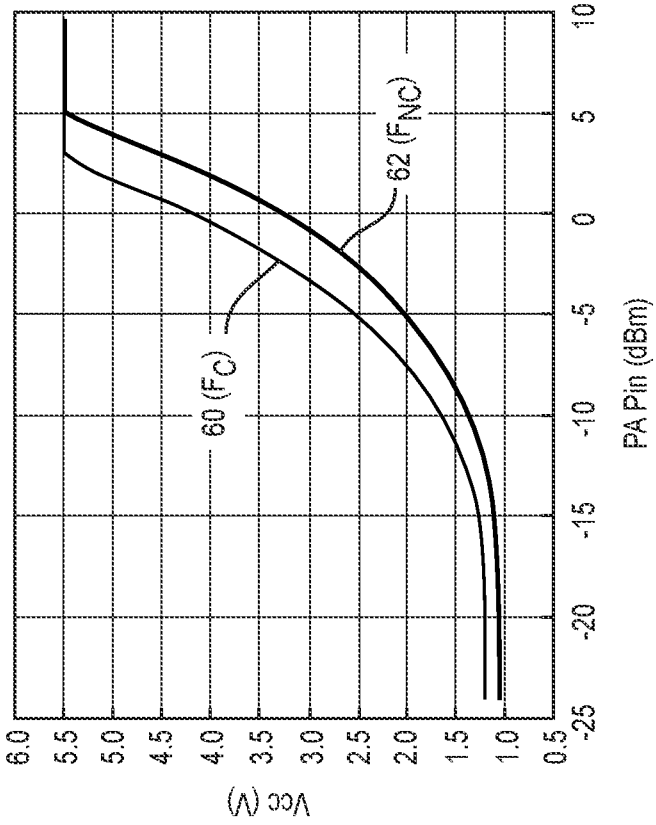

FIG. 4A
(RELATED ART)

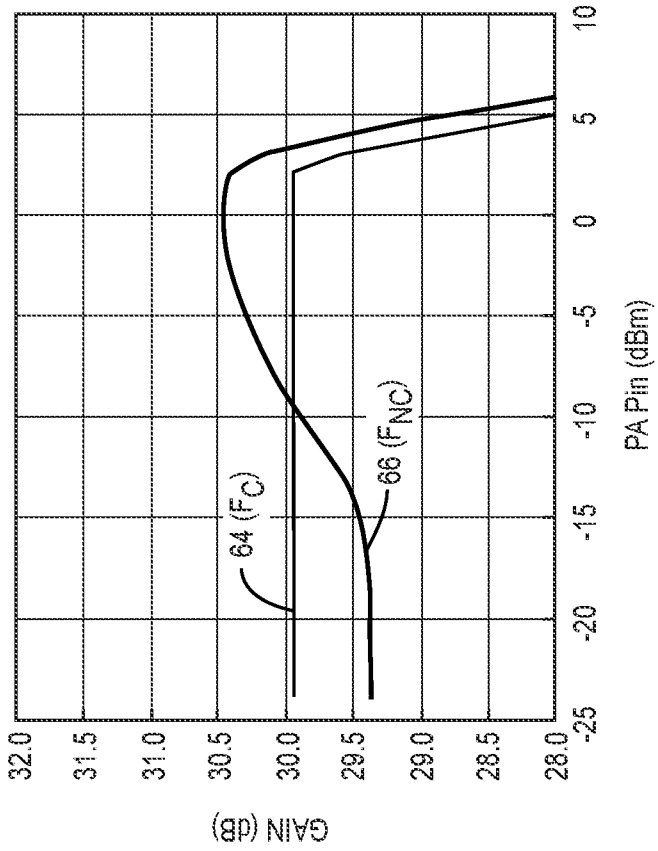

FIG. 4C
(RELATED ART)

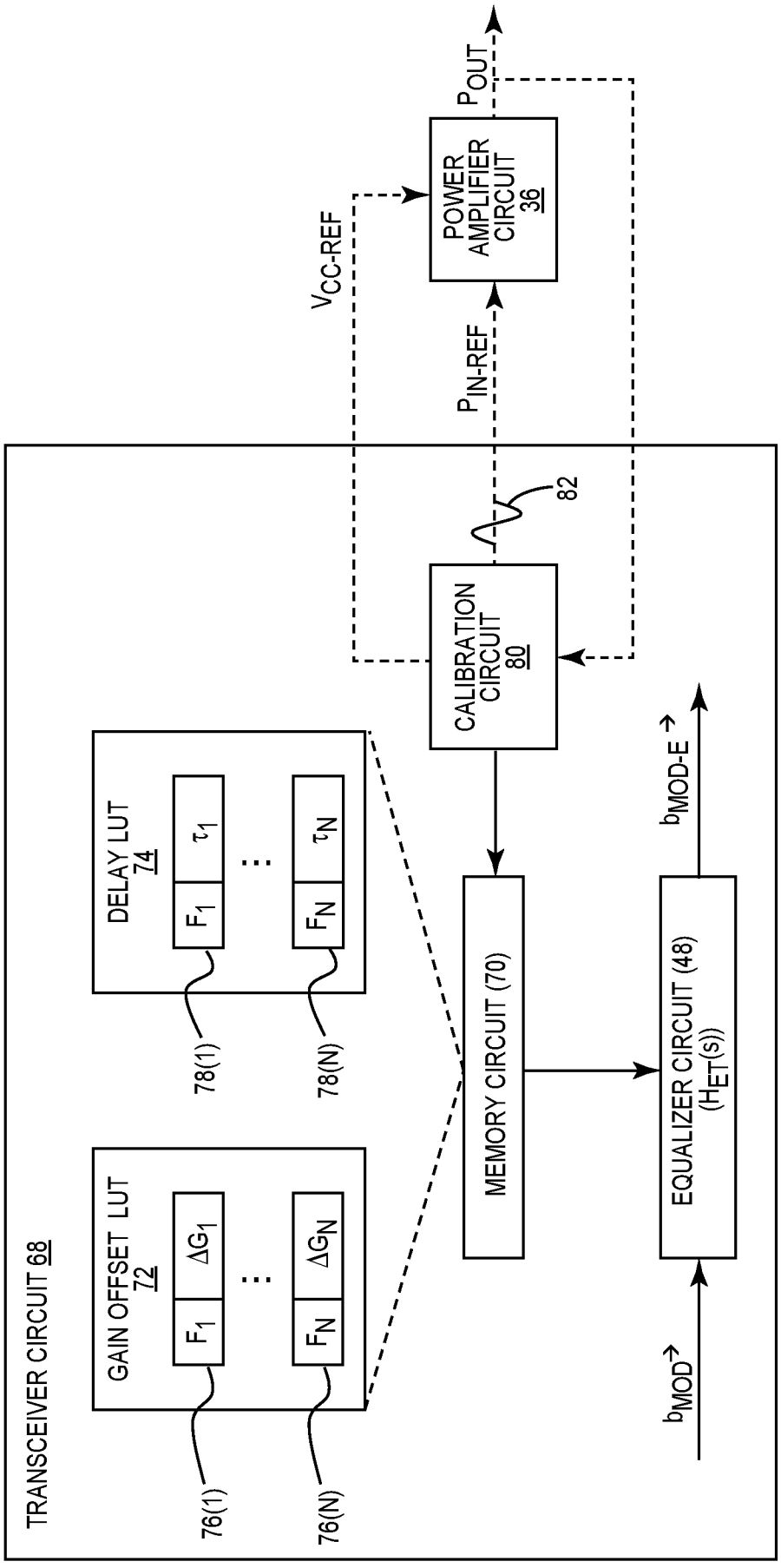
TRANSCEIVER CIRCUIT 68
GAIN OFFSET LUT 72
F1
ΔG1
FN
ΔGN
DELAY LUT 74
F1
τ1
FN
τN
76(1)
76(N)
78(1)
78(N)
MEMORY CIRCUIT (70)
CALIBRATION CIRCUIT 80
82
EQUALIZER CIRCUIT (48) (HET(s))
bMOD
bMOD-E
POWER AMPLIFIER CIRCUIT 36
VCC-REF
PIN-REF
POUT

FIG. 5

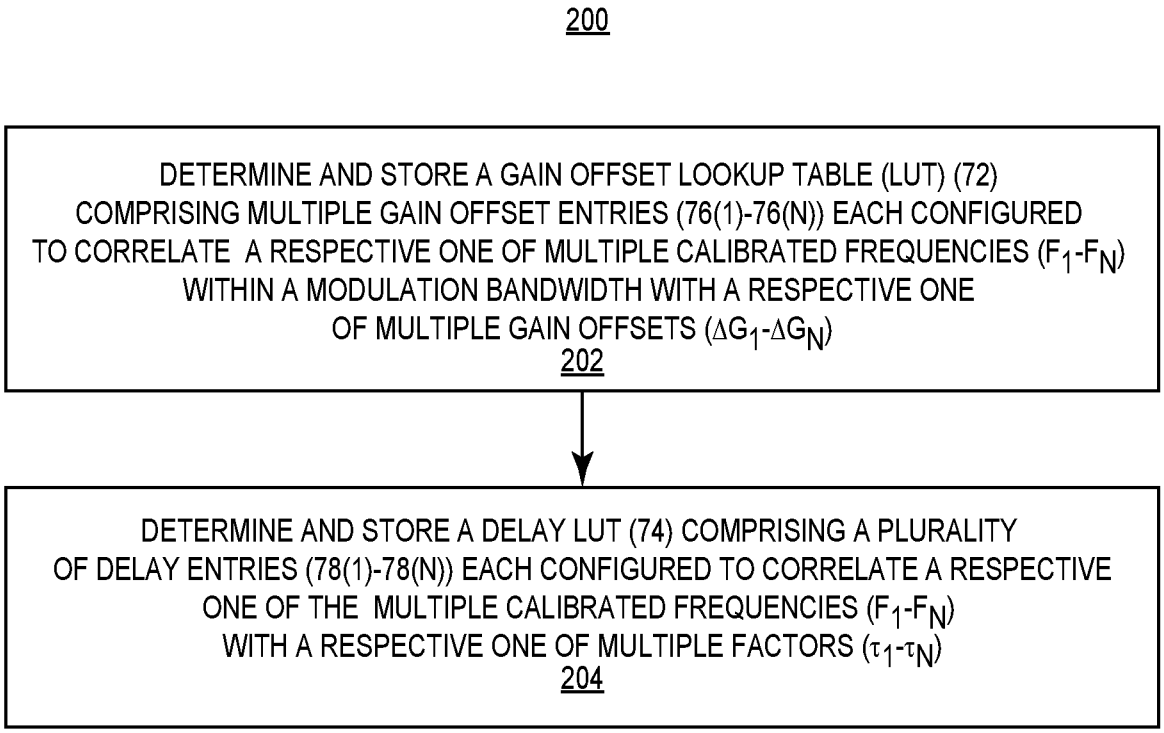
200
DETERMINE AND STORE A GAIN OFFSET LOOKUP TABLE (LUT) (72) COMPRISING MULTIPLE GAIN OFFSET ENTRIES (76(1)-76(N)) EACH CONFIGURED TO CORRELATE A RESPECTIVE ONE OF MULTIPLE CALIBRATED FREQUENCIES (F_1-F_N) WITHIN A MODULATION BANDWIDTH WITH A RESPECTIVE ONE OF MULTIPLE GAIN OFFSETS (ΔG_1-ΔG_N)
202
DETERMINE AND STORE A DELAY LUT (74) COMPRISING A PLURALITY OF DELAY ENTRIES (78(1)-78(N)) EACH CONFIGURED TO CORRELATE A RESPECTIVE ONE OF THE MULTIPLE CALIBRATED FREQUENCIES (F_1-F_N) WITH A RESPECTIVE ONE OF MULTIPLE FACTORS (τ_1-τ_N)
204

FIG. 6

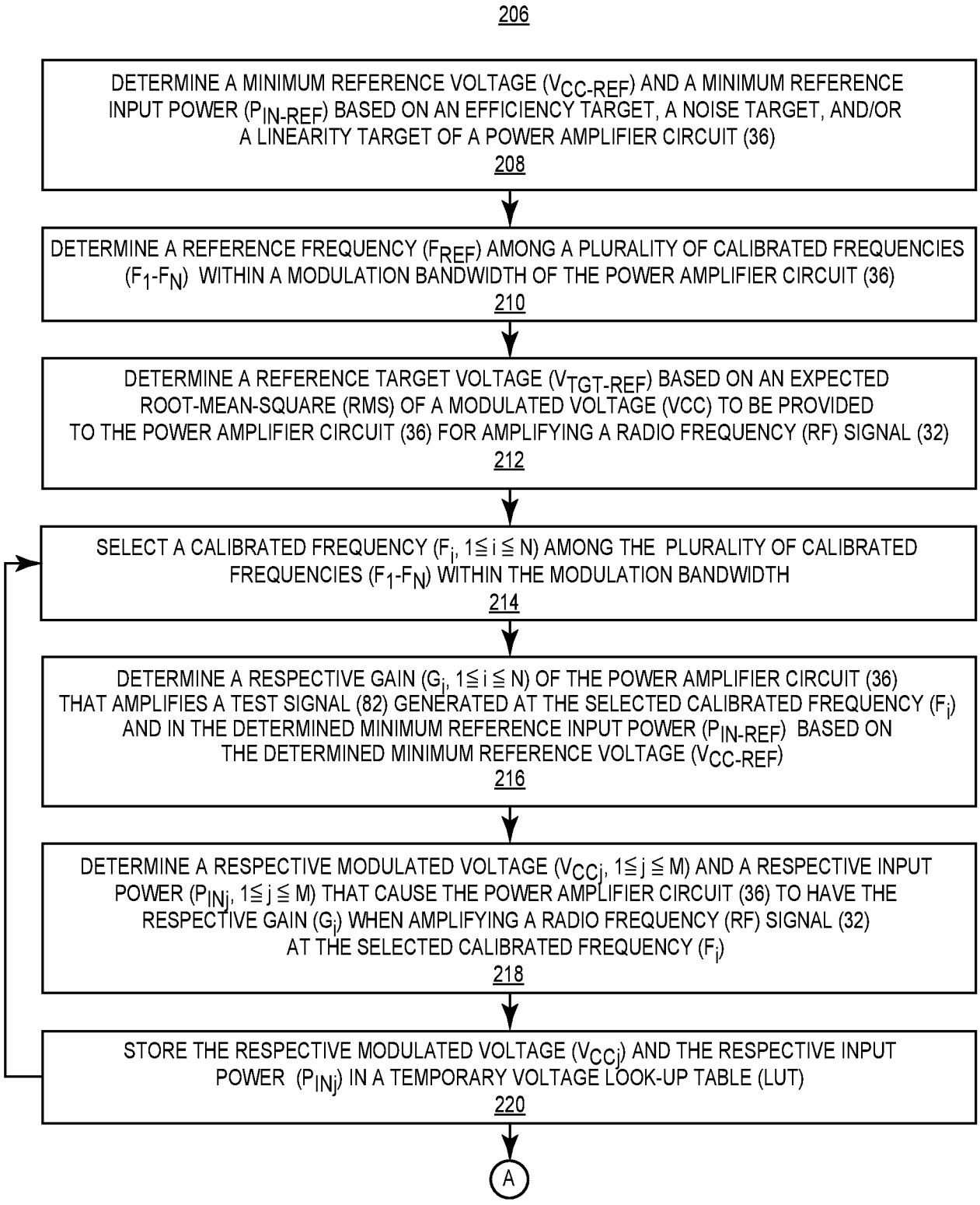
206
DETERMINE A MINIMUM REFERENCE VOLTAGE (V_{CC-REF}) AND A MINIMUM REFERENCE INPUT POWER (P_{IN-REF}) BASED ON AN EFFICIENCY TARGET, A NOISE TARGET, AND/OR A LINEARITY TARGET OF A POWER AMPLIFIER CIRCUIT (36)
208
DETERMINE A REFERENCE FREQUENCY (F_{REF}) AMONG A PLURALITY OF CALIBRATED FREQUENCIES (F_1-F_N) WITHIN A MODULATION BANDWIDTH OF THE POWER AMPLIFIER CIRCUIT (36)
210
DETERMINE A REFERENCE TARGET VOLTAGE ($V_{TGT-REF}$) BASED ON AN EXPECTED ROOT-MEAN-SQUARE (RMS) OF A MODULATED VOLTAGE (VCC) TO BE PROVIDED TO THE POWER AMPLIFIER CIRCUIT (36) FOR AMPLIFYING A RADIO FREQUENCY (RF) SIGNAL (32)
212
SELECT A CALIBRATED FREQUENCY (F_i, $1 \leqq i \leqq N$) AMONG THE PLURALITY OF CALIBRATED FREQUENCIES (F_1-F_N) WITHIN THE MODULATION BANDWIDTH
214
DETERMINE A RESPECTIVE GAIN (G_i, $1 \leqq i \leqq N$) OF THE POWER AMPLIFIER CIRCUIT (36) THAT AMPLIFIES A TEST SIGNAL (82) GENERATED AT THE SELECTED CALIBRATED FREQUENCY (F_i) AND IN THE DETERMINED MINIMUM REFERENCE INPUT POWER (P_{IN-REF}) BASED ON THE DETERMINED MINIMUM REFERENCE VOLTAGE (V_{CC-REF})
216
DETERMINE A RESPECTIVE MODULATED VOLTAGE (V_{CCj}, $1 \leqq j \leqq M$) AND A RESPECTIVE INPUT POWER (P_{INj}, $1 \leqq j \leqq M$) THAT CAUSE THE POWER AMPLIFIER CIRCUIT (36) TO HAVE THE RESPECTIVE GAIN (G_i) WHEN AMPLIFYING A RADIO FREQUENCY (RF) SIGNAL (32) AT THE SELECTED CALIBRATED FREQUENCY (F_i)
218
STORE THE RESPECTIVE MODULATED VOLTAGE (V_{CCj}) AND THE RESPECTIVE INPUT POWER (P_{INj}) IN A TEMPORARY VOLTAGE LOOK-UP TABLE (LUT)
220
A

FIG. 7

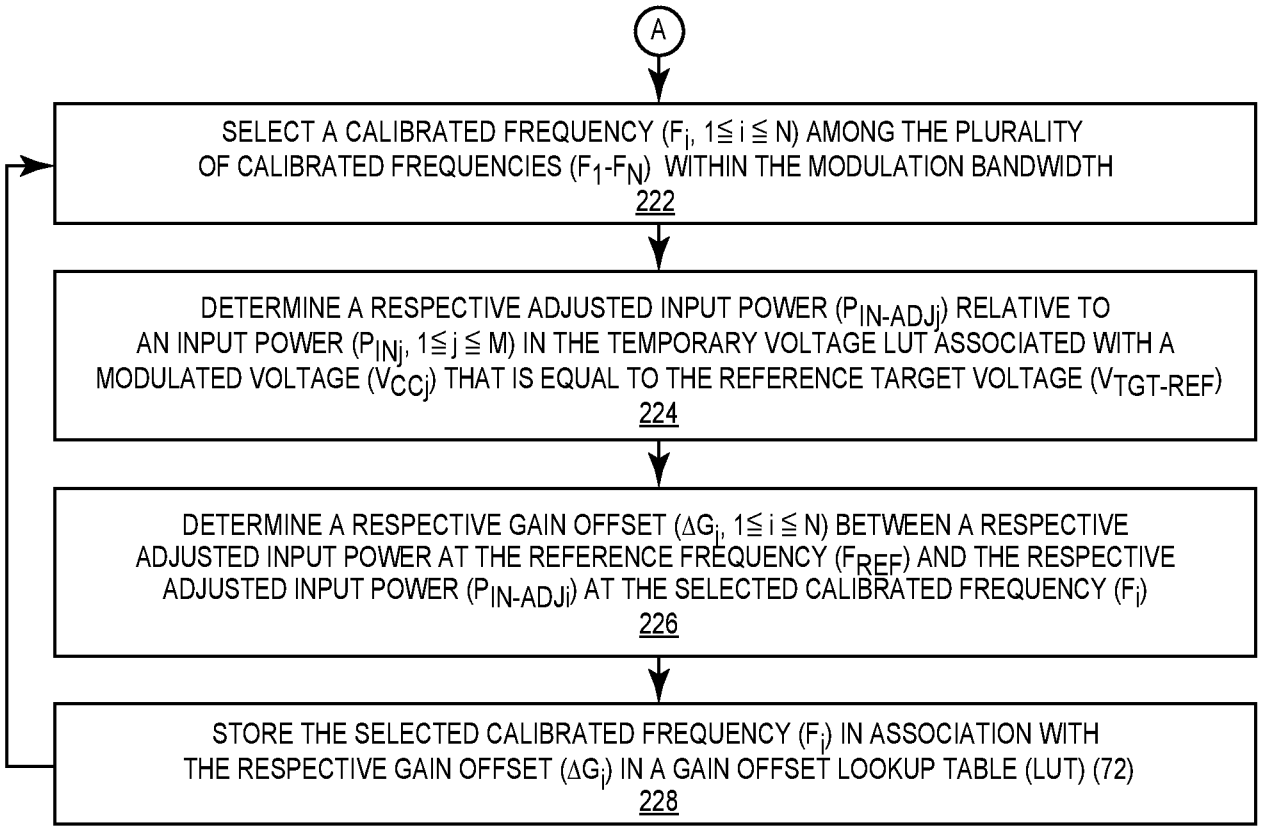
A
SELECT A CALIBRATED FREQUENCY (F_i, $1 \leqq i \leqq N$) AMONG THE PLURALITY OF CALIBRATED FREQUENCIES (F_1-F_N) WITHIN THE MODULATION BANDWIDTH
222
DETERMINE A RESPECTIVE ADJUSTED INPUT POWER ($P_{IN-ADJi}$) RELATIVE TO AN INPUT POWER (P_{INj}, $1 \leqq j \leqq M$) IN THE TEMPORARY VOLTAGE LUT ASSOCIATED WITH A MODULATED VOLTAGE (V_{CCj}) THAT IS EQUAL TO THE REFERENCE TARGET VOLTAGE ($V_{TGT-REF}$)
224
DETERMINE A RESPECTIVE GAIN OFFSET (ΔG_i, $1 \leqq i \leqq N$) BETWEEN A RESPECTIVE ADJUSTED INPUT POWER AT THE REFERENCE FREQUENCY (F_{REF}) AND THE RESPECTIVE ADJUSTED INPUT POWER ($P_{IN-ADJi}$) AT THE SELECTED CALIBRATED FREQUENCY (F_i)
226
STORE THE SELECTED CALIBRATED FREQUENCY (F_i) IN ASSOCIATION WITH THE RESPECTIVE GAIN OFFSET (ΔG_i) IN A GAIN OFFSET LOOKUP TABLE (LUT) (72)
228

FIG. 7 (cont.)

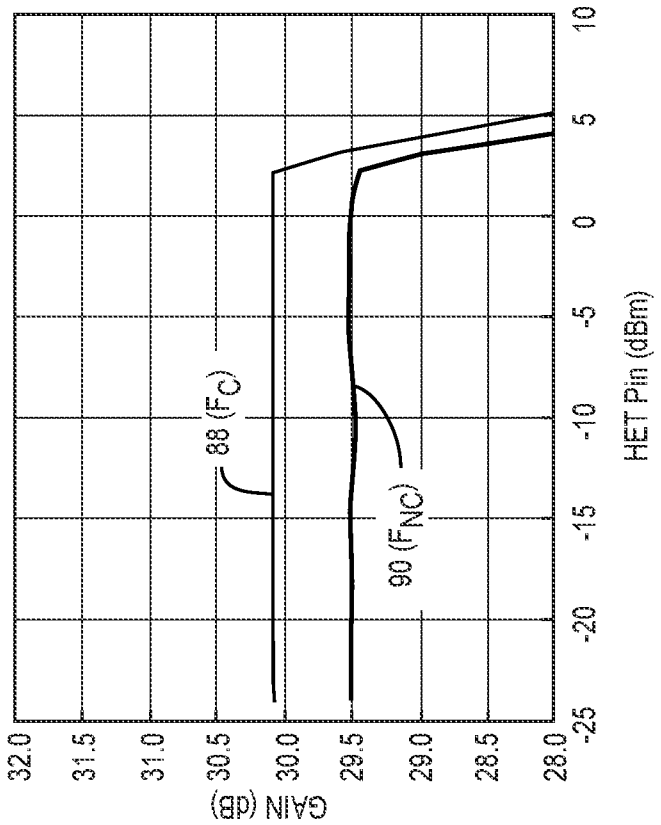
GAIN (dB)
32.0
31.5
31.0
30.5
30.0
29.5
29.0
28.5
28.0
88 (F_C)
90 (F_{NC})
10
5
0
-5
-10
-15
-20
-25
HET Pin (dBm)

FIG. 8B

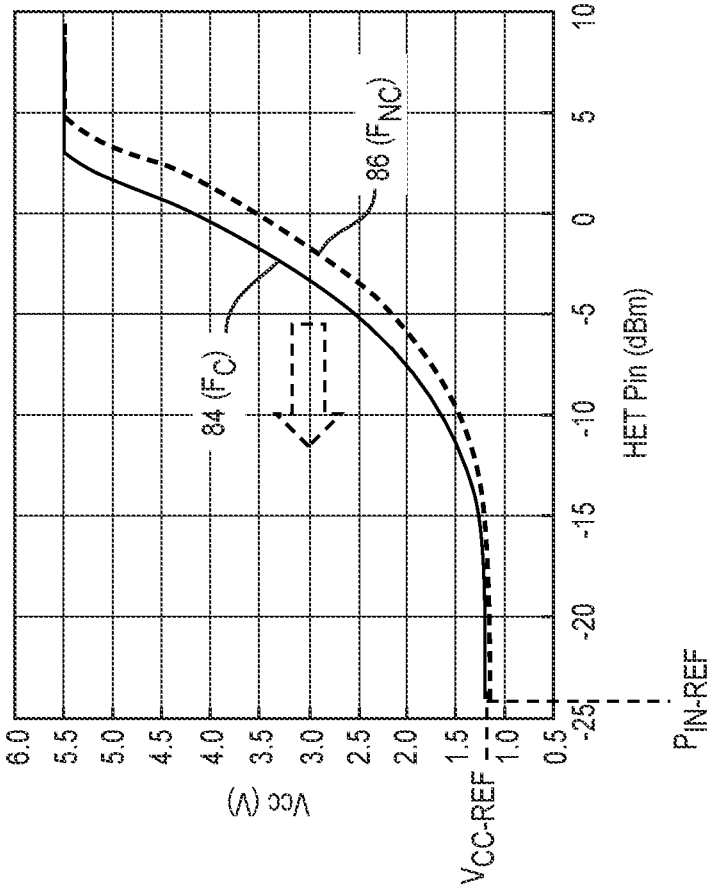
Vcc (V)
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
84 (F_C)
86 (F_{NC})
10
5
0
-5
-10
-15
-20
-25
HET Pin (dBm)
V_{CC-REF}
P_{IN-REF}

FIG. 8A

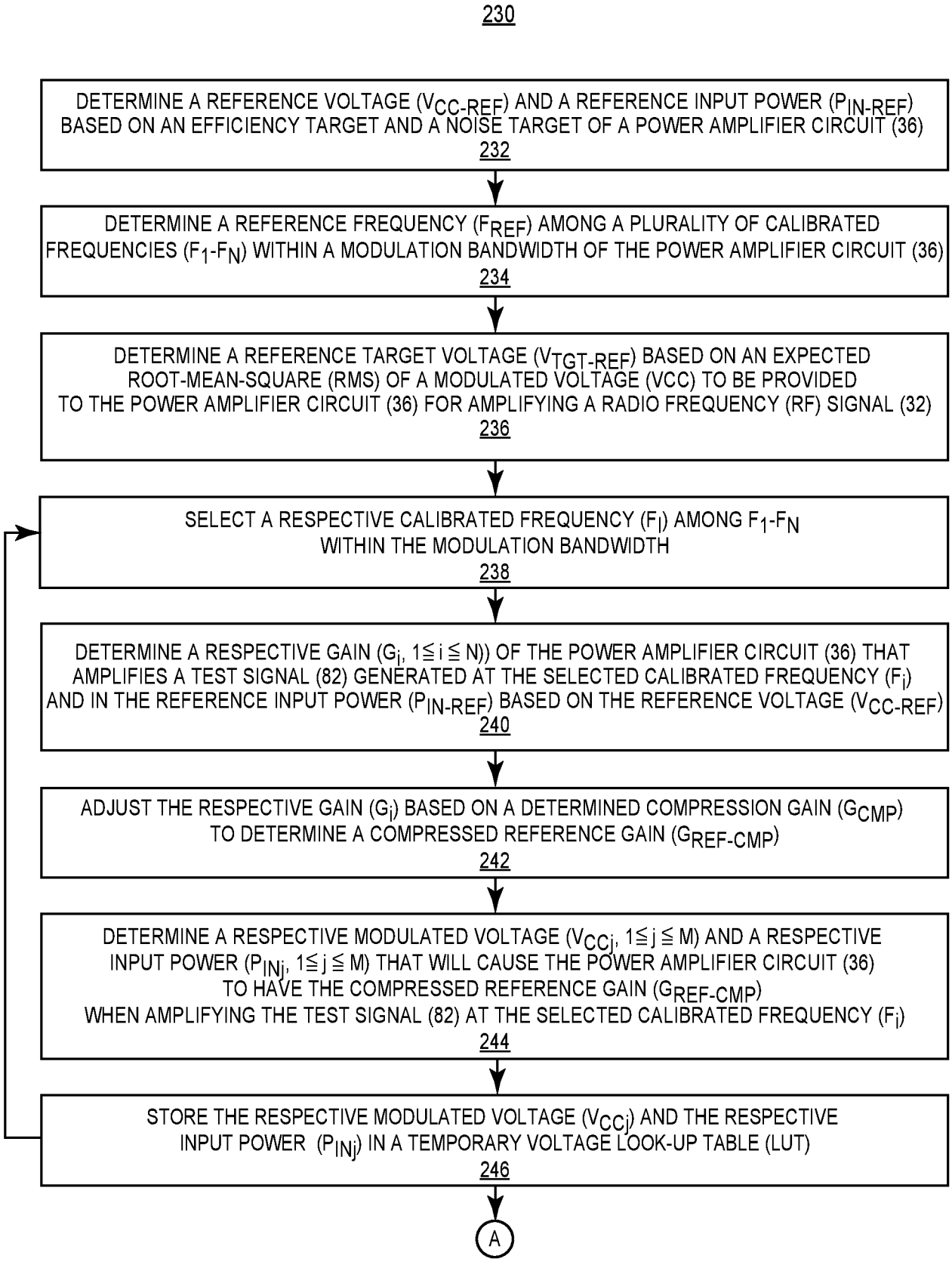
230
DETERMINE A REFERENCE VOLTAGE (V_{CC-REF}) AND A REFERENCE INPUT POWER (P_{IN-REF}) BASED ON AN EFFICIENCY TARGET AND A NOISE TARGET OF A POWER AMPLIFIER CIRCUIT (36)
232
DETERMINE A REFERENCE FREQUENCY (F_{REF}) AMONG A PLURALITY OF CALIBRATED FREQUENCIES (F_1-F_N) WITHIN A MODULATION BANDWIDTH OF THE POWER AMPLIFIER CIRCUIT (36)
234
DETERMINE A REFERENCE TARGET VOLTAGE ($V_{TGT-REF}$) BASED ON AN EXPECTED ROOT-MEAN-SQUARE (RMS) OF A MODULATED VOLTAGE (VCC) TO BE PROVIDED TO THE POWER AMPLIFIER CIRCUIT (36) FOR AMPLIFYING A RADIO FREQUENCY (RF) SIGNAL (32)
236
SELECT A RESPECTIVE CALIBRATED FREQUENCY (F_I) AMONG F_1-F_N WITHIN THE MODULATION BANDWIDTH
238
DETERMINE A RESPECTIVE GAIN (G_i, $1 \leqq i \leqq N$)) OF THE POWER AMPLIFIER CIRCUIT (36) THAT AMPLIFIES A TEST SIGNAL (82) GENERATED AT THE SELECTED CALIBRATED FREQUENCY (F_i) AND IN THE REFERENCE INPUT POWER (P_{IN-REF}) BASED ON THE REFERENCE VOLTAGE (V_{CC-REF})
240
ADJUST THE RESPECTIVE GAIN (G_i) BASED ON A DETERMINED COMPRESSION GAIN (G_{CMP}) TO DETERMINE A COMPRESSED REFERENCE GAIN ($G_{REF-CMP}$)
242
DETERMINE A RESPECTIVE MODULATED VOLTAGE (V_{CCj}, $1 \leqq j \leqq M$) AND A RESPECTIVE INPUT POWER (P_{INj}, $1 \leqq j \leqq M$) THAT WILL CAUSE THE POWER AMPLIFIER CIRCUIT (36) TO HAVE THE COMPRESSED REFERENCE GAIN ($G_{REF-CMP}$) WHEN AMPLIFYING THE TEST SIGNAL (82) AT THE SELECTED CALIBRATED FREQUENCY (F_i)
244
STORE THE RESPECTIVE MODULATED VOLTAGE (V_{CCj}) AND THE RESPECTIVE INPUT POWER (P_{INj}) IN A TEMPORARY VOLTAGE LOOK-UP TABLE (LUT)
246
A

FIG. 9

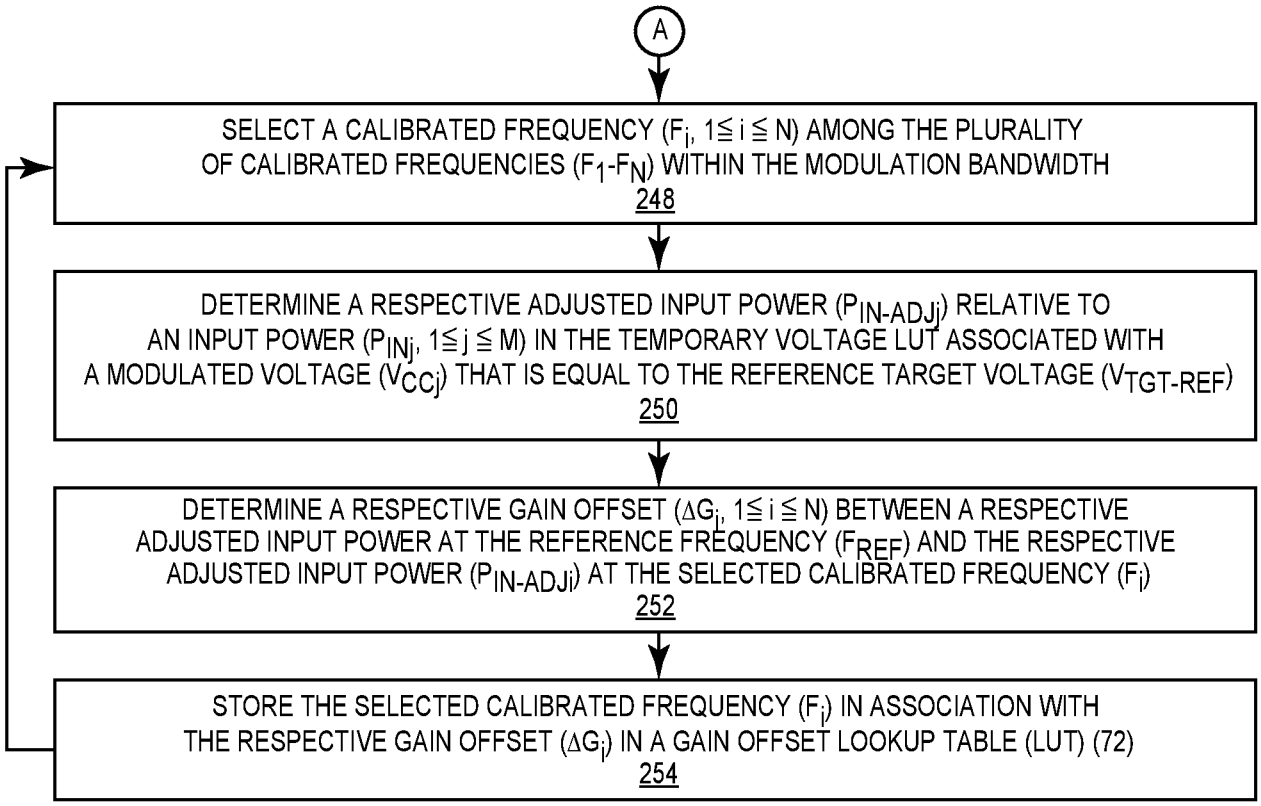
A
SELECT A CALIBRATED FREQUENCY (F_i, $1 \leqq i \leqq N$) AMONG THE PLURALITY OF CALIBRATED FREQUENCIES (F_1-F_N) WITHIN THE MODULATION BANDWIDTH
248
DETERMINE A RESPECTIVE ADJUSTED INPUT POWER ($P_{IN-ADJi}$) RELATIVE TO AN INPUT POWER (P_{INj}, $1 \leqq j \leqq M$) IN THE TEMPORARY VOLTAGE LUT ASSOCIATED WITH A MODULATED VOLTAGE (V_{CCj}) THAT IS EQUAL TO THE REFERENCE TARGET VOLTAGE ($V_{TGT-REF}$)
250
DETERMINE A RESPECTIVE GAIN OFFSET (ΔG_i, $1 \leqq i \leqq N$) BETWEEN A RESPECTIVE ADJUSTED INPUT POWER AT THE REFERENCE FREQUENCY (F_{REF}) AND THE RESPECTIVE ADJUSTED INPUT POWER ($P_{IN-ADJi}$) AT THE SELECTED CALIBRATED FREQUENCY (F_i)
252
STORE THE SELECTED CALIBRATED FREQUENCY (F_i) IN ASSOCIATION WITH THE RESPECTIVE GAIN OFFSET (ΔG_i) IN A GAIN OFFSET LOOKUP TABLE (LUT) (72)
254

FIG. 9 (cont.)

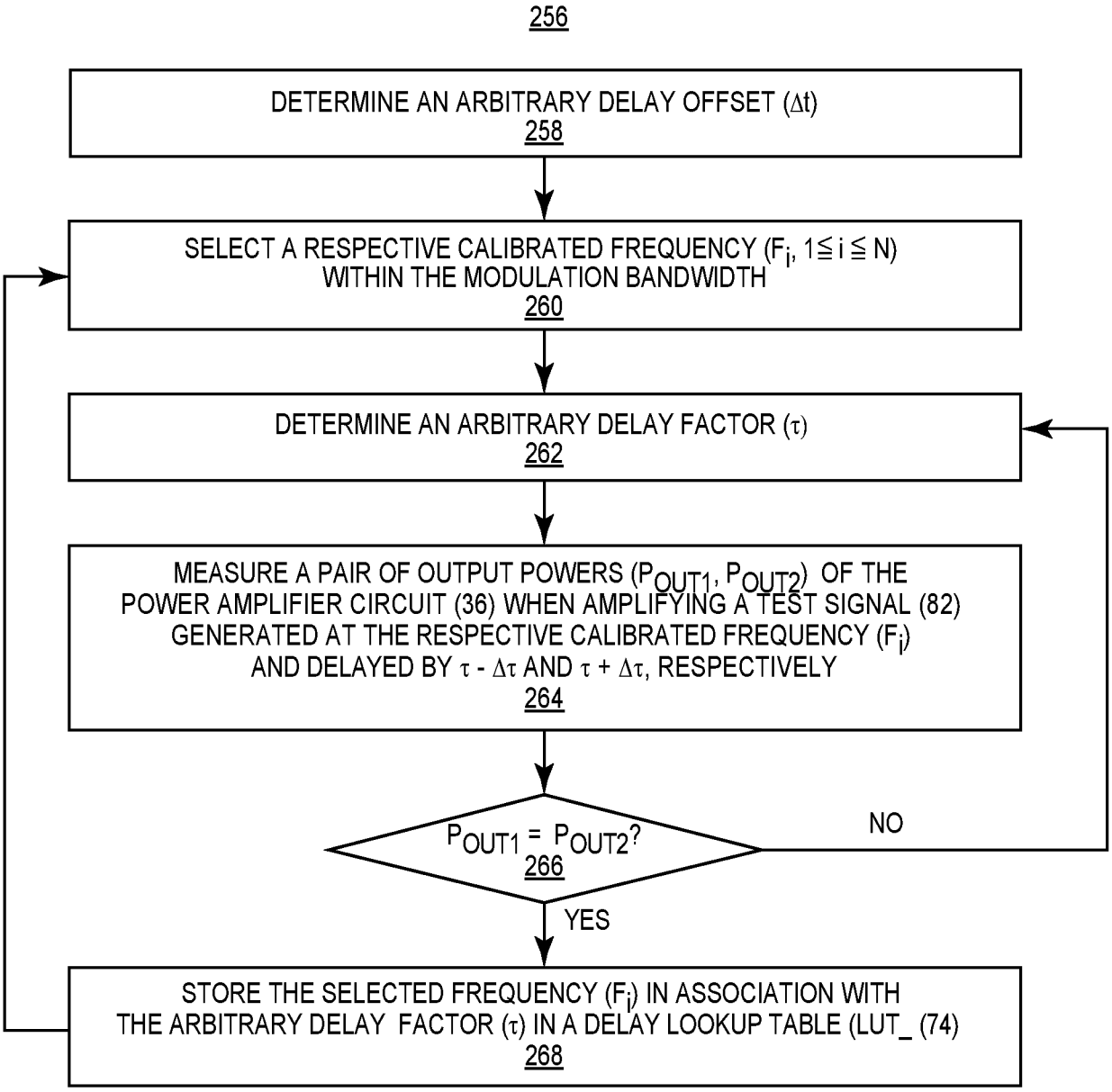
256
DETERMINE AN ARBITRARY DELAY OFFSET (Δt)
258
SELECT A RESPECTIVE CALIBRATED FREQUENCY (F_i, $1 \leqq i \leqq N$) WITHIN THE MODULATION BANDWIDTH
260
DETERMINE AN ARBITRARY DELAY FACTOR (τ)
262
MEASURE A PAIR OF OUTPUT POWERS (P_{OUT1}, P_{OUT2}) OF THE POWER AMPLIFIER CIRCUIT (36) WHEN AMPLIFYING A TEST SIGNAL (82) GENERATED AT THE RESPECTIVE CALIBRATED FREQUENCY (F_i) AND DELAYED BY τ - Δτ AND τ + Δτ, RESPECTIVELY
264
$P_{OUT1} = P_{OUT2}$?
266
NO
YES
STORE THE SELECTED FREQUENCY (F_i) IN ASSOCIATION WITH THE ARBITRARY DELAY FACTOR (τ) IN A DELAY LOOKUP TABLE (LUT_ (74)
268

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2022/043600

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03F1/02 H03F3/24 H03G3/30 H04B17/13 H03F3/19
ADD. H04B1/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F H04B H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 9 692 366 B2 (INTEL CORP [US]) 27 June 2017 (2017-06-27) column 1, line 6 - column 18, line 12; figures 1-8	1-20
A	US 2021/281228 A1 (KHLAT NADIM [FR]) 9 September 2021 (2021-09-09) paragraphs [0002] - [0038]; figures 1-4	1-20
A	US 2020/136563 A1 (KHLAT NADIM [FR]) 30 April 2020 (2020-04-30) paragraphs [0002] - [0037]; figures 1-5	1-20
A	US 2014/213196 A1 (LANGER ANDREAS [DE] ET AL) 31 July 2014 (2014-07-31) paragraphs [0001] - [0089]; figures 1-14	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 December 2022	11/01/2023

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Fedi, Giulio

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2022/043600

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 9692366 B2	27-06-2017	CN 105680807 A	15-06-2016
		EP 3032737 A1	15-06-2016
		TW 201630357 A	16-08-2016
		US 2016164550 A1	09-06-2016
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US 2020136563 A1	30-04-2020	NONE	
US 2014213196 A1	31-07-2014	CN 103973248 A	06-08-2014
		CN 107093987 A	25-08-2017
		DE 102014101142 A1	31-07-2014
		US 2014213196 A1	31-07-2014

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17/737,300 2022.05.05 US

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2024.03.05

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(87)PCT国际申请的公布数据
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专利代理师 张鑫

(51)Int.Cl.
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H04B 1/04(2006.01)
H03F 3/19(2006.01)
H04B 17/13(2006.01)
H03G 3/30(2006.01)
H03F 3/24(2006.01)

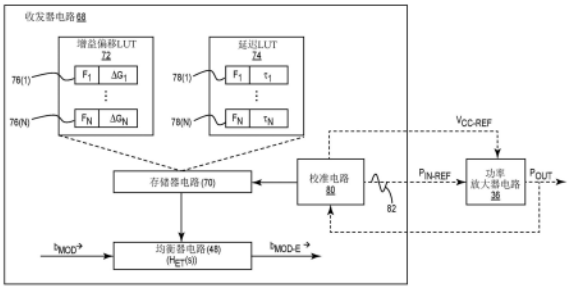
权利要求书4页 说明书10页 附图15页

(54)发明名称

收发器电路中的均衡滤波校准

(57)摘要

一种收发器电路(68)从时变调制向量生成射频(RF)信号,并且功率放大器电路(36)基于已调制电压放大所述RF信号。所述收发器电路(68)被配置成将均衡滤波施加到所述时变调制向量,从而补偿在所述功率放大器电路(36)的输出级处产生的电压畸变滤波。在本文公开的实施例中,校准电路可以被配置成在所述功率放大器电路(36)的调制带宽内的多个频率内校准所述均衡滤波,以生成增益偏移LUT(72)和延迟LUT(74)。因此,所述均衡滤波可以动态地适于减少由所述功率放大器电路(36)的所述调制带宽内的电压畸变滤波引起的不期望的瞬时过度压缩和/或频谱再生长。



CN 117917001 A

1.一种收发器电路,其包括:

存储器电路;以及

校准电路,所述校准电路耦合到功率放大器电路并且被配置成:

确定增益偏移查找表(LUT)并将其存储在所述存储器电路中,以分别使所述功率放大器电路的调制带宽内的多个已校准频率与多个增益偏移相关;并且

确定延迟偏移LUT并将其存储在所述存储器电路中,以分别使所述多个已校准频率与多个延迟因数相关。

2.根据权利要求1所述的收发器电路,其中相对于所述调制带宽内的参考频率确定所述多个增益偏移中的每一个。

3.根据权利要求2所述的收发器电路,其中所述参考频率对应于所述调制带宽的中心频率。

4.根据权利要求1所述的收发器电路,其中所述校准电路进一步被配置成:

确定最小参考电压和最小参考输入功率;

确定所述调制带宽内的所述多个已校准频率之间的参考频率;

基于待提供到所述功率放大器电路用于放大射频(RF)信号的已调制电压的预期均方根(RMS)来确定参考目标电压;并且

针对所述多个已校准频率中的每一个:

基于所确定的最小参考电压确定放大在所述已校准频率和所确定的最小参考输入功率下生成的测试信号的所述功率放大器电路的相应增益;

确定使所述功率放大器电路在放大所述已校准频率下的所述测试信号时具有所述相应增益的相应已调制电压和相应输入功率;并且

将所述相应已调制电压与所述相应输入功率相关联地存储在临时电压LUT中。

5.根据权利要求4所述的收发器电路,其中所述校准电路进一步被配置成基于以下中的一个或多个之间的折衷来确定所述最小参考电压和所述最小参考输入功率:

所述功率放大器电路的效率目标;

所述功率放大器电路的噪声目标;以及

所述功率放大器电路的线性目标。

6.根据权利要求4所述的收发器电路,其中,针对所述多个已校准频率中的每一个,所述校准电路进一步被配置成:

确定相对于与等于所述参考目标电压的已调制电压相关联的所述临时电压LUT中的输入功率的相应调整后输入功率;

确定在所述参考频率下的相应调整后输入功率与所述已校准频率下的所述相应调整后输入功率之间的所述多个增益偏移中的相应一个;并且

将所述相应已校准频率与所述多个增益偏移中的所述相应一个相关联地存储在所述增益偏移LUT中。

7.根据权利要求1所述的收发器电路,其中所述校准电路进一步被配置成:

确定参考电压和参考输入功率;

确定所述调制带宽内的所述多个已校准频率之间的参考频率;

基于待提供到所述功率放大器电路用于放大射频(RF)信号的已调制电压的预期均方

根(RMS)来确定参考目标电压;并且

针对所述多个已校准频率中的每一个:

基于所确定的参考电压确定放大在所述已校准频率和所确定的参考输入功率下生成的测试信号的所述功率放大器电路的相应增益;

基于所确定的压缩增益调整所述相应增益以确定已压缩增益;

确定将使所述功率放大器电路在放大所述已校准频率下的所述测试信号时具有所述已压缩增益的相应已调制电压和相应输入功率;并且

将所述相应已调制电压与所述相应输入功率存储在临时电压LUT中。

8.根据权利要求7所述的收发器电路,其中所述校准电路进一步被配置成基于以下中的一个或多个之间的折衷来确定所述参考电压和所述参考输入功率:

所述功率放大器电路的效率目标;以及

所述功率放大器电路的噪声目标。

9.根据权利要求7所述的收发器电路,其中,针对所述多个已校准频率中的每一个,所述校准电路进一步被配置成:

确定相对于与等于所述参考目标电压的已调制电压相关联的所述临时电压LUT中的输入功率的相应调整后输入功率;

确定在所述参考频率下的相应输入功率与所述已校准频率下的所述相应输入功率之间的所述多个增益偏移中的相应一个;并且

将所述已校准频率与所述多个增益偏移中的所述相应一个相关联地存储在所述增益偏移LUT中。

10.根据权利要求1所述的收发器电路,其中,针对所述多个已校准频率中的每一个,所述校准电路进一步被配置成:

确定任意延迟因数;

测量所述功率放大器电路放大在所述相应已校准频率下生成且延迟所述任意延迟因数减去任意延迟偏移和所述任意延迟因数加上所述任意延迟偏移的测试信号时的一对输出功率;并且

响应于所述一对输出功率相等而将所述相应已校准频率与所述任意延迟因数相关联地存储在所述延迟LUT中。

11.根据权利要求10所述的收发器电路,其中所述校准电路进一步被配置成:

响应于所述一对输出功率不相等而确定新的任意延迟因数;

测量所述功率放大器电路放大在所述相应已校准频率下生成且延迟所述新的任意延迟因数减去所述任意延迟偏移和所述新的任意延迟因数加上所述任意延迟偏移的所述测试信号时的新的一对输出功率;并且

响应于所述一对输出功率相等而将所述相应已校准频率与所述新的任意延迟因数相关联地存储在所述延迟LUT中。

12.一种用于校准收发器电路中的均衡滤波的方法,其包括:

确定并存储增益偏移查找表(LUT),以分别使调制带宽内的多个已校准频率与多个增益偏移相关;以及

确定并存储延迟偏移LUT,以分别使所述多个已校准频率与多个延迟因数相关。

13.根据权利要求12所述的方法,其进一步包括相对于所述调制带宽内的参考频率确定所述多个增益偏移中的每一个。

14.根据权利要求13所述的方法,其进一步包括选择所述调制带宽的中心频率作为所述参考频率。

15.根据权利要求12所述的方法,其进一步包括:

确定最小参考电压和最小参考输入功率;

确定所述调制带宽内的所述多个已校准频率之间的参考频率;

基于待提供到功率放大器电路用于放大射频(RF)信号的已调制电压的预期均方根(RMS)来确定参考目标电压;以及

针对所述多个已校准频率中的每一个:

基于所确定的最小参考电压确定放大在所述已校准频率和所确定的最小参考输入功率下生成的测试信号的所述功率放大器电路的相应增益;

确定使所述功率放大器电路在放大所述已校准频率下的所述测试信号时具有所述相应增益的相应已调制电压和相应输入功率;以及

将所述相应已调制电压与所述相应输入功率相关联地存储在临时电压LUT中。

16.根据权利要求15所述的方法,其进一步包括,针对所述多个已校准频率中的每一个:

确定相对于与等于所述目标电压的已调制电压相关联的所述临时电压LUT中的输入功率的相应调整后输入功率;

确定在所述参考频率下的相应调整后输入功率与所述已校准频率下的所述相应调整后输入功率之间的所述多个增益偏移中的相应一个;以及

将所述相应已校准频率与所述多个增益偏移中的所述相应一个相关联地存储在所述增益偏移LUT中。

17.根据权利要求12所述的方法,其进一步包括:

确定参考电压和参考输入功率;

确定所述调制带宽内的所述多个已校准频率之间的参考频率;

基于待提供到功率放大器电路用于放大射频(RF)信号的已调制电压的预期均方根(RMS)来确定参考目标电压;以及

针对所述多个已校准频率中的每一个:

基于所确定的参考电压确定放大在所述已校准频率和所确定的参考输入功率下生成的测试信号的所述功率放大器电路的相应增益;

基于所确定的压缩增益调整所述相应增益以确定已压缩参考增益;以及

确定将使所述功率放大器电路在放大所述已校准频率下的所述测试信号时具有所述已压缩参考增益的相应已调制电压和相应输入功率;以及

将所述相应已调制电压与所述相应输入功率存储在临时电压LUT中。

18.根据权利要求17所述的方法,其进一步包括,针对所述多个已校准频率中的每一个:

确定相对于与等于所述目标电压的已调制电压相关联的所述临时电压LUT中的输入功率的相应调整后输入功率;

确定在所述参考频率下的相应输入功率与所述已校准频率下的所述相应输入功率之间的所述多个增益偏移中的相应一个;以及

将所述相应已校准频率与所述多个增益偏移中的所述相应一个相关联地存储在所述增益偏移LUT中。

19.根据权利要求12所述的方法,其进一步包括,针对所述多个已校准频率中的每一个:

确定任意延迟因数;

测量功率放大器电路放大在所述相应已校准频率下生成且延迟所述任意延迟因数减去任意延迟偏移和所述任意延迟因数加上所述任意延迟偏移的测试信号时的一对输出功率;以及

响应于所述一对输出功率相等而将所述相应已校准频率与所述任意延迟因数相关联地存储在所述延迟LUT中。

20.根据权利要求19所述的方法,其进一步包括:

响应于所述一对输出功率不相等而确定新的任意延迟因数;

测量所述功率放大器电路放大在所述相应已校准频率下生成且延迟所述新的任意延迟因数减去所述任意延迟偏移和所述新的任意延迟因数加上所述任意延迟偏移的所述测试信号时的新的一对输出功率;以及

响应于所述一对输出功率相等而将所述相应已校准频率与所述新的任意延迟因数相关联地存储在所述延迟LUT中。

收发器电路中的均衡滤波校准

[0001] 相关申请交叉引用

[0002] 本申请要求2021年9月16日提交的第63/245,139号临时专利申请、2022年1月27日提交的第63/303,531号临时专利申请和2022年5月5日提交的第17/737,300号美国专利申请的权益,前述申请的公开内容以全文引用的方式并入本文中。

技术领域

[0003] 本公开的技术大体上涉及一种发射在宽调制带宽中调制的射频(RF)信号的发射电路。

背景技术

[0004] 移动通信装置对于提供无线通信服务而言,在当前社会中已变得越来越普遍。这些移动通信装置的普及部分地由目前在此类装置上启用的许多功能驱动。此类装置处理能力的增强意味着移动通信装置已从纯通信工具演化为能够增强用户体验的复杂移动多媒体中心。

[0005] 重新定义的用户体验依赖于由高级第五代(5G)和5G新无线电(5G-NR)技术提供的更高数据速率,所述技术通常以毫米波频谱发射和接收射频(RF)信号。鉴于RF信号更易受到毫米波频谱中的衰减和干扰,RF信号通常由最先进的功率放大器放大,以帮助在发射之前将RF信号增加到更高的功率。

[0006] 包络跟踪(ET)是设计成提高功率放大器的工作效率和/或线性度性能的功率管理技术。在ET功率管理电路中,功率管理集成电路(PMIC)被配置成基于RF信号的时变电压包络生成时变ET电压,并且功率放大器被配置成基于时变ET电压放大RF信号。可以理解的是,时变ET电压在时间和振幅上与时变电压包络对准得越好,在功率放大器处可实现的性能(例如,效率和/或线性度)就越好。然而,由于一系列因素(例如,群延迟、阻抗失配等),时变ET电压可能在时间和/或振幅上与时变电压包络不对准。因此,期望始终保持时变电压与时变电压包络之间以及宽调制带宽内的良好对准。

发明内容

[0007] 本公开的实施例涉及收发器电路中的均衡滤波校准。收发器电路从时变调制向量生成射频(RF)信号,并且功率放大器电路基于已调制电压放大RF信号并将已放大RF信号提供到所耦合的RF前端电路(例如,滤波/多路复用器电路)。值得注意的是,当功率放大器电路耦合到RF前端电路时,功率放大器电路的输出反射系数(例如,S_{22})可以与RF前端电路的输入反射系数(例如,S_{11})相互作用,以在功率放大器电路的输出级上产生电压畸变滤波,这可能导致RF信号中不想要的畸变。在这方面,收发器电路被配置成将均衡滤波应用于时变调制向量,从而补偿功率放大器电路的输出级处的电压畸变滤波。在本文公开的实施例中,校准电路可以被配置成在功率放大器电路的调制带宽内的多个频率内校准均衡滤波,以生成增益偏移(LUT)和延迟LUT。因此,均衡滤波可以动态地适于减少由功率放大器电路的调

制带宽内的电压畸变滤波引起的不期望的瞬时过度压缩和/或频谱再生长。

[0008] 在一个方面,提供一种收发器电路。所述收发器电路包含存储器电路。所述收发器电路还包含校准电路。校准电路耦合到功率放大器电路。校准电路被配置成确定增益偏移LUT并将其存储在存储器电路中,以分别使功率放大器电路的调制带宽内的多个已校准频率与多个增益偏移相关。校准电路还被配置成确定延迟偏移LUT并将其存储在存储器电路中,以分别使多个已校准频率与多个延迟因数相关。

[0009] 在另一方面,提供了一种用于校准收发器电路中的均衡滤波的方法。所述方法包含确定并存储增益偏移LUT,以分别使调制带宽内的多个已校准频率与多个增益偏移相关。所述方法还包含确定并存储延迟偏移LUT,以分别使多个已校准频率与多个延迟因数相关。

[0010] 本领域技术人员在阅读以下对于优选实施例的具体说明以及相关的附图后,将会认识到本公开的范围并且了解其另外的方面。

附图说明

[0011] 并入本说明书中并形成本说明书的一部分的附图说明了本公开的几个方面,并且连同说明书一起用于解释本公开的原理。

[0012] 图1A是示例性现有发射电路的示意图,其中当功率放大器电路耦合到射频(RF)前端电路时可能在功率放大器电路上产生不需要的电压畸变滤波;

[0013] 图1B是提供图1A中的功率放大器电路的输出级的示例性图示的示意图;

[0014] 图2是示例性等效模型的示意图,提供因图1A中的功率放大器电路与RF前端电路14之间的耦合而产生的不需要的电压畸变滤波的示例性图示;

[0015] 图3是被配置成基于均衡滤波补偿图1A的现有发射电路中的不需要的电压畸变滤波的示例性发射电路的示意图;

[0016] 图4A-4C是提供关于为什么必须在发射电路的调制带宽内校准图3中的均衡滤波的示例性图示的图表;

[0017] 图5是示例性收发器电路的示意图,所述收发器电路可以根据本公开的实施例被配置成在图3的发射电路的调制带宽内校准均衡滤波;

[0018] 图6是可由图5的收发器电路用于校准均衡滤波的示例性校准过程的流程图;

[0019] 图7是作为图6的校准过程的一部分的可由图5的收发器电路用于确定增益偏移查找表(LUT)的示例性过程的流程图;

[0020] 图8A-8B是示出基于图6和7的过程执行的均衡滤波校准的影响的图表;

[0021] 图9是根据本公开的替代实施例的可由图5的收发器电路用于确定增益偏移LUT的示例性过程的流程图;并且

[0022] 图10是作为图6的校准过程的一部分的可由图5的收发器电路用于确定延迟LUT的示例性过程的流程图。

具体实施方式

[0023] 下文阐述的实施例表示使本领域技术人员能够实践实施例并且示出实践实施例的最佳模式所必需的信息。在根据附图阅读以下描述时,本领域技术人员将理解本公开的概念,并将认识到这些概念在此未特别述及的应用。应理解,这些概念和应用落入本公开和

所附权利要求的范围内。

[0024] 应理解,尽管术语第一、第二等在本文中可以用于描述各种元件,但这些元件不应受这些术语限制。这些术语仅用于区分一个元件与另一个元件。例如,在不脱离本公开的范围的情况下,第一元件可以被称为第二元件,并且类似地,第二元件可以被称为第一元件。如本文所用,术语“和/或”包含相关联所列项目中的一个或多个项目的任何和所有组合。

[0025] 应当理解,当例如层、区或衬底的元件被称为“在另一元件上”或“延伸到”另一元件上时,其可以直接在另一元件上或直接延伸到另一元件上,或者也可以存在中间元件。相反,当元件被称为“直接在另一元件上”或“直接延伸到另一元件上”时,不存在中间元件。同样,应理解,当例如层、区或衬底的元件被称为“在另一元件上方”或“在另一元件上方延伸”时,其可以直接在另一元件上方或直接在另一元件上方延伸,或者也可以存在中间元件。相反,当元件被称为“直接在另一元件上方”或“直接在另一元件上方”延伸时,不存在中间元件。还将理解,当元件被称为“连接”或“耦合”到另一元件时,其可以直接连接或耦合到另一元件,或者可以存在中间元件。相反,当元件被称为“直接连接”或“直接耦合”到另一元件时,不存在中间元件。

[0026] 例如“以下”或“以上”或“上”或“下”或“水平”或“竖直”的相对术语在本文中可以用于描述一个元件、层或区与如图所示的另一元件、层或区的关系。应理解,这些术语和上面讨论的那些旨在包括除附图中描绘的朝向之外的装置的不同朝向。

[0027] 本文所用的术语仅用于描述特定实施例的目的,并且不旨在限制本公开。如本文所用,除非上下文另外明确指示,否则单数形式“一(a/an)”和“所述”也旨在包含复数形式。还应理解,当在本文中使用时,项“包括(comprises/comprising)”和/或包含(includes/including)指定存在所述特征、整数、步骤、操作、元件和/或组件,但不排除存在或添加一个或多个其它特征、整数、步骤、操作、元件、组件和/或它们的群组。

[0028] 除非另外定义,否则本文使用的所有术语(包含技术和科学术语)具有与本公开所属领域的普通技术人员通常理解的相同含义。将进一步理解的是,除非本文明确地定义,否则本文使用的术语应被解释为具有与其在本说明书的上下文和相关技术中的含义一致的含义,并且将不以理想化或过于正式的意义来解释。

[0029] 本公开的实施例涉及收发器电路中的均衡滤波校准。收发器电路基于时变调制向量生成射频(RF)信号,并且功率放大器电路基于已调制电压放大RF信号并将已放大RF信号提供到所耦合的RF前端电路(例如,滤波/多路复用器电路)。值得注意的是,当功率放大器电路耦合到RF前端电路时,功率放大器电路的输出反射系数(例如,S_{22})可以与RF前端电路的输入反射系数(例如,S_{11})相互作用,以在功率放大器电路的输出级上产生电压畸变滤波,这可能导致RF信号中不想要的畸变。在这方面,收发器电路被配置成将均衡滤波应用于时变调制向量,从而补偿功率放大器电路的输出级处的电压畸变滤波。在本文公开的实施例中,校准电路可以被配置成在功率放大器电路的调制带宽内的多个频率内校准均衡滤波,以生成增益偏移(LUT)和延迟LUT。因此,均衡滤波可以动态地适于减少由功率放大器电路的调制带宽内的电压畸变滤波引起的不期望的瞬时过度压缩和/或频谱再生长。

[0030] 在论述根据本公开的收发器电路和校准过程之前,从图5开始,首先提供简要论述以帮助解释为什么需要校准现有发射电路中使用的均衡滤波以抑制不想要的电压畸变滤波。

[0031] 图1A是示例性现有发射电路10的示意图,其中当功率放大器电路12耦合到RF前端电路14时,呈现给功率放大器电路12的不想要的电压畸变滤波$H_{IV}(s)$可能导致功率放大器电路12中的存储器畸变。值得注意的是,在不想要的电压畸变滤波$H_{IV}(s)$中,“s”是拉普拉斯(Laplace)变换的表示。

[0032] 现有发射电路10包含收发器电路16、ETIC 18和发射器电路20,所述发射器电路可包含例如天线(未示出)。收发器电路16被配置成生成具有时变输入功率P_{IN}的RF信号22,并将RF信号22提供给功率放大器电路12。收发器电路16还被配置成生成时变目标电压V_{TGT},其跟踪RF信号22的时变输入功率P_{IN}。ETIC 18被配置成生成跟踪时变目标电压V_{TGT}的已调制电压V_{CC},并将已调制电压V_{CC}提供给功率放大器电路12。因此,功率放大器电路12可以根据时变输出电压V_{OUT}将RF信号22放大到时变输出功率P_{OUT}。接着,功率放大器电路12将放大的RF信号22提供到RF前端电路14。RF前端电路14可以是在将放大的RF信号22提供到发射器电路20以进行发射之前对放大的RF信号22执行进一步频率滤波的滤波电路。

[0033] 图1B是提供图1A中的功率放大器电路12的输出级24的示例性图示的示意图。图1A和1B之间的共同元件以共同的元件标号示出,并且本文将不再重新描述。

[0034] 输出级24可包含至少一个晶体管26,例如双极结晶体管(BJT)或互补金属氧化物半导体(CMOS)晶体管。以BJT为例,晶体管26可包含基电极B、集电极C和发射极E。基电极B被配置成接收偏置电压V_{BIAS},且集电极C被配置成接收已调制电压V_{CC}。集电极C还耦合到RF前端电路14,并且被配置成以输出电压V_{OUT}输出放大的RF信号22。在这方面,输出电压V_{OUT}可以取决于已调制电压V_{CC}。可以理解的是,当时变已调制电压V_{CC}与时变输入功率P_{IN}对准时,功率放大器电路12将以良好效率和线性度工作。

[0035] 图2是示例性等效模型28的示意图,提供因图1A的现有发射电路10中的功率放大器电路12与RF前端电路14之间的耦合而产生的电压畸变滤波$H_{IV}(s)$的示例性图示。图1A和1B中的元件在图2中被提及,且在本文中不再重新描述。

[0036] 在等效模型28中,V_{PA}和Z_{PA}分别表示功率放大器电路12的输出级24和功率放大器电路12的固有阻抗,并且Z_{11}表示与RF前端电路14的输入端口相关联的固有阻抗。在本文中,V_{OUT}表示在功率放大器电路12耦合到RF前端电路14之前与RF信号22相关联的输出电压,且V'_{OUT}表示在功率放大器电路12耦合到RF前端电路14之后与RF信号22相关联的输出电压。在下文中,输出电压V_{OUT}和V'_{OUT}分别被称为“非耦合输出电压”和“耦合输出电压”以进行区分。

[0037] 代表耦合输出电压V'_{OUT}的拉普拉斯变换可以下面等式(等式1)表示。

[0038] $$V'_{OUT}(s)=\frac{V_{OUT}(s)*[1-T_{PA}(s)]*[1+T_I(s)]}{2*[1-T_{PA}(s)*T_I(s)]}=V_{OUT}(s)*H_{IV}(s) \qquad (等式\ 1)$$

[0039] $$H_{IV}(s)=\frac{[1-T_{PA}(s)]*[1+T_I(s)]}{2*[1-T_{PA}(s)*T_I(s)]}$$

[0040] 在上述等式(等式1)中,$T_{PA}(s)$表示回望到功率放大器电路12的输出级24的反射系数,且$T_I(s)$表示到RF前端电路14的反射系数。值得注意的是,$T_{PA}(s)$和$T_I(s)$是含有振幅和相位信息的复杂滤波。在这方面,$T_{PA}(s)$、$T_I(s)$以及因此电压畸变滤波$H_{IV}(s)$取决于调制带宽、RF频率和/或电压驻波比(VSWR)等因素。

[0041] 等式(等式1)表明当功率放大器电路12耦合到RF前端电路14时,耦合输出电压V'_{OUT}将通过电压畸变滤波$H_{IV}(s)$将从非耦合输出电压V_{OUT}改变。因此,所耦合的输出电压

V'_{OUT}可能与已调制电压V_{CC}不对准,因此导致RF信号22中不想要的畸变。

[0042] 值得注意的是,可以修改已调制电压V_{CC}以补偿电压畸变滤波$H_{IV}(s)$,从而减小或消除未耦合的输出电压V_{OUT}与所耦合的输出电压V'_{OUT}之间的差。因此,可以减少由电压畸变滤波$H_{IV}(s)$引起的不期望的瞬时过度压缩和/或频谱再生长。

[0043] 在这方面,图3是被配置成基于均衡滤波$H_{ET}(s)$补偿图1A的现有发射电路10中的不想要的电压畸变滤波$H_{IV}(s)$的示例性发射电路30的示意图。发射电路30被配置成发射在广泛范围的调制带宽中调制的RF信号32。在非限制性实例中,RF信号32可以在200MHz或更高的调制带宽中调制,并且在毫米波RF频谱中发射。

[0044] 发射电路30包含收发器电路34、功率放大器电路36和ETIC 38。功率放大器电路36经由RF前端电路42耦合到发射器电路40。在非限制性实例中,RF前端电路42可以包含滤波电路和多路复用器电路(未示出)中的一个或多个。滤波电路可以被配置成包含滤波网络,例如具有尖锐截止频率的滤波网络。功率放大器电路36可以与图1B中的功率放大器电路12相同或功能上等效。因此,功率放大器电路36还可以包含如功率放大器电路12中的输出级24。

[0045] 收发器电路34包含信号处理电路44和目标电压电路46。信号处理电路44被配置成从时变调制向量$\vec{b}_{MOD}$生成RF信号32。时变调制向量$\vec{b}_{MOD}$可由收发器电路34中的数字基带电路(未示出)生成,并且包含同相(I)和正交(Q)分量两者。目标电压电路46被配置成检测来自时变调制向量$\vec{b}_{MOD}$的RF信号32的时变振幅包络$\sqrt{I^2+Q^2}$。因此,目标电压电路46可以基于检测到的时变振幅包络$\sqrt{I^2+Q^2}$生成已调制目标电压V_{TGT}。

[0046] ETIC 38被配置成基于已调制目标电压V_{TGT}生成已调制电压V_{CC},并将已调制电压V_{CC}提供给功率放大器电路36。功率放大器电路36继而基于已调制电压V_{CC}将RF信号32放大到输出电压V_{OUT},以供经由RF前端电路42和发射器电路40发射。

[0047] 如先前所描述,输出电压V_{OUT}取决于已调制电压V_{CC}。在这方面,有可能通过生成已调制电压V_{CC}以补偿电压畸变滤波$H_{IV}(s)$来减小或甚至消除未耦合的输出电压V_{OUT}与所耦合的输出电压V'_{OUT}之间的差。考虑到ETIC 38被配置成基于已调制目标电压V_{TGT}生成已调制电压V_{CC},因此有可能通过生成已调制目标电压V_{TGT}以补偿电压畸变滤波$H_{IV}(s)$来减小或甚至消除未耦合的输出电压V_{OUT}与所耦合的输出电压V'_{OUT}之间的差。

[0048] 在这方面,收发器电路34进一步包含均衡器电路48。均衡器电路48被配置成在目标电压电路46生成已调制目标电压V_{TGT}之前将均衡滤波$H_{ET}(s)$应用于时变调制向量$\vec{b}_{MOD}$。在实施例中,均衡滤波$H_{ET}(s)$可以通过下面的等式(等式2)来描述。

[0049] $$H_{ET}(s)=H_{IQ}(s)*H_{PA}(s)*H_{IV}(s) \quad \text{(等式2)}$$

[0050] 在上述等式(等式2)中,$H_{IQ}(s)$表示信号处理电路44的传递函数,并且$H_{PA}(s)$表示功率放大器电路36的电压增益传递函数。在这方面,均衡滤波$H_{ET}(s)$被配置成匹配组合信号路径滤波,所述组合信号路径滤波包含传递函数$H_{IQ}(s)$、电压增益传递函数$H_{PA}(s)$和电压畸变滤波$H_{IV}(s)$。

[0051] 在实施例中,均衡器电路48将均衡滤波$H_{ET}(s)$应用于时变调制向量$\vec{b}_{MOD}$以生成均衡的时变调制向量$\vec{b}_{MOD-E}$,并将均衡的时变调制向量$\vec{b}_{MOD-E}$→提供给目标电压电路46。目标电压电路46继而检测来自均衡的时变调制向量$\vec{b}_{MOD-E}$的时变振幅包络$\sqrt{I^2+Q^2}$,并且基于

检测到的时变振幅包络$\sqrt{I^2+Q^2}$生成已调制目标电压V_{TGT}。由于已调制目标电压V_{TGT}是由均衡的时变调制向量$\vec{b}_{MOD-E}$生成,因此已调制目标电压V_{TGT}以及因此已调制电压V_{CC}将能够补偿电压畸变滤波$H_{IV}(s)$,所述电压畸变滤波是通过将功率放大器电路36与RF前端电路42耦合而在功率放大器电路36的输出级24上产生。

[0052] 在实施例中,目标电压电路46包含振幅检测器电路50、ET LUT电路52和数/模转换器(DAC)54。振幅检测器电路50被配置成检测来自均衡的时变调制向量$\vec{b}_{MOD-E}$的时变振幅包络$\sqrt{I^2+Q^2}$。可包含使时变振幅包络$\sqrt{I^2+Q^2}$与各种电压电平相关的isogain LUT(未示出)的ET LUT电路52被配置成基于检测到的时变振幅包络$\sqrt{I^2+Q^2}$生成时变数字目标电压V_{DTGT}。DAC 54被配置成将时变数字目标电压V_{DTGT}转换成已调制目标电压V_{TGT},并且将已调制目标电压V_{TGT}提供到ETIC 38。

[0053] 在实施例中,信号处理电路44可包含存储器数字预失真(mDPD)电路56和调制器电路58。mDPD电路56被配置成接收时变调制向量$\vec{b}_{MOD-E}$,并且以数字方式使时变调制向量$\vec{b}_{MOD-E}$预失真以生成预失真的时变调制向量$\vec{b}_{MOD-DPD}$。调制器电路58被配置成从预失真的时变调制向量$\vec{b}_{MOD-DPD}$生成RF信号32,并且将RF信号32提供到功率放大器电路36。

[0054] 如前所述,RF信号32可以在广泛范围的调制带宽中调制。本文中,调制带宽是指RF信号32可以被调制到和/或发射电路30被配置成处理的RF频率范围。例如,如果RF信号32可以在2554MHz与2654MHz之间调制,则调制带宽将为100MHz并且调制带宽的中心频率(F_C)将为2604MHz。因此,调制带宽内的任何其它频率将被视为非中心频率(F_{NC})(2554MHz≦F_{NC}<2604MHz且2604MHz<F_{NC}≦2654MHz)。下文中,RF信号32的调制带宽可互换地称为发射电路30的调制带宽。

[0055] 在这方面,均衡滤波$H_{ET}(s)$需要抑制整个调制带宽内的电压畸变滤波$H_{IV}(s)$。然而,由于ET LUT电路52中的isogain LUT通常是基于调制带宽内的中心频率而确定,因此ET LUT电路52中的isogain LUT可能无法针对调制带宽内的所有其它频率提供恒定的isogain。因此,必须校准均衡滤波$H_{ET}(s)$以确保基于中心频率而确定的isogain LUT可以在调制带宽内的所有频率内提供恒定的isogain。

[0056] 图4A-4C是提供关于为什么必须在发射电路30的调制带宽内校准图3中的均衡滤波$H_{ET}(s)$的示例性图示的图表。图4A-4C之间的共同元件以共同的元件标号示出,并且本文将不再重新描述。

[0057] 图4A示出了对应于发射电路30的调制带宽内的中心频率F_C的中心频率LUT 60和对应于发射电路30的调制带宽内的非中心频率F_{NC}的非中心频率LUT 62。

[0058] 图4B示出了由中心频率LUT 60提供的中心频率增益64和由非中心频率LUT 62提供的非中心频率增益66。如图所示,当RF信号32在中心频率F_C下调制并且针对中心频率F_C具有在-25dBm与3dBm之间的输入功率P_{IN}时,中心频率LUT 60可以提供30dB的恒定增益。另一方面,当RF信号32在非中心频率F_{NC}下调制并且具有在-25dBm与4dBm之间的输入功率P_{IN}时,非中心频率LUT 62可以提供29dB的恒定增益。在这方面,如果ET LUT电路52采用中心频率LUT 60和非中心频率LUT 62两者,则当RF信号32在中心频率F_C和非中心频率F_{NC}两者下调制时,将有可能实现恒定增益。

[0059] 然而,当ET LUT电路52仅采用中心频率LUT 60时,非中心频率LUT 62将无法在非中心频率F_{NC}下维持29dB的恒定增益。如图4C所示,图4A中的中心频率LUT 60在-25dBm与+2dBm之间提供29.4dB到30.5dB的变化增益,但当RF信号32在非中心频率F_{NC}下调制时不提供29dB的恒定增益。因此,期望校准均衡滤波$H_{ET}(s)$以确保中心频率LUT 60可以在RF信号32的调制带宽内的中心和非中心频率内提供恒定增益。

[0060] 在这方面,图5是示例性收发器电路68的示意图,所述收发器电路可以根据本公开的实施例被配置成在图3的发射电路的调制带宽内校准均衡滤波$H_{ET}(s)$。图3与5之间的共同元件以共同的元件标号示出,并且本文将不再重新描述。在实施例中,收发器电路68可用在发射电路30中以替换收发器电路34。

[0061] 在实施例中,收发器电路68包含存储器电路70。例如,可包含如随机存取存储器(RAM)、快闪存储装置、固态硬盘(SSD)等存储电路的存储器电路70被配置成存储增益偏移LUT 72和延迟LUT 74。在非限制性实例中,增益偏移LUT 72包含多个增益偏移条目76(1)-76(N),每个增益偏移条目被配置成用多个增益偏移ΔG_1-ΔG_N中的相应一个校正调制带宽内的多个已校准频率F_1-F_N中的相应一个。本文中,已校准频率F_1-F_N包含在调制带宽内的所有非中心频率(F_{NC})和中心频率(F_C)。在另一非限制性实例中,延迟LUT 74包含多个延迟条目78(1)-78(N),每个延迟条目被配置成使已校准频率F_1-F_N中的相应一个与多个延迟因数τ_1-τ_N中的相应一个相关。

[0062] 在实施例中,收发器电路68可以被配置成包含校准电路80,其可以例如是现场可编程门阵列(FPGA)。尽管如本文中所说明,校准电路80设置在收发器电路68内部,但应了解,校准电路80可以与收发器电路68分离,但经由例如通用输入/输出(GPIO)接口耦合到收发器电路68。如下文所论述,校准电路80可以被配置成确定并填充增益偏移LUT 72和延迟LUT 74,使得均衡滤波$H_{ET}(s)$可被校准以使ET LUT电路52基于例如图4A中的中心频率LUT 60在所有已校准频率F_1-F_N内提供恒定增益。

[0063] 校准电路80可以被配置成基于过程校准均衡滤波$H_{ET}(s)$。在这方面,图6是可由图5的收发器电路68中的校准电路80用于校准均衡滤波$H_{ET}(s)$的示例性校准过程200的流程图。

[0064] 本文中,校准电路80首先被配置成确定并存储包含增益偏移条目76(1)-76(N)的增益偏移LUT 72,其中增益偏移条目76(1)-76(N)中的每一个被配置成使调制带宽内的已校准频率F_1-F_N中的相应一个与增益偏移ΔG_1-ΔG_N中的相应一个相关(步骤202)。接下来,校准电路80被配置成确定并存储包含延迟条目78(1)-78(N)的延迟LUT 74,其中延迟条目78(1)-78(N)中的每一个被配置成使已校准频率F_1-F_N中的相应一个与延迟因数τ_1-τ_N中的相应一个相关(步骤204)。

[0065] 在实施例中,校准电路80可以基于过程确定增益偏移LUT 72并将其存储在存储器电路70中(步骤202)。在这方面,图7是作为图6的校准过程200的一部分的可由图5的收发器电路68中的校准电路80用于确定增益偏移LUT 72的示例性过程206的流程图。图5中的元件连同图7的论述一起被提及,且在本文中将不再重新描述。

[0066] 本文中,校准电路80被配置成基于功率放大器电路36的效率目标、噪声目标和/或线性度目标来确定最小参考电压V_{CC-REF}和最小参考输入功率P_{IN-REF}(步骤208)。换句话说,可以凭经验确定最小参考电压V_{CC-REF}和最小参考输入功率P_{IN-REF}以实现功率放大器电路36的效率目标、噪声目标和/或线性度目标之间的期望折衷。尽管校准电路80在本文中被配置成

确定最小参考输入功率P_{IN-REF},但应了解,也可以用对应输出功率替换输入功率$P_{IN-}REF$。

[0067] 校准电路80接着确定功率放大器电路36的调制带宽内的已校准频率F_1-F_N当中的参考频率F_{REF}(步骤210)。在非限制性实例中,参考频率F_{REF}可以是已校准频率F_1-F_N当中的中心频率F_C。

[0068] 接下来,校准电路80基于待提供到功率放大器电路36用于放大图3的发射电路30中的RF信号32的已调制电压V_{CC}(例如,2.5V)的预期均方根(RMS)来确定参考目标电压($V_{TGT-REF}$)(步骤212)。

[0069] 接下来,校准电路80选择调制带宽内的已校准频率F_1-F_N当中的已校准频率F_i(步骤214)。校准电路80接着基于最小参考电压V_{CC-REF}确定当功率放大器电路36放大在选定已校准频率F_i和最小参考输入功率P_{IN-REF}下生成的测试信号82时功率放大器电路36的相应增益G_i(步骤216)。值得注意的是,测试信号82可以由校准电路80或单独的信号发生器(未示出)生成。在非限制性实例中,校准电路80可以测量功率放大器电路36的输出功率P_{OUT},并且基于所测得的输出功率P_{OUT}和所确定的最小参考输入功率P_{IN-REF}确定相应参考增益G_{REF}。随后,校准电路80可以确定可使功率放大器电路36在以选定已校准频率F_i放大RF信号32时具有相应增益G_i的相应已调制电压V_{CCj}($1 \leqq j \leqq M$)和相应输入功率P_{INj}($1 \leqq j \leqq M$)(步骤218)。本文中,M可以与N相同或不同。因此,校准电路80可以将相应已调制电压V_{CCj}和相应输入功率P_{INj}存储在存储器电路70中的临时电压LUT(未示出)中(步骤220)。校准电路80被配置成针对已校准频率F_1-F_N中的每一个重复步骤214-220。

[0070] 继续参考图7,校准电路80再次选择调制带宽内的已校准频率F_1-F_N当中的已校准频率F_i($1 \leqq i \leqq N$)(步骤222)。校准电路80接着确定相对于与等于参考目标电压$V_{TGT-REF}$的已调制电压V_{CCj}相关联的临时电压LUT中的输入功率P_{INj}($1 \leqq j \leqq M$)的相应调整后输入功率$P_{IN-ADJi}$($1 \leqq i \leqq N$)(步骤224)。随后,校准电路80确定参考频率F_{REF}处的相应调整后输入功率与选定已校准频率F_i处的相应调整后输入功率$P_{IN-ADJi}$之间的相应增益偏移ΔG_i($1 \leqq i \leqq N$)(步骤226)。校准电路80接着将选定已校准频率Fi与相应增益偏移ΔG_i相关联地存储在增益偏移LUT 72中(步骤228)。值得注意的是,校准电路80被配置成针对已校准频率F_1-F_N中的每一个重复步骤222-228。

[0071] 返回参考图5,针对已校准频率F_1-F_N中的每一个,均衡器电路48被配置成基于增益偏移LUT 72生成均衡滤波HET(s),并将均衡滤波$H_{ET}(s)$应用于时变调制向量$\vec{b}_{MOD}$以生成均衡的时变调制向量$\vec{b}_{MOD-E}$。图8A-8B是示出基于图6的过程200和图7的过程206执行的均衡滤波校准的影响的图表。

[0072] 图8A示出了对应于已校准频率F_1-F_N中的中心频率F_C的中心频率LUT 84和对应于校准频率F_1-F_N中的非中心频率F_{NC}的非中心频率LUT 86。值得注意的是,中心频率LUT 84和非中心频率LUT 86均基于相同的最小参考电压V_{CC-REF}和相同的最小参考输入功率P_{IN-REF}。中心频率LUT 84将存储在发射电路30中的ET LUT电路52中,用于从检测到的时变振幅包络$\sqrt{I^2+Q^2}$生成时变数字目标电压V_{DTGT}。另一方面,非中心频率LUT 86不存储在ET LUT电路52中,并且可以被视为“虚拟”LUT。均衡滤波$H_{ET}(s)$可以使用非中心频率F_{NC}中的对应增益偏移ΔG_i($1 \leqq i \leqq N$)将非中心频率LUT 86叠加在中心频率LUT 84上。如图8A中可见,其等效于使非中心频率LUT 86左移以与中心频率LUT 84重叠。因此,如图8B中所示,中心频率增益88和

非中心频率增益90都是相对恒定的。

[0073] 在实施例中,校准电路80可以基于替代过程确定增益偏移LUT 72并将其存储在存储器电路70中(步骤202)。在这方面,图9是根据本公开的另一实施例的可由图5的收发器电路68中的校准电路80用于确定增益偏移LUT 72的示例性过程230的流程图。图5中的元件连同图9的论述一起被提及,且在本文中将不再重新描述。

[0074] 本文中,校准电路80被配置成基于功率放大器电路36的效率目标和/或噪声目标来确定参考电压V_{CC-REF}和参考输入功率P_{IN-REF}(步骤232)。换句话说,可以凭经验确定参考电压V_{CC-REF}和参考输入功率P_{IN-REF}以实现功率放大器电路36的效率目标与噪声目标之间的期望折衷。尽管校准电路80在本文中被配置成确定参考输入功率P_{IN-REF},但应了解,也可以用对应参考输出功率替换参考输入功率P_{IN-REF}。

[0075] 校准电路80接着确定功率放大器电路36的调制带宽内的已校准频率F_1-F_N当中的参考频率F_{REF}(步骤234)。在非限制性实例中,参考频率F_{REF}可以是已校准频率F_1-F_N当中的中心频率F_C。

[0076] 接下来,校准电路80基于待提供到功率放大器电路36用于放大图3的发射电路30中的RF信号32的已调制电压V_{CC}(例如,2.5V)的预期RMS来确定参考目标电压($V_{TGT-REF}$)(步骤236)。

[0077] 接下来,校准电路80选择调制带宽内的已校准频率F_1-F_N当中的已校准频率F_i(步骤238)。校准电路80基于参考电压V_{CC-REF}确定当功率放大器电路36放大在选定已校准频率F_i和参考输入功率P_{IN-REF}下生成的测试信号82时功率放大器电路36的相应增益G_i($1 \leqq i \leqq N$)(步骤240)。

[0078] 校准电路80接着基于所确定的压缩增益G_{CMP}调整相应增益G_i以确定已压缩参考增益$G_{REF-CMP}$(步骤242)。值得注意的是,校准电路80可以凭经验确定已压缩增益G_{CMP}以实现功率放大器电路36的期望线性度目标。

[0079] 校准电路80接着确定将使功率放大器电路36在以选定已校准频率F_i放大测试信号82时具有已压缩参考增益$G_{REF-CMP}$的相应已调制电压V_{CCj}($1 \leqq j \leqq M$)和相应输入功率P_{INj}($1 \leqq j \leqq M$)(步骤244)。本文中,M可以与N相同或不同。因此,校准电路80可以将相应已调制电压V_{CCj}和相应输入功率P_{INj}存储在存储器电路70中的临时电压LUT(未示出)中(步骤246)。校准电路80被配置成针对已校准频率F_1-F_N中的每一个重复步骤238-246。

[0080] 继续参考图9,校准电路80选择调制带宽内的已校准频率F_1-F_N当中的已校准频率F_i($1 \leqq i \leqq N$)(步骤248)。校准电路80接着确定相对于与等于参考目标电压$V_{TGT-REF}$的已调制电压V_{CCj}($1 \leqq j \leqq M$)相关联的临时电压LUT中的输入功率P_{INj}($1 \leqq j \leqq M$)的相应调整后输入功率$P_{IN-ADJi}$($1 \leqq i \leqq N$)(步骤250)。

[0081] 随后,校准电路80确定参考频率F_{REF}处的相应调整后输入功率与选定已校准频率F_i处的相应调整后输入功率$P_{IN-ADJi}$之间的相应增益偏移ΔG_i($1 \leqq i \leqq N$)(步骤252)。校准电路80接着将选定已校准频率Fi与相应增益偏移G_i相关联地存储在增益偏移LUT 72中(步骤254)。值得注意的是,校准电路80被配置成针对已校准频率F_1-F_N中的每一个重复步骤248-254。

[0082] 在实施例中,校准电路80可以基于过程确定延迟LUT 74并将其存储在存储器电路70中(步骤204)。在这方面,图10是作为图6的校准过程200的一部分的可由图5的收发器电

路68用于确定延迟LUT 74的示例性过程256的流程图。图5中的元件连同图10的论述一起被提及,且在本文中将不再重新描述。

[0083] 本文中,校准电路80首先确定任意延迟偏移Δt(步骤258)。接下来,校准电路80选择调制带宽内的已校准频率F_1-F_N当中的已校准频率F_i(1≦i≦N)(步骤260)。校准电路80接着确定任意延迟因数τ(步骤264)。校准电路80接着分别测量当功率放大器电路36放大在选定已校准频率F_i下生成且延迟τ±Δt的测试信号82时功率放大器电路36的一对输出功率P_{OUT1}、P_{OUT2}(步骤264)。

[0084] 校准电路80检查一对输出功率P_{OUT1}和P_{OUT2}是否相等(步骤266)。在实施例中,如果一对输出功率P_{OUT1}和P_{OUT2}之间的差小于预定义阈值,则校准电路80可以将一对输出功率P_{OUT1}和P_{OUT2}视为相等。

[0085] 如果一对输出功率P_{OUT1}和P_{OUT2}相等,则校准电路80将选定已校准频率F_i与任意延迟因数τ相关联地存储在延迟LUT 74中(步骤268)。否则,校准电路80将返回到步骤262并确定新的任意延迟因数τ。在一对输出功率P_{OUT1}和P_{OUT2}在数次迭代之后仍不相等的情况下,校准电路80可以调整(例如,增加)预定义阈值。值得注意的是,校准电路80被配置成针对已校准频率F_1-F_N中的每一个重复步骤260-268。

[0086] 本领域的技术人员将认识到对本公开的优选实施例的改进和修改。所有这种改进和修改都被认为是在本文所公开的概念和下文的权利要求的距离内。

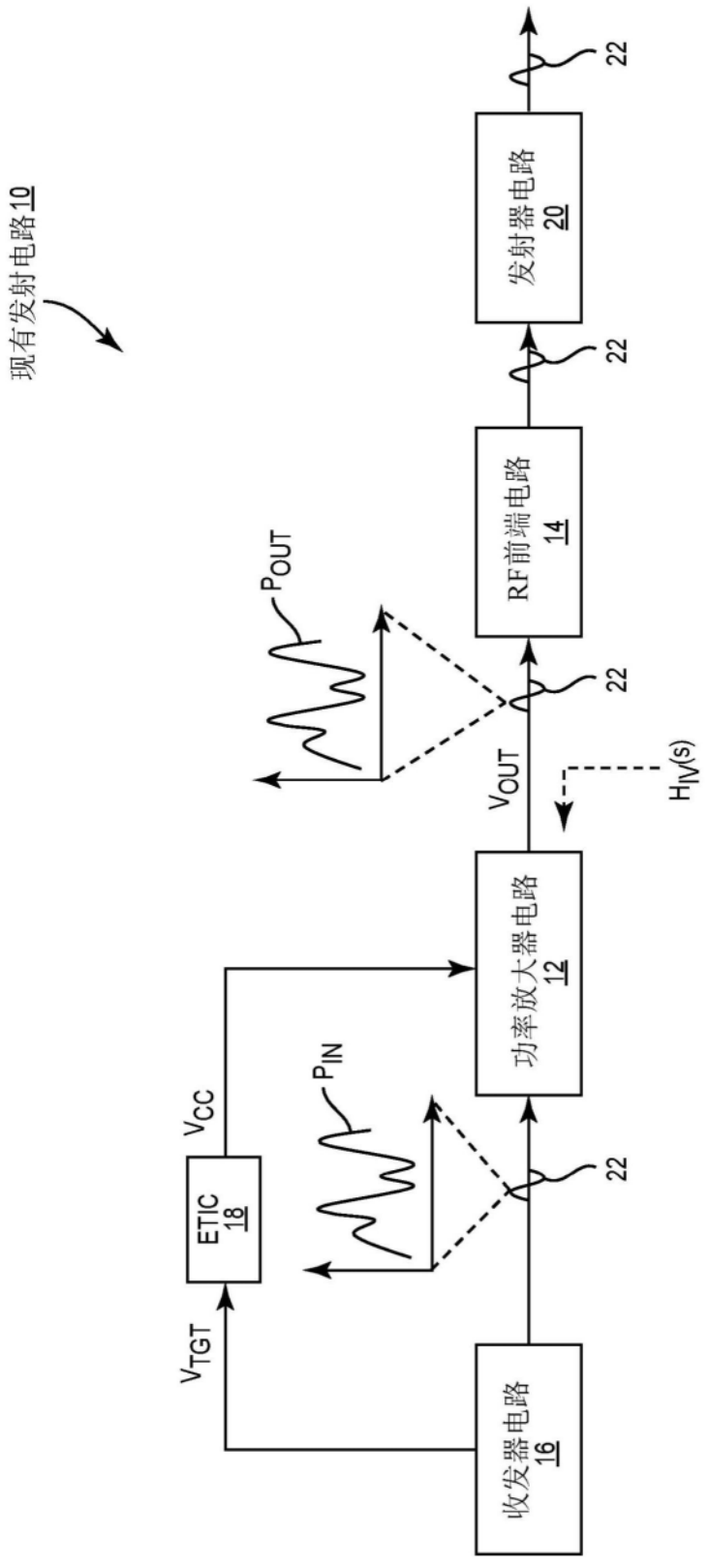

现有发射电路10
收发器电路
16
ETIC
18
VTGT
VCC
PIN
功率放大器电路
12
VOUT
HV(s)
POUT
RF前端电路
14
发射器电路
20
22

图1A(相关技术)

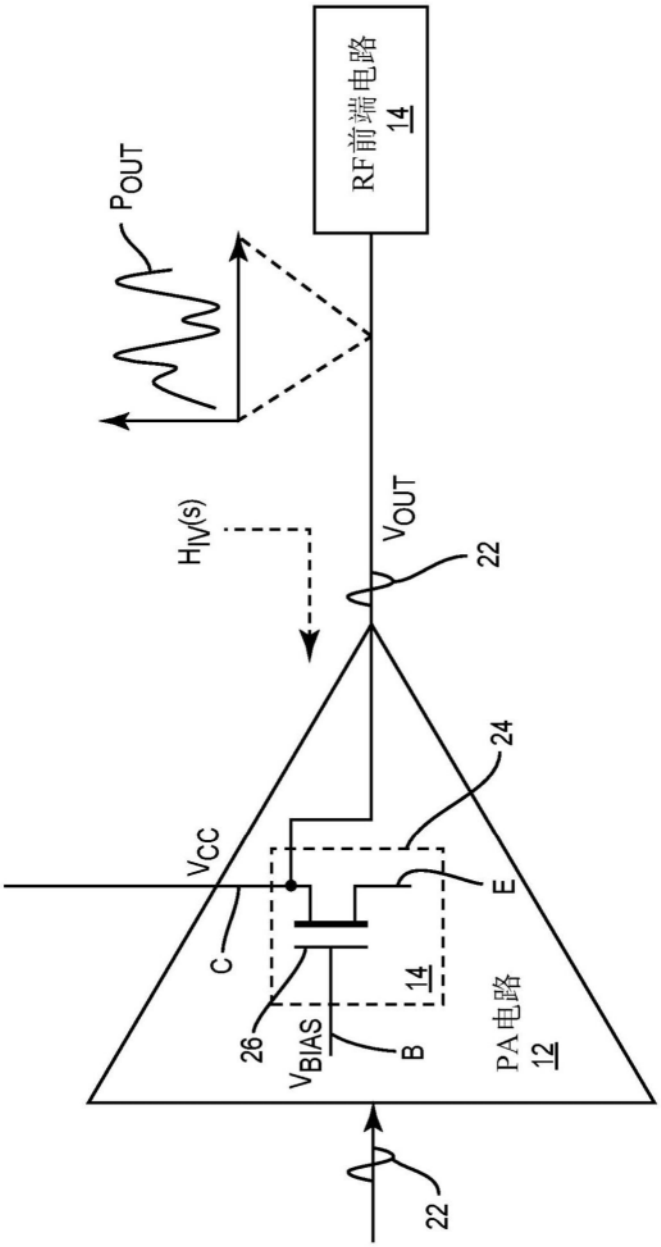


图1B(相关技术)

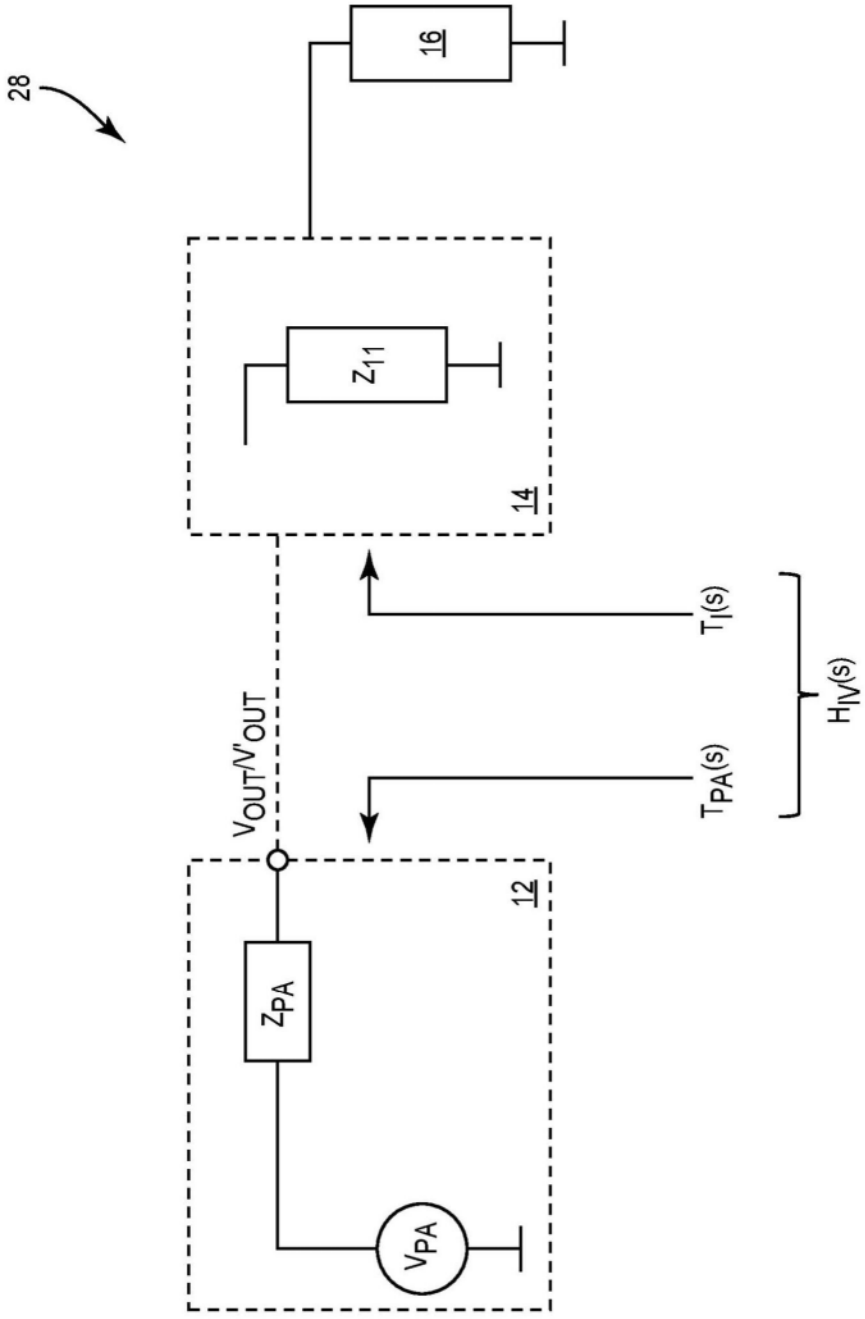


图2(相关技术)

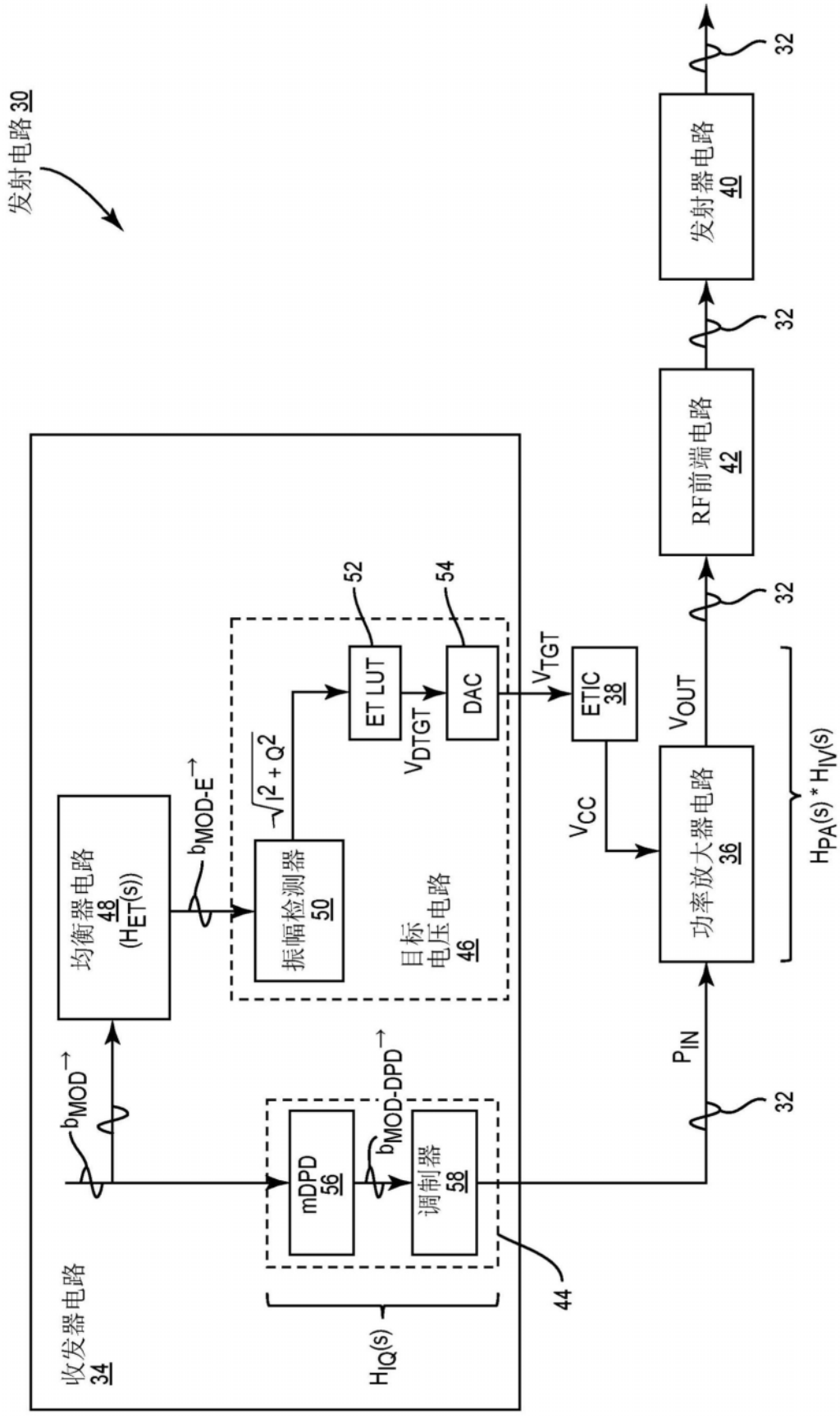

发射电路 30
收发器电路 34
均衡器电路 48 ($H_{ET}(s)$)
b_{MOD}
b_{MOD-E}
$\sqrt{I^2+Q^2}$
振幅检测器 50
目标电压电路 46
52
ET LUT
54
DAC
V_{DTGT}
V_{TGT}
ETIC 38
V_{CC}
mDPD 56
$b_{MOD-DPD}$
调制器 58
$H_{IQ}(s)$
44
P_{IN}
功率放大器电路 36
V_{OUT}
$H_{PA}(s) * H_{IV}(s)$
RF前端电路 42
发射器电路 40
32

图3(相关技术)

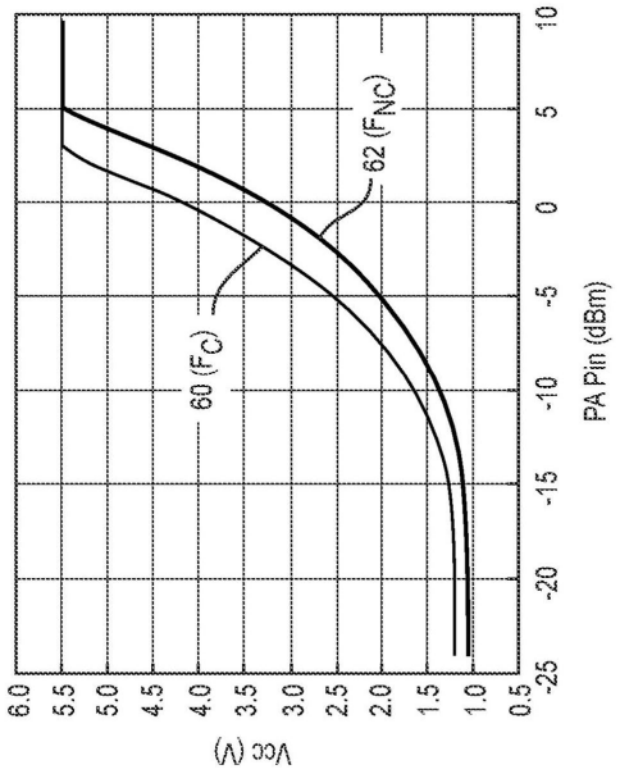


图4A(相关技术)

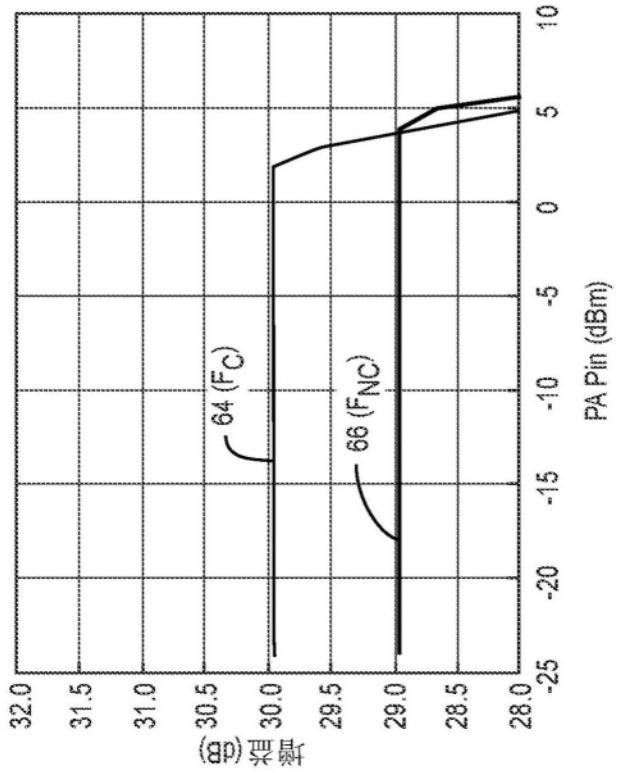


图4B(相关技术)

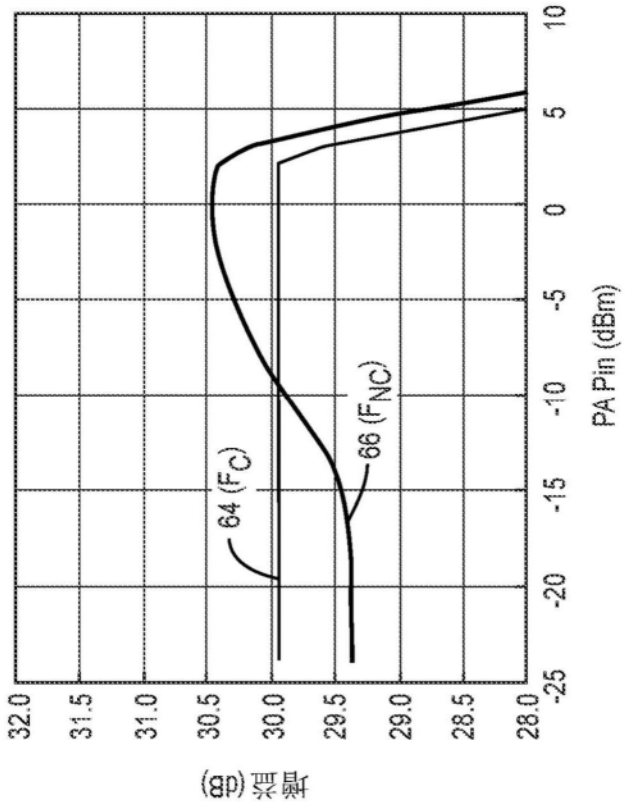

增益(dB)
32.0
31.5
31.0
30.5
30.0
29.5
29.0
28.5
28.0
PA Pin (dBm)
10
5
0
-5
-10
-15
-20
-25
64 (F_C)
66 (F_{NC})

图4C(相关技术)

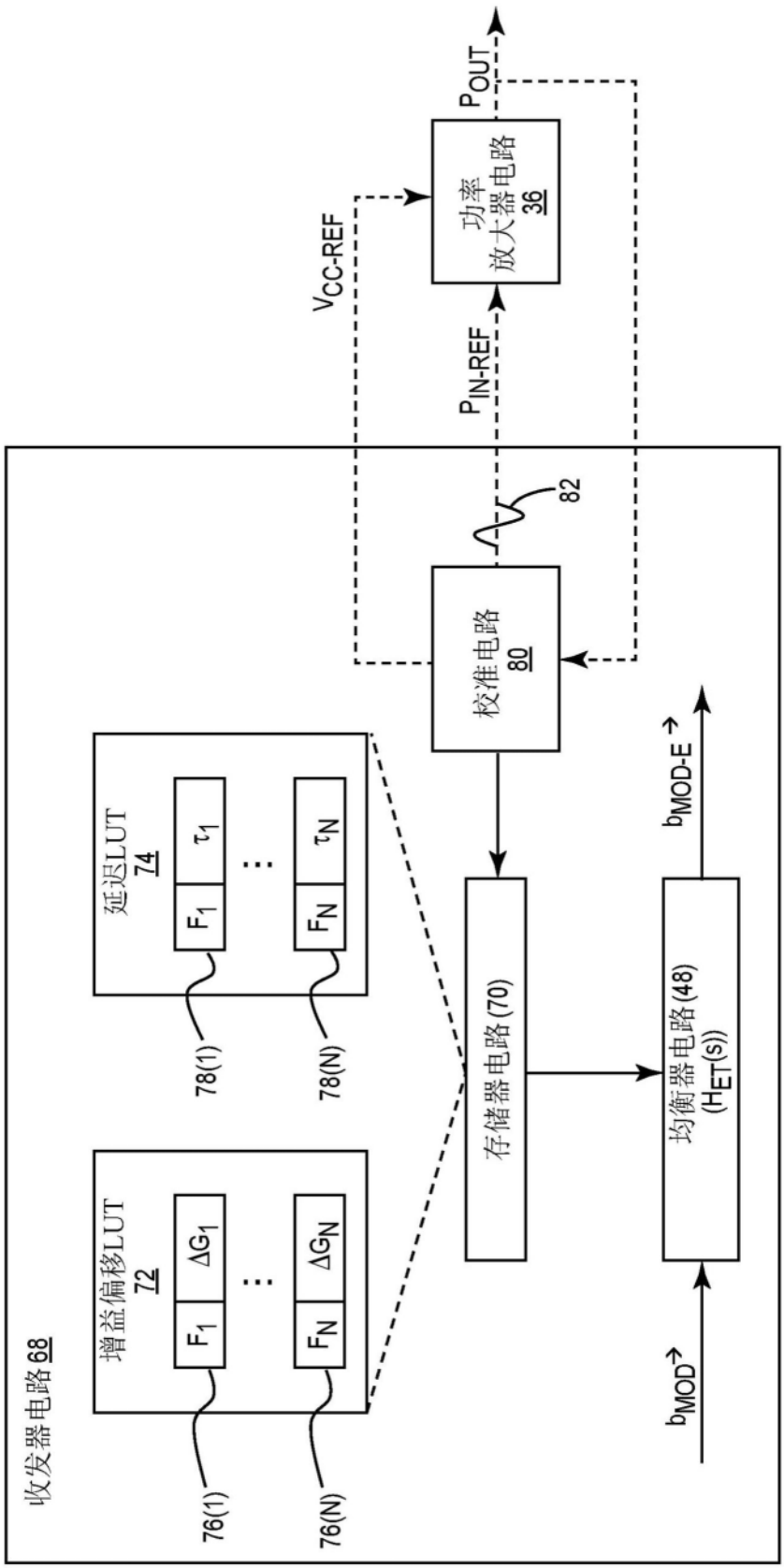

收发器电路 68
增益偏移LUT 72
F1
ΔG1
FN
ΔGN
76(1)
76(N)
延迟LUT 74
F1
τ1
FN
τN
78(1)
78(N)
存储器电路(70)
校准电路 80
82
功率放大器电路 36
VCC-REF
PIN-REF
POUT
均衡器电路(48) (HET(s))
bMOD
bMOD-E

图5

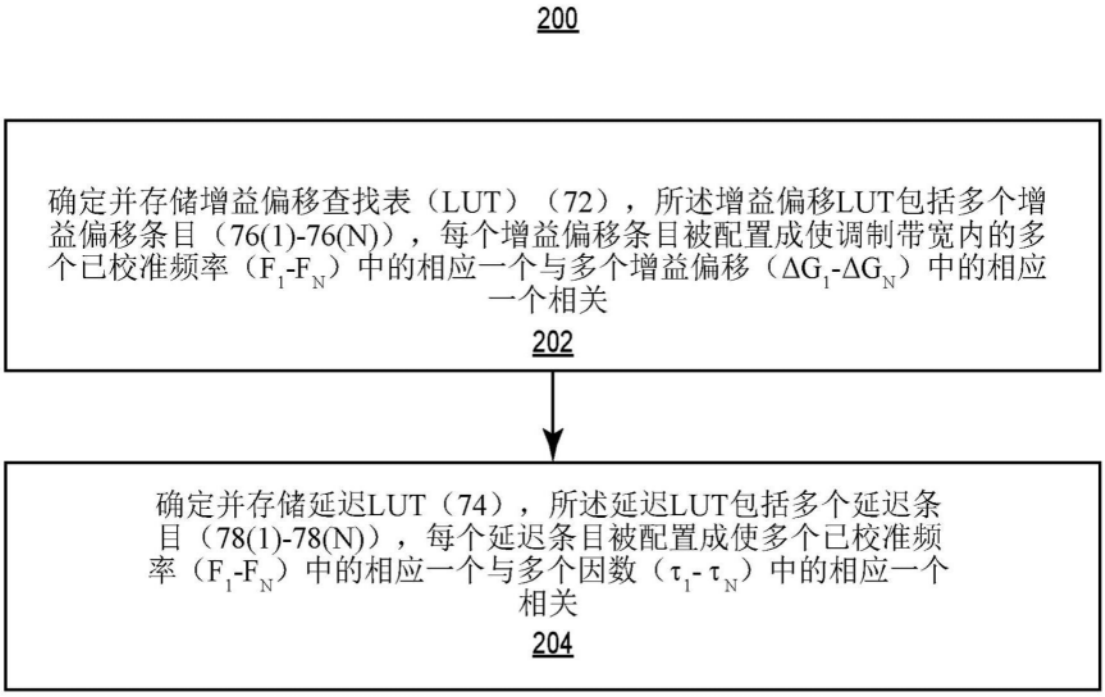

200
确定并存储增益偏移查找表（LUT）（72），所述增益偏移LUT包括多个增益偏移条目（76(1)-76(N)），每个增益偏移条目被配置成使调制带宽内的多个已校准频率（F_1-F_N）中的相应一个与多个增益偏移（ΔG_1-ΔG_N）中的相应一个相关
202
确定并存储延迟LUT（74），所述延迟LUT包括多个延迟条目（78(1)-78(N)），每个延迟条目被配置成使多个已校准频率（F_1-F_N）中的相应一个与多个因数（τ_1-τ_N）中的相应一个相关
204

图6

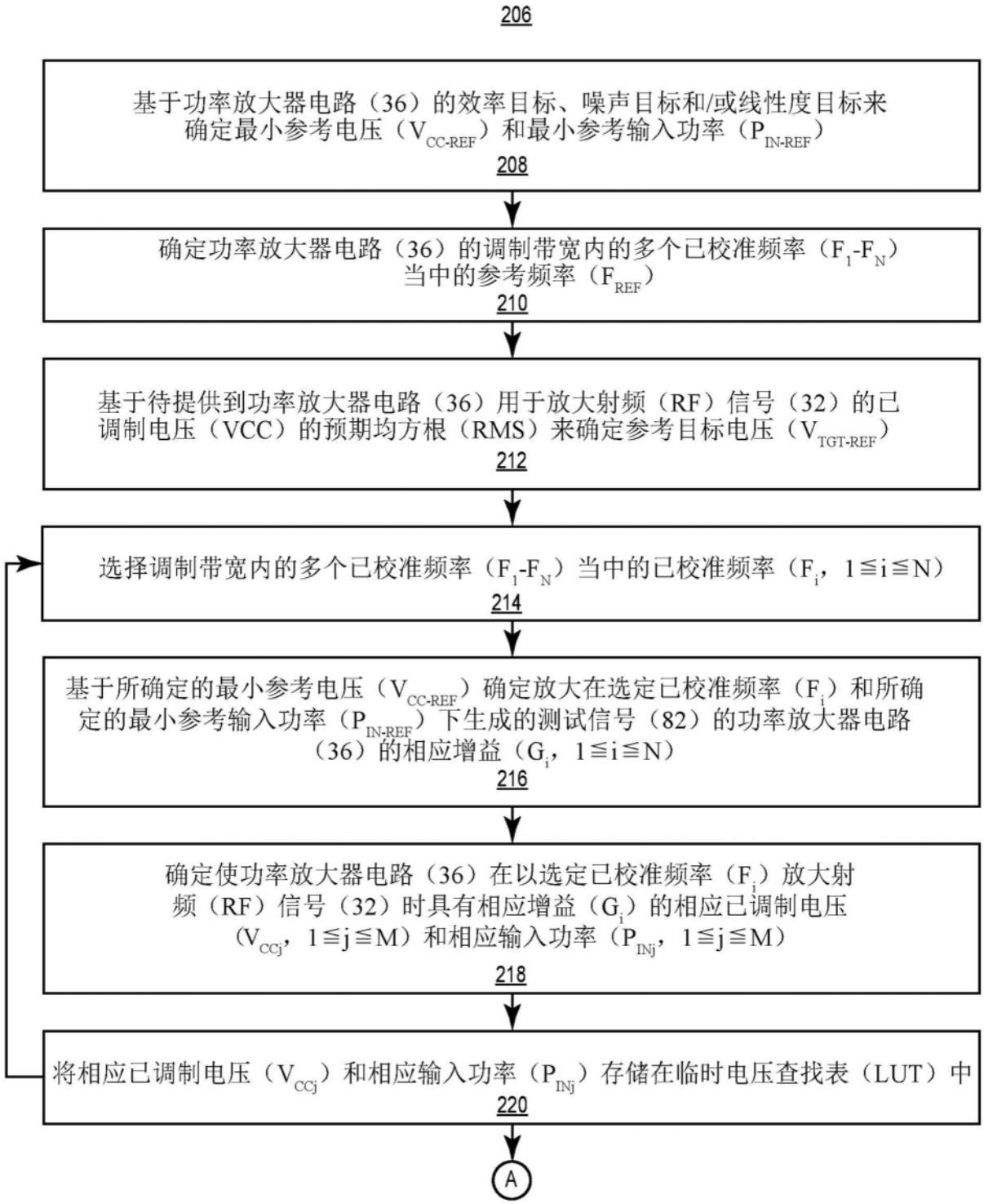

206
基于功率放大器电路（36）的效率目标、噪声目标和/或线性度目标来确定最小参考电压（V_{CC-REF}）和最小参考输入功率（P_{IN-REF}）
208
确定功率放大器电路（36）的调制带宽内的多个已校准频率（F_1-F_N）当中的参考频率（F_{REF}）
210
基于待提供到功率放大器电路（36）用于放大射频（RF）信号（32）的已调制电压（VCC）的预期均方根（RMS）来确定参考目标电压（$V_{TGT-REF}$）
212
选择调制带宽内的多个已校准频率（F_1-F_N）当中的已校准频率（F_i，$1 \leqq i \leqq N$）
214
基于所确定的最小参考电压（V_{CC-REF}）确定放大在选定已校准频率（F_i）和所确定的最小参考输入功率（P_{IN-REF}）下生成的测试信号（82）的功率放大器电路（36）的相应增益（G_i，$1 \leqq i \leqq N$）
216
确定使功率放大器电路（36）在以选定已校准频率（F_i）放大射频（RF）信号（32）时具有相应增益（G_i）的相应已调制电压（V_{CCj}，$1 \leqq j \leqq M$）和相应输入功率（P_{INj}，$1 \leqq j \leqq M$）
218
将相应已调制电压（V_{CCj}）和相应输入功率（P_{INj}）存储在临时电压查找表（LUT）中
220
A

图7

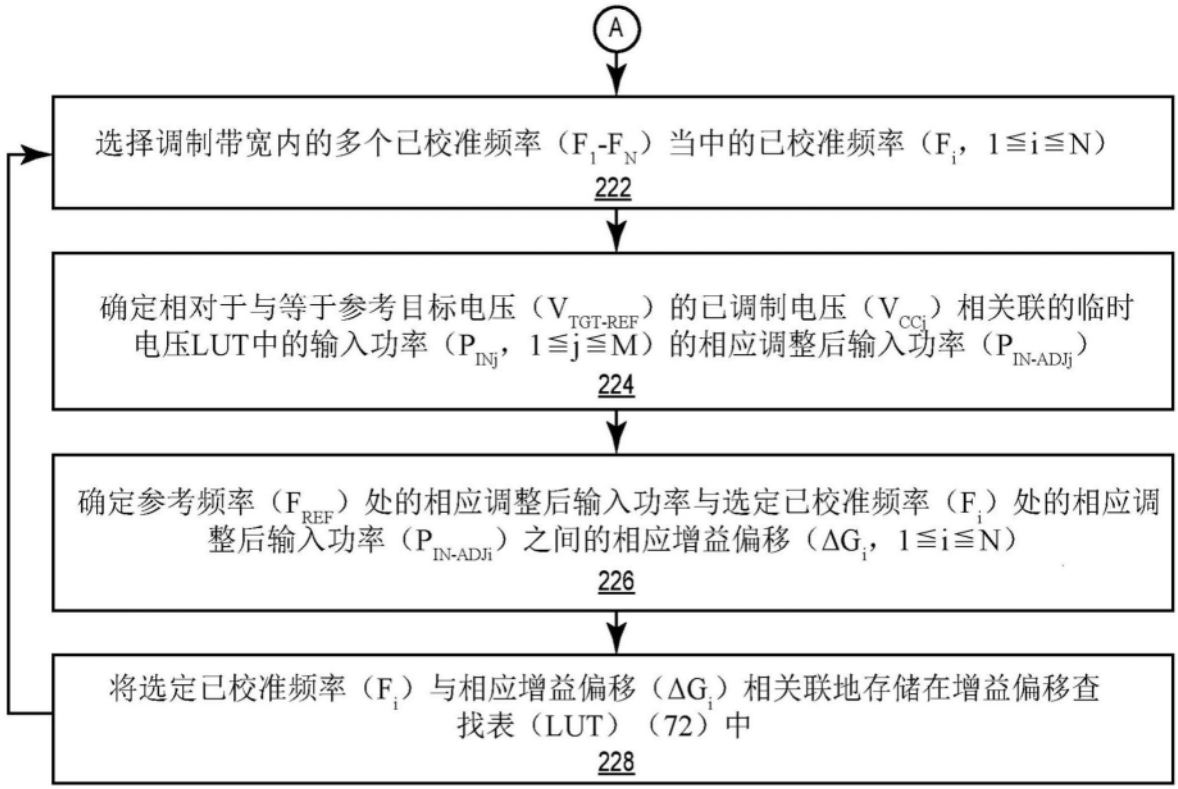

A
选择调制带宽内的多个已校准频率（F_1-F_N）当中的已校准频率（F_i，$1 \leqq i \leqq N$）
222
确定相对于与等于参考目标电压（$V_{TGT-REF}$）的已调制电压（V_{CCj}）相关联的临时电压LUT中的输入功率（P_{INj}，$1 \leqq j \leqq M$）的相应调整后输入功率（$P_{IN-ADJj}$）
224
确定参考频率（F_{REF}）处的相应调整后输入功率与选定已校准频率（F_i）处的相应调整后输入功率（$P_{IN-ADJi}$）之间的相应增益偏移（ΔG_i，$1 \leqq i \leqq N$）
226
将选定已校准频率（F_i）与相应增益偏移（ΔG_i）相关联地存储在增益偏移查找表（LUT）（72）中
228

图7(续)

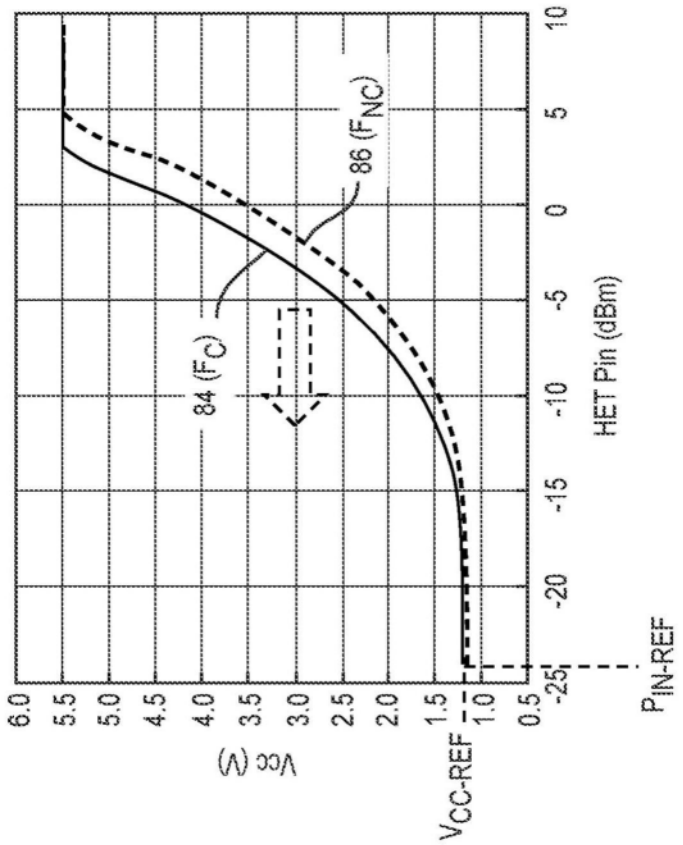

86 (F_{NC})
84 (F_C)
HET Pin (dBm)
10
5
0
-5
-10
-15
-20
-25
P_{IN-REF}
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
Vcc (V)
V_{CC-REF}

图8A

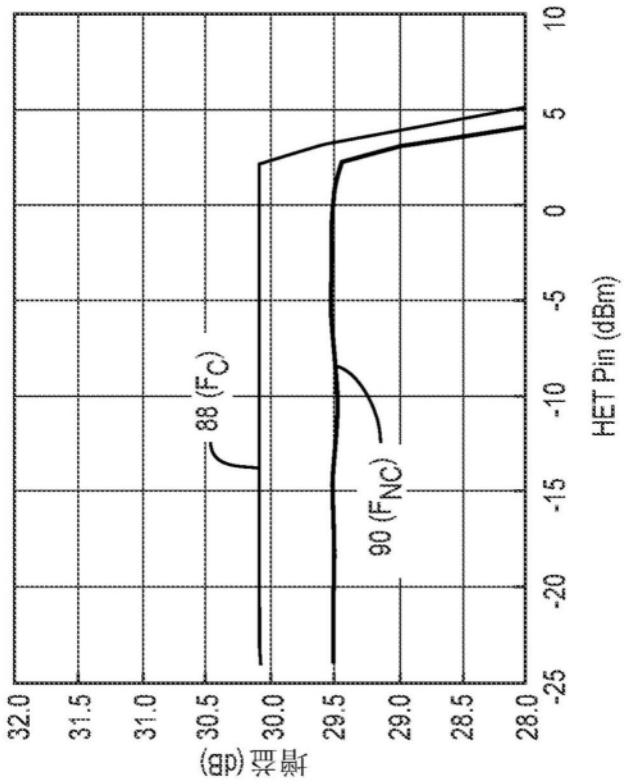

32.0
31.5
31.0
30.5
30.0
29.5
29.0
28.5
28.0
增益(dB)
10
5
0
-5
-10
-15
-20
-25
HET Pin (dBm)
88 (FC)
90 (FNC)

图8B

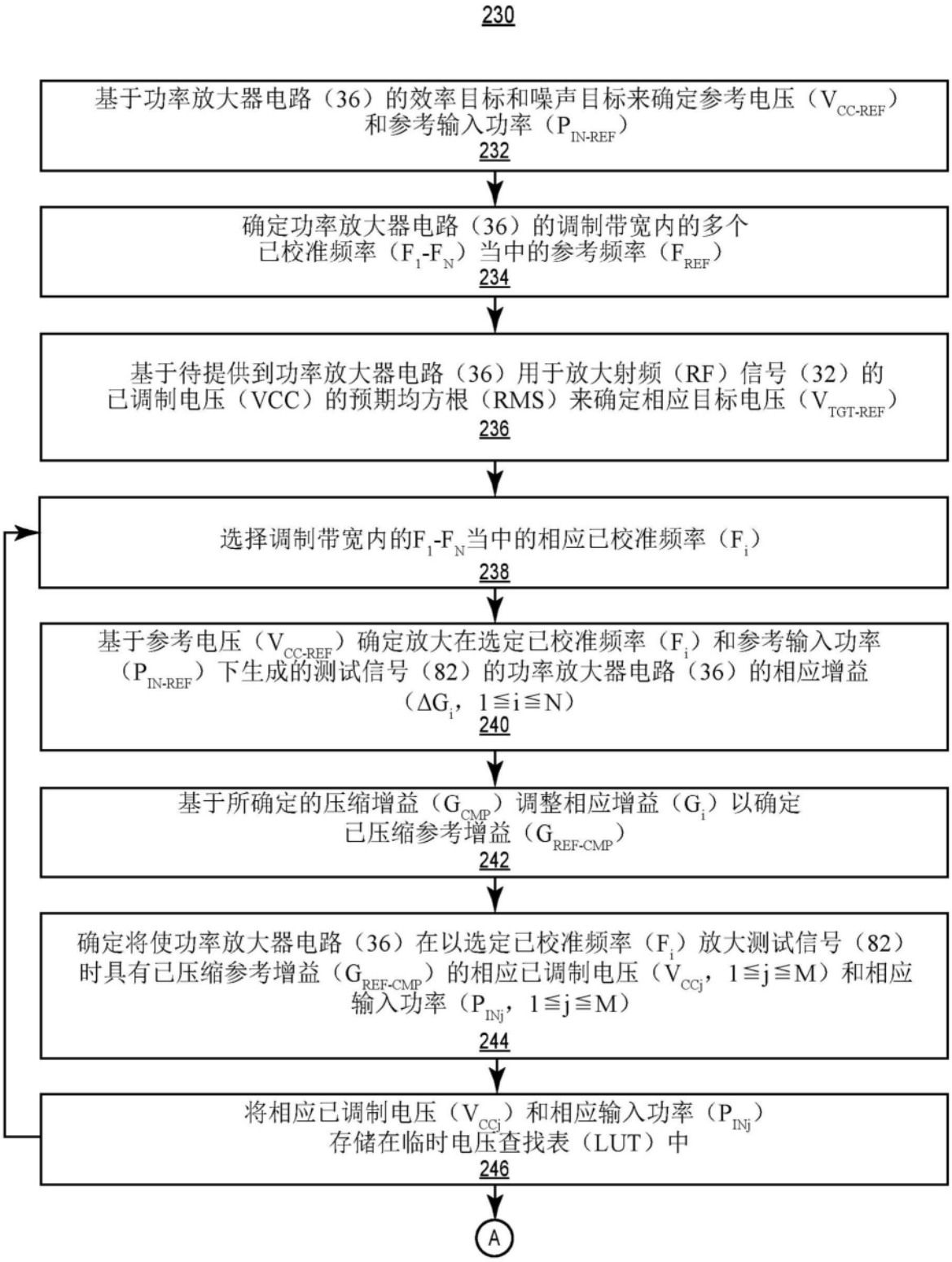

230
基于功率放大器电路（36）的效率目标和噪声目标来确定参考电压（V_{CC-REF}）和参考输入功率（P_{IN-REF}）
232
确定功率放大器电路（36）的调制带宽内的多个已校准频率（F_1-F_N）当中的参考频率（F_{REF}）
234
基于待提供到功率放大器电路（36）用于放大射频（RF）信号（32）的已调制电压（VCC）的预期均方根（RMS）来确定相应目标电压（$V_{TGT-REF}$）
236
选择调制带宽内的F_1-F_N当中的相应已校准频率（F_i）
238
基于参考电压（V_{CC-REF}）确定放大在选定已校准频率（F_i）和参考输入功率（P_{IN-REF}）下生成的测试信号（82）的功率放大器电路（36）的相应增益（ΔG_i，$1 \leqq i \leqq N$）
240
基于所确定的压缩增益（G_{CMP}）调整相应增益（G_i）以确定已压缩参考增益（$G_{REF-CMP}$）
242
确定将使功率放大器电路（36）在以选定已校准频率（F_i）放大测试信号（82）时具有已压缩参考增益（$G_{REF-CMP}$）的相应已调制电压（V_{CCj}，$1 \leqq j \leqq M$）和相应输入功率（P_{INj}，$1 \leqq j \leqq M$）
244
将相应已调制电压（V_{CCj}）和相应输入功率（P_{INj}）存储在临时电压查找表（LUT）中
246
A

图9

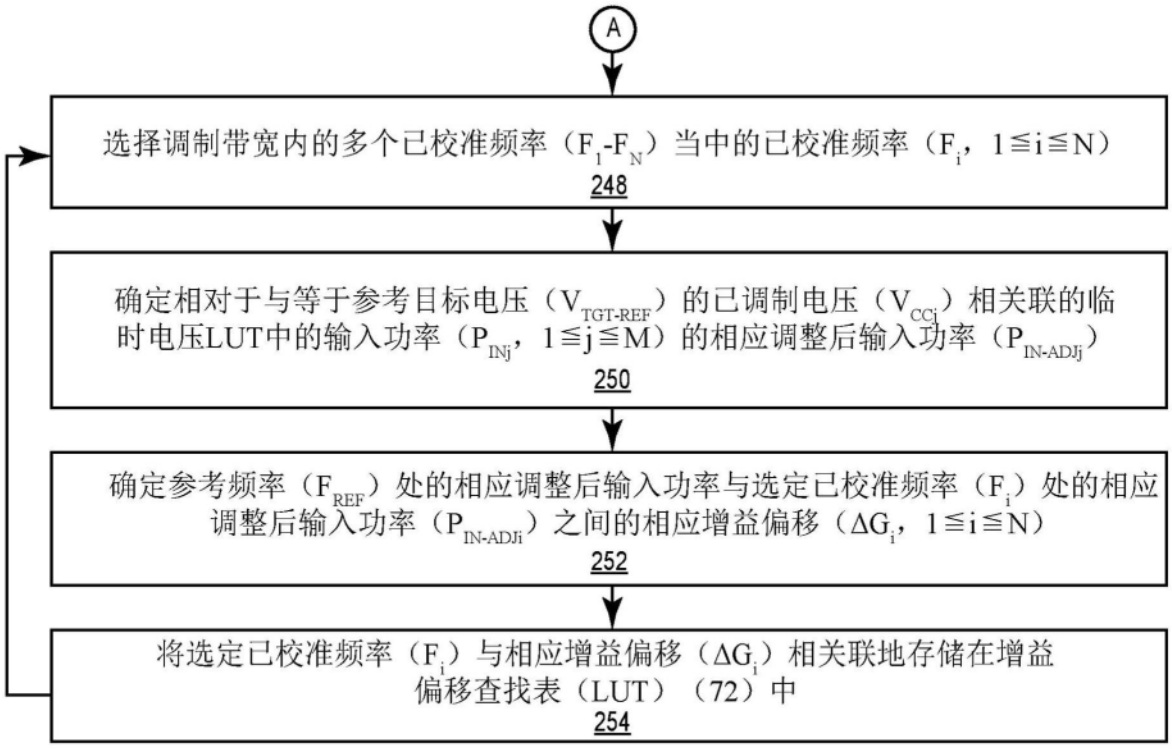

A
选择调制带宽内的多个已校准频率（F_1-F_N）当中的已校准频率（F_i，$1 \leqq i \leqq N$）
248
确定相对于与等于参考目标电压（$V_{TGT-REF}$）的已调制电压（V_{CCj}）相关联的临时电压LUT中的输入功率（P_{INj}，$1 \leqq j \leqq M$）的相应调整后输入功率（$P_{IN-ADJj}$）
250
确定参考频率（F_{REF}）处的相应调整后输入功率与选定已校准频率（F_i）处的相应调整后输入功率（$P_{IN-ADJi}$）之间的相应增益偏移（ΔG_i，$1 \leqq i \leqq N$）
252
将选定已校准频率（F_i）与相应增益偏移（ΔG_i）相关联地存储在增益偏移查找表（LUT）（72）中
254

图9(续)

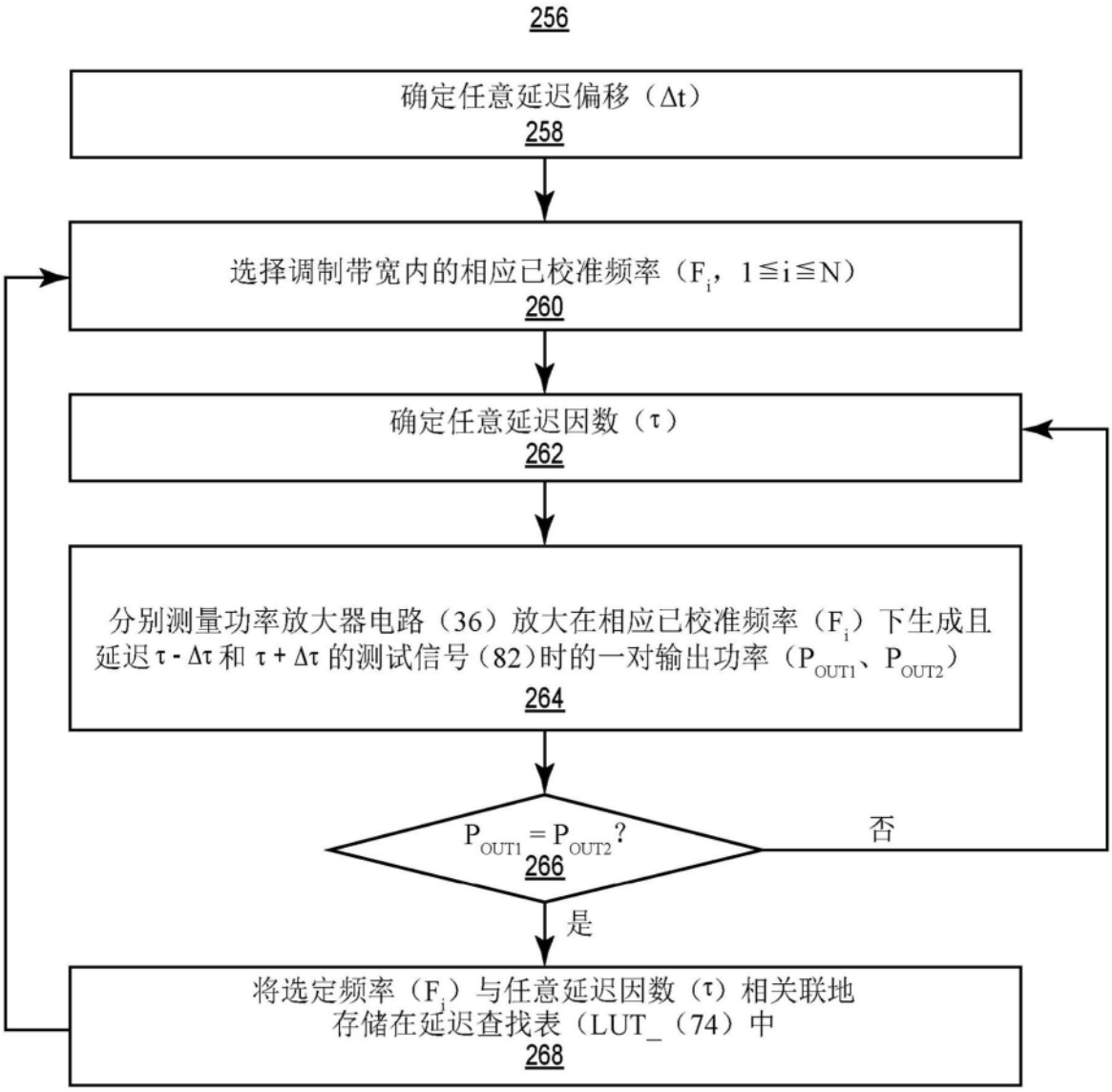

256
确定任意延迟偏移（Δt）
258
选择调制带宽内的相应已校准频率（F_i，1≦i≦N）
260
确定任意延迟因数（τ）
262
分别测量功率放大器电路（36）放大在相应已校准频率（F_i）下生成且延迟τ - Δτ和τ + Δτ的测试信号（82）时的一对输出功率（P_{OUT1}、P_{OUT2}）
264
$P_{OUT1} = P_{OUT2}$?
266
否
是
将选定频率（F_j）与任意延迟因数（τ）相关联地存储在延迟查找表（LUT_（74）中
268

图10