United States Patent

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[45] **July 25, 1972**

[54] SERIAL DIGITAL PULSE PHASE INTERFACE DRIVER AND RECEIVER

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[22] Filed: **July 10, 1970**

[21] Appl. No.: **53,751**

[52] **U.S. Cl.** .....**340/167 R,** 340/168 S

[51] **Int. Cl.** **H04q 1/32**

[58] **Field of Search** .....340/168 SR, 167, 170

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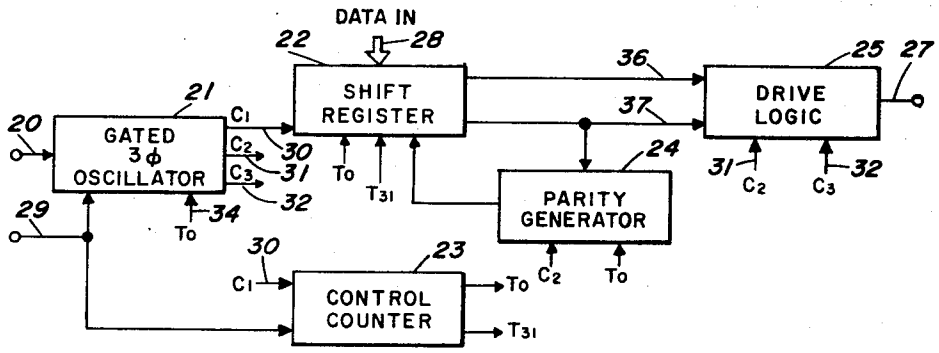
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[57] **ABSTRACT**

A digital transmission system comprising a transmitter and receiver capable of transmitting and receiving digital data at high bit rates in a noisy environment, utilizing transformer coupling to a single transmission line, serial to parallel and parallel to serial conversion, and parity generation and checking circuits. The system is capable of operation from a 5 volt source and of being densely packaged. The serial digital receiver utilizes a decoding and filtering circuit which provides high noise immunity for the system. Data transmitted and received is in the form of pulses having a positive and negative peak so as to eliminate the necessity of a separate syne line.

9 Claims, 11 Drawing Figures



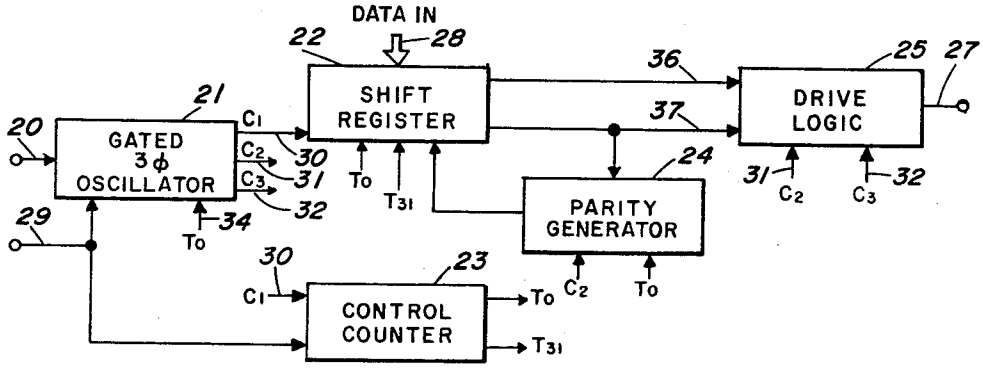


FIG. 1

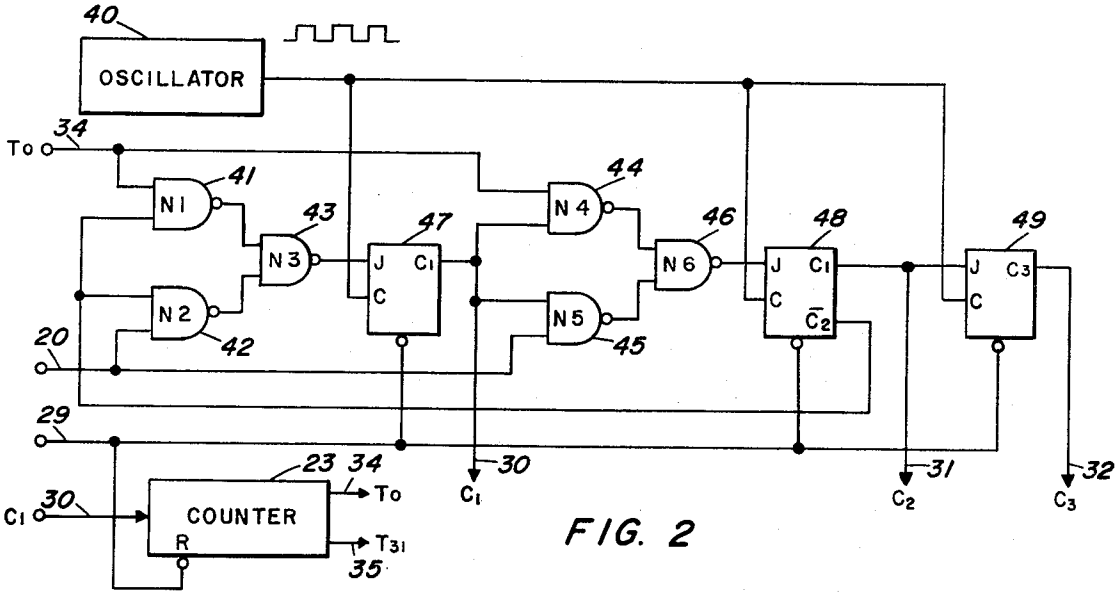


FIG. 2

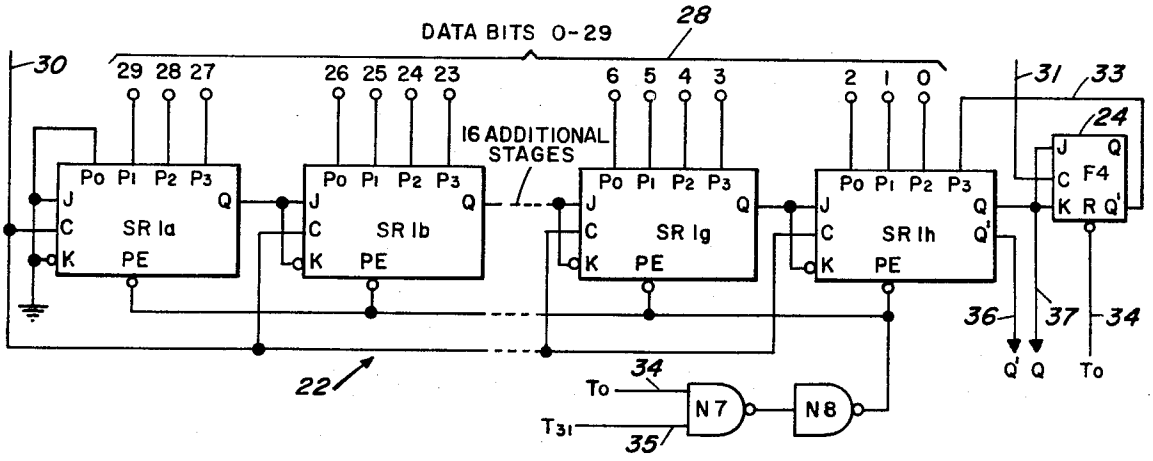


FIG. 3

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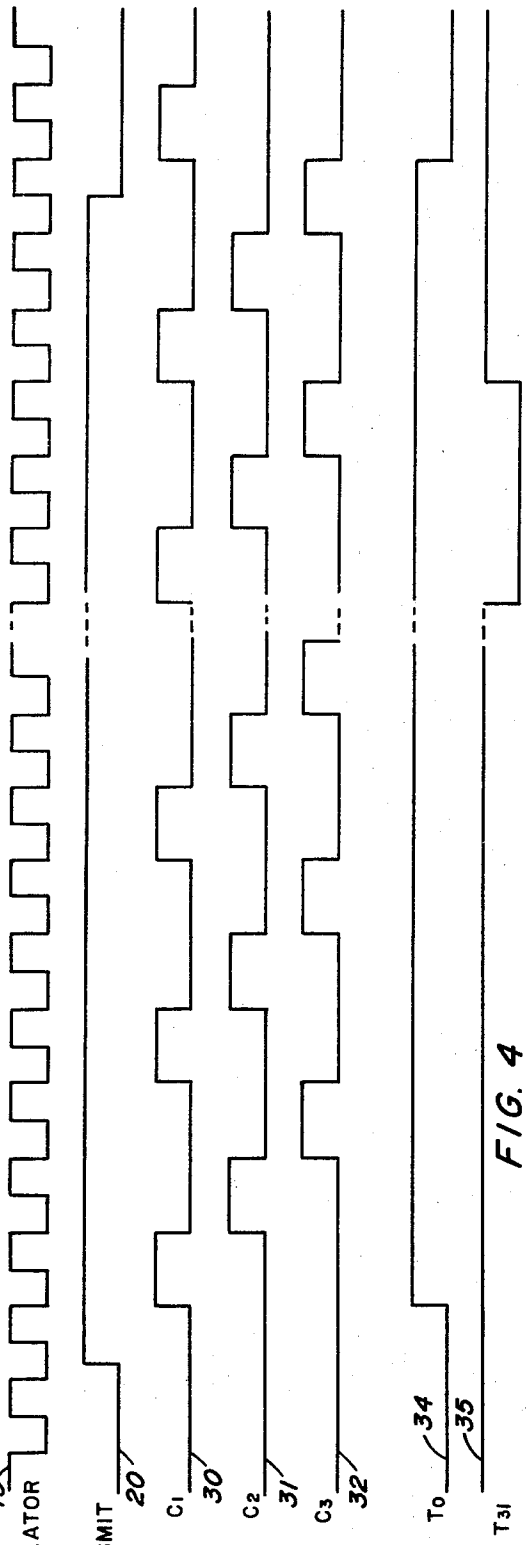


FIG. 4

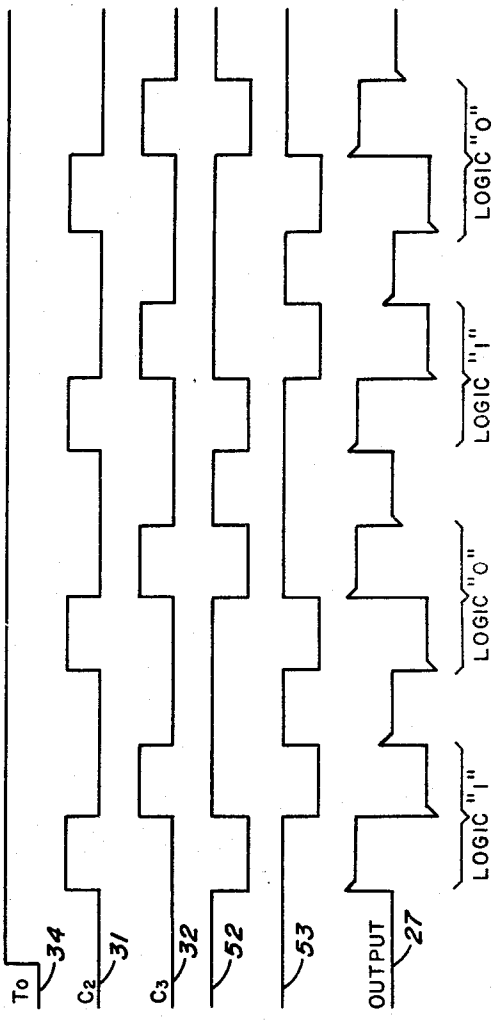


FIG. 6

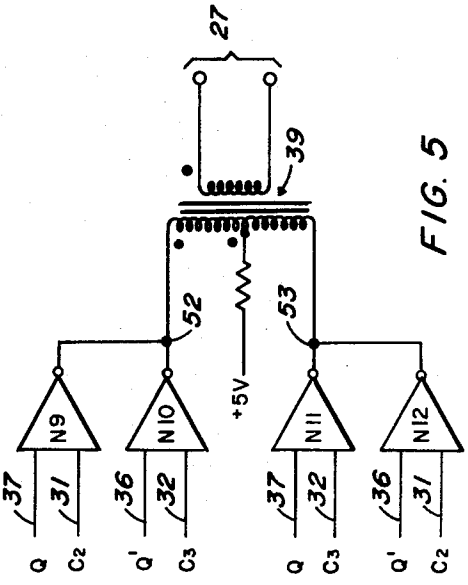


FIG. 5

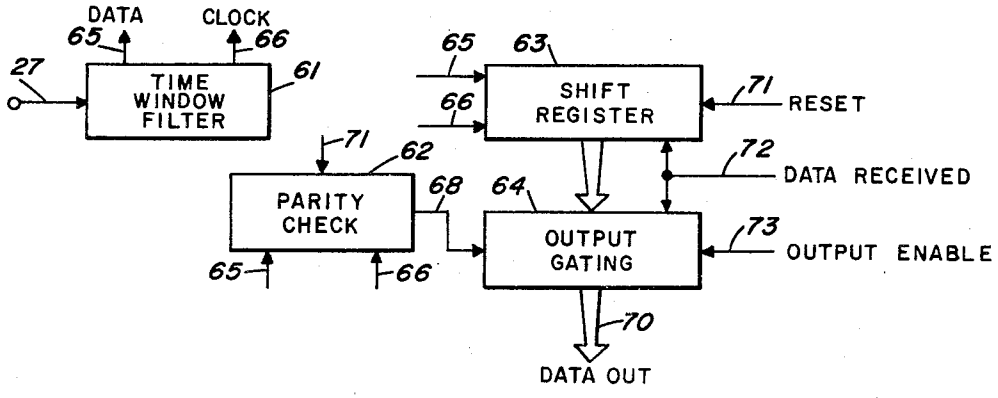

DATA
CLOCK
65
66
27
TIME WINDOW FILTER
61
65
63
66
SHIFT REGISTER
71
RESET
71
62
72
DATA RECEIVED
PARITY CHECK
68
64
OUTPUT GATING
73
OUTPUT ENABLE
65
66
70
DATA OUT

FIG. 7

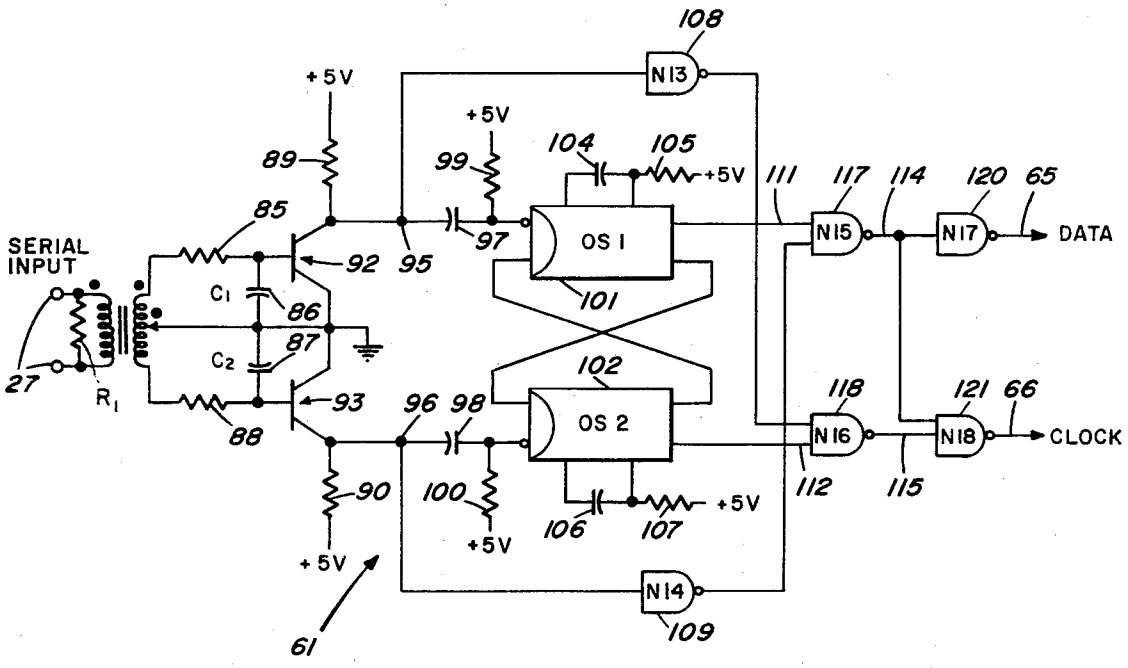

108
N13
+5V
+5V
89
99
104
105
+5V
111
117
114
120
65
85
OS 1
N15
N17
DATA
SERIAL INPUT
92
95
97
C1
86
101
87
C2
102
27
R1
93
96
98
OS 2
118
121
66
N16
N18
CLOCK
88
90
100
112
115
+5V
+5V
106
107
+5V
+5V
N14
109
61

FIG. 8

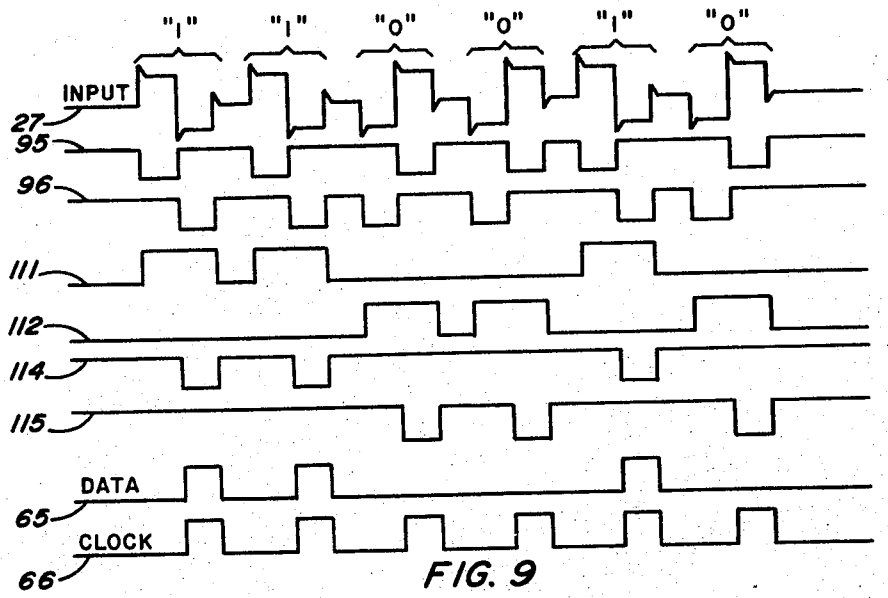


FIG. 9

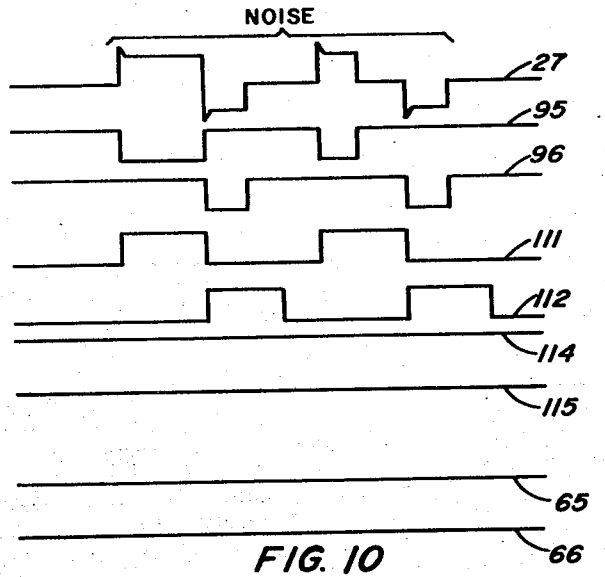


FIG. 10

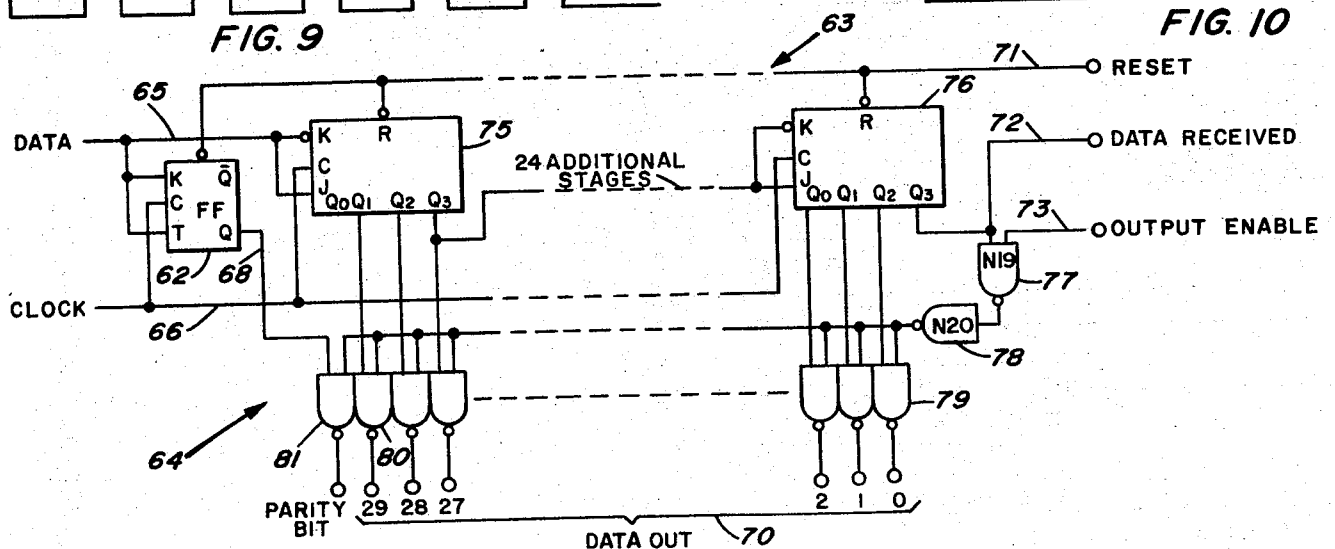


FIG. 11

SERIAL DIGITAL PULSE PHASE INTERFACE DRIVER AND RECEIVER

STATEMENT OF GOVERNMENT INTEREST

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment of any royalties thereon or therefor.

BACKGROUND OF THE INVENTION

The present invention relates generally to improvements in serial digital transmission systems, and more particularly, pertains to a new and improved interface driver and receiver in such systems wherein transformer coupling to the transmission line, high noise immunity, built in serial to parallel and parallel to serial conversation, integrated parity generation and parity checking, operation from a single 5 volt power supply, and transmission on a single transmission line in the form of positive and negative pulses is provided. One of the more critical problems confronting developers of digital data transmission systems has been the coherent transmission of digital data at high bit rates in a noisy environment by means of a transmission system that is compact and capable of operating on low power supplies. These problems are overcome by the present invention.

SUMMARY OF THE INVENTION

The system of the present invention has the capability of transmitting digital data at high bit rates (greater than 5×10^6 bits per second) in a relatively noisy environment. The serial digital transmitter and the serial digital receiver employ transformers for coupling to the transmission lines. Built in serial to parallel and parallel to serial conversation and integrated parity generation and checking circuits are also used. The system is capable of operating from a single 5 volt power supply. In addition, the serial digital receiver has a decoding and filtering circuit that provides high noise immunity to the system. The building blocks of the system are capable of high packaging density, thus, providing for a very compact system.

The general purpose of this invention is to provide a digital data transmission system that has all the advantages of similarly employed transmission systems and has none of the above described disadvantages. To obtain this purpose, the present invention provides a unique digital data transmitter and digital data receiver, said receiver employing a decoding and filtering circuit which provides high noise immunity for the system.

OBJECTS OF THE INVENTION

An object of the present invention is the provision of an improved serial digital data transmission system capable of transmitting data at high bit rates in a noisy environment.

Another object is to provide an improved serial digital transmission system capable of transmitting data at high bit rates in a noisy environment that requires only one transmission line.

A further object of the invention is the provision of an improved serial digital transmission system capable of transmitting data at high bit rates in a noisy environment that requires only one transmission line and is capable of operating from a 5 volt source.

Still another object is to provide an improved serial digital transmission system capable of transmitting data at high bit rates in a noisy environment that has built in serial to parallel and parallel to serial conversion and parity generation and checking circuits.

A still further object is to provide an improved serial transmission system having a transmitter and receiver capable of transmitting and receiving data at high bit rates in a noisy environment that utilize a decoding and filtering circuit in the receiver to provide high noise immunity.

Other objects, advantages and novel features of the invention will become apparent from the following detailed description of the invention when considered in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a preferred embodiment of the digital data transmitter;

FIG. 2 illustrates the gated three phase oscillator of the digital data transmitter of FIG. 1;

FIG. 3 illustrates the shift register of the transmitter of FIG. 1;

FIG. 4 illustrates the various pulses that are generated by the components of the transmitter of FIG. 1;

FIG. 5 illustrates the driver logic and output section of the transmitter of FIG. 1;

FIG. 6 illustrates the various pulses that are generated by the driver logic of FIG. 5;

FIG. 7 illustrates a preferred embodiment of the digital data receiver of this invention;

FIG. 8 illustrates the time window filter of the digital data receiver of FIG. 7;

FIG. 9 illustrates the various signal states in the time window filter of FIG. 8;

FIG. 10 illustrates the various noise states in time window filter of FIG. 8; and

FIG. 11 illustrates the shift register and output gating of the serial digital data receiver of FIG. 7.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 is a block diagram illustration of the basic components in the digital data transmitter of the system. Shift register **22** is a 32 bit shift register which receives data at data input **28** in parallel form and converts it to a serial pulse train at output **36, 37**. Gated three phase oscillator **21** has outputs **30, 31** and **32** which supply timing pulses to the various components of the transmitter. Control counter **23** controls the length of the transmit cycle, causes the data words to be transmitted to be loaded into shift register **22** and clocks in the parity bit at the end of each transmit cycle. Parity generator **24** generates a parity pulse at the end of each transmit cycle in response to a signal received from control counter **23**. Driver logic **25** produces 5 volt bipolar pulses for application to the transmission line **27**.

FIG. 2 represents the gated three phase oscillator **21** in combination with control counter **23**. The three phase oscillator is comprised of a 15 MHz square wave oscillator **40** and a four state sequential logic circuit which has outputs C_1, C_2, and C_3 on lines **30, 31** and **32** respectively. These outputs are produced by the oscillator **40** working in conjunction with the four state sequential logic circuit. The logic circuit comprises NAND gates **41, 42, 43, 44, 45, 46** and flip-flops **47, 48,** and **49**. All the NAND gates employed and all the flip-flops employed are TTL. Counter **23** is a control counter which consists of a module **33** counter, in other words has 33 states and two decoded outputs. The counter may be mechanized in any convenient fashion well known in the art.

With the aid of the pulse trains of FIG. 4 the operation of the three phase oscillator and control counter will now be explained. In its non-transmitting or quiescent state, three phase gated oscillator **21** has outputs C_1, C_2, and C_3 on lines **30, 31,** and **32** respectively which are all logic zero. If a logic one pulse is applied to terminal **20**, which is the data transmit terminal, three phase gated oscillator **21** enters a cyclic mode generating a string of sequential pulses at its three outputs. Referring to FIG. 4, these outputs are illustrated at **30, 31** and **32**. The outputs of oscillator **40** is illustrated as a pulse train **49**. The data transmit pulse is illustrated at **20**. The preferred embodiment is directed towards a transmitting system that can handle 32 bits. Therefore, the outputs **30, 31** and **32** of the three phase sequential oscillator continue in their cyclic mode for 32 cycles until the entire data word has been completely

transmitted. At this time, the control counter output T_o, illustrated at **34**, returns to a logic zero. Output C_1 at **30** is used to shift data out of shift register **22** and also to increment control counter **23**. Outputs C_2 and C_3 at **31** and **32** respectively are clock pulses that time the initial and final phases respectively of the transmitted serial pulse train. The data transmit pulse, illustrated at **20**, must remain at a logic one throughout the transmit cycle and must be returned to a logic zero prior to output T_O of counter **22** switching to a logic zero. Output T_O of counter **23** is a logic zero upon initiation of three phase oscillator **21** and is a logic one at all other times. Output T_{31}, at **35**, of counter **23** is a logic zero at bit time **31**, and a logic one at all other times. This is clearly illustrated by pulse trains **34** and **35** respectively.

Counter **23** may be cleared by the application of a logic zero at master clear line **29** at any time during the transmit cycle. The transmission system of this invention has been mechanized to transmit 30 bit data words. However, data words of any length can be accommodated by designing the appropriate number of bits into control counter **23** and shift register **22**. In addition to the 30 data bits, two other bits must also be transmitted. The first bit transmitted is a logic one and is used as a control for the serial receiver. The last bit transmitted is a parity bit which may be optional and is generated by the parity generator **24**.

FIG. **3** illustrates an embodiment of shift register **22** and parity generator **24** which may be employed in the invention. During the nontransmit or quiescent state, when output T_O of counter **23** is a logic zero, parity generator **24** is set at zero and the preset enable input of all the stages of the shift register is conditioned by way of gates N_7 and N_8. Upon pulse C_1 being placed on line **30**, the data word at input **28** is loaded into the shift register which is composed of serial registers SRIA to SR1H comprising **29** stages in all. A logic one is loaded into last stage P_3 of the shift register by parity generator **24** so that the output Q of the shift register is a logic one during the remaining portion of the time that the first pulse C_1 is on line **30**. The signal Q is transmitted as a pair of properly phased bipolar pulses when the second C_1 pulse appears on line **30**. The data in serial register **22** is shifted to the right and the first data bit of the data word is launched on the transmission line. This process continues until all 30 data bits have been transmitted. During this transmission process, parity generator **24** is toggled each time a logic one appears at output **37** of the shift register. Therefore, if an odd number of ones have appeared on line **37** parity generator **24** will be reset.

During transmission of the last data bit, output T_{31} of counter **23** is a logic zero and the preset enable input of the shift register is again conditioned via gates N_7 and N_8 so that when parity bit generator **24** transmits the parity bit the shift register will be preset and output Q on line **37** will assume the complement of the stage of parity generator **24**. Since this bit is transmitted during bit time **32**, in other words the 32nd bit to be transmitted in the cycle, an odd number of ones is always transmitted (parity in essence being odd parity). At the termination of this last bit, time control counter **23** returns to its quiescent state as does the transmitter itself.

Driver logic **25**, shown in FIG. **5**, places bipolar pulses such as illustrated at **27** of FIG. **6** on transmission line **27**. It consists of four driver gates which are 944 DTL power NAND gates. These driver gates N_9–N_{12} are power buffers and are connected as shown to a resistor and tap transformer. The output Q and Q′ of shift register **22** are supplied to the four gates in conjunction with timing pulse trans C_2 and C_3, on lines **31**, **32**, and **36**, **37** respectively. As can be seen from the wave form diagrams of FIG. **6**, the pulse trains C_2 and C_3 on lines **31** and **32** are timing pulses that produce an output at point **52** and **53** of the driver logic circuit such as shown at lines **52** and **53** of FIG. **6**. In response to the pulses in pulse trains **31** and **32** coinciding with output Q and Q′ of shift register **22** the pulses placed on transmission line **27** for each logic signal is a bipolar pulse such as shown at **27** of FIG. **6**.

Referring now to FIG. **7** which illustrates the serial digital receiver of the system, it can be seen that the receiver is made up of three basic components, time window filter **61**, shift register **63** and parity check **62**, and output gating **64**.

FIG. **8** more specifically illustrates time window filter **61**. The pulses transmitted over transmission line **27** are introduced to the time window filter **61** by way of a transformer which has a resistor R_1 coupled across its primary windings to terminate transmission line **27**. Resistor capacitor combination **85**, **86** and resistor capacitor combination **88**, **87** function as single pole filters to provide high frequency attenuation to the received bipolar pulses. Two level thresholding is accomplished by the voltage base to emitter drop of transistors **92** and **93** in conjunction with the turns ratio of the input transformer. These two thresholds are set at approximately +1 volt and −1 volt. Therefore, a logic zero at point **95** will correspond to an input signal in excess of IV, and a logic zero at point **96** will correspond to an input signal less than −1 volt. Both points, **95** and **96**, will have a logic one for all input signals less than 1 volt and greater than −1 volt. The time window filter of FIG. **8** performs two functions. The first is to examine the time relationship between the positive and negative pulses on the transmission line in order to **10** ascertain whether a valid logic one or zero signal has been received. Secondly, the time window filter discriminates against all other signals and blocks those which do not correspond to the predetermined phase relationship of valid logic one and logic zero signals. The circuit accomplishes this by employing a pair of one-shot multivibrators **101** and **102** that are cross-coupled to establish timing windows. Resistor capacitor network **99**, **97** differentiates the signal at point **95** such that a negative going spike is presented to the inverting input of one-shot multivibrator **101**. Similarly, resistor capacitor network **100**, **98** differentiates the wave form at point **96** such that a negative going spike is presented to the inverting input of one-shot multivibrator **102**. Either one-shot multivibrator will be triggered by this spike if a logic one is also presented at its non-inverting input. The cross-coupling, therefore, will prevent either one-shot from being triggered when the other is in its stable state. Resistor capacitor network **105**, **104** and **107**, **106** establish the output pulse width of one-shot multivibrators **101** and **102** respectively. For a bit rate of 5 MHz a bit period of 200 nanoseconds is required which is divided into three equal 67 nanosecond intervals. The pulse widths of the one-shot multivibrator must be twice this interval or 134 nanoseconds.

Referring now to FIG. **9** which illustrates the various signals within time window filter **61**, it can be seen that if a logic one signal for example, is being received at input **27**, such as shown at **27** of FIG. **9**, point **95** will go to a logic zero for 67 nanoseconds and trigger one-shot multivibrator **101** which thereby inhibits the triggering of one-shot multivibrator **102**. Point **96** will then subsequently go to a logic zero for 67 nanoseconds as shown at **96** of FIG. **9**. This logic zero at point **96** is inverted by NOT gate **109** and nanded with the output **111** of one-shot multivibrator **101** to produce a 67 nanosecond logic zero pulse at point **114**, the output of NAND gate **117**. In a similar fashion, if a logic zero signal is being received such, as the third signal on input line **27**, point **96** will go to a logic zero for 67 nanoseconds and trigger one-shot multivibrator **102** which in turn inhibits the triggering of one-shot multivibrator **101**. Point **95** will then go to a logic zero for 67 nanoseconds and this zero signal is inverted by gate **108** and nanded with output **112** of multivibrator **102** by nand gate **118** to produce a 67 nanoseconds logic zero pulse on line **115**. NOT gate **120** and NAND gate **121** function to produce data on line **65** and clock pulses on line **66**. The data pulses are 67 nanosecond logic one pulses for every logic one signal received and the clock pulses are 67 nanosecond logic one pulses for every logic one and logic zero signal received. They are illustrated at pulse train **65** and **66** of FIG. **9**.

FIG. **10** illustrates the progression of noise through the time window filter. As can be seen from the figure, noise and all signals with improper phase and time relationship will produce

no logic zero pulses at points **114** or **115** of the filter circuit because of the lack of time coincidence between the signals at point **95** and **96** with the signals generated by one-shot multivibrators **101** and **102** respectively.

Referring now to FIG. **11**, which illustrates the shift register of the receiver, which performs the function of serial to parallel conversion, connected to the output gating and the parity checking circuit. The first bit of each word received is a control bit and a logic one. When this bit has been shifted into the last stage of shift register **63**, it enables the data word in the shift register to be gated, by means of gates **79–81**, to the output of the interface lines **70**. At this point, the output of flip-flop **62** can be examined. This flip-flop which is the parity check circuit is toggled for each logic one signal received and should be set at the end of the transmission of a word. It will be so set if an odd number of logic one signals have been received which is indicative of no one having occurred. Flip-flop **62** and shift register **63** is cleared by applying a logic zero pulse at reset line **71** prior to the reception of a subsequent data word. All four bit shift registers such as **75** and **76** are Fairchild 9300 and all gates such as **77**, **78** and **79**, **81** are DTL.

It can thus be seen that this invention provides an improved serial digital data transmission system that is capable of transmitting at high bit rates in a noisy environment and that it only requires one transmission line, is capable of operating from a 5 volt source, has built in serial to parallel and parallel to serial conversion, and parity generation and checking circuits, and utilizes a decoding and filtering circuit that provides high noise immunity. Various modifications are contemplated and may obviously be resorted to those skilled in the art without departing from the spirit or scope of the invention as hereinafter defined by the appended claims as only a preferred embodiment thereof has been disclosed.

What is claimed is:

1. In combination with a transmission system for transmitting and receiving digital data in the form of bits in a serial manner wherein the transmitting means receives the data to be transmitted in parallel form and converts it to series form before placing it on a transmission medium and the receiver means converts the data received into parallel form before delivering it to its output, the improvement which comprises:

driver logic means connected to the output of said transmitter means and to the transmission medium for generating, for each bit received from said transmitter, a bipolar pulse having positive and negative portions of equal amplitude and time and having a phase which is indicative of whether the bit received is a logic one or a logic zero; and

time window filter means connected to the transmission medium and said receiver means for receiving the bipolar pulses, examining the time relationship between the positive and negative portions of the pulses on the transmission line to determine whether a valid signal has been received, and examining the phase of a received valid signal to determine whether the signal represents a logic one or a logic zero.

2. The improved digital data transmission system of claim **1** wherein said driver logic means comprises:

four NAND gates connected together in parallel into first and second pairs; and

a transformer having its secondary winding connected to the transmission medium and having said NAND gates connected to its primary winding.

3. The improved digital data transmission system of claim **2** wherein said transformer comprises:

a primary winding with three taps, a first and second outside tap and a center tap, the first outside tap connected to the first pair of NAND gates and the second outside tap connected to the second pair of NAND gates, the center tap being connected to a power source.

4. The improved digital data transmission system of claim **2** wherein said time window filter means comprises:

a plurality of multivibrators connected to the transmission medium; and

logic circuit means connected to said multivibrators for delivering logic data and clock output pulses in response to said multivibrators.

5. The improved data transmission system of claim **4** wherein said multivibrators comprise:

a pair of one-shot multivibrators connected together in a cross-coupled manner.

6. A compact, low power transmission system for transmitting and receiving digital data in a serial manner, having a transmitter connected to one end of a transmission medium and a receiver on the other end of the transmission medium, said system comprising:

a transmitting shift register for receiving the data to be transmitted;

a control counter connected to said shift register for enabling said register so that the data to be transmitted is loaded into said register, and for controlling the length of the transmit cycle in response to the extent of loading of said shift register;

a parity generator connected to said shift register and said control counter, responsive to said control counter to generate a parity bit at the end of the transmit cycle;

driver logic means connected to said shift register, responsive to the pulse output of said serial register to place bipolar pulses having positive and negative portions of predetermined time and phase relationship on the sending end of the transmission medium;

a gated three phase oscillator connected to said shift register, control counter, parity generator and driver logic for supplying timing pulses to said shift register, control counter, parity generator and driver logic; and

time window filter means connected to the receiving end of the transmission medium for decoding and filtering the received digital data by examining the time relationship of the positive and negative portions of the bipolar pulses and blocking all signals which do not correspond to the predetermined time relationship and by examing the phase relationship of the positive and negative portions of the bipolar pulses to decode the data;

a receiving shift register connected to said time window filter means and responsive thereto to receive the decoded digital data;

output gating connected to said shift register for removing data stored in said receiving shift register in response to an output enable signal;

a parity check circuit connected to said time window filter means, and said output gating for determining whether an error has occurred during transmission.

7. The transmission system of claim **6** wherein said logic means comprises:

four NAND gates connected together in parallel into first and second pairs; and

a transformer having its secondary winding connected to the transmission medium and having said NAND gates connected to its primary winding.

8. The transmission system of claim **7** wherein said time window filter means comprises:

a plurality of multivibrators connected to the transmission medium between the positive and negative pulses received on the transmission; and

logic circuit means connected to said multi-vibrators for delivering logic and clock output pulses in response to said multivibrators.

9. The transmission system of claim **8** wherein said multivibrators comprise:

a pair of one-shot multivibrators connected together in a cross-coupled manner.

* * * * *