US 20210367563A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2021/0367563 A1**

Pinto et al. (43) **Pub. Date: Nov. 25, 2021**

(54) **SYSTEMS AND METHODS FOR TIA BASE CURRENT DETECTION AND COMPENSATION**

(71) Applicant: **VELODYNE LIDAR USA, INC.**, San Jose, CA (US)

(72) Inventors: **Roger Pinto**, Alameda, CA (US); **Pravin Kumar Venkatesan**, Fremont, CA (US)

(21) Appl. No.: **17/392,062**

(22) Filed: **Aug. 2, 2021**

Related U.S. Application Data

(63) Continuation of application No. 16/181,523, filed on Nov. 6, 2018, now Pat. No. 11,082,010.

Publication Classification

(51) **Int. Cl.**

H03F 1/30	(2006.01)
H03G 3/00	(2006.01)
H03F 3/343	(2006.01)
H03G 3/30	(2006.01)
H03M 1/74	(2006.01)

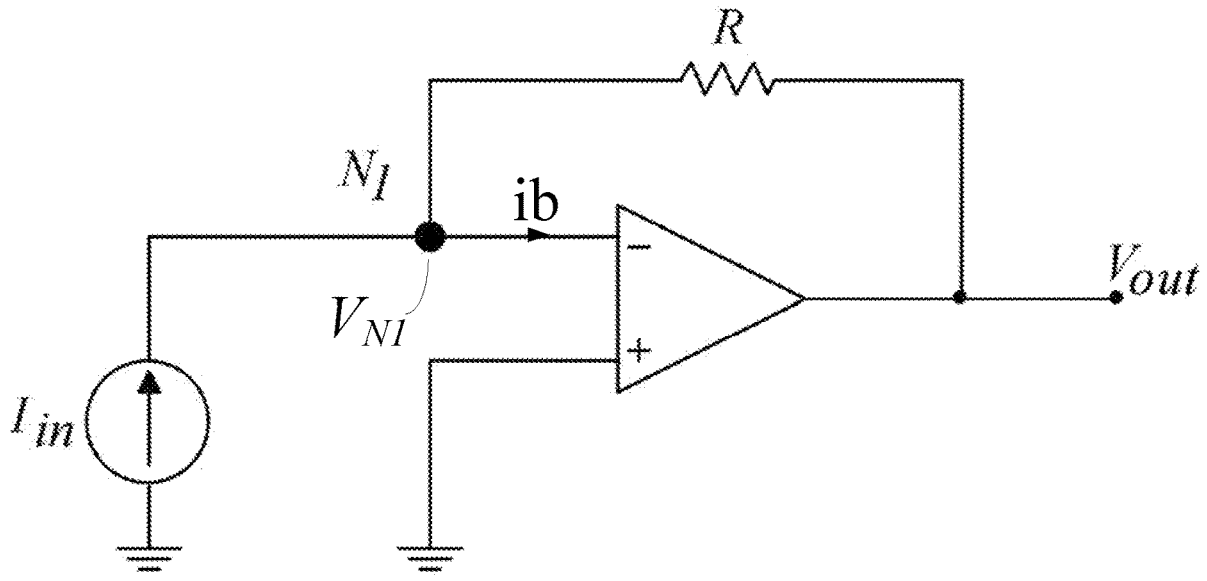
(52) **U.S. Cl.**

CPC ***H03F 1/302*** (2013.01); ***H03G 3/001*** (2013.01); ***H03G 3/007*** (2013.01); ***H03G 3/3089*** (2013.01); ***H03M 1/742*** (2013.01); ***H03F 3/3432*** (2013.01)

(57) **ABSTRACT**

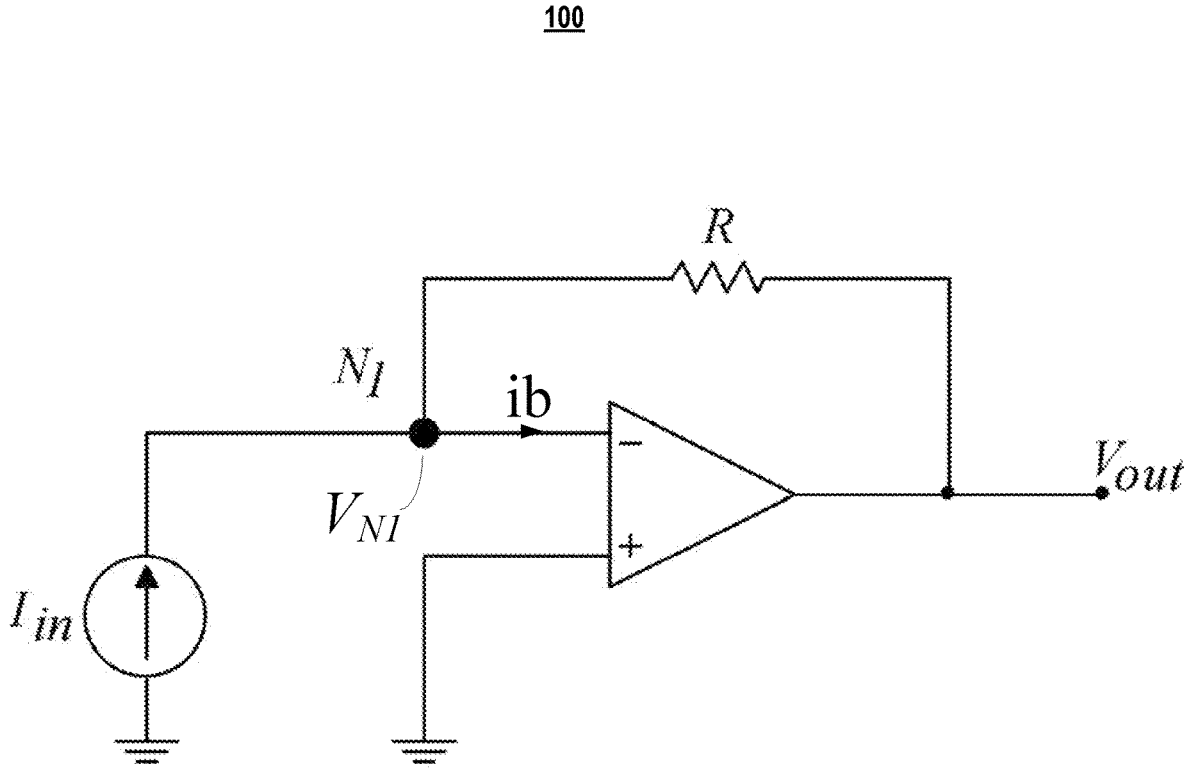
Described herein are systems and methods that can adjust the performance of a transimpedance amplifier (TIA) in order to compensate for changing environmental and/or manufacturing conditions. In some embodiments, the changing environmental and/or manufacturing conditions may cause a reduction in beta of a bipolar junction transistor (BJT) in the TIA. A low beta may result in a high base current for the BJT causing the output voltage of the TIA to be formatted as an unusable signal output. To compensate for the low beta, the TIA generates an intermediate signal voltage, based on the base current and beta that is compared with the PN junction bias voltage on another BJT. Based on the comparison, the state of a digital state machine may be incremented, and a threshold base current is determined. This threshold base current may decide whether to compensate the operation of the TIA, or discard the chip.

100



$$I_{in} + ((V_{out} - V_{N1})/R) - ib = 0$$

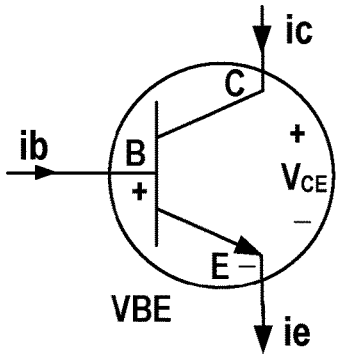
$$V_{out} = R(ib\text{-}I_{in}) + V_{N1}$$



$$I_{in} + ((V_{out} - V_{N1})/R) - ib = 0$$
$$V_{out} = R(ib\text{-}I_{in}) + V_{N1}$$

FIG. 1A

120



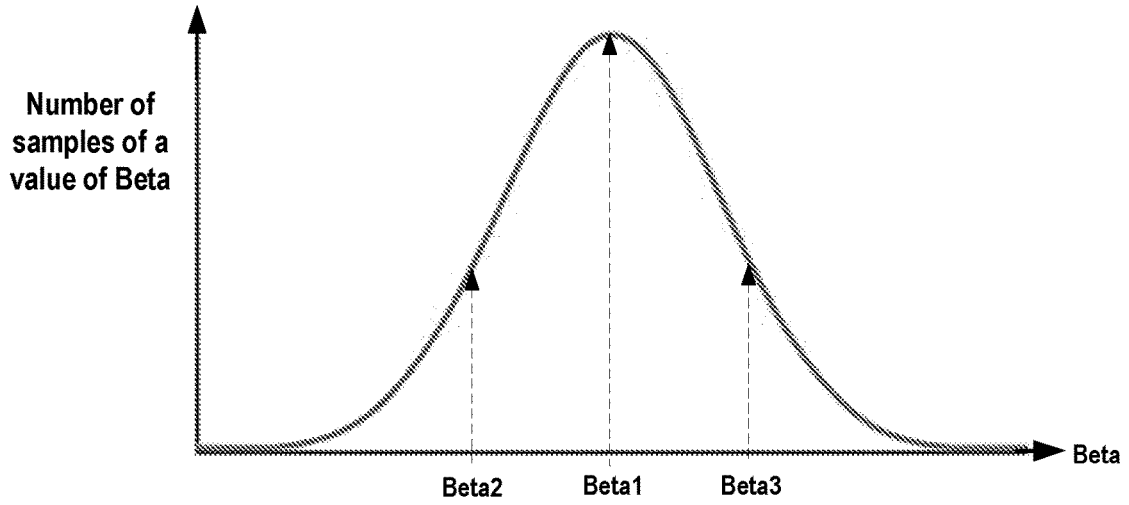
Bipolar Junction Transistor

Currrent Gain = Beta = ic/ib

ie = ic +ib

FIG. 1B

140



Beta1 has a maximum number of samples of a particular value of beta and represents a nominal value of beta. Beta2 has a lower number of samples of a particular value of beta and represents a reduced value of beta, or a low beta. Beta3 has a higher number of samples of a particular value of beta and represents an increased value of beta, or a high beta

FIG. 1C

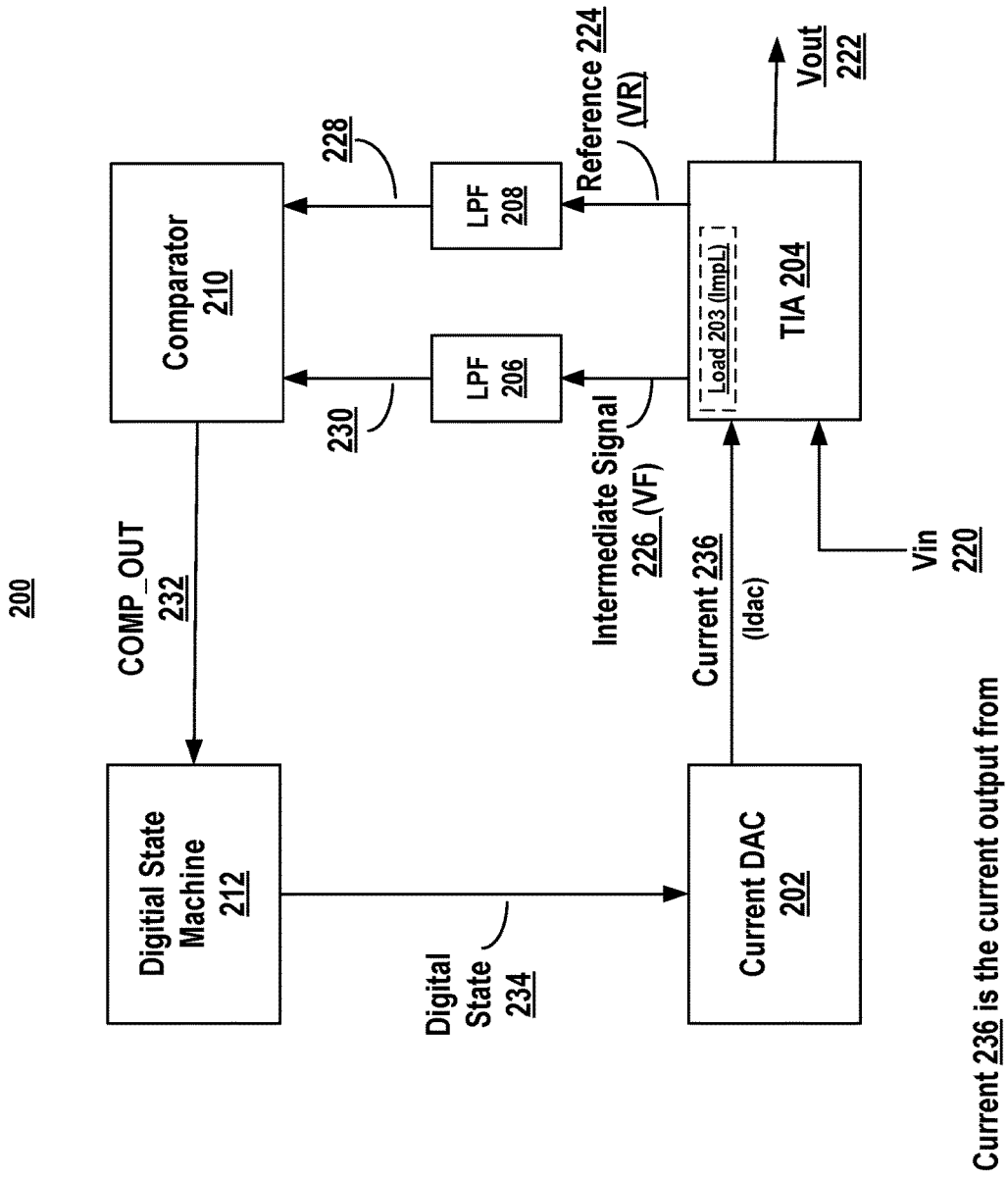
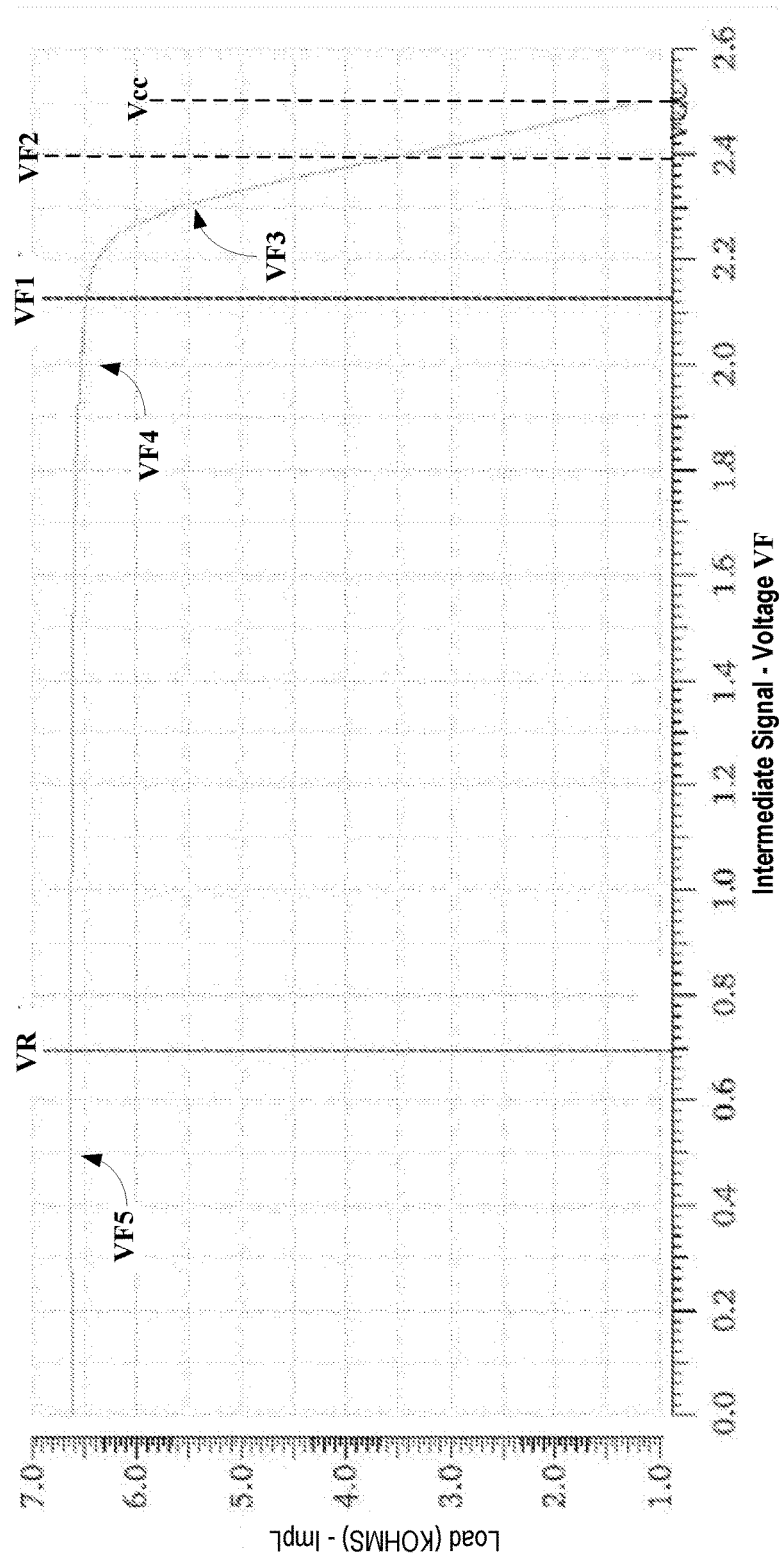

200
Digitial State Machine 212
COMP_OUT 232
Comparator 210
228
230
LPF 208
LPF 206
Reference 224 (VR)
Intermediate Signal 226 (VF)
Load 203 (ImpL)
TIA 204
Vout 222
Vin 220
Current 236 (Idac)
Current DAC 202
Digital State 234
Current 236 is the current output from Current DAC 202, or idac

FIG. 2A



An increase in VF (Intermediate Signal Voltage) relative to the Load (ImpL), may cause a decrease in component performance of a TIA. As illustrated, ImpL is relatively constant at lower VF voltages. At voltage VF1, the ImpL begins to rapidly decrease; at voltage VF2, TIA becomes non-operational; at voltage VF3, TIA is operational but with degraded performance; at voltage VF4, TIA is operational with acceptable performance; VR = Reference Voltage; Vcc = power supply voltage. In sample embodiment **250**, VF1 = 2.12 volts; VF2 = 2.4 volts, VF3 = 2.3 volts, VF4 = 2.0 volts; VR = 0.7 volts, Vcc = 2.5 volts. Values are approximate.

As illustrated, a TIA with an intermediate signal voltage of VF3 is operational but with degraded performance. With a calibration method, the TIA can compensate for deficiencies in component performance and reduce the intermediate signal voltage to VF4 to obtain acceptable performance. In some embodiments with a BJT, the component deficiency may be a high beta.

FIG. 2B

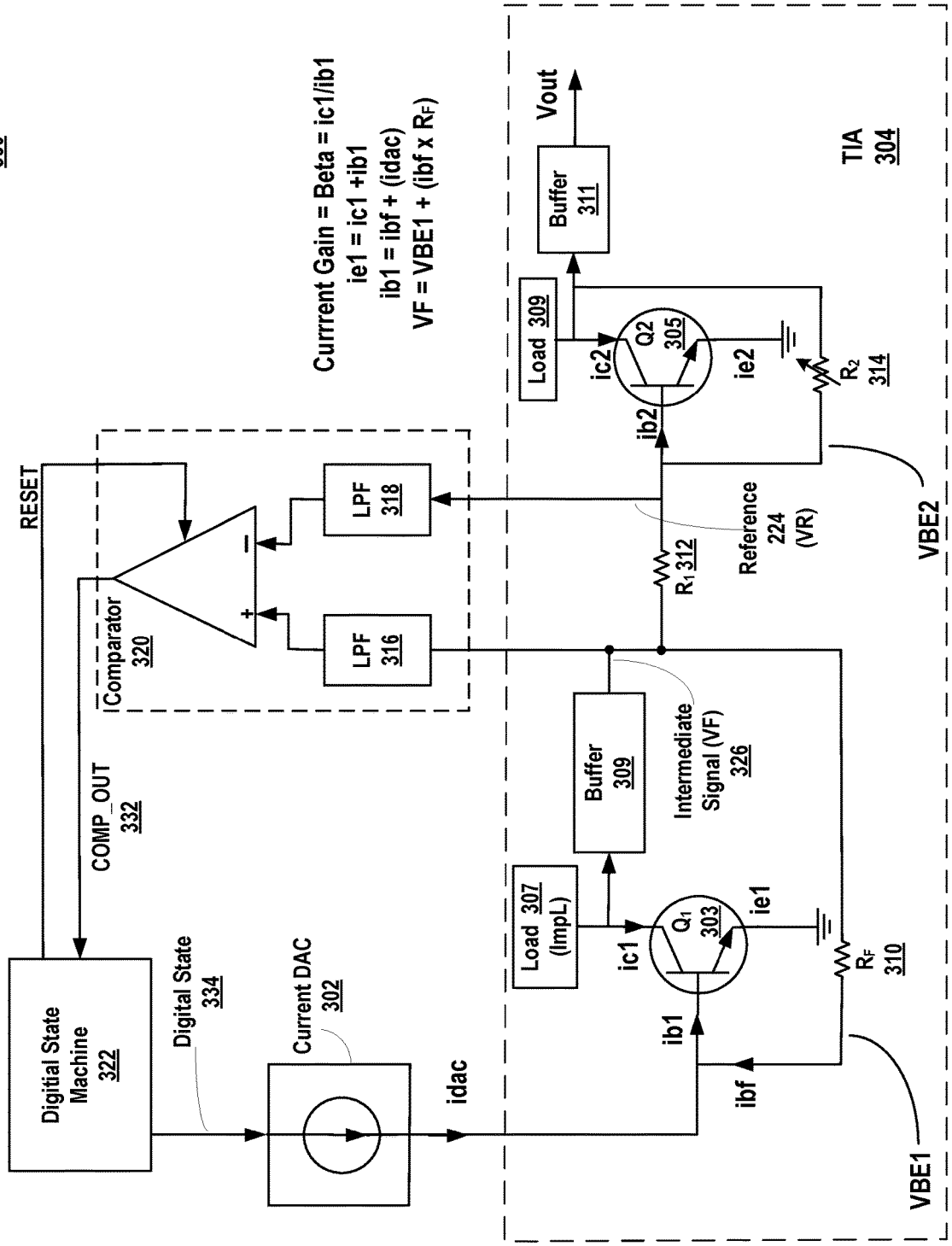

300
Currrent Gain = Beta = ic1/ib1
ie1 = ic1 +ib1
ib1 = ibf + (idac)
VF = VBE1 + (ibf x RF)
TIA 304
Vout
Buffer 311
Load 309
ic2
Q2 305
ie2
R2 314
ib2
VBE2
Reference 224 (VR)
R1 312
RESET
LPF 318
LPF 316
Comparator 320
COMP_OUT 332
Buffer 309
Intermediate Signal (VF) 326
Load 307 (ImpL)
ic1
Q1 303
ie1
RF 310
Digitial State Machine 322
Digital State 334
Current DAC 302
idac
ib1
ibf
VBE1

FIG. 3

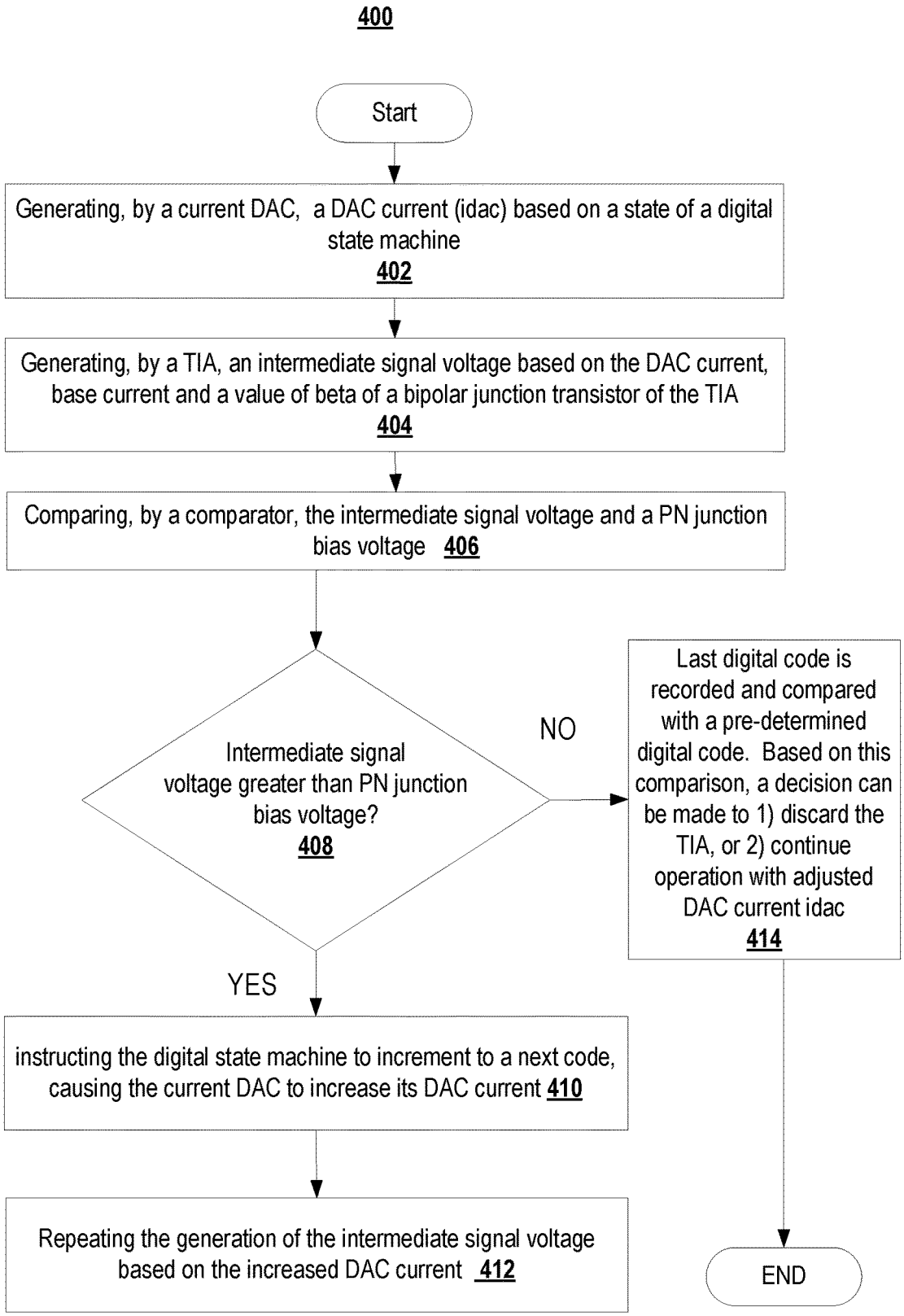

400
Start
Generating, by a current DAC, a DAC current (idac) based on a state of a digital state machine
402
Generating, by a TIA, an intermediate signal voltage based on the DAC current, base current and a value of beta of a bipolar junction transistor of the TIA
404
Comparing, by a comparator, the intermediate signal voltage and a PN junction bias voltage 406
Intermediate signal voltage greater than PN junction bias voltage?
408
NO
Last digital code is recorded and compared with a pre-determined digital code. Based on this comparison, a decision can be made to 1) discard the TIA, or 2) continue operation with adjusted DAC current idac
414
YES
instructing the digital state machine to increment to a next code, causing the current DAC to increase its DAC current 410
Repeating the generation of the intermediate signal voltage based on the increased DAC current 412
END

FIG. 4

SYSTEMS AND METHODS FOR TIA BASE CURRENT DETECTION AND COMPENSATION

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of and claims priority to U.S. patent application Ser. No. 16/181,523, titled "SYSTEMS AND METHODS FOR TIA BASE CURRENT DETECTION AND COMPENSATION" and filed on Nov. 6, 2018 (Attorney Docket No. VLI-023), which is hereby incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates generally to systems and methods for transimpedance amplifier (TIA), and more particularly to detect a base current of a bipolar junction transistor (BJT) in a TIA and to adjust the TIA operation to compensate for changing environmental and/or manufacturing conditions.

BACKGROUND

[0003] A transimpedance amplifier (TIA) may convert an input current source into an output voltage. The current to voltage gain may be based on a feedback resistance. A TIA may provide simple linear signal processing using an operational amplifier and a feedback resistor for dissipating current. The circuit may be able to maintain a constant voltage bias across the input source as the input current changes, which may be beneficial in a network of sensors. Transimpedance amplifiers may be used to process the current output of photodiodes, pressure transducers, accelerometers, and other types of sensors to a voltage formatted as a useable signal output. However, the performance of a TIA may be negatively impacted by 1) a change in environment, e.g. temperature, and 2) silicon wafer manufacturing variations.

[0004] Accordingly, what are needed are systems and methods that may detect performance deficiencies due the aforementioned conditions, and provide a recommendation to select either to discard the TIA or to cause adjustments in the operation of the TIA to improve the performance of the TIA.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] References will be made to embodiments of the invention, examples of which may be illustrated in the accompanying figures. These figures are intended to be illustrative, not limiting. Although the invention is generally described in the context of these embodiments, it should be understood that it is not intended to limit the scope of the invention to these particular embodiments. Items in the figures are not to scale.

[0006] FIG. **1**A illustrates a basic transimpedance amplifier circuit according to embodiments of the present document.

[0007] FIG. **1**B illustrates a schematic of a npn bipolar junction transistors (BJT).

[0008] FIG. **1**C illustrates a Gaussian distribution of the value of beta (β) according to embodiments of the present disclosure.

[0009] FIG. **2**A depicts an implementation of TIA Base Current Detection and Compensation Functional Blocks according to embodiments of the present disclosure.

[0010] FIG. **2**B illustrates conditions of operation of a TIA based on the relationship between intermediate signal, (voltageVF), and the impedance of a load of TIA, ImpL.

[0011] FIG. **3** depicts an implementation of TIA Base Current Detection and Compensation Circuits according to embodiments of the present disclosure.

[0012] FIG. **4** graphically illustrates a flowchart of a method of calibration to detect and compensate for a high base current in a bipolar junction transistor (BJT) according to embodiments of the current disclosure.

DETAILED DESCRIPTION OF EMBODIMENTS

[0013] In the following description, for purposes of explanation, specific details are set forth in order to provide an understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these details. Furthermore, one skilled in the art will recognize that embodiments of the present invention, described below, may be implemented in a variety of ways, such as a process, an apparatus, a system, a device, or a method on a tangible computer-readable medium.

[0014] Components, or modules, shown in diagrams are illustrative of exemplary embodiments of the invention and are meant to avoid obscuring the invention. It shall also be understood that throughout this discussion that components may be described as separate functional units, which may comprise sub-units, but those skilled in the art will recognize that various components, or portions thereof, may be divided into separate components or may be integrated together, including integrated within a single system or component. It should be noted that functions or operations discussed herein may be implemented as components. Components may be implemented in software, hardware, or a combination thereof.

[0015] Furthermore, connections between components or systems within the figures are not intended to be limited to direct connections. Rather, data between these components may be modified, re-formatted, or otherwise changed by intermediary components. Also, additional or fewer connections may be used. It shall also be noted that the terms "coupled," "connected," or "communicatively coupled" shall be understood to include direct connections, indirect connections through one or more intermediary devices, and wireless connections.

[0016] Reference in the specification to "one embodiment," "preferred embodiment," "an embodiment," or "embodiments" means that a particular feature, structure, characteristic, or function described in connection with the embodiment is included in at least one embodiment of the invention and may be in more than one embodiment. Also, the appearances of the above-noted phrases in various places in the specification are not necessarily all referring to the same embodiment or embodiments.

[0017] The use of certain terms in various places in the specification is for illustration and should not be construed as limiting. A service, function, or resource is not limited to a single service, function, or resource; usage of these terms may refer to a grouping of related services, functions, or resources, which may be distributed or aggregated.

[0018] The terms "include," "including," "comprise," and "comprising" shall be understood to be open terms and any

lists the follow are examples and not meant to be limited to the listed items. Any headings used herein are for organizational purposes only and shall not be used to limit the scope of the description or the claims. Each reference mentioned in this patent document is incorporate by reference herein in its entirety.

[0019] Furthermore, one skilled in the art shall recognize that: (1) certain steps may optionally be performed; (2) steps may not be limited to the specific order set forth herein; (3) certain steps may be performed in different orders; and (4) certain steps may be done concurrently.

A. Transimpedance Amplifier (TIA) and Bipolar Junction Transistors (BJT)

[0020] A transimpedance amplifier (TIA) may convert current to voltage. TIAs may be used to process the current output of photodiodes, pressure transducers, accelerometers, and other types of sensors to a voltage formatted as a useable signal output. TIAs provide linear signal processing using an operational amplifier and a feedback resistor for dissipating current. FIG. **1**A shows a basic transimpedance amplifier circuit **100**.

[0021] In FIG. **1**A, I_{in} represents the current output from a sensor and the gain (sensitivity) is resistance, R. Using Kirchhoff's Current Law (KCL), the sum of all currents flowing into a node is zero. If one assumes that the current flowing into the op amp is ib, KCL at node **N1** provides an equation:

$$I_{in}+((Vout-V_{n1})/R)-ib=0,$$

as noted in FIG. **1**A. The equation provides a voltage output, $Vout=R(ib-I_{in})+V_{n1}$.

[0022] Bipolar Junction Transistor (BJT) is a semiconductor device constructed with three doped Semiconductor Regions (Base, Collector and Emitter) separated by two p-n Junctions. The p-n junction between the Base and the Emitter has a Barrier Voltage (V_o) of about 0.6 V to 0.8 V. FIG. **1**B illustrates BJT **120** of a npn BJT. As illustrated in FIG. **1**B, V_o=VBE. A companion BJT has a pnp structure.

[0023] Per FIG. **1**B, the current flowing out of BJT **120**, emitter current ie, is equal to the currents flowing into BJT **120**, collector current ic and base current ib; thus the equation: ie=ic+ib. The current gain, or beta, of BJT **120** is equal to the ratio: ic divided by ib (ic/ib). In some embodiments, with a load resistance connected in series with the collector, the current gain (beta) of the common emitter transistor configuration may be quite large. Small changes in current flowing in the base of BJT **120** control the current in the emitter-collector circuit. In some embodiments, beta may have a value between 20 and 200 for general purpose transistors.

[0024] The value of beta may vary depending on changes in environment, e.g. 1) temperature, and 2) silicon wafer manufacturing variations. FIG. **1**C illustrates a Gaussian distribution of the value of beta **140**, according to embodiments of the present disclosure. One sample of the Gaussian distribution is Beta1, which is associated with transistor BJT1. Beta1 represents a nominal value of beta as it has a maximum number of samples for a particular value of beta. Another sample of the Gaussian distribution is associated with transistor BJT2, which has a beta with a value of Beta2. Beta2 has a lower number of samples of a particular value of beta as compared with Beta1 and represents a reduced value of beta, or a "low beta". In some embodiments, since ic is designed to be a constant current, with the lower value of beta (Beta2), the transistor BJT2 may generate a higher value of ib as compared with transistor BJT1 since ic is essentially constant. A decision may be made to discard transistor BJT2 or adjust the TIA to compensate for the higher value of ib.

[0025] In another embodiment, a sample of the Gaussian distribution of FIG. **1**C is Beta3, which is associated with transistor BJT3. Beta3 has a higher number of samples for a particular value of beta as compared with Beta1, and represents an increased value of beta, or a "high beta". Since ic is generally designed to be a constant current, with the higher value of Beta3, transistor BJT3 may generate a lower value of ib as compared with transistor BJT1, which has a beta of Beta1.

B. TIA Base Current Detection and Compensation Functional Blocks

[0026] FIG. **2**A depicts TIA Base Current Detection and Compensation Functional Blocks **200**, hereinafter, "Functional Blocks **200**", according to embodiments of the present disclosure. In operation, Vin **220** is coupled to TIA **204** that amplifies the input current and may generate the voltage, Vout **222**. Periodically, there may be a need to update the input current to adapt for changing environmental conditions. In this case, TIA **204** measures the status of its performance based on internally generated Intermediate Signal **226** having an associated voltage, VF. Voltage VF may indicate deficiencies requiring action. Intermediate Signal **226** (voltage VF) and a Reference **224** (voltage VR) are voltages, and are coupled to Comparator **210** via two corresponding low pass filters, LPF **206** and LPF **208** via Signal **228** and Signal **230**. Voltage VR is associated with Reference **224**. The output of Comparator **210**, COMP_OUT **232**, may be coupled to Digital State Machine **212**. Digital State Machine **212**, when triggered, increments the digital state from a current state to a next state. An output of Digital State Machine **212**, Digital State **234**, may reflect the state of Digital State Machine **212**. In one embodiment, Digital State Machine **212** may have 16 states.

[0027] If the voltage VF for Intermediate Signal **226** is greater than the voltage VR of Reference **224**, the output of Comparator **210** is a "1", which triggers an increment from a current state to a next state in Digital State Machine **212**. In one embodiment, the state may change from State2 to State3. Digital State Machine **212** is coupled via Digital State **234** to Current Digital-Analog-Converter (Current DAC) **202**. Current DAC **202** then converts the digital state, i.e., Digital State **234**, to a current indicated by Current **236**, which is the current output from Current DAC **202** (The current of Currrent DAC **202** is referred to as idac). In other words, Current DAC **202** is a state machine controlled low noise current DAC. In some embodiments, the change for State2 to State3 causes an increased value of current for Current **236**. Current **236** is in turn coupled to TIA **204**. TIA **204** then responds to Current **236** and implements another cycle of comparing voltage VF to voltage VR.

[0028] If the voltage VF for Intermediate Signal **226** is less than the voltage VR of Reference **224**, the output of Comparator **210** maintains a value of "0". In this case, the state of Digital State Machine **212** remains the same, and there is no change in Current **236**.

[0029] Functional Blocks **200** may be utilized in a calibration method in order to detect performance deficiencies

and provide a recommendation to select either to discard the TIA or to cause adjustments in the operation of the TIA to improve the performance. Performance may be based on the relationship between a load in the TIA and the voltage VF, as discussed relative to FIG. **2**B. Key elements in the calibration method are the relationships between current idac, and voltages VF and VR. In a beginning state, idac=0, and VF>VR, causing an increment in the digital code of the state machine (Digital State Machine **234**), which causes an increase in idac. Based on the increased idac, the process may repeat. As idac increases, VF decreases. At some point VF<VR, causing the state machine stop incrementing the digital code. At this point, TIA **204** may be considered calibrated and the last digital code is recorded.

[0030] With the completion of calibration and the digital code of the state machine recorded, the following decisions may be implemented: (1) compare the recoded digital code to a predetermined code to decide whether to discard the TIA. The predetermined code may be based on design, simulation and expectation parameters. Or, 2) based on the comparison of the recoded digital code to a predetermined code, proceed with operation of the TIA. In this case, the adjusted digital code has compensated for deficiencies in the operation.

[0031] An increase in VF may cause degradation in the performance of components of TIA **204**. Specifically, the condition of VF being "close" to the supply voltage Vcc may cause TIA **204** to be in a non-operating condition. FIG. **2**B illustrates via embodiment **250** the conditions for operation of TIA **204** based on the relationship between Intermediate Signal **226** (voltage VF) and the impedance of a Load **203**, ImpL, of TIA **204**. The value of the power supply voltage, Vcc and the value of VR are noted on FIG. **2**B. As illustrated, at lower values of VF, ImpL is relatively constant, with minimal declines in the value of the impedance. At a higher value of VF, for example, VF1, ImpL begins to rapidly decrease, significantly impacting the components and performance of TIA **204**. In some embodiments, VF1 may be 70% of Vcc, a power supply voltage for TIA **204**.

[0032] When VF increases to a value of VF2, TIA **204** may no longer be operational. The voltage VF2 may be a pre-determined value based on ImpL. This pre-determined value may be based on the design and components of TIA **204**. In some embodiments, this pre-determined value of VF2 may be 50% of ImpL. That is, TIA **204** may no longer be operational when ImpL has declined in value by 50%, as illustrated in FIG. **2**B.

[0033] Alternatively, for pnp bipolar junction transistors, the condition of the value of VF being "low", compared with Vcc may cause the TIA **204** to be in a non-operating condition. In embodiment **250**, VF5 illustrates a "low" condition. This condition may occur if VF5 is less than a pre-determined value of Vcc. In some embodiments, pre-determined value of VF5 may be 20%. That is, TIA **204** may be in a non-operating condition when VF5 is 20% of Vcc.

[0034] In summary, an increase in VF (Intermediate Signal Voltage) relative to the Load (ImpL) associated with a TIA, may cause a decrease in component performance of a TIA. As illustrated in embodiment **250**, ImpL is relatively constant at lower VF voltages. At voltage VF1, the ImpL begins to rapidly decrease; at voltage VF2,TIA becomes non-operational; at voltage VF3, TIA is operational but with degraded performance; at voltage VF4, TIA is operational with acceptable performance; VR=Reference Voltage; Vcc=power supply voltage. Voltage VF4 refers to a range of voltages below VF1. Voltage VF3 refers to a range of voltages between VF1 and VF2. In sample embodiment **250**, VF1=2.12 volts; VF2=2.4 volts, VF3=2.3 volts, VF4=2.0 volts; VR=0.7 volts, Vcc=2.5 volts. Values are approximate.

[0035] As illustrated in embodiment **250**, a TIA with an intermediate signal voltage of VF3 is operational but with degraded performance. With a calibration method, the TIA can compensate for deficiencies in component performance and reduce the intermediate signal voltage to VF4 to obtain acceptable performance. In some embodiments with a BJT, the component deficiency may be a high beta.

C. TIA Base Current Detection and Compensation Circuit

[0036] FIG. **3** depicts TIA Base Current Detection and Compensation Circuits **300** (hereinafter "Circuits **300**") according to embodiments of the present disclosure. FIG. **3** includes a BJT implementation of TIA **204** of Functional Blocks **200**. Circuits **300** implements detection and compensation of the TIA base current utilizing the properties of a BJT. The voltages, VBE1 and VBE2, are determined primarily by the P-N junction of silicon, which is approximately 0.7 volts (barrier voltage).

[0037] Circuit **300** comprises Current DAC **302**, TIA **304**, Comparator **320**, and Digital State Machine **322**. TIA **304** comprises several components including two BJTs as illustrated in FIG. **3**. One BJT is Q_1 **303**, which is coupled to a feedback resistor, R_F **310**. Associated with these components are: ib1−base current of Q_1 **303**; ibf−current through resistor R_F; idac−current from Current DAC **302**, where ib1=ibf+(idac).

[0038] An output of Current DAC **302** may be coupled to the base of Q_1 **303** and to one end of R_F **310**. The collector of Q_1 **303** may be coupled to Load **307** and Buffer **311**. An output of Buffer **311** may be coupled to the other end of R_F **310**, hence providing a feedback resistor for Q_1 **303**. An output of Buffer **311** is the Intermediate Signal **326** having an associated voltage, VF, where VF=VBE1+(ibf×R_F). Intermediate Signal **326** is coupled via R_1 **312** to the base of Q2 **305**. The components Load **309**, variable resistor, R_2 **314**, and Buffer **311** collectively operate to generate Vout, an output of the transimpedance amplifier.

[0039] Voltage VF and Voltage VR are separately coupled to Comparator **320**, which in turn is coupled via COMP_OUT **332** to Digital State Machine **322**, which in turn is coupled to Current DAC **302** via Digital State **334**. Current DAC **302** generates idac, which is coupled to the base of Q1 **303**. The operation of Comparator **320**, Digital State Machine **322**, and Current DAC **302** are equivalent to the previously described operation of Comparator **210**, Digital State Machine **212**, and Current DAC **202** as previous described for FIG. **2**A. The inputs to Comparator **320** are filtered by LPF **316** and LPF **318**.

[0040] A goal for the operation of Circuits **300** is the detection of performance deficiencies due to 1) a change in environment, e.g. temperature, and 2) silicon wafer manufacturing variations, and provide a recommendation to select either to discard the TIA or to cause adjustments in the operation of the TIA to achieve an acceptable performance. As previously discussed relative to FIG. **2**B, acceptable performance may be defined relative to the relationship between a load of a TIA and the Intermediate Signal Voltage VF. A consideration for Circuits **300** is the neutralization of

a "high" ibf current due to a "high" ib1 current caused due to low beta. The operation may be described as follows:

[0041] Ib1=ibf+idac

[0042] The base current, ib1 is dependent on beta of Q_1 **303**, which may vary with process and environment, as previously noted. Beta=ic1/ib1

[0043] An intermediate signal voltage: VF=VBE1+(ibf×RF)

[0044] If the beta is low (decreased), a large base current, ib1, may result, causing a large voltage drop across RF, and may place TIA in a non-operating mode.

[0045] If ib1 is high (increased), the level of current "idac" required to make ibf=0 may also be large.

[0046] When idac becomes equal to ib1, ibf becomes zero. Then, a further increase in idac may cause ibf to become negative and Comparator **320** will flip, i.e. transition from a "1" to a "0" state. The "1" state may cause Digital State **322** to increment Digital State **334**, which in turn increases idac current. The "0" state may cause Digital State **322** to not increment Digital State **334**, which in turn results in no change in the idac current. The status of Comparator **320** may be determined based on the value of voltage VF relative to the value of voltage VBE2, where VBE2 is primarily determined by the Barrier Voltage (V_0) of about 0.6 V to 0.8 V.

[0047] Hence, the value of idac that causes the Comparator **320** to flip or transition indicates a threshold base current. This threshold base current, from the Current DAC **302**, may be utilized to decide to neutralize ibf or discard the chip.

[0048] Periodic calibration of Circuits **300** may be appropriate to insure proper operation of the TIA. Changing environmental conditions may cause the need for the calibration, which may update the current level.

D. Methods

[0049] FIG. **4** graphically illustrates a flowchart **400** of a method of calibration to detect and compensate for a high base current in a bipolar junction transistor (BJT) according to embodiments of the current disclosure. The method may be referred to as a calibration process and may be based on utilizing Circuits **300**. . The method comprises the steps of:

[0050] Generating, by a current DAC **302**, a DAC current (idac) based on a state of a digital state machine **322** (step **402**)

[0051] Generating, by a TIA, an intermediate signal voltage VF based on the DAC current, base current ib1 and a value of beta of a bipolar junction transistor Q_1 **303** of the TIA. (step **404**)

[0052] Comparing, by Comparator **320**, the intermediate signal voltage VF and a PN junction bias voltage. (step **406**)

[0053] Is the intermediate signal voltage VF greater than the PN junction bias voltage? (step **408**)

[0054] If yes, the output of the comparator changes state, instructing a digital state machine to increment to a next digital code (or state of Digital State Machine **212**), causing the current DAC to increase its DAC current idac (step **410**)

[0055] Then, repeating the generation of the intermediate signal voltage VF based on the increased DAC current idac (step **412**)

[0056] If no, the last digital code is recorded and compared with a pre-determined digital code. Based on this comparison, a decision can be made to **1**) discard the TIA, or **2**) continue operation with adjusted DAC current idac. (step **414**)

[0057] As previously discussed for FIG. **2**B, an increase in VF may cause degradation in the performance of components of TIA **204**. Specifically, the condition of VF being "close" to the supply voltage Vcc may cause TIA **204** to be in a non-operating condition. FIG. **2**B illustrates conditions for operation of TIA **204** based on the relationship between Intermediate Signal **226** VF and the impedance of a Load **203**, ImpL, of TIA **204**. [move to summary?]

[0058] In summary, A system for detecting and adjusting the operation of a TIA comprises (1) a current digital to analog converter (DAC) operable to generate an idac current based on a first state level of a digital state machine; (2) a transimpedance amplifier (TIA) operable to receive the current and to generate an intermediate signal voltage (VF) and generate an output voltage (Vout); (3) a comparator operable to receive the intermediate signal voltage (VF) and a reference voltage and generate an output; and (4) the digital state machine operable to generate second state level based on the output of the comparator. The current DAC changes its idac generated current if there is a difference between the first state level and the second state level.

[0059] If the intermediate signal voltage is greater than the reference voltage, the output of the comparator is a "1", causing the digital state machine to increment the first state level to a higher level state for the second state, in turn causing the current DAC to increase the idac current coupled to the TIA. If the intermediate signal voltage is less than the reference voltage, the output of the comparator is a "0", causing no change in the state level of the digital state machine, and causing no change to idac current coupled to the TIA. The reference voltage is based on a barrier voltage of a bipolar junction transistor (BJT). The barrier voltage varies between 0.6 voltages and 0.8 voltages.

[0060] The TIA comprises a first bipolar junction transistor (BJT), and the intermediate signal voltage (VF) is based in part on the value of beta of the first BJT. A first base current (ib1) for the first BJT is equal to the current from the current DAC (idac) plus a feedback current (ibf) received via a feedback resistor, wherein the intermediate signal voltage (VF) equals the barrier voltage plus the feedback current (ibf) times the resistance of the feedback resistor. When VF increases to a pre-determine value, the impedance of the load of the TIA decreases, causing the TIA to no longer operate. If the digital state machine increments to the higher level state, the idac current increases, and the TIA repeats the generation of another value of the intermediate signal voltage (VF) utilizing the increased idac current. If the digital state machine does not increment to a higher level state, a current state is recorded and compared with a pre-determined state, and wherein, based on the comparison, a decision is made to 1) discard the TIA, or 2) continue operation with last adjusted idac current. An operation status of the TIA is based on a relationship between intermediate signal voltage (VF) and an impedance of a load of the TIA, wherein an increase in intermediate signal voltage (VF) causes degradation in the operation status of the TIA.

[0061] A variation of a beta of the first BJT causes an inverse variation of the intermediate signal voltage that in turn causes a change in the first base current (ib1) for the first BJT, wherein the change in the first base current (ib1) compensates for the variation in the beta. The reference

voltage is based on the barrier voltage of a second BJT in the TIA. The current to voltage gain may be based on a feedback resistance. A goal for the operation of the system is the neutralization of a high ibf current due to a large ib1 current.

[0062] A method for detecting and adjusting the operation of a TIA comprises generating a DAC current by a current DAC and coupling the DAC current to a transimpedance amplifier (TIA); generating, by the TIA, an intermediate signal voltage (VE) based on the DAC current, a base current and a value of beta of a bipolar junction transistor of the TIA; comparing, by a comparator, the intermediate signal voltage (VF) and a PN junction bias voltage.

[0063] If the intermediate signal voltage is greater than the PN junction bias voltage, the output of the comparator changes, instructing a digital state machine to increment to a next digital code, causing the current DAC to increase its DAC current; and repeating the generation of the intermediate signal voltage (VF) based on the increased DAC current. If the intermediate signal voltage (VF) is not greater than a PN junction bias voltage, recording the last digital code and comparing the last digital code with a pre-determined digital code.

E. System Embodiments

[0064] It will be appreciated to those skilled in the art that the preceding examples and embodiments are exemplary and not limiting to the scope of the present disclosure. It is intended that all permutations, enhancements, equivalents, combinations, and improvements thereto that are apparent to those skilled in the art upon a reading of the specification and a study of the drawings are included within the true spirit and scope of the present disclosure. It shall also be noted that elements of any claims may be arranged differently including having multiple dependencies, configurations, and combinations.

What is claimed is:

1. A system comprising:

a current digital to analog converter (DAC) operable to generate an idac current based on a first state level of a digital state machine;

a transimpedance amplifier (TIA) operable to receive the idac current and to generate an intermediate signal voltage (VF) and generate an output voltage (Vout);

a comparator operable to receive the intermediate signal voltage (VF) and a reference voltage and generate an output; and

the digital state machine operable to generate a second state level based on the output of the comparator,

wherein, the current DAC changes its generated idac current if there is a difference between the first state level and the second state level.

2. The system of claim **1**, wherein if the intermediate signal voltage (VF) is greater than the reference voltage, the output of the comparator is a "1", causing the digital state machine to increment the first state level to a higher level state for the second state level, in turn causing the current DAC to increase the idac current.

3. The system of claim **2**, wherein if the digital state machine increments to the higher level state, the idac current increases, and the TIA repeats generation of another value of the intermediate signal voltage (VF) utilizing the increased idac current.

4. The system of claim **1**, wherein if the intermediate signal voltage (VF) is less than the reference voltage, the output of the comparator is a "0", causing no change in a state level of the digital state machine, and causing no change to idac current coupled to the TIA.

5. The system of claim **4**,

wherein, if the digital state machine does not increment to a higher level state, a current state is recorded and compared with a pre-determined state, and

wherein, based on the comparison, a decision is made to 1) discard the TIA, or 2) continue operation with last adjusted idac current.

6. The system of claim **1**, wherein the TIA comprises a first bipolar junction transistor (first BJT), and the intermediate signal voltage (VF) is based in part on a value of beta of the first BJT.

7. The system of claim **6**, wherein a first base current (ib1) for the first BJT is equal to the current from the idac current plus a feedback current (ibf) received via a feedback resistor, wherein the intermediate signal voltage (VF) equals a voltage VBE1, which is primarily based on a barrier voltage, plus the feedback current (ibf) times a resistance of the feedback resistor.

8. The system of claim **7**, wherein a decrease in the value of beta of the first BJT, that causes an increase in the first base current (ib1), is neutralized by incrementing a digital state of the digital state machine in order to increase the idac current.

9. The system of claim **7**, wherein when the idac current equals the first base current (ib1), then the idac current increases in value to cause feedback current (ibf) to become negative, the comparator to transitions from a "1" to a "0".

10. The system of claim **6**, wherein a variation of a beta of the first BJT causes an inverse variation of the intermediate signal voltage (VF) that in turn causes a change in a first base current (ib1) for the first BJT, wherein the change in the first base current (ib1) compensates for the variation in the beta.

11. The system of claim **6**, wherein the value of beta may vary depending on changes in environment, e.g. 1) temperature, and 2) silicon wafer manufacturing variations.

12. The system of claim **1**, wherein the reference voltage is based on a barrier voltage of a second BJT in the TIA.

13. The system of claim **1**, wherein an operation status of the TIA is based on a relationship between the intermediate signal voltage (VF) and an impedance of a load of the TIA.

14. The system of claim **13**, wherein when VF increases to a pre-determine value, the impedance of the load of the TIA decreases, causing the TIA to no longer operate.

15. A method comprising:

generating a DAC current by a current DAC and coupling the DAC current to a transimpedance amplifier (TIA);

generating, by the TIA, an intermediate signal voltage (VF) based on the DAC current, a base current and a value of beta of a bipolar junction transistor of the TIA;

comparing, by a comparator, the intermediate signal voltage (VF) and a PN junction bias voltage;

if the intermediate signal voltage (VF) is greater than the PN junction bias voltage and an output of the comparator changes, instructing a digital state machine to increment to a next digital code, causing the current DAC to increase its DAC current; and

repeating the generation of the intermediate signal voltage (VF) based on the increased DAC current.

16. The method of claim **15**, further comprising:

if the intermediate signal voltage (VF) is not greater than the PN junction bias voltage, recording the last digital code and comparing the last digital code with a pre-determined digital code.

17. The method of claim **16**, further comprising:

based on the comparison, deciding to 1) discard the TIA, or 2) continue operation with adjusted DAC current idac.

18. A system comprising:

a current digital to analog converter (DAC) operable to generate an idac current based on a first state level of a digital state machine;

a transimpedance amplifier (TIA) comprising a first bipolar junction transistor (BJT) having an associated load, and a second BJT, operable to receive the idac current and to generate an intermediate signal voltage (VF) and generate an output voltage (Vout);

a comparator operable to receive the intermediate signal voltage (VF) and a reference voltage and generate an output; and

the digital state machine operable to generate a second state level based on the output of the comparator,

wherein, the current DAC changes its generated idac current if there is a difference between the first state level and the second state level.

19. The system of claim **18**, wherein when VF increases to a pre-determine value, an impedance of the associated load of the TIA decreases, causing the TIA to no longer operate.

20. The system of claim **18**, wherein if the intermediate signal voltage (VF) is greater than the reference voltage, the output of the comparator is at a "STATE1", causing the digital state machine to increment the first state level to a higher level state for the second state level, in turn causing the current DAC to increase the idac current, wherein if the intermediate signal voltage (VF) becomes less than the reference voltage, the output of the comparator is a "STATE2", causing no change in a state level of the digital state machine, and causing no change to idac current coupled to the TIA.

* * * * *