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(54) METHOD FOR SHAPING THIN FILMS IN THE NEAR-EDGE REGIONS OF IN-PROCESS SEMICONDUCTOR SUBSTRATES

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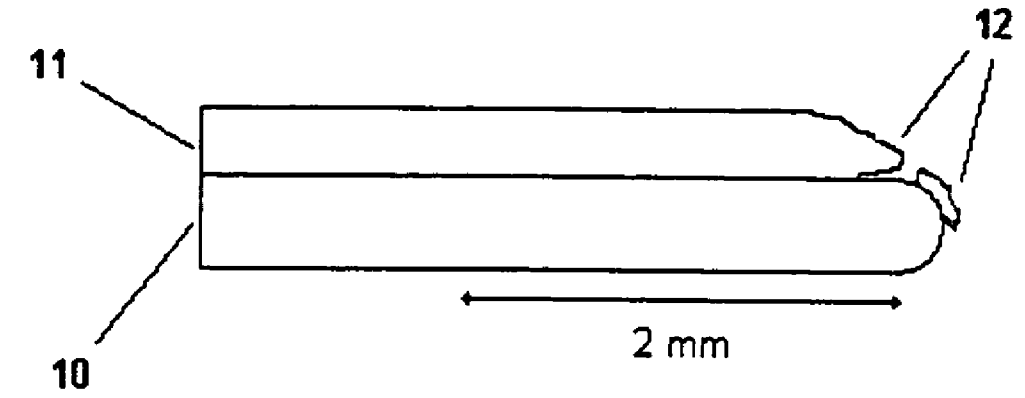
(57) **ABSTRACT**

A method for shaping and/or encapsulating near-edge regions of a substrate wafer is described. A housing provides channels for flowing a reactive gas towards the wafer edge. The reactive gas is directed towards the wafer edge for removing or depositing a thin film on the wafer edge. Gasses are exhausted downstream from the flow of the reactive gas. A second channel in the housing directs a flow of diluent/quenching gas onto the wafer for exhausting of the diluent/quenching gas and the reactive gas away from the wafer. The method may also provide a sequence of process steps, for example, selectively etching of a material on the wafer, etching of second material on the wafer and depositing an encapsulating material layer on the wafer.



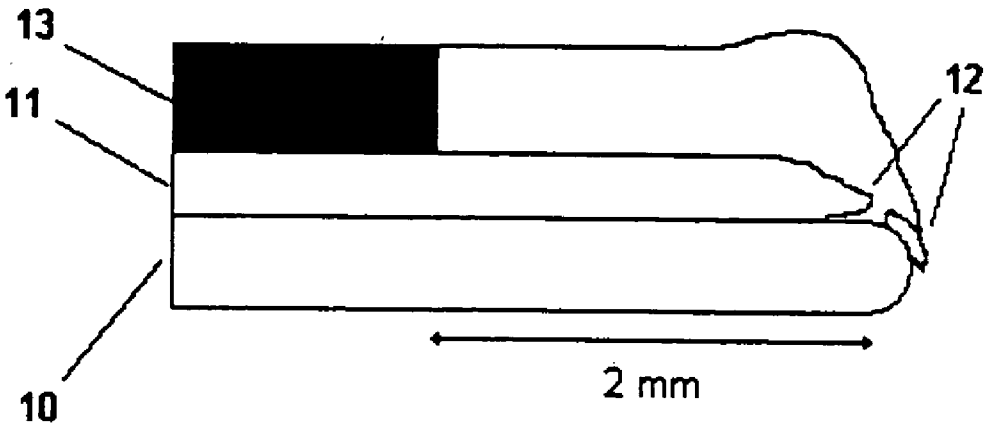


Fig. 1a

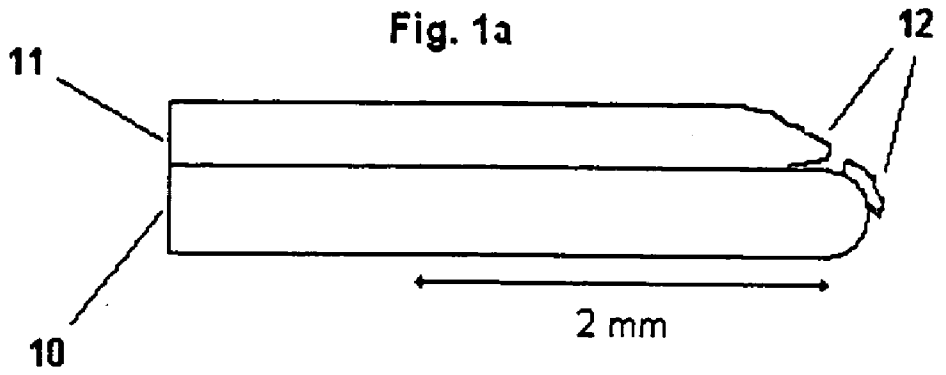


Fig. 1b

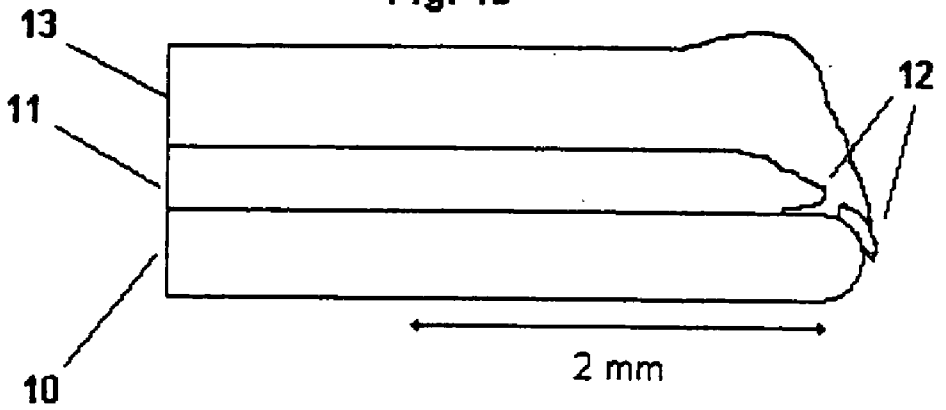


Fig. 1c

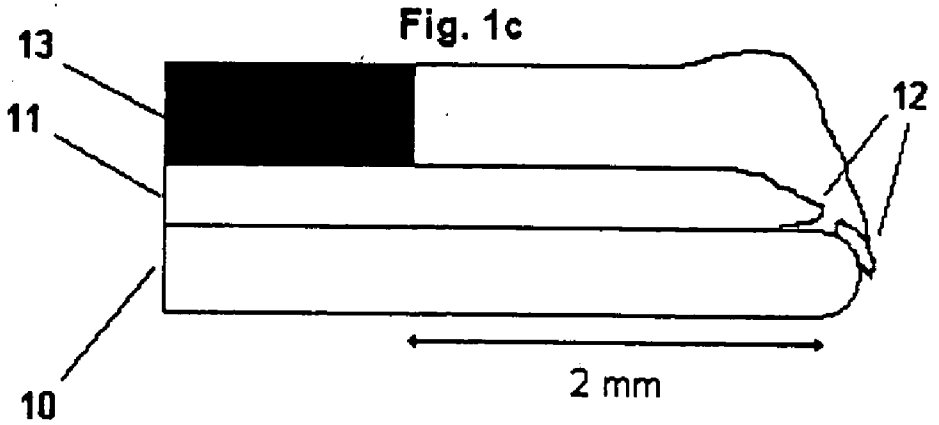


Fig. 1d

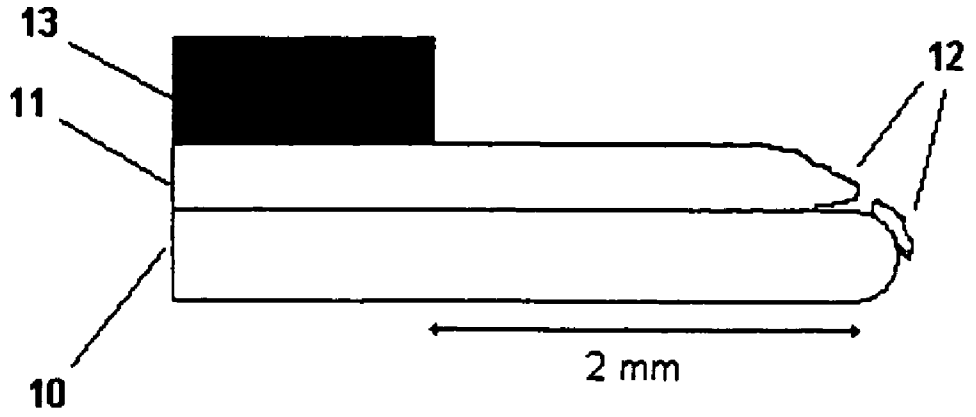


Fig. 1e

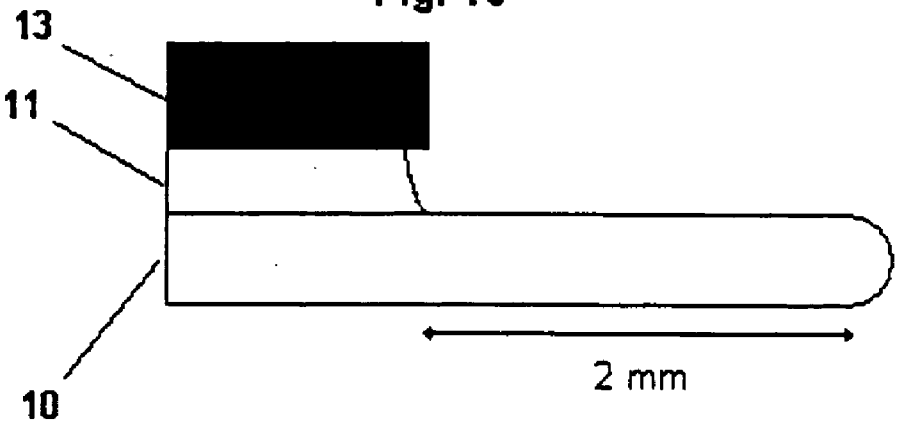


Fig. 1f

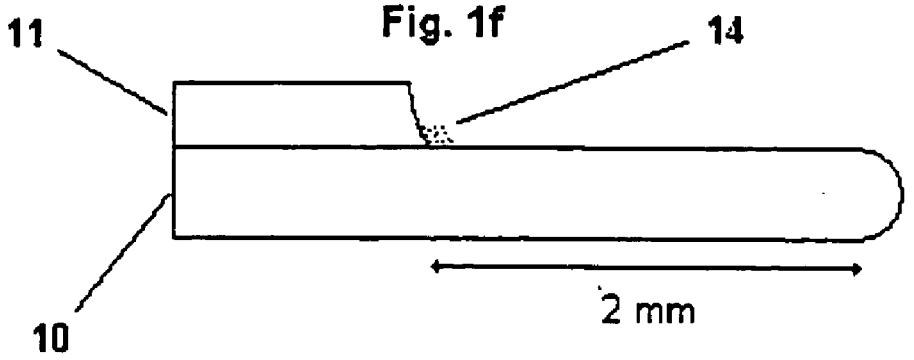


Fig. 2a

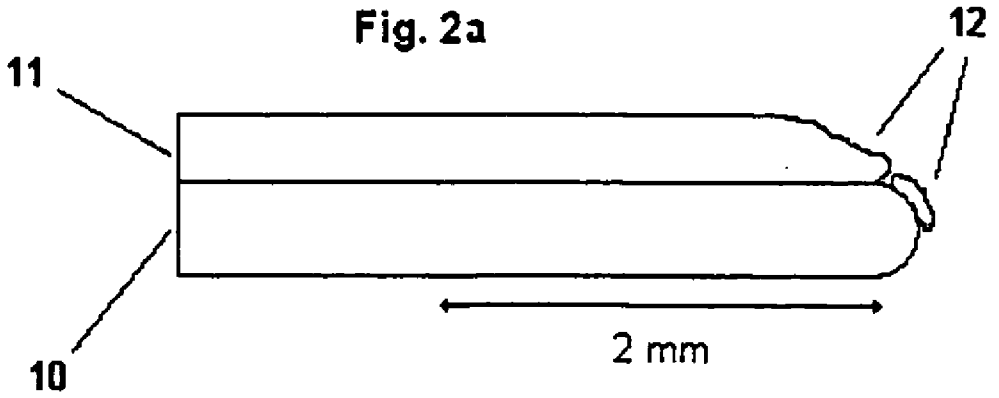


Fig. 2b

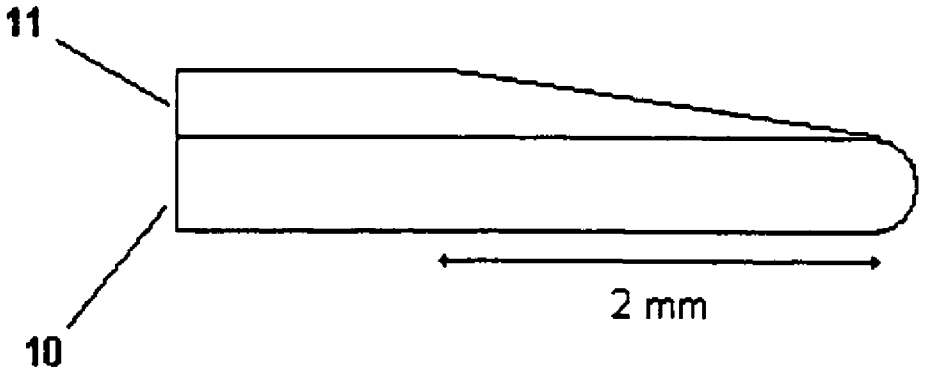


Fig. 2c

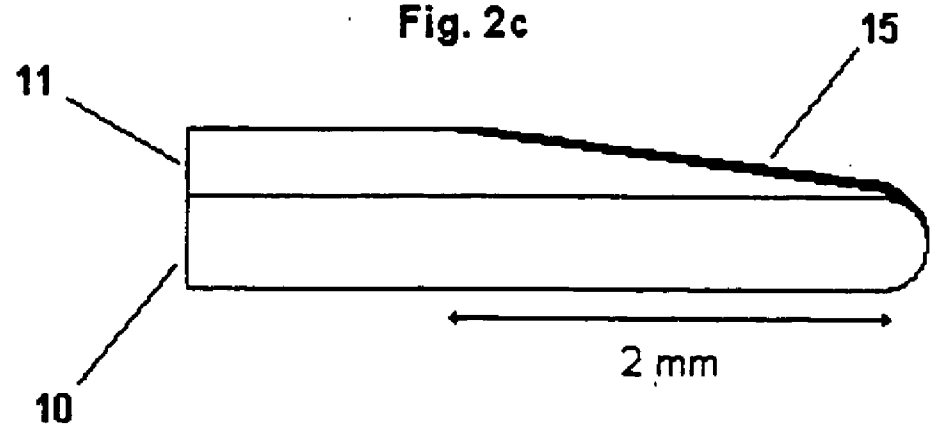


Fig. 3

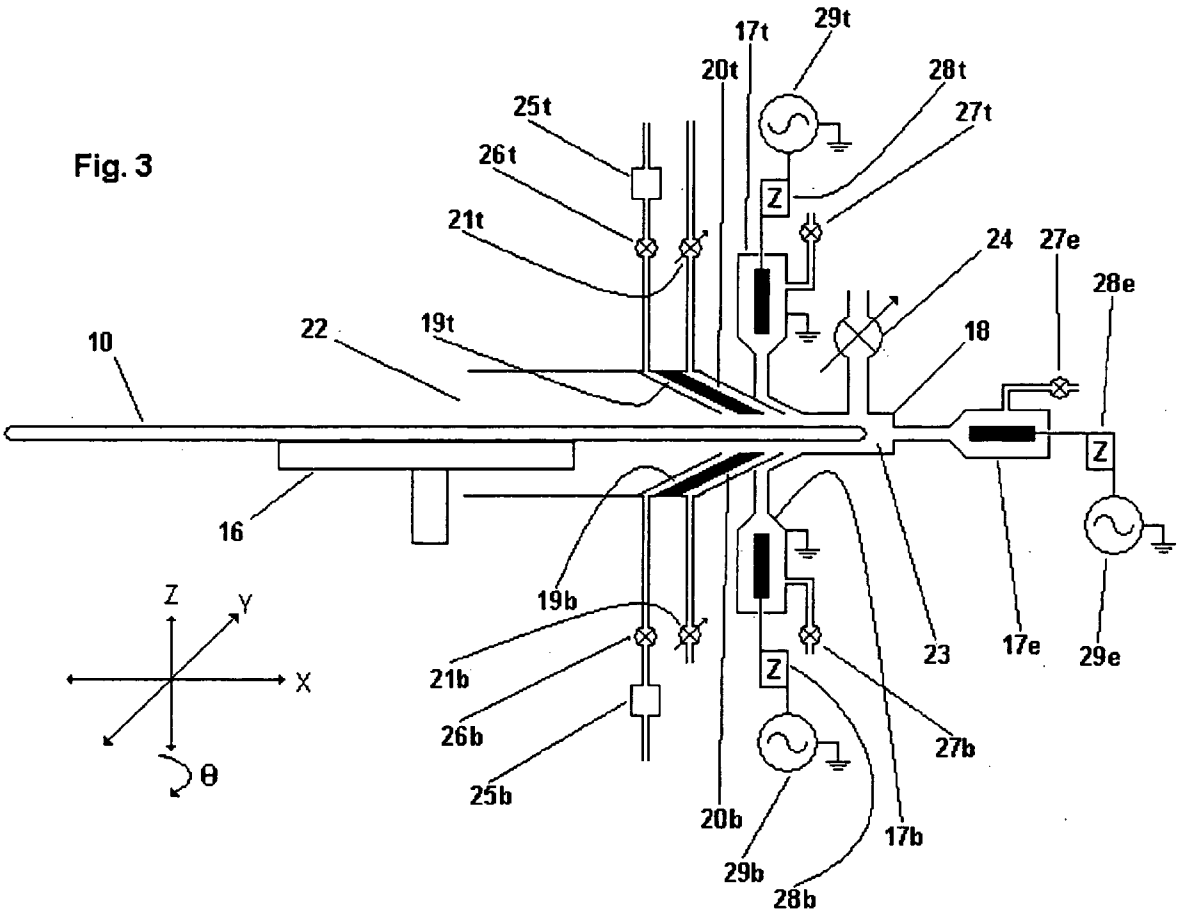

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Fig. 4

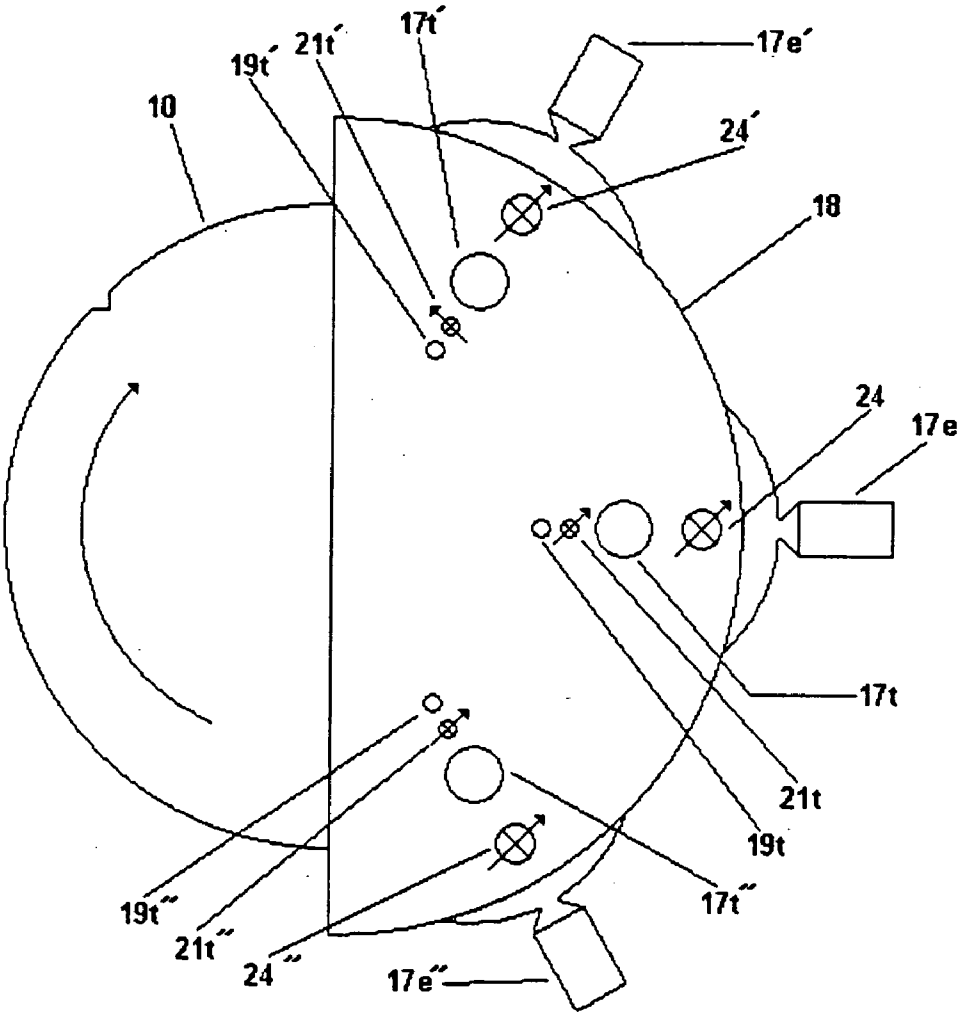

Fig. 5

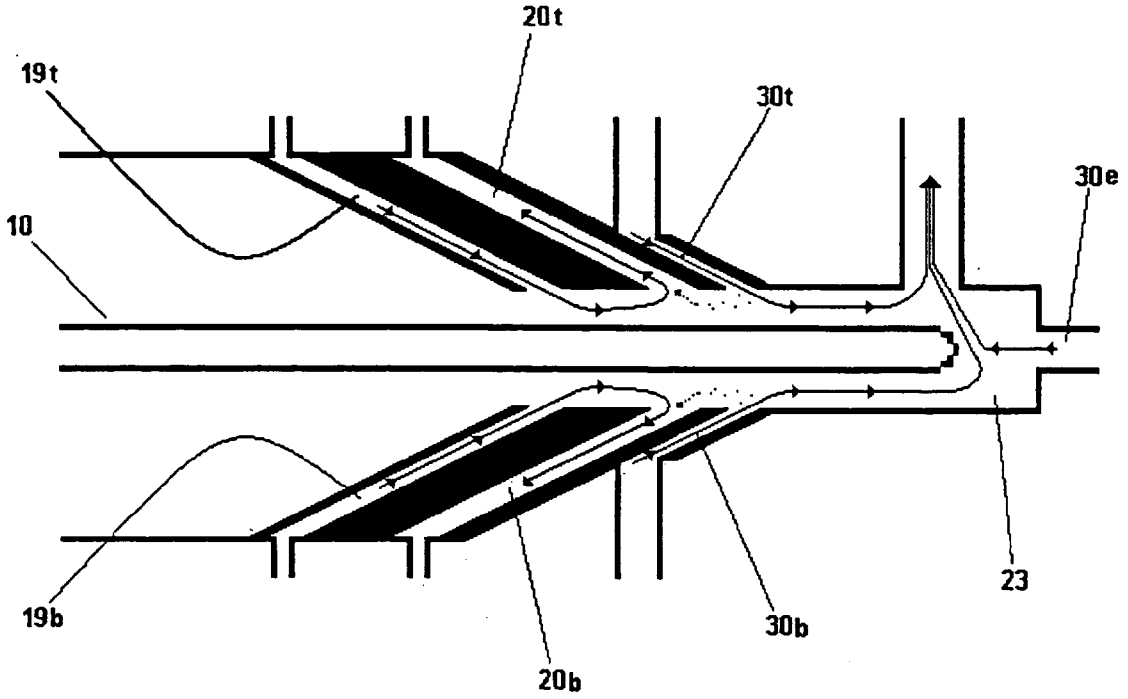

Fig. 6

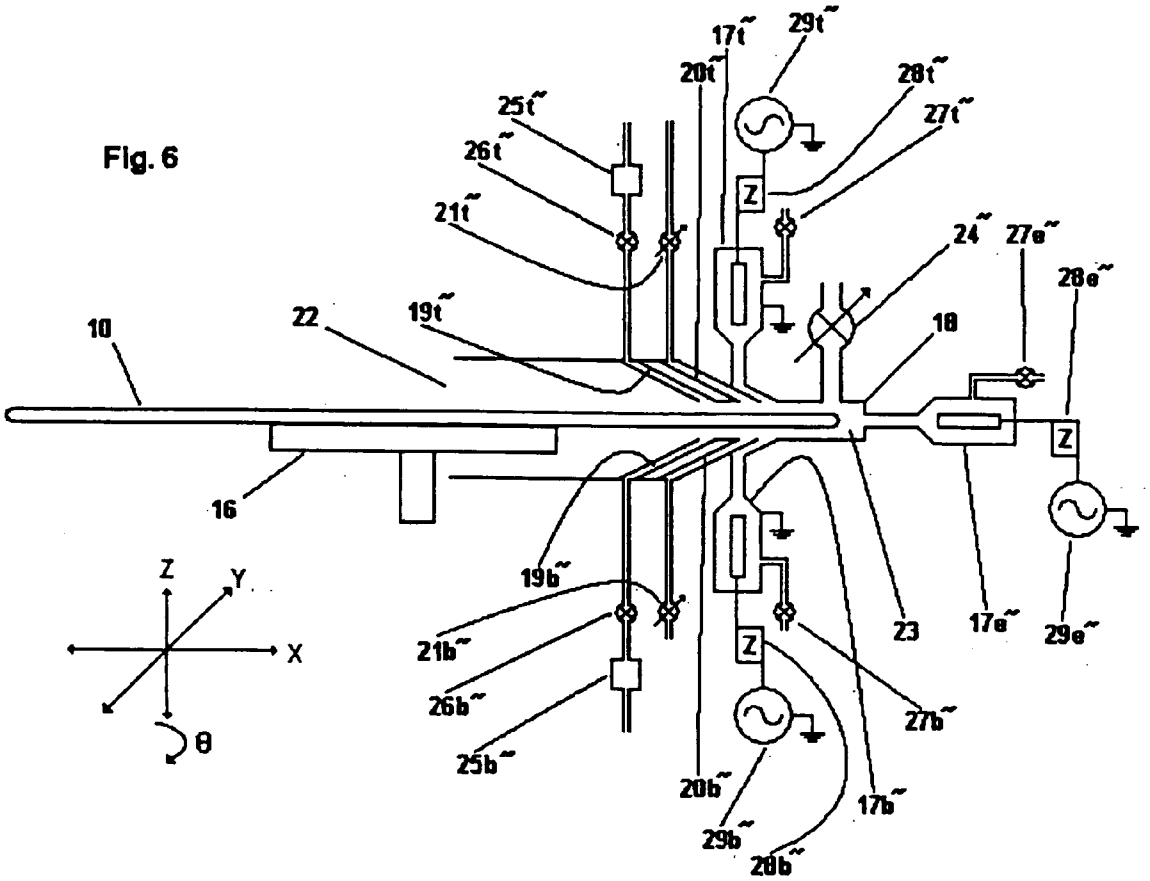
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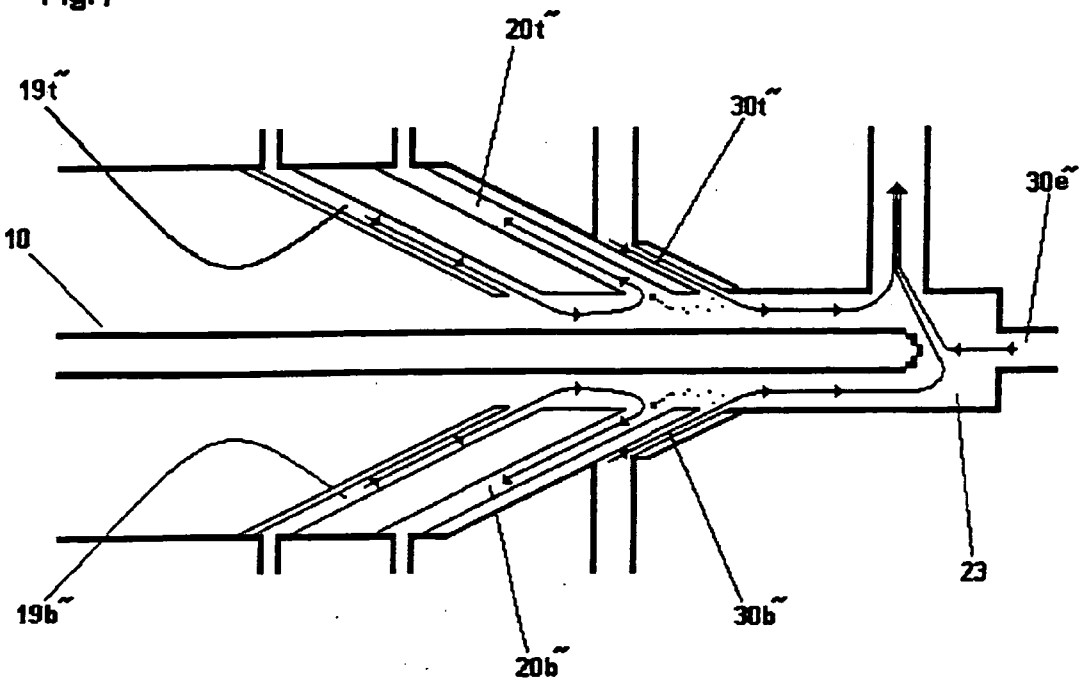
Fig. 7



METHOD FOR SHAPING THIN FILMS IN THE NEAR-EDGE REGIONS OF IN-PROCESS SEMICONDUCTOR SUBSTRATES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. patent application Ser. No. 10/401,074 filed on Mar. 27, 2003, which claims the benefit of Provisional Application 60/376,154, filed Apr. 26, 2002. The disclosures of the above applications are incorporated herein by reference.

FIELD OF THE INVENTION

[0002] This invention relates to a method and apparatus for shaping thin films on in-process semiconductor substrates. More particularly, this invention relates to a method and apparatus for shaping thin films in the near-edge regions of in-process semiconductor substrates employing plasma techniques.

BACKGROUND

[0003] Future trends in integrated circuit (IC) manufacturing processes require manufacturing engineers to become more attentive to the root causes of contamination. An emerging awareness, within the IC manufacturing engineering community, has recognized the substrate's edge exclusion area and edge surfaces as source locations of contamination. Contamination problems originating in these edge areas are the result of poorly adhering films that partially delaminate and break loose from the surface. These loose film fragments, or flakes, if they migrate towards the center of the wafer where active devices are being constructed, can become killer defects.

[0004] There is also a problem with existing remedies (Edge Bead Removal or EBR) for the flaking films. Traditional EBR methods are time consuming and expensive. Additionally, these EBR processes produce large volumes of hazardous waste. Finally, EBR processes yield topography near the edge that is not readily cleanable and traps particles.

[0005] Accordingly, it is an object of the invention to enable the use of relatively simple techniques for removing flaking films during the processing of a wafer.

[0006] It is another object of the invention to control the film shape on a processed wafer.

[0007] It is another object of the invention to provide an economical technique for shaping the edge of a wafer during processing.

SUMMARY OF THE INVENTION

[0008] Briefly, the invention provides an apparatus and method for shaping a thin film on a wafer.

[0009] The apparatus of the invention employs a rotatable chuck for holding a wafer, a housing having a slot for receiving an edge of a wafer on the chuck, at least one plasma source mounted on the housing for generating a flow of reactive gas and a channel in the housing communicating with the plasma source to direct the flow of reactive gas toward the edge of the wafer in the slot of the housing.

[0010] In addition, an exhaust plenum is disposed within the housing for receiving the reactive gas and an exhaust line communicates with and extends from the exhaust plenum for expelling reactive gas from the plenum.

[0011] Still further, there is at least one additional channel in the housing radially within the first channel for directing a flow of diluent/quenching gas onto the wafer; and at least one exhaust channel in the housing between this additional channel and the first channel for exhausting the diluent/quenching gas and reactive gas therefrom.

[0012] Generally, the housing is of semi-circular shape to receive a major portion of the wafer on the chuck in the slot but may be of any other suitable shape.

[0013] The apparatus may also be constructed with multiple sets of the inlet channels and exhaust channel and a plurality of plasma sources, for example, three plasma sources spaced circumferentially of the housing, for selectively etching of a polymer on a wafer, etching of silicon dioxide on a wafer and depositing an encapsulating silicon dioxide layer on a wafer.

[0014] The method of the invention comprises the steps of mounting a wafer having a thin film on a rotatable chuck; directing a flow of diluent/quenching gas onto the wafer in a radially outward direction; exhausting the flow of diluent/quenching gas from the wafer downstream of the flow of diluent/quenching gas; directing a flow of reactive gases towards the wafer radially outward of the diluent/quenching gas to react with the wafer; and rotating the wafer relative to the flow of reactive gas to remove film fragments from the edge of the wafer or to deposit material on the wafer.

[0015] During rotation, the wafer is moved in a rectilinear direction relative to the flow of reactive gas to allow removal of material from the thin film normally on the wafer while shaping the thin film to a predetermined shape. Thereafter, a second flow of reactive gases can be directed towards the wafer radially outward of the diluent/quenching gas to react with the wafer to deposit material thereon while the wafer is rotated to deposit a thin protective film of the material on the shaped thin film on the wafer.

[0016] The processing capability enabled by the method and apparatus described herein addresses both removal of the flaking films and control of the film shape that remains after processing. The film shaping capability allows for the use of conventional cleaning processes without particle trapping. Further, the process can also encapsulate the freshly processed surface with a thin film that prevents future flaking.

[0017] In accordance with the invention, an in-process semiconductor substrate (wafer) is held in place on a platen (e.g., using vacuum). The platen is sufficiently smaller, in diameter, than the wafer, allowing access to all of the edge surfaces of the wafer. The platen is attached to a spindle, which, in-turn, is connected to a rotational electromechanical system. The electromechanical system enables computer control of the rotational movement of the wafer during processing. Further, the entire platen assembly is mounted on a 3-axis (X, Y, Z) linear electromechanical positioning device. Plasma sources, similar to one described in U.S. Pat. No. 5,961,772, are located in proximity to the edge surfaces of the wafer. The gaseous output-flow from the plasma source (the flame) is directed to impinge on the edge surfaces by means of gas flow hardware design and electromechanical positioning devices (X, Y and Z wafer motion axes).

[0018] Proper selection of the input gases will determine the nature of the processing performed on the wafer. Certain gas mixtures will cause material on the wafer to react with the constituents in the flame such that the reaction by-products are volatile at the operating pressure. In such cases, the process is subtractive and is commonly referred to as etching. Other input gas mixtures will cause flame constituents to react with each other to deposit material onto the wafer. In such cases, the process is additive and is commonly referred to as chemical vapor deposition (CVD).

[0019] The dwell time of the reactive gas flow on any one location of the wafer's edge surfaces shall be controlled via the computer controlled, electro-mechanical positioning devices. For shaping the local topography using an etching process, the flame shall be commanded to dwell for longer times on areas where large material removal is desired and dwell shorter times on areas where less material removal is desired. For CVD processes, the flame shall be commanded to dwell longer times where thicker films are desired and shorter times where thinner films are desired.

[0020] For both etching and CVD processes, it will be important for the boundary between the processed area and the unprocessed area to be sharply defined. For this purpose, a flow of diluent and/or quenching gas shall be provided. The diluent and/or quenching gas flow is oriented to inhibit the diffusion of reactive gases from affecting areas on the wafer not intended for processing. Further, adjustable exhaust ports will be employed to direct the reactive gas flow away from the areas not intended for processing. These and other objects and advantages will become more apparent from the following detailed description taken in conjunction with the accompanying drawings.

[0021] Further areas of applicability of the present invention will become apparent from the detailed description provided hereinafter. It should be understood that the detailed description and specific examples, while indicating the preferred embodiment of the invention, are intended for purposes of illustration only and are not intended to limit the scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The present invention will become more fully understood from the detailed description and the accompanying drawings, wherein:

[0023] **FIG. 1***a* illustrates a part cross-sectional view of a wafer having flaking film fragments in a peripheral edge region;

[0024] **FIG. 1***b* illustrates the wafer of **FIG. 1***a* after application of a photoresist coating in accordance with a prior art technique to remedy flaking film;

[0025] **FIG. 1***c* illustrates the wafer of **FIG. 1***b* after exposure of the photoresist in accordance with the prior art technique;

[0026] **FIG. 1***d* illustrates the wafer of **FIG. 1***c* after development of the photoresist in accordance with the prior art technique;

[0027] **FIG. 1***e* illustrates the wafer of **FIG. 1***d* after a wet or dry thin film etch in accordance with the prior art technique;

[0028] **FIG. 1***f* illustrates the wafer of **FIG. 1***e* after a photoresist strip and cleaning in accordance with the prior art technique;

[0029] **FIG. 2***a* illustrates a part cross-sectional view of a wafer having flaking film fragments in a peripheral edge region;

[0030] **FIG. 2***b* illustrates a part cross-sectional view of the wafer of **FIG. 2***a* after removal of the flaking film fragments and shaping of the remaining film topography in accordance with a preferred embodiment of the invention;

[0031] **FIG. 2***c* illustrates the wafer of **FIG. 2***b* after encapsulation of the processed surface in accordance with the preferred embodiment of the invention;

[0032] **FIG. 3** illustrates a schematic side view of an apparatus for etching of the peripheral edge region of a wafer in accordance with the preferred embodiment of the invention;

[0033] **FIG. 4** illustrates a plan view of the apparatus of **FIG. 3**;

[0034] **FIG. 5** illustrates an enlarged view of a peripheral edge region of a wafer during etching in accordance with the preferred embodiment of the invention.

[0035] **FIG. 6** illustrates a schematic side view of an apparatus for thin film deposition onto the peripheral edge region of a wafer in accordance with the preferred embodiment of the invention;

[0036] **FIG. 7** illustrates an enlarged view of a peripheral edge region of a wafer during thin film deposition in accordance with the preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0037] The following description of the preferred embodiment(s) is merely exemplary in nature and is in no way intended to limit the invention, its application, or uses.

[0038] Referring to **FIGS. 1***a* to **1***f*, a previously known technique for edge bead removal (E.B.R.) frequently results in topography near the edge of a wafer **10** that is not readably cleanable and that traps particles.

[0039] In accordance with the prior art technique, the wafer **10** is provided with a thin film coating **11** of any suitable material. As indicated, fragment flakes **12** may break away in the form of thin film flakes. Subsequently, as indicated in **FIG. 1***b*, a photoresist coating **13** is applied. After the photoresist coating **13** is exposed using conventional techniques, as indicated in **FIG. 1***c*, and subsequently developed as indicated in **FIG. 1***d*, the coating **11** and flakes **12** at the peripheral edge of the wafer **10** are again uncovered. A wet or dry thin film etch step may then be carried out to remove the coating **11** and flakes **12** at the peripheral edge of the wafer **10**, as indicated in **FIG. 1***e* (depicts a wet etch profile). Finally, the photoresist coating **13** is stripped and the surface is cleaned as indicated in **FIG. 1***f*. However, small particles **14** may become trapped in the region where the coating **11** ends on the wafer **10**.

[0040] Referring to **FIGS. 2***a*, **2***b* and **2***c*, the invention proposes to process a coated wafer as shown in **FIG. 2***a* by removing the flaking film fragments and shaping the remain-

ing film topography in a manner as illustrated. For example as indicated in **FIG. 2***b*, the peripheral edge of the coating **11** is tapered radially outwardly adjacent to the outermost periphery of the wafer **10**. Thereafter, as indicated in **FIG. 2***c*, the processed surface of the coating **11** is encapsulated within a layer **15**.

[**0041**] Referring to **FIG. 3**, a wafer **10** is placed on a vacuum chuck **16** that is able to move horizontally in the X and Y axes and also vertically in the Z axis. In addition, the vacuum chuck, **16**, is configured with a rotational axis, E as shown. The vacuum chuck is typically incorporated in an electro-mechanical system (not shown) having suitable means for moving the vacuum chuck **16** with these 4 degrees of freedom (X, Y, Z, E).

[**0042**] Referring to **FIG. 3**, three plasma sources, **17***t*, **17***e* and **17***b* are respectively located in proximity to the top side, the edge and the bottom side of the wafer **10** in order to supply the reactive gas flow toward the three surfaces of the wafer **10**. Each plasma source is constructed, such as the atmospheric pressure plasma jet described in U.S. Pat. No. 5,961,772. This arrangement of three plasma sources allows for maximum flexibility in processing options as follows:

[**0043**] Independent processing of the top, bottom or edge surfaces of wafer **10**

[**0044**] Simultaneous processing of any two of the above named surfaces of the wafer **10**

[**0045**] Simultaneous processing of all three of the above named surfaces of the wafer **10**.

[**0046**] Referring to **FIGS. 3 and 5**, pairs of flow channels **19***t*, **19***b* and **20***t*, **20***b* associated with their respective plasma sources **17***t* and **17***b* provide a means to control the unwanted diffusion of reactive gas flow onto portions of the wafer **10** where processing is unwanted. Channels **19***t* and **19***b* supply a diluent or quenching gas flow inward toward the wafer, **10**, and directed radially outwards towards the edge of wafer **10**. Fine exhaust channels **20***t* and **20***b* provide an exhaust flow directed outward from the plane of the wafer **10**. Conductance adjustment valves, **21***t* and **21***b* are tuned to match the diluent or quenching gas flow rate of the channels **19***t* and **19***b* respectively. Reactive gases from plasma sources **17***t*, **17***e* and **17***b* that diffuse towards the center of the wafer are neutralized, entrained in the exhaust flow and removed via fine exhaust channels **20***t* and **20***b*. This technique provides for the sharp boundary between the processed and unprocessed regions.

[**0047**] Referring to **FIGS. 3 and 4**, the plasma sources, **17***t*, **17***t*' and **17***t*" are mounted to a semi-circular housing, **18**. The housing includes a slot **22** for receiving the wafer **10** as indicated in **FIG. 3**, the housing **18** is equal to or approximately equal to one-half the size of the wafer **10**. The housing also includes an exhaust plenum, **23**, which is connected to the exhaust source (not shown) via an adjustable conductance control valve **24**.

[**0048**] As illustrated three sets of plasma sources, **17** (including **17***t*, **17***e*, and **17***b*), **17**' (including **17***t*', **17***e*', and **17***b*') and **17**" (including **17***t*", **17***e*" and **17***b*"), quenching gas lines, **19** (including **19***t* and **19***b*), **19**' (including **19**t' and **19***b*') and **19**" (including **19***t*" and **19***b*") and exhaust conductance control valves **21** (including **21***t* and **21***b*), **21**' (including **21***t*' and **21***b*') **21**" (including **21***t*" and **21***b*") and **24**, **24**' and **24**" may be arranged around the housing, **18**, as shown. In this arrangement each set can operate independently with respect to process chemistry. For example, one set can perform etching of polymers, as indicated by **17***t*', **17***e*', **17***b*', **19***t*', **19***b*', **21***t*', **21***b*' and **24**', while another set performs etching of SiO_2, as indicated by items, **17***t*, **17***e*, **17***b*, **19***t*, **19***b*, **21***t*, **21***b* and **24**, while a third set, as indicated by items **17***t*", **17***e*", **17***b*", **19***t*", **19***b*, **21***t*", **21***b*" and **24**" deposits an encapsulating SiO_2 layer.

[**0049**] Examples of processes are shown in Table 1. The first column contains the input gases. The second column contains the active output species. The third column contains the type of process performed and the fourth column contains the thin film addressed by the process.

TABLE 1

Input Gases	Active output species	Process Type	Thin Film
He, CF_4, O_2	Atomic Fluorine	Etch	Si, SiO_2, Si_3N_4, W, Ta
He, O_2	Atomic Oxygen	Etch	Organic Polymers
He, O_3, TEOS	(O—Si—O)	CVD	SiO_2

[**0050**] A typical sequence of events to shape an SiO_2 thin film on the top surface of a wafer followed by an SiO_2 CVD encapsulation process as depicted in **FIGS. 2***a*, **2***b* and **2***c* is described below with reference to **FIGS. 3 and 5**:

[**0051**] 1. A well-centered wafer, **10**, is placed on the vacuum wafer platen, **16**.

[**0052**] 2. The vacuum wafer platen is moved in X, Y and Z axes such that the wafer is centered within the slot, **22**, and the edge portion of the wafer is located immediately adjacent to diluent/quenching gas supply channels **19***t* and **19***b*.

[**0053**] 3. Diluent/quenching gas flow rate setpoints are sent to the mass flow controllers (MFC) **25***t* and **25***b* and the diluent/quenching gas shutoff valves **26***t* and **26***b* are commanded to open. Gas begins to flow down diluent/quenching gas supply channels **19***t* and **19***b* and impinges on the edge of the wafer **10**.

[**0054**] 4. Fine exhaust channel conductance control valve, **21***t*, is commanded open to a predefined position. (Conductance control valve **21***b* is not opened. This allows the diluent/quenching gas flow from channel **19***b* to protect the backside of the wafer **10** from unwanted diffusion of reactive gases).

[**0055**] 5. Process gas flow rate setpoints are sent to the process input gas MFCs (not shown) and process input gas shutoff valve **27***t* is commanded to open. Process input gases He, O_2 and CF_4 begin to flow through channel **30***t*.

[**0056**] 6. The conductance control valve **24** of housing exhaust plenum **23** is commanded to a pre-defined position.

[**0057**] 7. A forward power setpoint is sent to the RF power supply **29***t* and the RF power is commanded on. A plasma is formed inside the plasma source **17***t* and reactive gases begin to flow through channel **30***t* into the housing exhaust plenum **23** and out through the conductance control valve **24** to the exhaust system (not shown).

[**0058**] 8. The impedance matching network, **28***t*, tunes the load impedance to match the output impedance of the RF

power supply **29***t*. The control system (not shown) compares the magnitude of the power reflected back to power supply **29***t* to a pre-defined threshold value. The control system (not shown) decides to halt the process or continue based upon the reflected power comparison. A successful comparison signifies formation of a stable plasma inside plasma source **17***t*.

[**0059**] 9. Assuming the decision is to continue, the vacuum wafer platen **16** is commanded to begin rotating at a predefined angular velocity.

[**0060**] 10. The vacuum wafer platen **16** is commanded to move in the X, Y and Z axes, positioning the edge surfaces into the reactive gas stream flowing from reactive gas channel **30***t*.

[**0061**] 11. The shaping of the thin films is controlled by the dynamics of the vacuum wafer platen's, **16**, motion as follows:

[**0062**] 12. Referring to **FIGS. 2, 3** and **5**, from the starting position the wafer **10** is moved in the positive X direction in a smoothly accelerating motion. As the edge of the wafer moves beneath reactive gas channel **30***t* the SiO_2 thin film fragment begins to react with the atomic fluorine in the reactive gas flow to produce a volatile by-product according to the following chemical equation:

$$SiO_2+F_4 \rightarrow SiF_4+O_2$$

[**0063**] As the process effluent, SiF_4+O_2 is produced, the exhaust plenum **23** directs the effluent flow towards the exhaust system (not shown) under control of the conductance control valve **24**. Continued movement of the wafer in the positive X axis brings the main portion of the coating **11** into contact with the reactive gas flowing through channel **30***t* and the above chemical reaction proceeds to remove a portion of coating **11**. When the preprogrammed edge exclusion limit is reached the vacuum wafer platen **16** is commanded to reverse direction and move in a smoothly decelerating motion until it it arrives back at its starting position. The described motion will yield an SiO_2 removal profile that, when applied to the thin film shape **11** and **12** depicted in **FIG. 2***a*, will result in the thin film shape **11** depicted in **FIG. 2***b*.

[**0064**] 13. Once the thin film removal shaping is complete the RF power supply **29***t* is commanded off.

[**0065**] 14. The process input gas shutoff valve **27***t* is closed.

[**0066**] 15. The diluent/quenching gas shutoff valves **26***t* and **26***b* are closed.

[**0067**] 16. The diluent/quenching gas supply channel conductance control valve **21***t* is closed.

[**0068**] 17. The housing exhaust plenum's conductance control valve **24** is closed.

[**0069**] Depending on the application, certain metal films may have become exposed during the oxide removal step. To prevent these metal films from flaking, an encapsulating SiO_2 thin film **15** can be deposited as follows:

[**0070**] 18. Referring to **FIGS. 6 and 7**, diluent/quenching gas flow rate setpoints are sent to the mass flow controllers (MFC) **25***t*" and **25***b*" and the diluent/quenching gas shutoff valves **26***t*" and **26***b*" are commanded to open. Gas begins to flow down diluent/quenching gas supply channels **19***t*" and **19***b*" and impinges on the edge of the wafer **10**.

[**0071**] 19. Fine exhaust channel conductance control valve **21***t*" is commanded open to a predefined position. (Conductance control valve **21***b*" is not opened. This allows the diluent/quenching gas flow from channel **19***b*" to protect the backside of the wafer **10** from unwanted diffusion of reactive gases).

[**0072**] 20. Process gas flow rate setpoints are sent to the process input gas MFCs (not shown) and process input gas shutoff valve **27***t*" is commanded to open. Process input gases He, TEOS and O_3 begin to flow through channel **30***t*".

[**0073**] 21. The conductance control valve **24**" of the housing exhaust plenum **23** is commanded to a pre-defined position.

[**0074**] 22. A forward power setpoint is sent to the RF power supply **29***t*" and the RF power is commanded on. A plasma is formed inside the plasma source **17***t*" and reactive gases begin to flow through channel **30***t*" into the housing exhaust plenum **23** and out through the conductance control valve **24**" to the exhaust system (not shown).

[**0075**] 23. The impedance matching network **28***t*" tunes the load impedance to match the output impedance of the RF power supply **29***t*". The control system (not shown) compares the magnitude of the power reflected back to power supply **29***t*" to a pre-defined threshold value. The control system (not shown) decides to halt the process or continue based upon the reflected power comparison. A successful comparison signifies formation of a stable plasma inside plasma source **17***t*".

[**0076**] 24. Assuming the decision is to continue, the vacuum wafer platen **16** is commanded to begin rotating at a predefined angular velocity.

[**0077**] 25. The vacuum wafer platen **16** is commanded to move in the X, Y and Z axes, positioning the edge surfaces into the reactive gas stream flowing from reactive gas channel **30***t*".

[**0078**] 26. The shaping of the thin film deposition is controlled by the dynamics of the motion of the vacuum wafer platen **16** as follows:

[**0079**] 27. From the starting position the wafer **10** is moved in the X and Y direction such that the net direction vector is pointing in the direction of the plasma source **17***t*". A smoothly accelerating motion is employed. As the edge of the wafer moves beneath reactive gas channel **30***t*" the SiO_2 thin film begins to deposit on the wafer, **10**, surface according to the following chemical equation:

$$Si(OC_2H_5)+8O_3 \rightarrow SiO_2+10H_2O+8CO_2$$

[**0080**] As the process effluent, $10H_2O+8CO_2$, is produced, the exhaust plenum **23** directs the flow towards the exhaust system (not shown) under control of the conductance control valve **24**". Continued movement of the wafer brings more of the previously etched thin film **11** into contact with the reactive gas flow and the above chemical reaction continues depositing the thin film **15**. When the pre-programmed edge exclusion limit is reached the vacuum wafer platen **16** is commanded to reverse direction and move in a smoothly decelerating motion until it arrives back at its starting

position. The described motion will yield an SiO_2 thin film deposition profile that, when applied to the thin film shape **11** depicted in **FIG. 2***b*, will result in the deposited thin film shape **15** depicted in **FIG. 2***c*.

[**0081**] 28. Once the thin film deposition shaping is complete the RF power supply **29***t*" is commanded off.

[**0082**] 29. The process input gas shutoff valve **27***t*" is closed.

[**0083**] 30. The diluent/quenching gas shutoff valves **26***t*" and **26***b*" are closed.

[**0084**] 31. The diluent/quenching gas supply channel conductance control valve **21***t*" is closed.

[**0085**] 32. The housing exhaust plenum's conductance control valve **24**" is closed.

[**0086**] 33. With the processing sequence complete, the wafer **10** can be removed from the vacuum wafer platen **16**.

[**0087**] The shape of the etched surface can be nearly anything. The limiting factors are the spatial frequency capabilities of the reactive gas footprint shape and the servo system dynamic response. Other shapes of interest might include convex or concave shapes or shapes that intersect the wafer top surface plane further in from the edge.

[**0088**] The protective thin film **15** may be of any suitable thickness. Typically, the film **15** is thin enough such that none of the layer of film **15** extends above the plane of the remaining film **11** and thick enough to be mechanically strong enough to weather the stresses exerted by the film **11** the protective film **15** is covering. For example, a thickness of 0.1 to 0.3 um should be sufficient. The thickness of the layer of film **15** may also be varied in the same way the etching process profile is varied, via a spatial variation of the reactive gas footprint dwell time.

[**0089**] The invention thus provides an apparatus and method of shaping thin films in the regions of in-process semiconductor substrates that are economical and relatively simple and efficient.

[**0090**] The invention also provides a method that allows flakes to be readily removed from a semiconductor substrate and the edge region of the processed substrate to be contoured to a desired shape.

[**0091**] The description of the invention is merely exemplary in nature and, thus, variations that do not depart from the gist of the invention are intended to be within the scope of the invention. Such variations are not to be regarded as a departure from the spirit and scope of the invention.

What is claimed is:

1. A method of processing a thin film on an edge of a substrate comprising the steps of:

mounting a substrate having a thin film thereon on a rotatable chuck;

directing a flow of reactive species through a channel in a housing angled towards the edge of the substrate; and

rotating the substrate relative to the flow of reactive species to process the thin film on the edge of the substrate.

2. The method of claim 1 wherein the channel is angled towards the edge of the substrate between greater than a vertical position and less than a horizontal position in relation to a top surface of the substrate.

3. The method of claim 1 further comprising the steps of:

directing a flow of diluent/quenching gas onto the substrate in a radially outward direction.

4. The method of claim 3 further comprising the steps of:

exhausting the flow of diluent/quenching gas from the substrate downstream of the flow of diluent/quenching gas.

5. The method of claim 1 further comprising the steps of:

directing a flow of diluent/quenching gas onto the substrate in a radially outward direction.

6. The method of claim 1 further comprising the steps of:

moving the substrate in a rectilinear direction relative to the flow of the reactive species to remove material from a thin film on the substrate while shaping the thin film to a predetermined shape.

7. The method of claim 1 wherein the reactive species comprises fluorine.

8. The method of claim 1 further comprising the steps of:

directing a flow of a second reactive species through a second channel in the housing angled towards the edge of the substrate for depositing a new thin film on the substrate.

9. The method of claim 8 further comprising the steps of:

directing a second flow of diluent/quenching gas onto the substrate in a radially outward direction.

10. The method of claim 1 further comprising the steps of:

directing a flow of a second reactive species through a second channel in the housing angled towards the edge of the substrate for depositing a new thin film on the substrate, wherein the second channel is co-radial with the channel, wherein the second channel is angled towards the edge of the substrate between greater than a vertical position and less than a horizontal position in relation to a top surface of the substrate; and

directing a second flow of diluent/quenching gas onto the substrate in a radially outward direction.

11. The method of claim 10 wherein the new thin film has a thickness in the range of from 0.1 to 0.3 μm.

12. The method of claim 1 further comprising the steps of:

collecting the reactive species in a plenum located about the edge of the substrate and exhausting the reactive species from said plenum.

13. The method of claim 1 further comprising the steps of:

generating the reactive species from a plasma source.

14. The method of claim 1 further comprising the steps of:

generating the reactive species from an atmospheric-pressure plasma jet.

15. The method of claim 1 wherein the thin film is a silicon dioxide.

16. A method for processing a substrate comprising:

providing a housing having a plurality of channels for directing a flow of reactive species towards an edge of a substrate wherein the channels are radially angled in a direction towards the edge of the substrate;

flowing gases through at least one of the channels towards the edge of the substrate; and

exhausting exhaust gases downstream from the at least one of the channels.

17. A method of shaping a thin film on a wafer comprising the steps of mounting a wafer having a thin film thereon on a rotatable chuck;

directing a flow of diluent/quenching gas onto the wafer in a radially outward direction;

exhausting the flow of diluent/quenching gas from the wafer downstream of the flow of diluent/quenching gas;

directing a flow of reactive gases towards the wafer radially outward of the diluent/quenching gas to react with the wafer; and

rotating the wafer relative to the flow of reactive gas to deposit a thin protective film of material on the edge of the wafer.

18. A method as set forth in claim 17 wherein the thin protective film has a thickness in the range of from 0.1 to 0.3 μm.

19. A method of processing a wafer comprising the steps of:

rotating the wafer;

directing a flow of a first reactive species radially outward towards an edge of the wafer for etching the edge, wherein the first reactive species are directed through a first channel angled towards the edge; and

directing a flow of a second reactive species radially outward towards the edge of the wafer for deposition of a material on the edge, wherein the second reactive species are directed through a second channel angled towards the edge.

20. The method of claim 19 further comprising the steps of:

flowing a diluent/quenching gas radially outward towards the edge for preventing movement of the first reactive species radially inward, wherein the diluent/quenching gas originates from within the radial origin of the flow of the first reactive species.

21. The method of claim 19 further comprising the steps of:

providing a plurality of channels for directing the first reactive species towards near-edge, top bevel, crown, and bottom bevel of the wafer.

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